

Linear Integrated Circuits

3

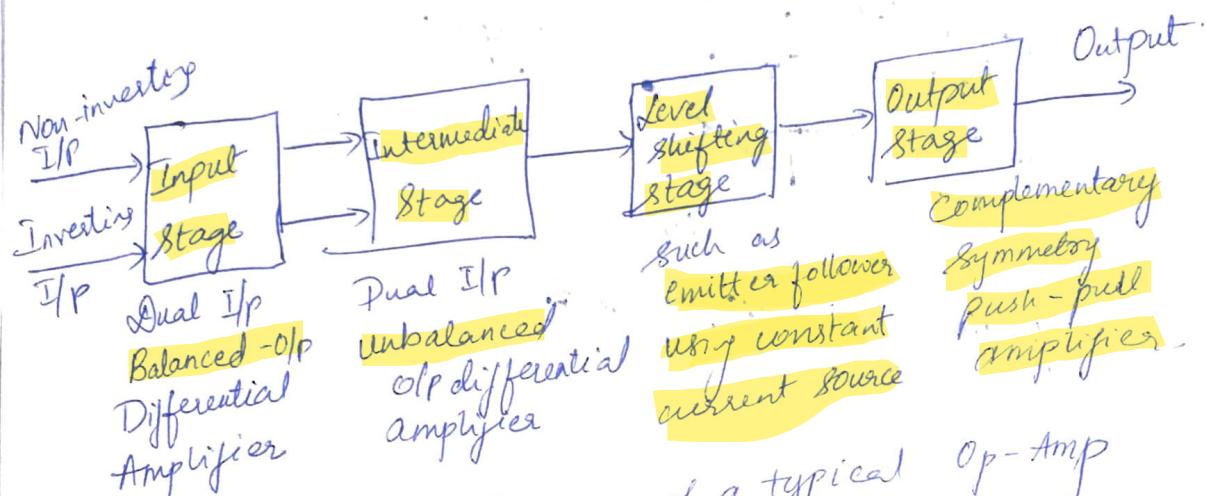
Unit 1. Op-Amp Basics, DC and AC Amplifiers

An operational amplifier is a direct-coupled high gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and an output stage.

Op-amps are very high gain amplifier circuits with 2 high-impedance input terminals and one low-impedance output

- 2 I/Ps [inverting input]
- 2 I/Ps [non-inverting input]

Block diagram representation of a typical Op-amp



Block diagram of a typical Op-Amp

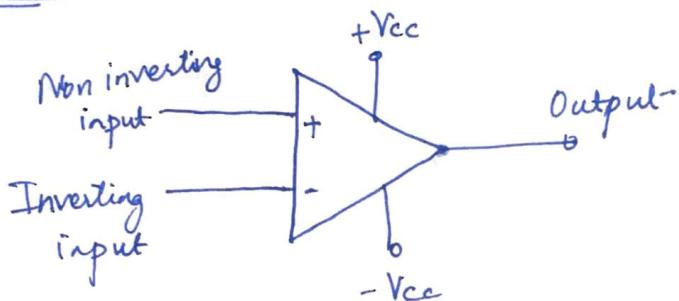
The input stage is the dual-input, balanced O/P differential amplifier which provides most of the voltage gain of the amplifier. It establishes the input resistance of the op-amp.

Intermediate Stage differential amplifier which is driven by the O/P of the first stage dual I/P, unbalanced (single-ended) output. Direct coupling is used, the dc v/g at O/P of intermediate stage is above ground potential.

level shifting stage → shift the dc level at the output of the intermediate stage downward to zero w.r.t ground.

Final stage → push-pull complementary amplifier Op stage.
The output stage increases the output voltage swing and raises the current supplying capability of the op-amp.
→ A well designed Op stage also provides low output resistance.

Op-Amp Symbol



op-Amp circuit symbols

Basic Op-Amp circuit

It consists of ~~a dar - opamp~~ a BJT, differential amplifier input stage combined with emitter follower op-

+Vcc } positive & negative voltage applied to
-Vee } the Op-Amp

⇒ Op-Amp IC is available in three popular packages

- ① The metal can (TO) package
- ② The dual in line package (DIP)
- ③ Flat package or flat pack.

Op-Amp Terminals

Op-Amp packages may contain single, dual or four (quad) op-amps.

Typical packages have 8 terminals, 10 terminals & 14 terminals

The widely used very popular type is $U\text{A}741$ - single op-amp μA741 is a single op-amp and is available as 8 pin DIP -

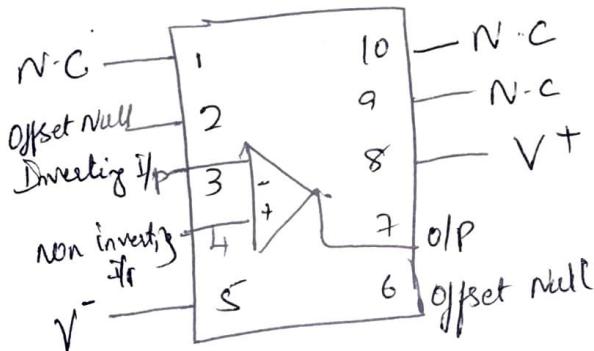
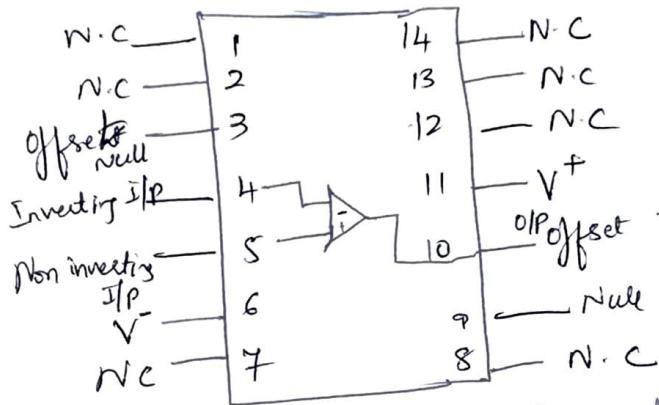
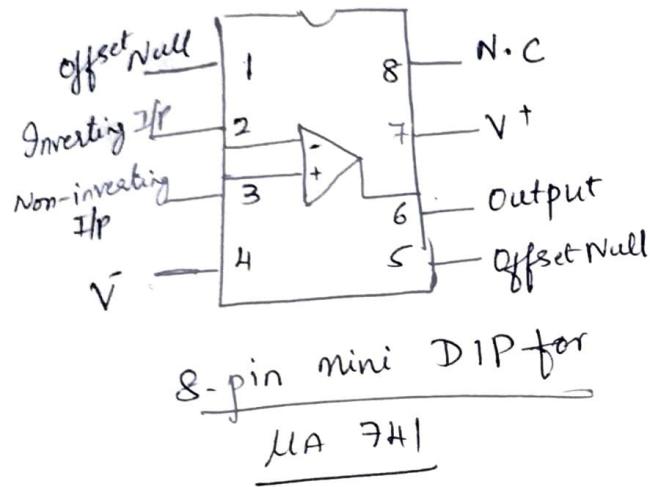
Op-Amp terminals

Op-Amp have five basic terminals

→ 2 I/P terminals

→ 1 O/P terminal

→ 2 power supply

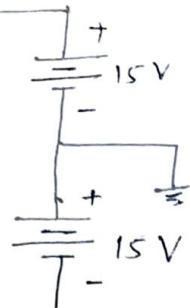
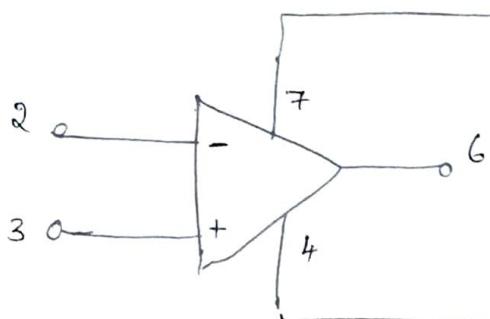


10 pin flat pack.

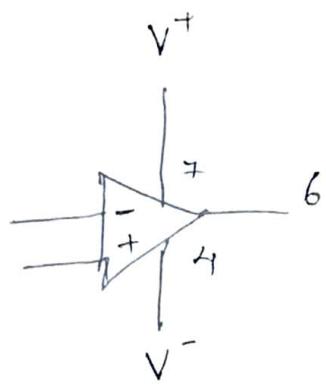
N.C. → No Connection

Power Supply Connections

V^+ and V^- power supply terminals connected to two dc V/g sources



≡



power supply connections of op-amp

Manufacturers of IC's

Fairchild

Codes
MA, MAF

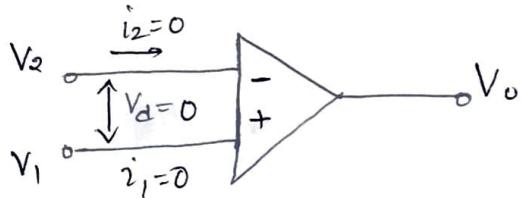
National Semiconductor

Motorola

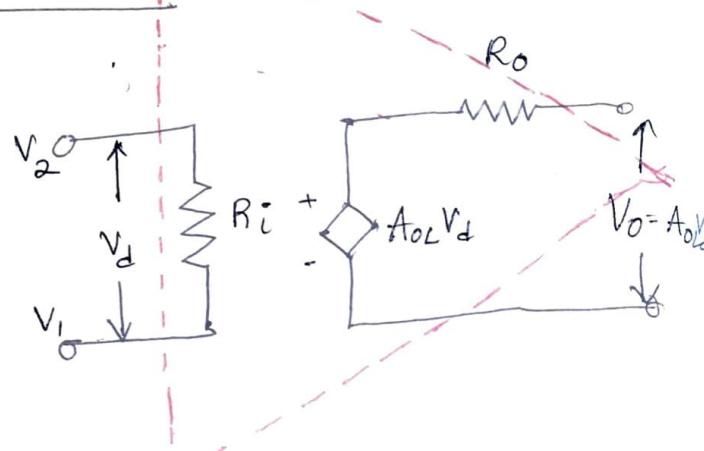
RCA

Texas Instruments.

The Ideal Operational Amplifier

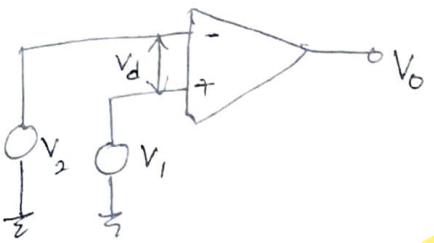


Ideal opamp



Equivalent circuit of an op-amp

V_2 is the inverting terminal (180° out of phase with V_2)
 $V_1 \rightarrow$ non-inverting terminal



Open Loop circuit

$V_d \rightarrow$ differential input voltage

Features of an ideal Op-amps

→ draws no current at both the input terminals. i.e. $i_1 = 0$ & $i_2 = 0$.

∴ of high input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

→ Gain is ∞ , the voltage between the Inverting and non-inverting terminals $V_d = (V_1 - V_2)$,

↙ zero for finite output voltage.

→ Output voltage V_o is independent of the current drawn from output as $R_o = 0$

∴ It can drive an infinite number of other devices.

$$V_o = A_{OL} V_d$$

$$V_o = A_{OL} (V_1 - V_2)$$

Physical Amplifier is non an ideal one.

Op-Amp is a voltage controlled voltage source and $A_{OL} V_d$ is an equivalent Thevenin's v/g source and R_o is the Thevenin's equivalent resistance.

(5)

Characteristics of an op-amp
to be the ideal op-amp

Op voltage gain $A_{OL} = \infty$

Input impedance $R_i = \infty$

Output impedance $R_o = 0$

Bandwidth $BW = \infty$

Zero offset i.e. $V_o = 0$, when $V_1 = V_2 = 0$

Open Loop operation of Op-amp

→ Simplest way to use an op-amp. is in open loop mode.

The gain of an ideal opamp is ∞ (infinity) thus the output voltage is a positive saturation voltage ($+V_{sat}$) or negative saturation voltage ($-V_{sat}$)

Saturation V/g → maximum V/g of the op-amp

The output can be present in any one of the two possible states i.e. $+V_{sat}$ or $-V_{sat}$. and amplifiers acts as an switch

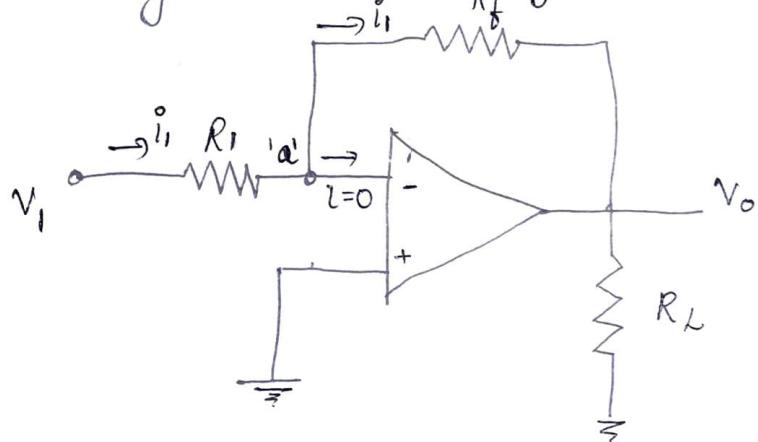
→ Open loop configuration has limited number of applications such as voltage comparator, zero crossing detector etc.

Feedback in an Ideal Op-amp

Op-amp can be utilized greatly ~~using~~ by providing negative feedback.

Inverting Amplifier

→ ~~mostly~~ → most widely used of all op-amp circuits



Inverting Amplifier.

The inverting amplifier circuit is as shown in the fig. (7)
 → O/P voltage V_o is fed back to the inverting terminal of the op-amp through the $R_f - R_i$ network where $R_f \rightarrow$ feedback resistor.

→ Input voltage is applied to inverting terminal through R_i , non inverting terminal is grounded.

For an ideal op-amp As $V_d = 0$, node 'a' is at ground potential.

$$\text{Current } i_1 \text{ through } R_i \Rightarrow i_1 = \frac{V_i}{R_i}$$

Due to virtual short/virtual ground no current ~~flows~~ is drawn by op-amp.

$$\therefore V_o = -i_1 R_f$$

$$V_o = -\frac{V_i}{R_i} R_f = -V_i \frac{R_f}{R_i}$$

Gain of inverting amplifier

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

Alternate Nodal equation at node a

$$\frac{V_a - V_i}{R_i} + \frac{V_a - V_o}{R_f} = 0$$

$V_a \rightarrow v_{fg}$ at node a
 ↓
 virtual gnd

$$V_a = 0$$

$$-\frac{V_i}{R_i} - \frac{V_o}{R_f} = 0$$

$$+\frac{V_o}{R_f} = -\frac{V_i}{R_i}$$

$$V_o = -V_i \frac{R_f}{R_i}$$

$$\therefore A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

-ve sign indicated a phase shift of 180° b/w V_i & V_o . (3)

Inverting input terminal is at virtual ground, the effective input impedance is R_i .

$\therefore R_i$ should be kept fairly large to avoid loading effect. This however ~~effectively~~ limits the gain that can be obtained from this circuit.

Load Resistor R_L is used at the output, otherwise the input impedance of the measuring device such as oscilloscope or DVM acts as the load. ~~This makes~~

If R_i and R_f are replaced by impedances Z_i and Z_f respectively then the voltage gain, A_{CL} will be

$$A_{CL} = -\frac{Z_f}{Z_i}$$

→ This expression of voltage gain will be used in op-amp applications such as integrator, differentiator etc.

Problems

inverting

- ① Design an ^{inverting} amplifier with a gain of -10 and input resistance equal to $10k\Omega$

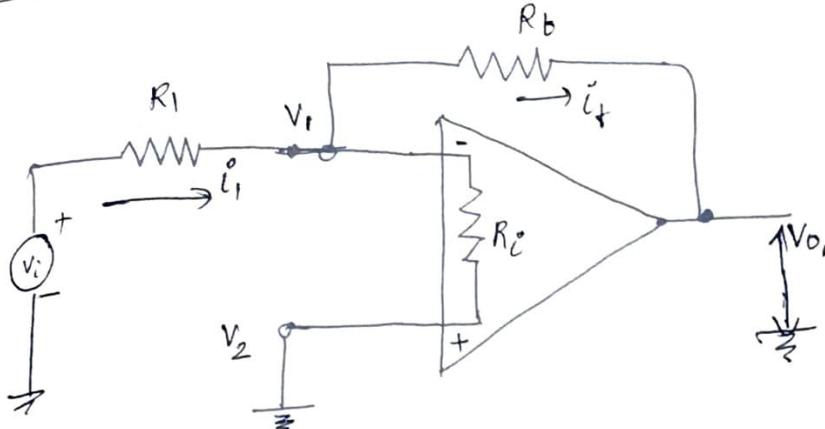
Given $A_{CL} = -10$

$$R_i = 10k\Omega$$

$$A_{CL} = \frac{-R_f}{R_i}$$

$$-10 = \frac{-R_f}{10k\Omega} \Rightarrow R_f = 100k\Omega$$

Virtual short in an op-amp



op-amp inverting amplifier with negative feedback

R_i → input resistance of op-amp.

$$\text{Op voltage } V_o = A_{OL} [V_2 - V_1]$$

A_{OL} → open loop voltage gain of op-amp.

$$V_d = \boxed{V_2 - V_1 = \frac{V_o}{A_{OL}}} \quad \text{--- (1)}$$

The output voltage V_o cannot exceed DC supply voltage to op-amp

Suppose for MA741 → Supply voltage = 12V

$$\text{Open loop v/g gain} = 2 \times 10^5 \approx A_{OL}$$

If we want $V_o = 10V$, Sub in (1)

$$\text{with } V_i = 1V$$

$$V_2 - V_1 = V_d = \frac{10}{2 \times 10^5} = 5 \times 10^{-5} = 50 \times 10^{-6} \text{ V}$$

0.5 μV is very small compared to the input and output voltages ∴ $V_2 - V_1 \approx 0V$

$$\text{Or } \boxed{V_2 = V_1} \quad \text{--- (2)}$$

Eqn (2) indicates both inverting and non-inverting inputs are at same potential i.e., they appear to be tied together or shorted. thus Voltage across R_i is zero.

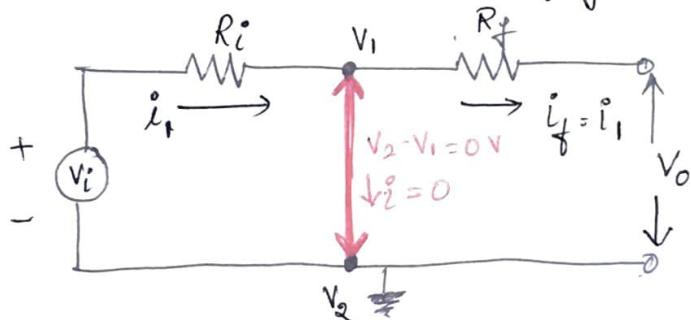
Since R_i is very large the current flowing through R_i is almost zero.

Current & voltage at $R_i = 0$

If two terminals are physically shorted, the voltage b/w the terminals is zero. ~~current flowing through the short~~ & the large current flows through the short.

whereas in the op-amps the v/g between inverting and non-inverting terminal is zero and no current flows through the short to the ground, hence we say virtual short exists b/w the input terminals of an op-amp.

The virtual short is also called virtual ground. The virtual ground is indicated by heavy line between the input terminals as shown in figure below.



Virtual ground in Op-amp

The same current flows through R_o and R_f . The concept of virtual short is very much useful in op-amp analysis.

Problem

(2) In the fig $R_1 = 10k\Omega$, $R_f = 100k\Omega$, $V_i = 1V$, A load of $25k\Omega$ is connected to the output terminal

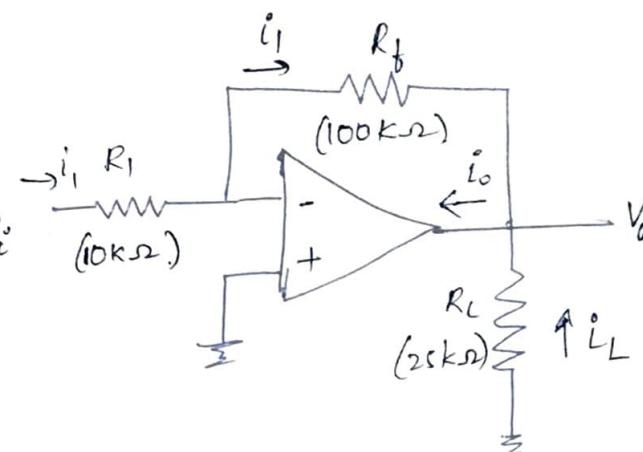
Calculate (i) i_1 , (ii) V_o (iii) i_L

(iv) total current i_o into the output pin

$$R_i = 10\text{ k}\Omega \quad R_f = 100\text{ k}\Omega \quad V_i = 1\text{ V} \quad R_L = 25\text{ k}\Omega$$

(i) $i_1 = \frac{V_i}{R_i} = \frac{1\text{ V}}{10\text{ k}\Omega} = 0.1\text{ mA}$

(ii) $V_o = -\frac{R_f}{R_i} V_i = -\frac{100\text{ k}\Omega}{10\text{ k}\Omega} \cdot 1\text{ V} = -10\text{ V}$



(iii) $i_L = \frac{V_o}{R_L} = \frac{10\text{ V}}{25\text{ k}\Omega} = 0.4\text{ mA}$

(iv) Applying KCL at V_o node $i_o = i_1 + i_L$

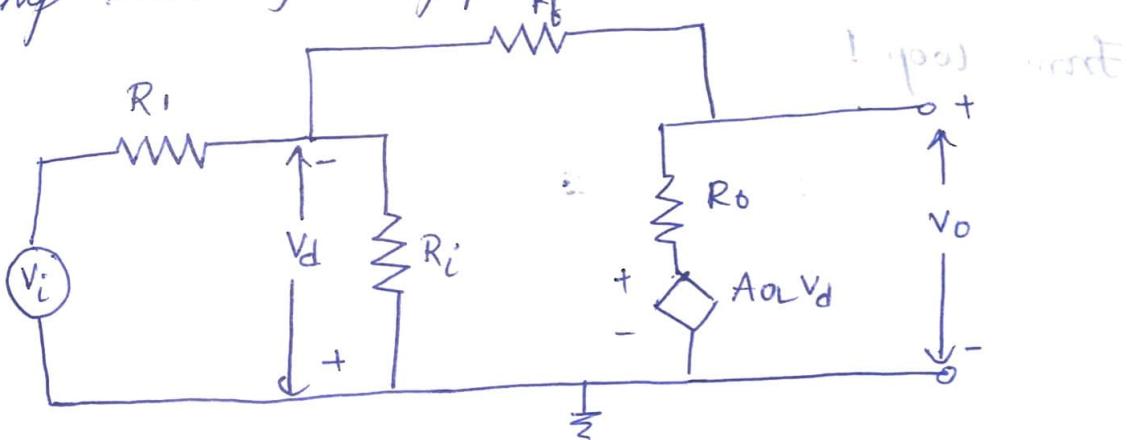
$$= 0.1\text{ mA} + 0.4\text{ mA}$$

$$\boxed{i_o = 0.5\text{ mA}}$$

In an inverting amplifier, for a +ve input, output will be -ve. ∴ direction of i_o is as shown in figure.

Practical Inverting Amplifier

For a practical opamp the expression for the closed loop voltage gain should be calculated using low frequency model of inverting amplifier. Equivalent practical inverting op-amp inverting amplifier is as shown in fig

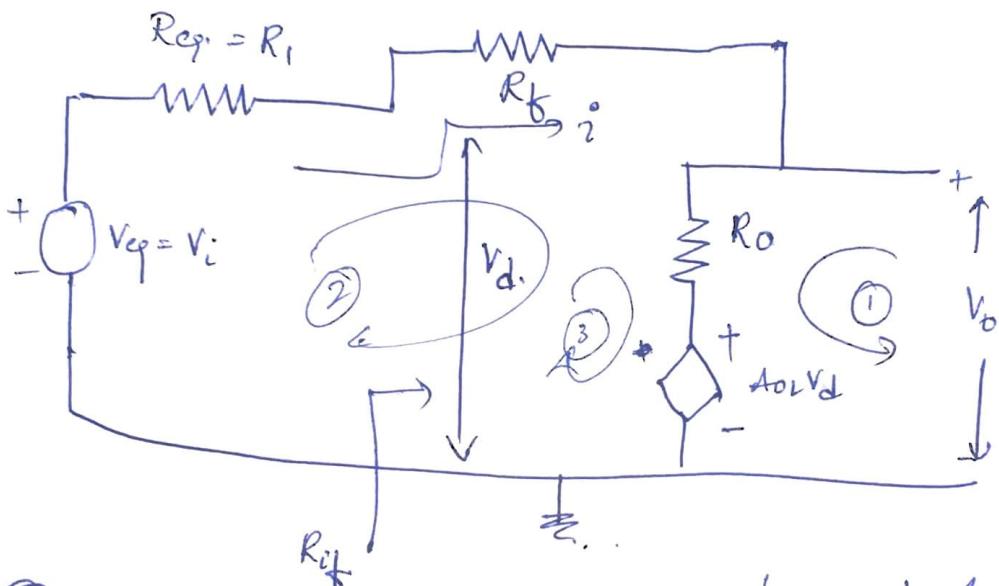


(a) Equivalent practical inverting op-amp amplifier

Simplify the circuit using Thvenin's equivalent ckt.
 $V_i \rightarrow$ veq. & R_{eq} with Req.

$$V_{\text{eq}} = \frac{V_i \cdot R_1}{R_1 + R_{i^*}} \cong V_i$$

$$\text{Req} = R_1 \parallel R_{i^*} = \frac{R_1 \cdot R_{i^*}}{R_1 + R_{i^*}} \cong R_1$$



(b) Simplified ckt using therenin's equivalent

The input impedance R_{i^*} of an op-amp is usually much greater than R_1 .

From loop 1:

$$V_o = i R_o + A_{OL} V_d \quad \text{--- (1)}$$

KVL to loop 3

$$V_d + i R_f + V_o = 0 \quad \text{--- (2)}$$

$$\Rightarrow V_d = \frac{V_o - i R_o}{A_{OL}}$$

Sub V_d in (2).

$$\frac{V_o - iR_o}{AOL} + iR_f + V_o = 0$$

$$V_o - iR_o + iAOL R_f + AOL V_o = 0$$

$$V_o (1 + AOL) = iR_o - iAOL R_f$$

$$V_o (1 + AOL) = i(R_o - AOL R_f) \quad \text{--- (3)}$$

Applying KVL to loop ②

$$V_i = iR_1 + iR_f + V_o \\ = i(R_1 + R_f) + V_o$$

Sub i from (3)

$$V_i = \frac{V_o (1 + AOL)}{(R_o - AOL R_f)} (R_1 + R_f) + V_o$$

$$= \frac{V_o (1 + AOL) (R_1 + R_f) + V_o (R_o - AOL R_f)}{(R_o - AOL R_f)}$$

$$V_i = \frac{V_o [(1 + AOL) R_1 + R_f + AOL R_f + R_o - AOL R_f]}{(R_o - AOL R_f)}$$

$$V_i = \frac{V_o [(1 + AOL) R_1 + R_f + R_o]}{(R_o - AOL R_f)}$$

Re arranging

$$\boxed{\text{AOL} \frac{V_o}{V_i} = \frac{R_o - AOL R_f}{(1 + AOL) R_1 + R_f + R_o}} \quad \text{--- (A)}$$

$$\text{AOL} \gg 1 \Rightarrow 1 + AOL \approx AOL$$

$$\text{Also } \frac{AOL R_1 + R_f + R_o}{AOL R_1} \quad AOL R_1 \gg R_o + R_f$$

R_o is negligible

Closed loop
op. amp gain

$$\boxed{\text{AOL} = \frac{-AOL R_f}{AOL R_1} = -\frac{R_f}{R_1}}$$

Input Resistance (R_{if})

From ①

$$R_{if} = \frac{V_d}{i}$$

Apply KVL for Loop 3

$$V_d + i(R_f + R_o) + A_{OL}V_d = 0$$

$$V_d + i(R_f + R_o) + A_{OL}iR_{if} = 0$$

sub $V_d = iR_{if}$

~~$iR_{if} + iR_f + iR_o + iA_{OL}R_{if} = 0$~~

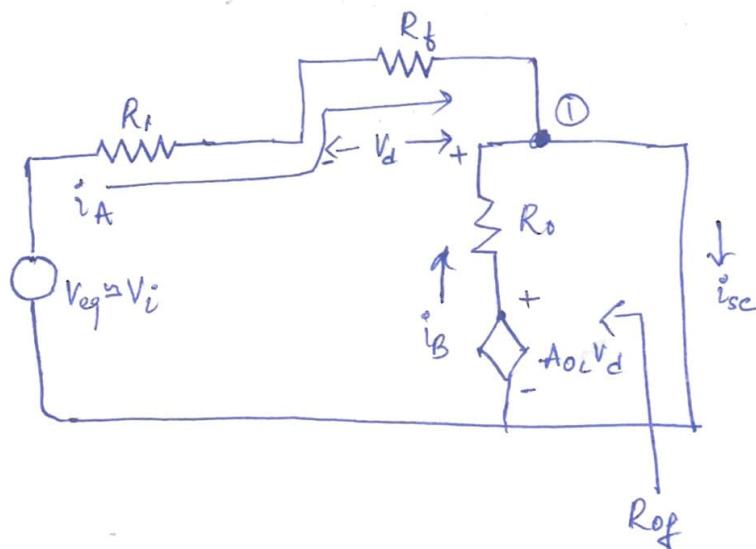
$$R_{if}(1 + A_{OL}) = (R_f + R_o)$$

for resistance
Sign ~~not~~ not
need not
be considered

$$\Rightarrow R_{if} = \frac{R_f + R_o}{1 + A_{OL}}$$

Output Resistance R_{of}

Output impedance R_{of} (without R_h) is calculated from the open circuit voltage V_{oc} and short circuit output current i_{sc} .



equivalent circuit for computing R_{of}

Under short circuit conditions at O/P

$$i_A = \frac{V_i - 0}{R_1 + R_f}$$

$$i_B = \frac{A_{OL} V_d}{R_o} \quad \text{--- (4)}$$

$$\boxed{V_d = -i_A R_f} \quad \text{Sub } V_d \text{ in (4)}$$

$$i_B = \frac{-A_{OL} i_A R_f}{R_o}$$

Applying KCL at node ①

$$i_{sc} = i_A + i_B = i_A + \frac{A_{OL} i_A R_f}{R_o} = i_A \left(1 + \frac{A_{OL} R_f}{R_o}\right)$$

$$= \frac{V_i}{R_i + R_f} \left[1 + \frac{A_{OL} R_f}{R_o}\right]$$

$$\boxed{i_{sc} = \frac{V_i (R_o - A_{OL} R_f)}{R_o (R_i + R_f)}} \quad \text{--- (5)}$$

Since $R_{of} = \frac{V_{oc}}{i_{sc}}$ --- (6) $A_{OL} = \frac{V_{oc}}{V_i} \Rightarrow \boxed{V_{oc} = A_{OL} V_i}$

Sub. ⑤ & 6 in ⑦

$$R_{of} = \frac{A_{OL} V_i}{V_i \left(\frac{R_o - A_{OL} R_f}{R_o (R_i + R_f)} \right)} = \frac{A_{OL}}{\frac{R_o - A_{OL} R_f}{R_o (R_i + R_f)}}$$

Sub. Act from (A)

$$R_{of} = \frac{\cancel{(R_o - A_{OL} R_f)}}{\cancel{R_o + R_f + R_i (1 + A_{OL})}} \cdot \frac{\cancel{R_o - A_{OL} R_f}}{\cancel{R_o (R_i + R_f)}}$$

$$\boxed{R_{of} = \frac{R_o (R_i + R_f)}{R_o + R_f + R_i (1 + A_{OL})}}$$

Re-arranging

$$R_{of} = \frac{\frac{R_o(R_i + R_f)}{R_o + R_i + R_f}}{1 + \frac{R_i A_{OL}}{R_o + R_i + R_f}}$$

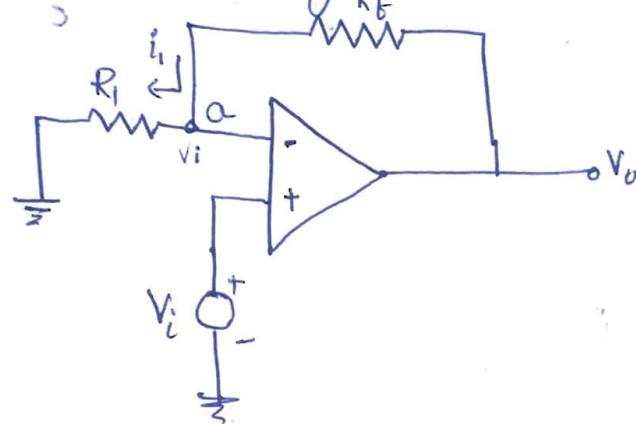
In eqn(8) numerator term shows $R_o || (R_i + R_f)$;

Equivalent resistance will be smaller than R_o .

The output resistance R_{of} (with feedback) is \therefore always than R_o and for $A_{OL} \rightarrow \infty$, $R_{of} \rightarrow 0$.

Non-inverting amplifier

If a signal is applied to the non-inverting input terminal and feedback is given as shown in fig.



Non-inverting amplifier

The circuit amplifies without inverting the input signal, ~~thus~~ thus it is called non-inverting amplifier.

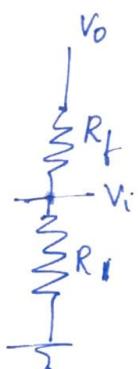
→ Negative feedback is given to the op-amp

As $v_d = 0$ (differential v/g) at the input terminals of the op-amp, the voltage at node 'a' is v_i , same as I/P v/g at non-inverting terminal.

⇒ R_f and R_i forms a potential divider circuit.

$$v_i = \frac{V_o R_i}{R_i + R_f}$$

$$\frac{V_o}{V_i} = \frac{R_i + R_f}{R_i}$$



$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

(17)

∴ The gain of the non-inverting op-amp in closed loop

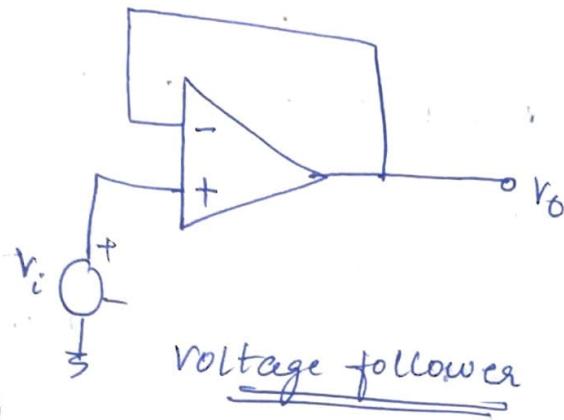
$$A_{cl} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_i} \quad \text{--- } ①$$

The gain can be adjusted to unity or more by proper selection of resistors R_f and R_i .

Compared to the inverting amplifier, the input resistance of the ~~non~~ non-inverting amplifier is extremely large ($= \infty$). As the op-amp draws negligible current from the signal source.

Voltage Follower

In the non inverting amplifier if $R_f = 0$ and $R_i = \infty$ the ckt would be as shown below



From eqn ①

$$\frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}$$

$$\frac{V_o}{V_i} = 1 \Rightarrow V_o = V_i$$

i.e, the output voltage is equal to input voltage, both in magnitude and phase.

This also indicates that the o/p follows I/p voltage
Hence this circuit is also called as voltage follower

Unity gain ckt is used due to high input impedance
(in $M\Omega$ for practical op-amp) and low output impedance

\therefore It draws negligible current from the source

→ Thus a V/g follower can be used as buffers for impedance matching. i.e ~~when~~ to connect a high impedance source to a low impedance load.

Problems

① Design an amplifier with a gain of +5V using one op-amp

Soln Gain is positive \Rightarrow non inverting amplifier

$$A_{CL} = +5V$$

$$\text{gain } A_{CL} = 1 + \frac{R_f}{R_1}$$

$$\text{Let } R_1 = 10k\Omega \Rightarrow 5 = 1 + \frac{R_f}{10k\Omega}$$

$$R_f = 40k\Omega$$

② For the op-amp non-inverting amplifier let $R_1 = 5k\Omega$,

$R_f = 20k\Omega$ and $V_i = 1V$. A load resistance of $5k\Omega$ is connected at the output. Calculate (i) V_o (ii) A_{CL} (iii) i_L

Load current

(iv) The output current i_o indicating proper direction of flow.

$$(i) V_o = \left(1 + \frac{R_f}{R_1}\right) V_i = \left(1 + \frac{20k\Omega}{5k\Omega}\right) 1 = 5V$$

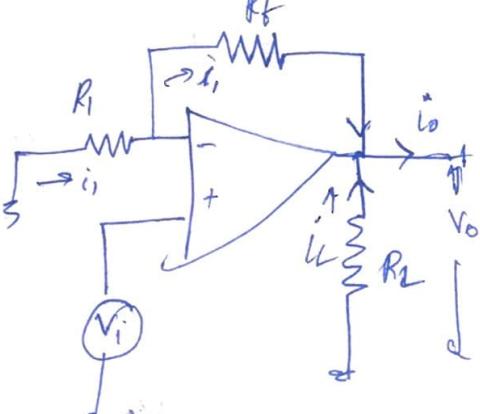
$$(ii) A_{CL} = 1 + \frac{R_f}{R_1} = 5 \quad \text{or} \quad A_{CL} = \frac{V_o}{V_i} = \frac{5V}{1V} = 5$$

$$(iii) \text{ Load current } i_L = \frac{V_o}{R_L} = \frac{5V}{5k\Omega} = 1mA$$

$$(iv) \text{ Total output current } i_o = i_L + i_1 \rightarrow \text{load current + current through } R_1$$

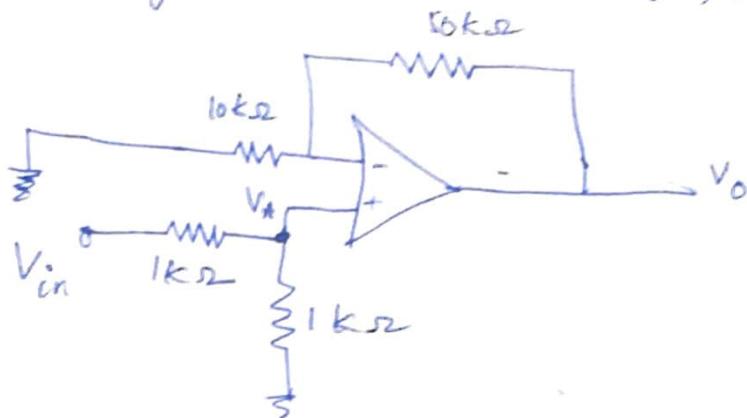
$$\text{Current } i_1 = \frac{V_o}{R_1} = \frac{1}{5k\Omega} = 0.2mA$$

$$i_o = 1mA + 0.2mA$$



Op-amp output current i_o flows outwards

③ For the fig shown calculate V_o , if $V_{in} = 1V$



Non-inverting amplifier

Voltage at node A is obtained by applying
Voltage divider

$$V_A = V_{in} \frac{1k\Omega}{1k\Omega + 10k\Omega} = 0.5V_{in}$$

$$\boxed{V_A = 0.5V}$$

Output voltage V_o

$$A_{CL} = \left(1 + \frac{R_f}{R_i}\right)$$

$$A_{CL} = 1 + \frac{50k\Omega}{10k\Omega} = 6$$

The same potential exists at ~~non-inverting~~ - inverting and non inverting terminal

$V_A \Rightarrow$ input given to opamp

$$\therefore A_{CL} = \frac{V_o}{V_A}$$

$$V_o = A_{CL} V_A \\ = 6 \times 0.5 V$$

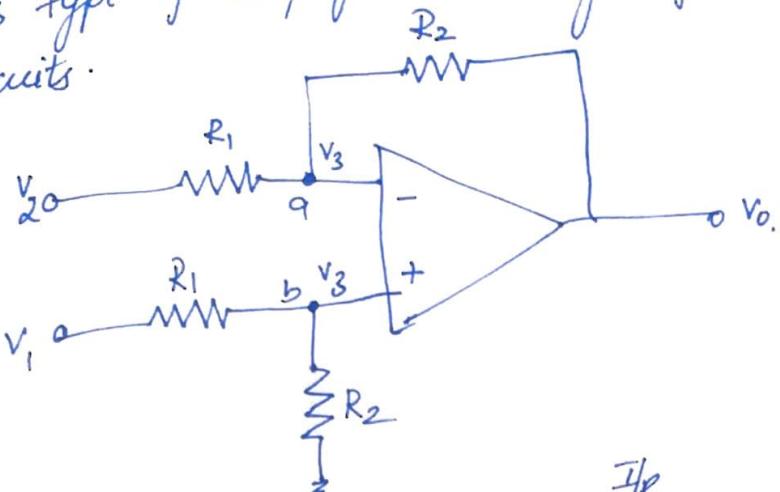
$$\boxed{V_o = 3V}$$

(27)

Differential Amplifier

A circuit the amplifier the signal b/w two signals is called a difference or differential amplifier.

→ This type of amplifiers is very useful in ~~the~~ instrumentation circuits.



The differential v/g b/w the terminals are zero. if
b are at same potential (V_3) .

Nodal Analysis at node 'a'

$$\frac{V_3 - V_2}{R_1} + \frac{V_3 - V_0}{R_2} = 0 \Rightarrow V_3 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_2}{R_1} = \frac{V_0}{R_2} \quad (1)$$

Nodal Analysis at 'b'

$$\frac{V_3 - V_1}{R_1} + \frac{V_3}{R_2} = 0 \Rightarrow V_3 \left(\frac{1}{R_1} + \frac{1}{R_2} \right) = \frac{V_1}{R_1} \quad (2)$$

Sub (2) in (1)

$$\frac{V_1}{R_1} - \frac{V_2}{R_1} = \frac{V_0}{R_2}$$

$$\frac{V_0}{R_2} = \frac{(V_1 - V_2)}{R_1}$$

$$\therefore V_0 = \frac{R_2}{R_1} (V_1 - V_2)$$

Such a circuit is very useful in detecting very small differences in signals. ∵ Gain $\frac{R_2}{R_1}$ can be chosen to be large.

Example :-

if $R_2 = 100R_1$, then even the small difference in $V_1 \& V_2$ (i.e. $V_1 - V_2$) is amplified 100 times.

Difference mode and Common-mode gains

If $V_1 = V_2$ then $V_O = 0$

i.e. signal common to both inputs gets cancelled and produces no output V_{Og} (in case of ideal opamp). A practical opamp exhibits some small responses to the common mode component of the input voltages too.

Ex:- The output will have different values for

Case 1: $V_1 = 100 \mu V$ and $V_2 = 50 \mu V$

Case 2: $V_1 = 1000 \mu V$ and $V_2 = 950 \mu V$

even though difference signal in both the cases is $50 \mu V$. The output V_{Og} depends not only on the difference $I/P(V_d)$ but also on the average voltage of the I/P signals called as the common-mode signal V_{cm} defined

$$V_{cm} = \frac{V_1 + V_2}{2} \quad \text{--- (1)}$$

For a differential op-amp though circuit is symmetric because of the mismatch the gain at the output w.r.t positive terminal is slightly different in magnitude to that of negative terminal. Thus with the same voltage applied to both the inputs, the output is not zero.

∴ the output is expressed as

$$V_O = A_1 V_1 + A_2 V_2 \quad \text{--- (2)}$$

(28)

where A_1 is

- gain of the op-amps when input is given to non inverting terminal and inverting terminal is grounded

$A_2 \rightarrow$ gain of opamp when I/p is given to inverting terminal and non-inverting terminal is grounded

$$\text{Wkt that } V_d = V_1 - V_2 \quad \text{--- (3)}$$

From equation (2) and (3)

$$V_{cm} = \frac{V_1 + V_2}{2} \quad V_d = V_1 - V_2$$

$$2V_{cm} = V_1 + V_2 \Rightarrow 2V_{cm} = V_1 + V_1 - V_d.$$

$$V_d = V_1 - V_2 \Rightarrow V_2 = V_1 - V_d \quad \downarrow$$

$$2V_{cm} = 2V_1 - V_d$$

$$2V_1 = 2V_{cm} + V_d$$

$$V_1 = V_{cm} + \frac{V_d}{2}$$

$$V_2 = V_d + V_2$$

~~$V_{cm} = \frac{V_d + V_2 + V_2}{2}$~~

$$V_{cm} = \frac{V_d + V_2}{2}$$

$$V_2 = V_{cm} - \frac{V_d}{2} \quad \text{--- (5)}$$

Sub (4) & (5) in (2)

$$V_o = A_1 \left(V_{cm} + \frac{V_d}{2} \right) + A_2 \left(V_{cm} - \frac{V_d}{2} \right)$$

$$= V_{cm} \left(A_1 + A_2 \right) + V_d \left(\frac{A_1}{2} - \frac{A_2}{2} \right)$$

$$V_o = A_{cm} V_{cm} + A_{dm} V_d \quad \text{--- (6)}$$

Common mode

Signal gain $A_{cm} = A_1 + A_2$ node v_{tg}/signal

$$A_{dm} = \frac{A_1 - A_2}{2}$$

differential gain

v_{tg} gain for the difference

Common mode Rejection Ratio (CMRR)

The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio (CMRR)

It gives the figure of merit (β) for the differential amplifier

CMRR is given by

$$\text{CMRR} = \beta = \left| \frac{A_{dm}}{A_{cm}} \right|$$

It is expressed in decibels.

MA741 op-amp has minimum CMRR for 40 dB precision op-amp MA725A has a minimum CMRR of 120 dB

A_{dm} should be large and A_{cm} should be zero

ideally

\Rightarrow Higher the value of CMRR, better is the op-amp.

Problems

- ① The figure shows the differential amplifier using ideal op-amps
- ⓐ Find the output voltage V_o
- ⓑ Show that the output corresponding to common mode voltage

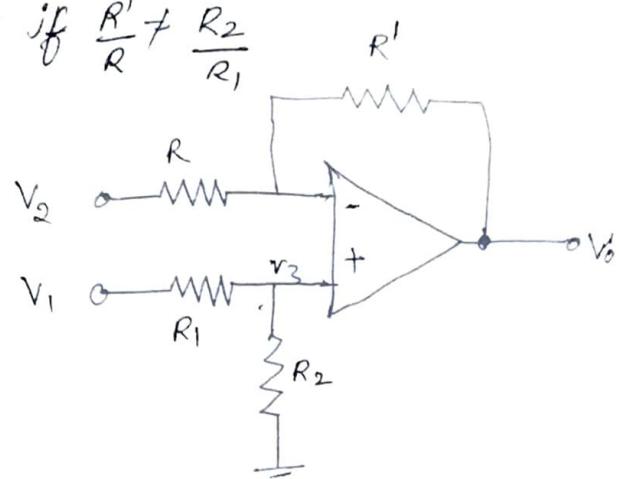
$$V_{cm} = \frac{V_1 + V_2}{2} \text{ is zero if } \frac{R'}{R} = \frac{R_2}{R_1} \quad \text{Find } V_o \text{ in this case}$$

Q) Find CMRR of the amplifier if $\frac{R'}{R} \neq \frac{R_2}{R_1}$

(2)

Ans: v/g at the non-inverting terminal

$$V_3 = \frac{R_2}{R_1 + R_2} V_1$$



O/P v/g in the inverting amplifier

$$V_{O2} = -\frac{R'}{R_1} V_2$$

O/P v/g in the non-inverting amplifier

$$V_{O1} = \left(1 + \frac{R'}{R}\right) V_3$$

We know that $V_0 = V_{O1} + V_{O2}$

$$V_0 = -\frac{R'}{R} V_2 + \frac{R+R'}{R} \left(\frac{R_2}{R_1+R_2}\right) V_1 \quad \text{--- (1)}$$

We know that

$$V_{CM} = \frac{(V_1 + V_2)}{2} \quad V_d = V_1 - V_2$$

Solve for

$$V_1 = V_{CM} + \frac{V_d}{2} \quad V_2 = V_{CM} - \frac{V_d}{2}$$

$$V_0 = -\frac{R'}{R} \left(V_{CM} - \frac{V_d}{2} \right) + \frac{R_2}{R} \frac{(R+R')}{(R_1+R_2)} \left(V_{CM} + \frac{V_d}{2} \right)$$

$$V_0 = V_{CM} \left[\frac{R_2}{R_1} \left(\frac{R+R'}{R_1+R_2} \right) - \frac{R'}{R} \right] + \frac{V_d}{2} \left[\frac{R_2}{R} \left(\frac{R+R'}{R_1+R_2} \right) + \frac{R'}{R} \right]$$

(b) if $\frac{R'}{R} = \frac{R_2}{R_1}$

--- (2)

$$\frac{R'}{R} + 1 = \frac{R_2 + R'}{R_1}$$

$$\frac{R' + R}{R} = \frac{R_2 + R_1}{R_1}$$

Sub in ②

$$V_o = \left(\frac{\cancel{R_1+R_2}}{R_1} \right) \left(\frac{R_2}{\cancel{R_1+R_2}} \right) - \frac{R_2}{R_1} V_{cm} + \frac{V_d}{2} \left[\frac{R_2}{R_1} + \left(\frac{R_1+R_2}{R_1} \right) \frac{R_2}{R_1+R_2} \right]$$

$$V_o = \left(\frac{R_2}{R_1} - \frac{R_2}{R_1} \right) V_{cm} + \frac{V_d}{2} \left(\frac{2R_2}{R_1} \right)$$

$$\boxed{V_o = \frac{R_2}{R_1} V_d}$$

$$\therefore (0) V_{cm} = 0$$

thus op[↑] corresponding to common mode V_g is zero

c) CMRR = ?

$$\frac{A_{dm}}{A_{cm}} = \frac{\left(\frac{R'}{R} + \frac{R_2}{R} \frac{R+R'}{R_1+R_2} \right) \frac{1}{2}}{\frac{R_2}{R} \left(\frac{R+R'}{R_1+R_2} \right) - \frac{R'}{R}}$$

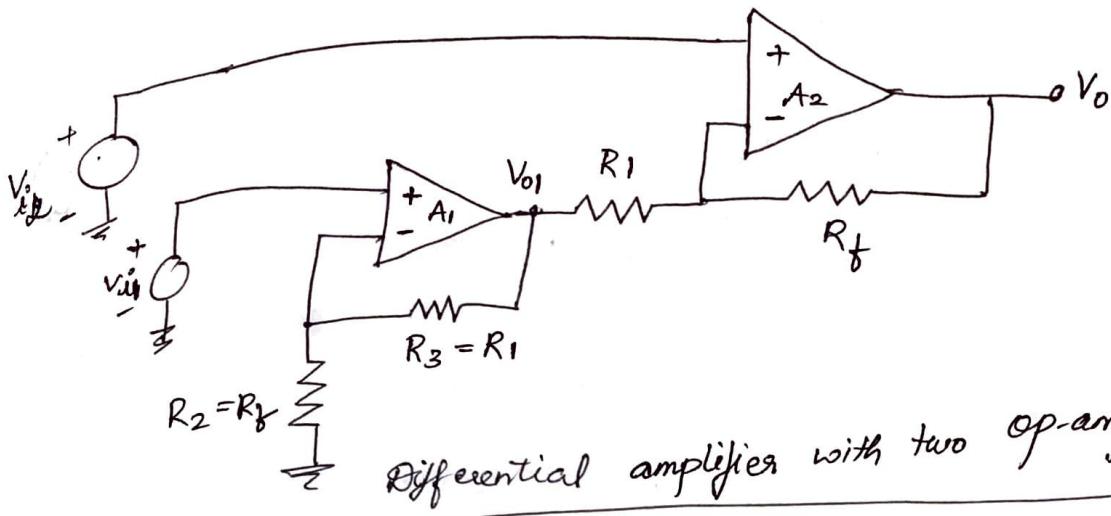
$$= \frac{\cancel{R} \left(\frac{R'(R_1+R_2) + R_2(R+R')}{R(R_1+R_2)} \right) \frac{1}{2}}{\cancel{R} \left(\frac{R_2(R+R') - R'(R_1+R_2)}{R(R_1+R_2)} \right)}$$

$$\boxed{CMRR = \frac{R'(R_1+R_2) + R_2(R+R')}{R'(R_1+R_2) - R_1(R+R')}}$$

Differential op-amp with Two Op-Amps

→ consists of a non inverting amplifier formed by A₁ op-amp

→ V_{o1} (output of A₁) goes to Op-Amp A₂ which is working as a differential amplifier.



→ The advantage of 2 stage differential amplifier is the overall gain can be increased and input resistance of such a circuit also increases.

o/p voltage of first stage

$$V_{o1} = \left(1 + \frac{R_3}{R_2}\right) V_{i1}^o \quad \textcircled{1}$$

For the differential amplifier A_2 , V_{o1} and V_{i2}^o are the inputs

$$V_o = \left(-\frac{R_f}{R_1}\right) V_{o1} + \left(1 + \frac{R_f}{R_1}\right) V_{i2}^o$$

Subs V_{o1} in $\textcircled{1}$

$$V_o = \left(-\frac{R_f}{R_1}\right) \left(1 + \frac{R_3}{R_2}\right) V_{i1}^o + \left(1 + \frac{R_f}{R_1}\right) V_{i2}^o$$

Assuming $R_3 = R_1$ & $R_f = R_2$

$$V_o = \left(-\frac{R_f}{R_1}\right) \left(1 + \frac{R_3}{R_f}\right) V_{i1}^o + \left(1 + \frac{R_f}{R_1}\right) V_{i2}^o$$

$$= \left(-\frac{R_f}{R_1} - 1\right) V_{i1}^o + \left(1 + \frac{R_f}{R_1}\right) V_{i2}^o$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) (V_{i2}^o - V_{i1}^o)$$

Gain of 2 op-amp differential amplifier is given by

$$A_D = \frac{V_o}{V_{i1}^o}$$

$$[V_{id} = V_{i2}^o - V_{i1}^o]$$

$$A_D = \left(1 + \frac{R_f}{R_i}\right) V_{od}$$

$$A_D = \left(1 + \frac{R_f}{R_i}\right)$$

Input Resistance

The input resistance R_i of a differential amplifier is the resistance looking into either of the two non-inverting I/P terminals with other I/P grounded.

1st stage is a non inverting amplifier & its input resistance is $R_{i1} = R_i (1 + A\beta_1)$

where $A \rightarrow$ Open loop gain of op-amp

$$\beta_1 = \frac{R_2}{R_2 + R_3}$$

$R_i \rightarrow$ open loop resistance of op-amp

By shorting V_{iz} input to ground, 2nd stage is also working as non-inverting amplifier.

Input resistance $R_{i2} = R_i (1 + A\beta_2)$

$$\text{where } \beta_2 = \frac{R_1}{R_1 + R_f}$$

Assuming $R_1 = R_3$ & $R_f = R_2$

we find that $R_{i1} \neq R_{i2}$ since $R_{i1} \neq R_{i2}$
loading of I/P sources V_{i1} and V_{i2} will take place &
op signal may be less amplified.

Problems on differential amplifier ~~contd~~ in page 35

operational Amplifiers Internal circuit

(24)

- Differential Amplifier
- Intermediate Stage / Diff. amplifier
- Buffer & level translator
- Output stage.

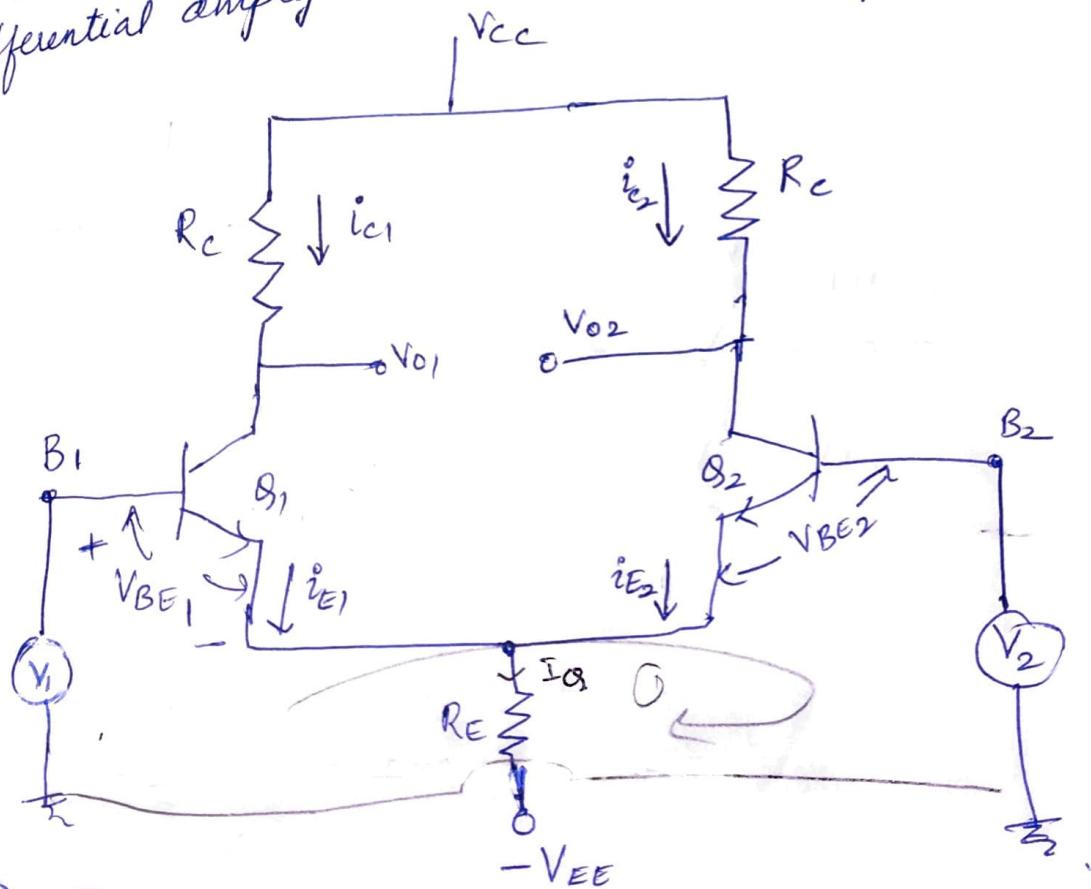
Differential Amplifier:-

→ purpose of differential amplifiers is to provide high gain to the difference mode signal and cancel the common mode signal.

A cascaded direct coupled amplifiers can provide high gain down to zero frequency as it has no coupling capacitors.

→ Such amplifiers suffers from major problem of drift of the operating point due to temperature dependency on I_{CO} , V_{BE} , life of the transistor.

→ It can be eliminated by using a balanced or differential amplifiers as shown in fig.



① The basic differential amplifier

→ Emitter coupled differential amplifier, it has low drift on account of symmetrical construction.

A differential amplifier can be used in four different configurations depending upon no. of I/P signals used & way O/P is taken. These configurations are

- ① differential I/P, differential O/P or Dual I/P balanced O/P
- ② Differential I/P single-ended O/P
- ③ Single I/P differential output.
- ④ Single I/P single ended O/P.

If signal is applied to both the inputs then it is differential input or dual I/P

If the output V_{dg} is measured between two collectors then it is a differential output. It is also referred to balanced O/P as both collectors are at same d.c. potential w.r.t ground.

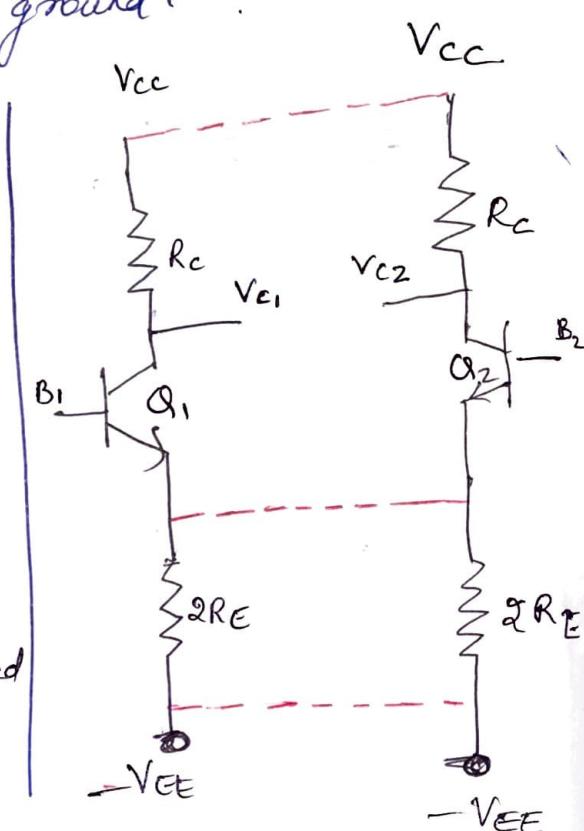
$$V_{O1} = V_{cc} - i_{C1} R_C$$

$$V_{O2} = V_{cc} - i_{C2} R_C$$

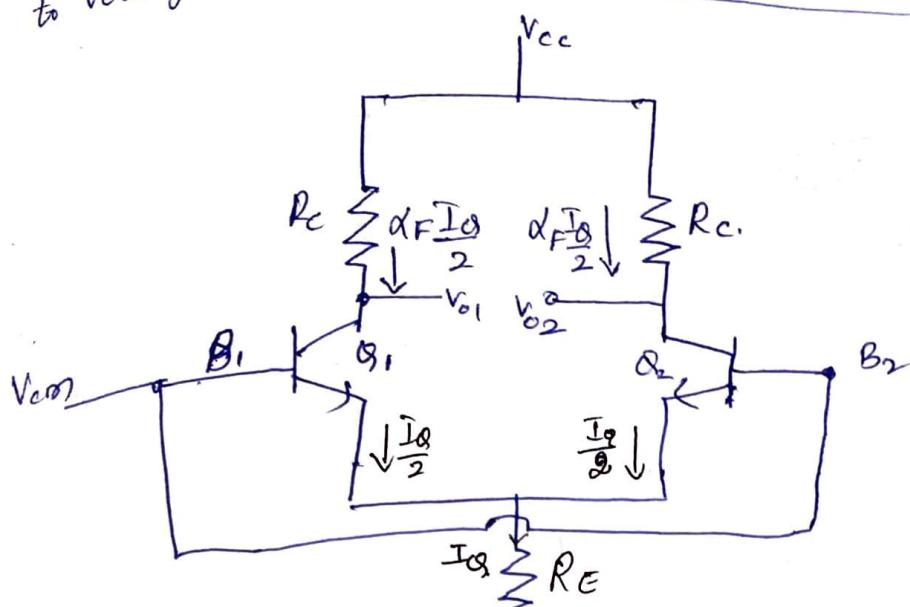
$$V_o = V_{O2} - V_{O1}$$

$$V_o = (i_{C2} - i_{C1}) R_C$$

2 CE amplifiers →
are directly
emitter coupled



Case 1 Let us consider when B_1 and B_2 are shorted and connected to voltage V_{cm} . called common mode voltage



Differential pair with a common-mode input signal V_{cm}

$$\therefore V_1 = V_2 = V_{cm}$$

Thus Q_1 & Q_2 are forward biased and matched due to circuit symmetry

↓
Current I_Q divides equally through Q_1 & Q_2

$$i_{E1} = i_{E2} = \frac{I_Q}{2}$$

We know that $i_C = \alpha i_E$

$$\text{Collector current } i_{C1} = \alpha i_{E1} = \alpha \frac{I_Q}{2}$$

$$\text{at } Q_1 \& Q_2 \quad i_{C2} = \alpha i_{E2} = \alpha \frac{I_Q}{2}$$

$$\therefore \text{Collector v/g } V_{o1} \text{ at } Q_1 = V_{cc} - R_c \left(\alpha \frac{I_Q}{2} \right)$$

$$\text{Collector v/g } V_{o2} \text{ at } Q_2 = V_{cc} - R_c \left(\alpha \frac{I_Q}{2} \right)$$

The difference v/g between the two collectors

$$V_o = V_{o1} - V_{o2} = 0$$

Even if V_{cm} is varied o/p V/g is not varied. Thus (32) the differential pair does not respond to the common mode signals.

Case 2:- V_2 is made zero.

$$V_1 = 1V.$$

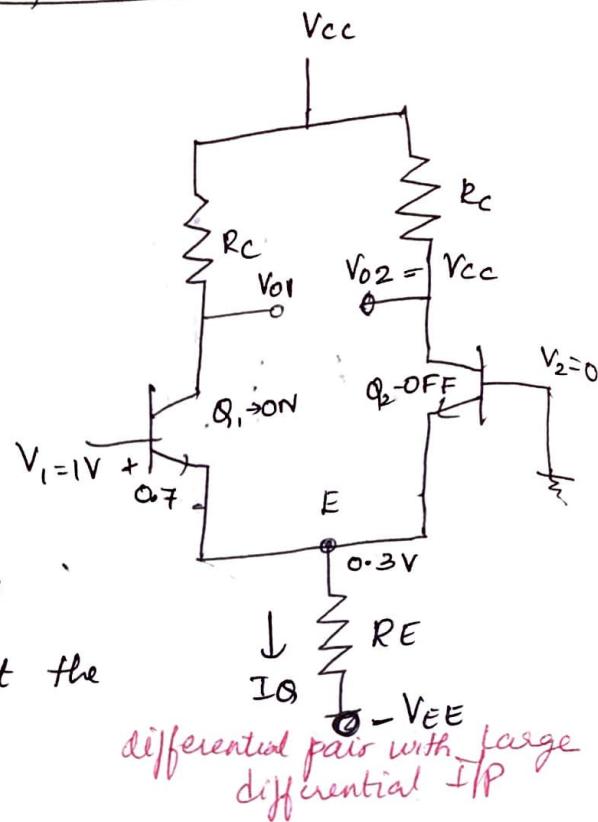
Q_1 will conduct (Q_1 is ON)

Q_2 is OFF.

\therefore The entire current I_Q

flows through the Emitter of Q_1

since Q_1 is on, Voltage at the
emitter $V_E = 0.3V$.



Emitter V/g of $Q_2 = 0.3V$ & Base V/g of $Q_2 = 0$ therefore

Emitter base junction of Q_2 is reverse biased.

$\therefore Q_2$ is OFF.

The collector voltages

$$\underline{V_{01} = V_{cc} - \alpha I_Q R_C}$$

$$\underline{V_{02} = V_{cc}}$$

Case 3 $V_2 = 0V$ $V_1 = -1V$.

Q_1 will be off Q_2 is ON.

\therefore the entire current flows through Q_2

The voltage at common Emitter point $E = -0.7V$

which makes Q_1 off and Q_2 ON.

Collector V/gs $V_{01} = V_{cc}$

$$V_{02} = V_{cc} - \alpha I_Q R_C.$$

from all the three cases we can observe that the differential pair responds only to the difference mode signals and rejects the common mode signals (33)

Transfer characteristics

The collector currents i_{C1} and i_{C2} for Q₁ & Q₂ in the differential amplifier is biased in forward active mode is given by

$$i_{C1} = \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad (1)$$

$$i_{C2} = \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad (2)$$

where I_{ES} \rightarrow reverse saturation current of emitter-base junction
 V_T \rightarrow volts equivalent to temperature

$$\frac{i_{C1}}{i_{C2}} = \frac{\alpha_F I_{ES} e^{V_{BE1}/V_T}}{\alpha_F I_{ES} e^{V_{BE2}/V_T}}$$

$$\frac{i_{C1}}{i_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \quad (3)$$

Applying KVL to the loop containing two emitter based junctions

$$V_1 - V_{BE1} + V_{BE2} - V_2 = 0$$

$$V_{BE1} - V_{BE2} = V_1 - V_2 = V_d$$

$V_d \rightarrow$ difference of 2 input voltages.

$$I_Q = i_{E1} + i_{E2}$$

$$\text{wkt } i_C = \alpha I_E \Rightarrow i_e = \frac{i_C}{\alpha}$$

$$I_Q = \frac{i_{C1}}{\alpha_F} + \frac{i_{C2}}{\alpha_F}$$

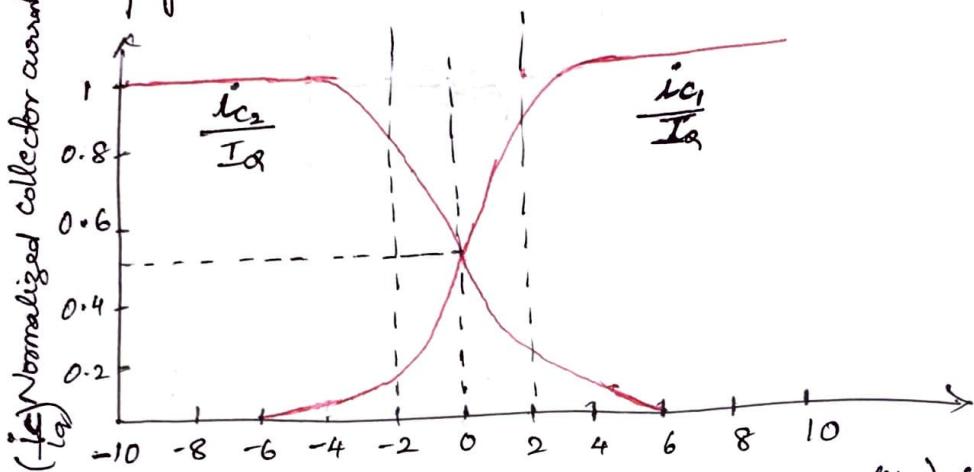
$$= \frac{i_{C1}}{\alpha_F} \left(1 + \frac{i_{C2}}{i_{C1}} \right) \quad (4)$$

Solving for \dot{i}_{c_1} & \dot{i}_{c_2} using ③ and ④

$$\dot{i}_{c_1} = \frac{\alpha_F I_Q}{1 + e^{-V_d/V_T}} \quad \text{--- } ⑤$$

$$\dot{i}_{c_2} = \frac{\alpha_F I_Q}{1 + e^{V_d/V_T}} \quad \text{--- } ⑥$$

From eqn ⑤ and ⑥ the normalized transfer characteristics
 $\left[\left(\frac{\dot{i}_c}{I_Q} \right) \text{ vs } \left(\frac{V_d}{V_T} \right) \text{ assuming } \alpha_F = 1 \right]$ for a
 differential amplifier are obtained as shown in fig



Normalized differential input voltage $\left(\frac{V_d}{V_T} \right)$ ($\alpha_F = 1$)

Normalized transfer characteristics for the differential pair

Inference from the transfer characteristics

- ① $V_d > 4V_T$ $\dot{i}_{c_1} \approx \alpha_F I_Q$ and $\dot{i}_{c_2} = 0$ By proper choice of
 $\therefore V_{o1} = V_{cc} - \alpha_F I_Q R_C$ R_C, V_{o1} can be made
 $V_{o2} = V_{cc}$ very small.

- ② $V_d < -4V_T$ $\dot{i}_{c_2} \approx \alpha_F I_Q$ and $\dot{i}_{c_1} = 0$ By choosing large R_C
 $V_{o1} = V_{cc}$
 $V_{o2} = V_{cc} - \alpha_F I_Q R_C$ V_{o2} can be made small
 (negligible)

$$\therefore 4V_T < V_d < -4V_T$$

differential amplifier behaves as a switch.

differential amplifier functions as a good limiter for

(3)

$$V_d > \pm 4V_T$$

(limiter circuit \rightarrow a circuit whose output is restricted to a certain range of values irrespective of the size of the input)

\rightarrow A limiter is a circuit that allows signals below a specified input power or level to pass ~~unattenuated~~ unaffected while attenuating (lowering) the peaks of stronger signals that exceed this threshold)

(4) Function as an automatic gain control (AGC) by varying V_d

(5) $-2V_T \leq V_d \leq 2V_T \rightarrow$ D.A functions as a linear

amplifier.

$V_d \leq 2V_T$ (ie V_d should be smaller than 50mV)

Problems

(1) For the differential amplifier circuit shown in fig. Given that $R_1 = R_3 = 560\Omega$, $R_f = R_2 = 5.6k\Omega$, $V_{i2} = 2V$ (P-P), $V_{i1} = 1V$ (P-P), $R_i = 2M\Omega$ and open loop gain $A_{OL} = 2 \times 10^5$.

Determine (i) Voltage gain

(ii) input resistance

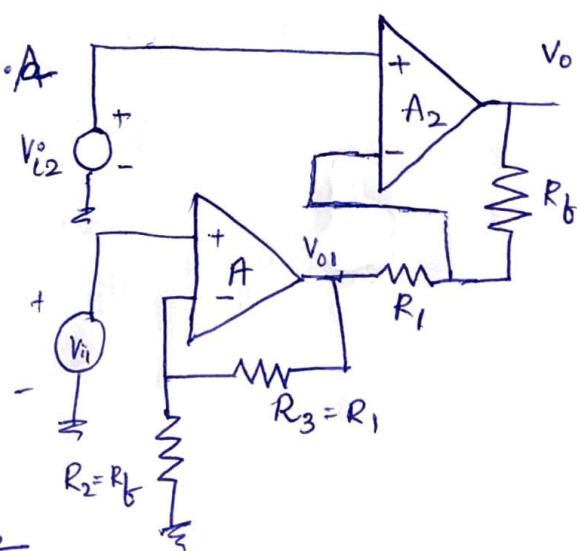
(iii) output voltage of the D.A

$$(i) A_D = 1 + \frac{R_f}{R_1}$$

$$= 1 + \frac{5.6k\Omega}{560\Omega} = 11$$

$$(ii) R_1 = R_3 \& R_f = R_2$$

\therefore the value of input resistance $R_{i1} = R_{i2}$



$$R_{i1} = R_i [1 + A_{OLB}]$$

$$= R_i \left[1 + \frac{A_{OL} R_2}{R_2 + R_3} \right] = 2 \times 10^6 \left[1 + \frac{2 \times 10^5 \times 560}{560 + 5.6 \times 10^3} \right]$$

$$= 36.37 \text{ GHz}$$

$$R_{i1} = R_{i2} = 36.37 \text{ GHz}$$

iii) Output voltage of the differential amplifier

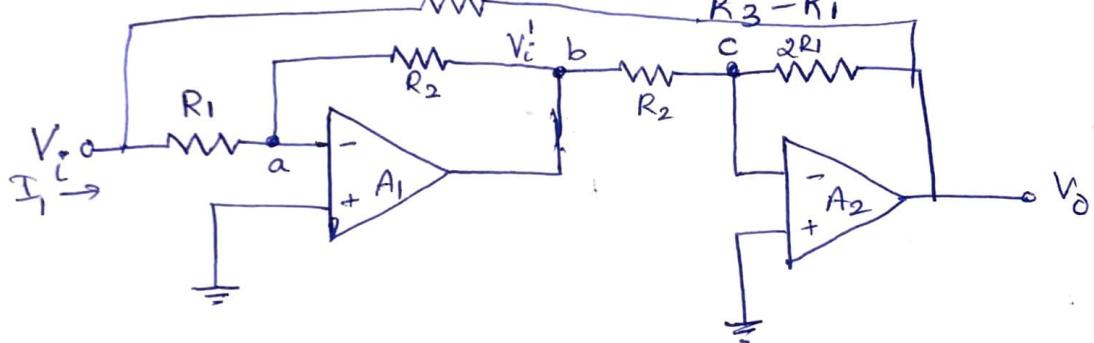
$$V_o = A_D V_{id}$$

$$= A_D (V_{i2} - V_{i1})$$

$$= 11 (2 - 1)$$

$$\boxed{V_o = 11 \text{ V (p-p)}}$$

(2) For the circuit shown in fig., show that the ~~input~~ input resistance is given by $R_i = \frac{R_1 R_3}{R_3 - R_1}$



Solution At node 'a' of op-amp A1, the current I_i is

$$\frac{V_i - 0}{R_1} = \frac{V_i' - 0}{R_2} \Rightarrow \frac{V_i}{R_1} = \frac{V_i'}{R_2} \quad \textcircled{1}$$

for op-amp A2 with input V_i' at node 'b' the current entering at node 'c' is given by

$$\frac{V_o - 0}{2R_1} = \frac{V_i' - 0}{R_2} \Rightarrow \frac{V_o}{2R_1} = \frac{V_i'}{R_2} \quad \textcircled{2}$$

From ① & ②

$$\frac{V_i^o}{R_1} = \frac{V_o}{2R_1}$$

$V_o = 2V_i^o$

— ③

The current I_i from source V_i is given by the sum of currents through R_1 and R_3

$$I_i^o = \frac{V_i - V_o}{R_1} + \frac{V_i - V_o}{R_3}$$

Sub V_o from ③

$$I_i^o = \frac{V_i}{R_1} + \frac{V_i - 2V_i^o}{R_3} = \frac{V_i}{R_1} - \frac{V_i^o}{R_3}$$

$$I_i^o = V_i^o \left[\frac{1}{R_1} - \frac{1}{R_3} \right] = \frac{V_i^o (R_3 - R_1)}{R_1 R_3}$$

The input impedance $R_i = \frac{V_i}{I_i^o}$

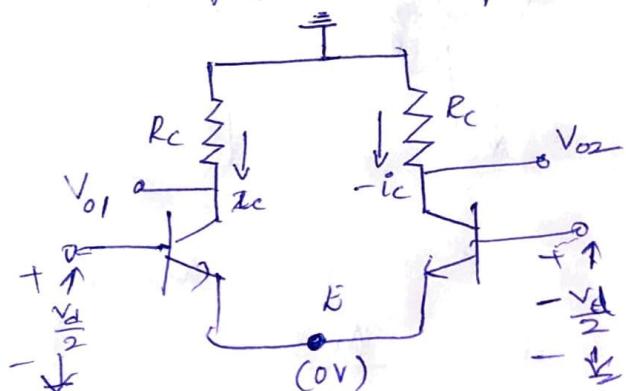
$$R_i = \frac{R_1 R_3}{R_3 - R_1}$$

Low frequency small signal analysis of differential amplifier

In case of practical transistors Q_1 & Q_2 are not equally matched and O/p appears even when the same voltage is applied to the input terminals.

The a.c analysis of the differential amplifier can be performed by using hybrid π -model
→ h-parameter model

Differential mode gain, A_{dm}



If $V_1 = V_2 \rightarrow I_Q$ divides equally in Q_1 & Q_2 \Rightarrow the circuit is symmetric.

If V_1 is \uparrow by voltage $\frac{V_d}{2}$
(small signal)

V_2 is \downarrow by small signal voltage $\left(\frac{V_d}{2}\right)$

There would be a small differential signal V_d .

i_{C1} increases by incremental amount i_c

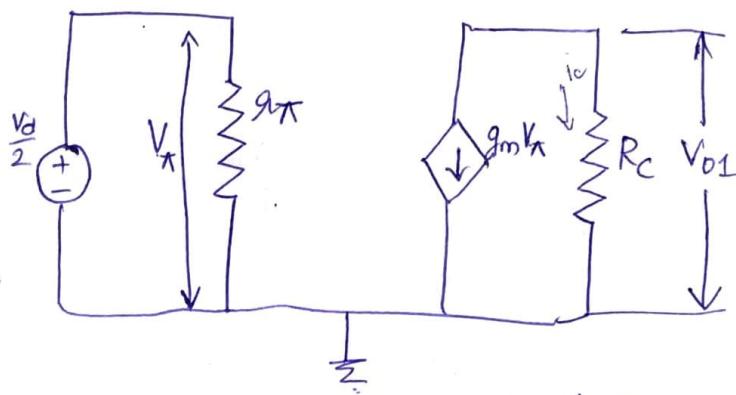
i_{C2} decreases by an equal amount

However total current in Q_1 & Q_2 is same due to const

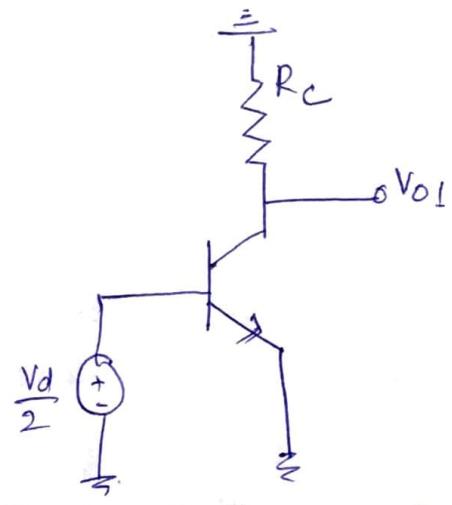
current $I_Q \rightarrow$ For \therefore small signal analysis the common emitter point E remains constant. Thus for small signals analysis, the common emitter can be considered to be at ground potential.

① Using hybrid π model

The performance of two sides of the differential amplifier is identical, we need to analyze only one side of the differential amplifier called differential-half circuit.



② ac-equivalent circuit using hybrid- π model.



③ differential mode half circuit

The fig @ shows the single stage ce amplifier fed by a small signal voltage $\frac{V_d}{2}$ and its a.c equivalent ckt using hybrid- π model is shown in fig (b)

In fig. b.

$$V_A = \frac{V_d}{2}$$

$g_m \rightarrow$ transconductance

$$g_m V_A = g_m \frac{V_d}{2}$$

$$\therefore V_{o1} = -g_m \frac{V_d}{2} R_C$$

$$\boxed{\frac{V_{o1}}{V_d} = -\frac{1}{2} g_m R_C}$$

Similarly

$$\boxed{\frac{V_{o2}}{V_d} = \frac{1}{2} g_m R_C}$$

The output voltage signal of a differential amplifier

\Rightarrow differential O/P \rightarrow differential I/P

$$A_{DM} = \frac{O/P \text{ voltage}}{\text{Input voltage}} = \frac{V_{o1} - V_{o2}}{V_d}$$

$$A_{DM} = \frac{V_{o1}}{V_d} - \frac{V_{o2}}{V_d}$$

$$\boxed{A_{DM} = -g_m R_C}$$

(differential I/P
- differential O/P)

\Rightarrow O/P is single-ended (O/P is taken between collector of transistor Q₁ & ground)

$$\boxed{\frac{A_{DM}}{V_d} = \frac{V_{o1}}{V_d} = -\frac{1}{2} g_m R_C}$$

(differential I/P
- single ended O/P)

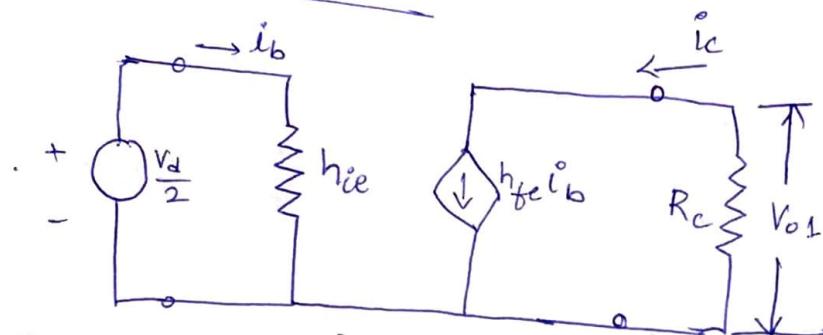
O/P is between Q₂ & ground

$$\boxed{A_{DM} = \frac{V_{o2}}{V_d} = \frac{1}{2} g_m R_C}$$

In the above analysis output resistance r_o of transistor is not considered. If r_o is included

$$\boxed{A_{DM} = -g_m (R_C \parallel r_o)}$$

21

Using 'h' parameters

$h_{fe} \rightarrow$ hybrid parameter
forward current
gain, common
emitter

$h_{ie} \rightarrow$ input impedance

Small signal equivalent circuit of differential half circuit using h-parameter model

$$V_{o1} = -i_c R_C = -h_{fe} i_b R_C$$

$$\text{and } \frac{V_d}{2} = i_b h_{ie} \Rightarrow V_d = 2 i_b h_{ie}$$

∴ differential mode gain A_{dm} is given by

$$A_{dm} = \frac{-V_{o1}}{V_d} = \frac{-h_{fe} i_b R_C}{2 i_b h_{ie}}$$

$$A_{dm} = \frac{V_{o1}}{V_d} = \frac{1}{2} \frac{h_{fe}}{h_{ie}} R_C \quad (\text{Single ended O/P})$$

Similarly $A_{dm} = \frac{V_{o2}}{V_d} = \frac{1}{2} \frac{h_{fe}}{h_{ie}} R_C \quad (\text{Single ended O/P})$

If the output is taken differentially b/w the two collectors then

$$A_{dm} = \frac{V_{o1} - V_{o2}}{V_d} = -\frac{h_{fe} R_C}{h_{ie}} \quad (\text{differential O/P})$$

The source resistance R_s is not considered.

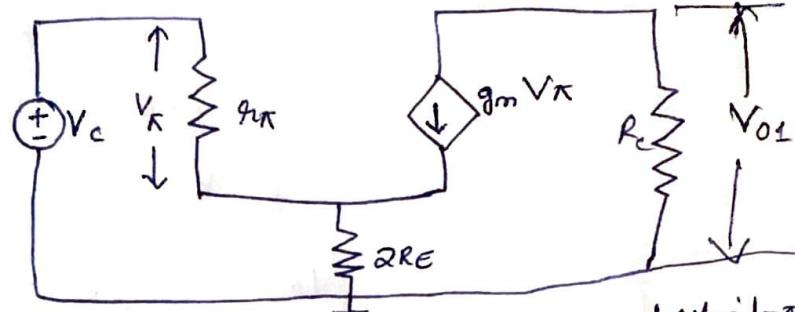
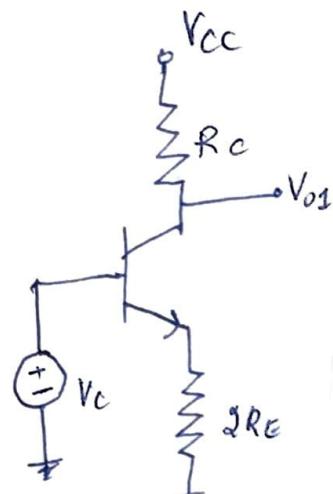
Common mode gain, A_{cm}

Consider when both V_1 and V_2 are increased by an incremental voltage V_c .

The differential signal V_d now is zero and common mode signal is V_c .

The currents i_{c1} & i_{c2} will increase by an incremental current Δi_c
 The current through $R_E \uparrow$ by Δi_c

The v/g V_E at emitter node is now increased by $\frac{\Delta i_c R_E}{2}$ &
 it is no longer constant.



ac-equivalent circuit using hybrid- π model

Common mode half circuit

A_{cm} is calculated from the small signal hybrid- π model shown in fig.

$$A_{cm} = \frac{V_{o1}}{V_c} = \frac{V_{o2}}{V_c} = \frac{-\beta_0 R_C}{g_{m\pi} + 2(1+\beta_0)R_E} \quad \text{--- (1)}$$

$\beta_0 \rightarrow$ small signal CE current gain & is same as h_{fe} .

$$\text{for } \beta_0 \gg 1, \quad A_{cm} = \frac{-g_m R_C}{1 + 2g_m R_E} \quad \text{--- (2)}$$

If o/p is taken single ended common mode gain will be finite.

~~Common~~ A_{cm} using h-parameter can be computed by

$$A_{cm} = \frac{V_{o1}}{V_{ce}} = \frac{-h_{fe} R_C}{h_{ie} + (1+h_{fe})2R_E}$$

$$\therefore CMRR = \frac{A_{cm}}{A_{cm}}$$

$$\text{For DI-DO } CMRR \approx \frac{g_m R_C}{g_m R_C + (1+2g_m R_E)} = 1 + 2g_m R_E$$

$$CMRR \approx \frac{g_m R_C}{2g_m R_E}$$

problems

① Differential amplifier uses a transistor with $\beta = 200$ and is biased at $I_{CQ} = 100 \text{ mA}$. Determine the value of R_C and R_E .

If $|A_{DM}| = 500$, $CMRR = 80 \text{ dB}$

Soh

$$I_{CQ} = 100 \text{ mA}$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{100 \times 10^{-3}}{25 \times 10^{-3}} = 4 \text{ mV} \quad (for V_T = 25 \text{ mV})$$

$$A_{DM} = -g_m R_C \Rightarrow R_C = \frac{A_{DM}}{g_m}$$

$$R_C = \frac{500}{4 \text{ mV}} = 125 \text{ k}\Omega \quad [130 \text{ k}\Omega]$$

To find out R_E

$$CMRR = 2g_m R_E \quad \text{--- (1)}$$

$$CMRR \text{ in } \text{dB} = 80 \leq 20 \log(CMRR)$$

$$\therefore CMRR = \log^{-1}\left(\frac{80}{20}\right)$$

$$CMRR = 10^4$$

Verify eqn (1)

$$10^4 = 2 \times 4 \text{ mV} \cdot R_E$$

$$Solving R_E = 1.25 \text{ M}\Omega$$

$$[1.30 \text{ M}\Omega]$$

② In the basic differential amplifier Given $R_E = 2 \text{ k}\Omega$

$R_E = 4.3 \text{ k}\Omega$, $V_{CC} = |V_{EE}| = 5 \text{ V}$, $\beta_0 = 200$, $V_{BE} = 0.7 \text{ V}$

Determine:

(i) for $V_1 = V_2 = 0$ i.e. for both the inputs grounded. The values of quiescent currents & voltages I_{BQ} , I_{CQ} , V_{OL} , V_{O2} , V_{CEQ}

(ii) A_{DM} , A_{CM} , $CMRR$

Soln (i) For $V_1 = V_2 = 0$ applying KVL for base emitter loop

$$V_{BE} + 2(1+\beta_0) I_{BQ} R_E - V_{EE} = 0$$

$$I_{BQ} = \frac{V_{EE} - V_{BE}}{2(1+\beta_0) R_E} = \frac{5 - 0.7}{2(1+200) 4.3k} = 0.0024 \text{ mA}$$

$$I_{BQ} = 0.0024 \text{ mA} = 2.4 \mu\text{A}$$

$$I_{CQ} = \beta_0 \cdot I_{BQ} = 200 \times 2.4 \mu\text{A} = 0.48 \text{ mA}$$

$$V_{O1} = V_{O2} = V_{cc} - I_C R_C$$

$$V_{O1} = V_{O2} = 5 \text{ V} - 2k2 \times 0.48 \text{ mA}$$

Due to symmetry $V_{O1} = V_{O2} = 4.04 \text{ V}$

$$V_{CEQ} = V_C - V_E \\ = V_{O1} - (-V_{BE}) = V_{O1} + V_{BE}$$

$$V_{CEO} = 4.04 + 0.7 = 4.74 \text{ V}$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.48 \text{ mA}}{26 \text{ mV}} = 18.86 \text{ mS}$$

$$g_{11} = \frac{\beta_0}{g_m} = \frac{200}{18.86 \text{ mS}} = 10.83 \text{ kS}$$

$$A_{dm} = -g_m R_C$$

$$A_{dm} = -18.86 \times 2 \text{ k} = -36.92$$

$$A_{cm} = \frac{-\beta_0 R_C}{g_{11} + 2(1+\beta_0) R_E}$$

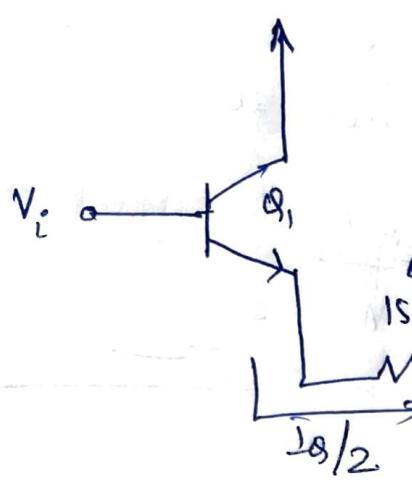
$$A_{cm} = -0.23$$

$$= -200 \times \frac{2.0 \text{ k}}{10.83 \text{ k} + 2(1+200) 4.3 \text{ k}}$$

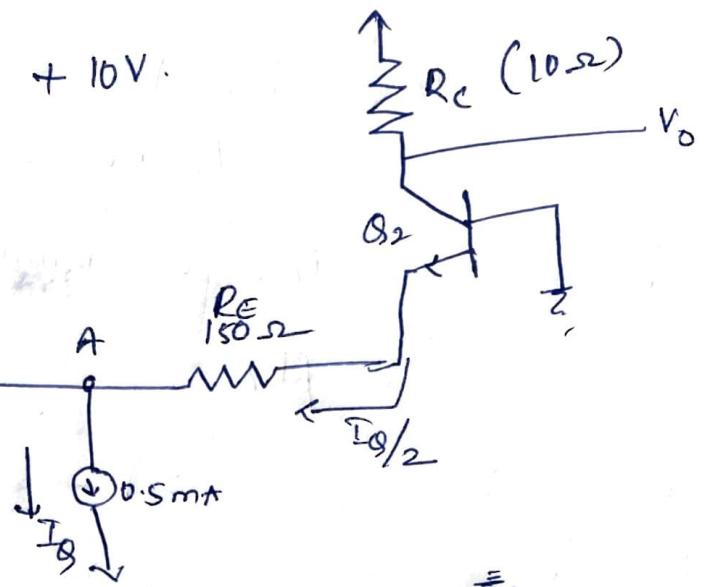
$$CMRR = \left| \frac{A_{dm}}{A_{cm}} \right| = \left| \frac{-36.92}{-0.23} \right| = 161.227$$

$$CMRR \text{ in dB} = 20 \log 161.227 = 44.4 \text{ dB}$$

③ For the differential amplifier shown in fig. Find the differential voltage gain Given $\beta_0 = 100$



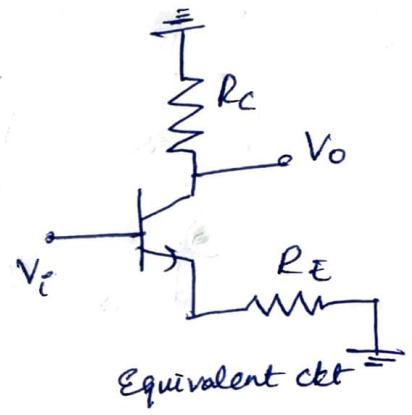
+ 10V.



$$\text{Solt: } I_{CQ} = \frac{I_Q}{2} = \frac{0.5 \text{ mA}}{2} = 0.25 \text{ mA}$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.25 \text{ mA}}{25 \text{ mV}} = \frac{1}{100} = 10^{-2}$$

$$\text{and } g_{m\pi} = \frac{\beta_0}{g_m} = \frac{100}{1/100} = 10 \text{ k}\Omega$$



Differential mode gain for a single stage is found from
the equivalent circuit can be written as

$$\begin{aligned} A_{dm} &= \frac{1}{2} \left(\frac{\beta_0 R_C}{g_{m\pi} + (1 + \beta_0) R_E} \right) \\ &= \frac{1}{2} \left(\frac{100 \times 10 \text{ k}\Omega}{10 \text{ k}\Omega + 101 \times 150 \Omega} \right) \end{aligned}$$

$$A_{dm} = 20$$

Sign of A_{dm} is positive because the O/p is taken at the collector of Q2 whereas the I/p is connected to base of Q1.

~~CMRR to large, A_{cm} should be as small as possible as $R_E \rightarrow \infty$~~

~~$A_{cm} \rightarrow 0$~~

$$A_{cm} = \frac{-h_{fe}R_C}{h_{ie} + (1+h_{fe})^2 R_E}$$

~~Practical limitations on the magnitude of R_E because of the quiescent dc voltage across it,~~

~~R_E is made large \rightarrow Emitter supply V_{EE} will also have to be increased in order to maintain the proper quiescent current.~~

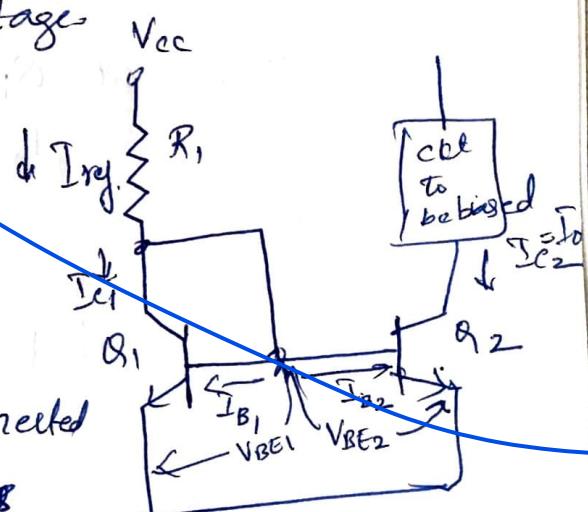
~~If Q (operating currents) of transistor is allowed to decrease then h_{ie} will decrease thereby reducing h_{fe} too. \Rightarrow also reduces CMRR~~

~~Use of constant current bias in place of R_E is found to be the practical solution to the problem.~~

~~constant current source (Current Mirror)~~

~~constant current source makes the transistor to operate in active mode of operation \rightarrow collector current is relatively independent of the collector voltage V_{CC}~~

~~Transistor Q_1 is connected as a diode by shorting its collector to base.~~



~~I_{ref} flows through diode connected to transistor Q_1 which establishes~~

~~Voltage across Q_1 .~~

~~this voltage appears between B & E of Q_2~~

The basic BJT current mirror

~~Q₁ & Q₂ are identical, hence the emitter currents are equal which is approximately equal to I_{ref}. Thus we can say~~

~~As long as Q₂ is in active region its collector current I_{C2} = I_O = I_{ref} \Rightarrow since the output current is a reflection or mirror of Reference current I_{ref}, the circuit is often referred to as current mirror.~~

This mirror effect is valid only for large values of

~~I_{C1} & I_{C2} for Q₁ & Q₂ can be approximately expressed as~~

$$I_{C1} = \alpha_F I_{ES} e^{\frac{V_{BE1}}{V_T}}$$

$$I_{C2} = \alpha_F I_{ES} e^{\frac{V_{BE2}}{V_T}}$$

$$\frac{I_{C2}}{I_{C1}} = e^{\frac{V_{BE2} - V_{BE1}}{V_T}}$$

$$V_{BE1} = V_{BE2} \Rightarrow I_{C2} = I_{C1} = I_C = I_O$$

Both transistor are identical $\beta_1 = \beta_2 = \beta$

KCL at Q₁ collector gives

$$\begin{aligned} I_{ref} &= I_{C1} + I_{B1} + I_{B2} \\ &= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2} \end{aligned}$$

$$I_{ref} = I_C \left(1 + \frac{2}{\beta} \right)$$

$$I_C = \frac{\beta}{\beta+2} I_{ref}$$

$$I_{ref} = \frac{V_{cc} - V_{BE}}{R_1} \approx \frac{V_{cc}}{R_1} \quad (\text{as } V_{BE} = 0.7V \text{ is small})$$

$\beta \gg 1$ ($\frac{\beta}{\beta+2}$) is almost unity

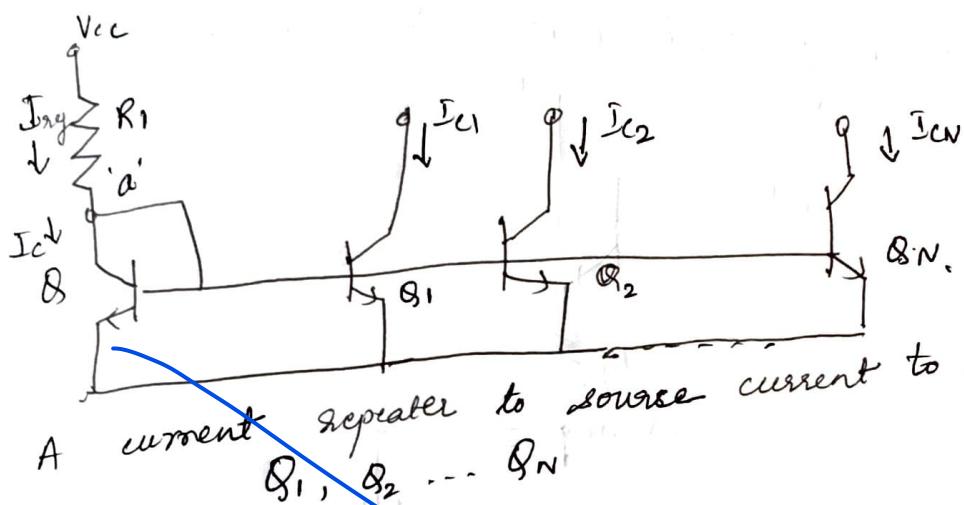
~~OP~~ current I_D is equal to I_{ref} , for given R_1 ,
~~I_D~~ constant.

~~I_D varies by about 3% for~~

$$So - 1 \leq 200.$$

~~Current Repeaters~~

The basic current mirror circuit can be used to source current to more than one load. Such a circuit is called current repeater.



At node 'a'
 $I_{ref} = I_c + I_B + N I_B$ (Assuming identical transistors)

$$\begin{aligned} I_{ref} &= I_c + I_B + N I_B \\ &= I_c + \frac{(1+N)}{\beta} I_c \\ &= I_c \left(1 + \frac{(1+N)}{\beta} \right) \end{aligned}$$

$$I_c = I_{ref} \left(\frac{\beta}{\beta + 1 + N} \right)$$

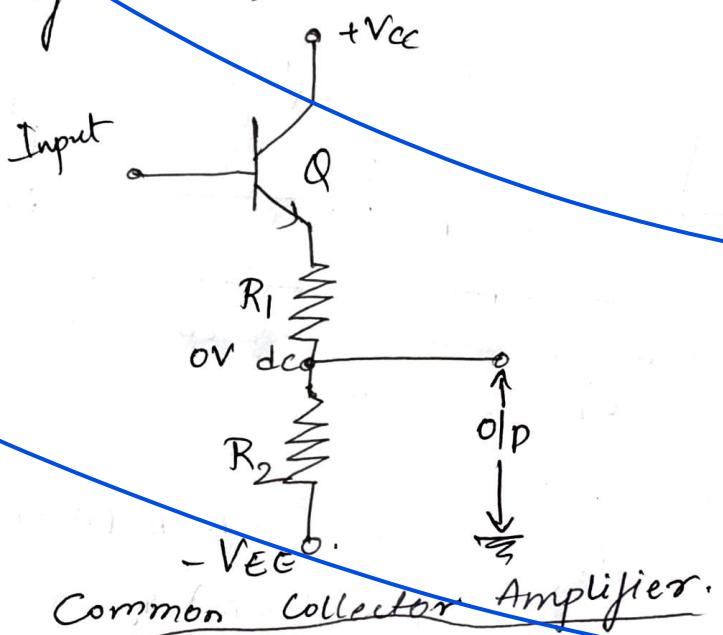
It is possible to achieve different value of $I_{c1}, I_{c2}, \dots, I_{cN}$ by scaling the emitter area of transistors Q_1, Q_2, \dots, Q_N

Level Translator

Because of the direct coupling the dc level at the emitter rises from stage to stage.

→ Increase in dc level tends to shift the operating point of the succeeding stages \therefore limits the voltage swing and may even distort the output signal.

→ To shift the dc level to zero, level translators are used. An emitter follower with voltage divider is the simplest form of level translator as shown in fig



Output Stage

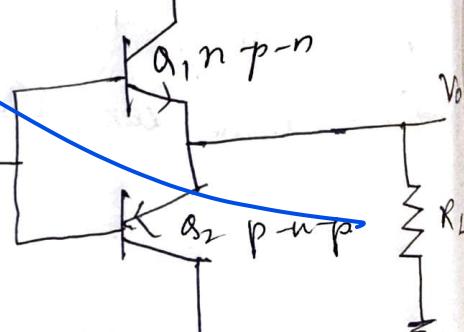
→ The function of last stage, i.e. output stage in an op-amps is to supply the load current and provide a low impedance output.

→ A simple output stage consists of 2 complementary transistors Q_1 (n-p-n) and Q_2 (p-n-p) connected as emitter followers as shown in fig.

When V_i is positive Q_1 is on & supplies current to load R_L .

When V_i is negative Q_1 is cut off and

Q_2 acts as a sink to remove current from the load R_L $-V_{EE}$

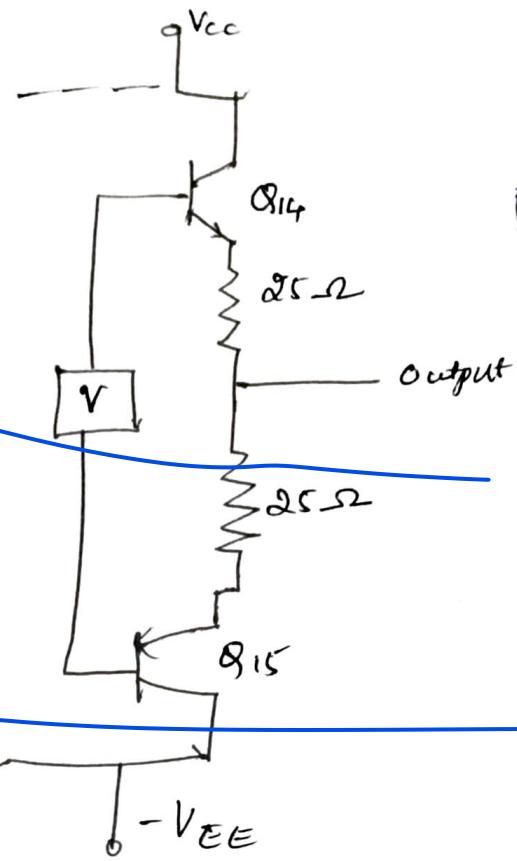


~~The output voltage V_o remains zero until the I/P v_i exceeds $V_{BE(\text{cut in})} = 0.5 \text{ V}$. This is called cross-over distortion.~~

~~It can be eliminated by applying bias v_b slightly greater than $2V_{BE(\text{cut in})} = 1 \text{ V}$ b/w the two bases.~~

~~The output stage of MA741 op-amp is shown in fig.~~

~~as shown in fig.
The small Emitter resistors ($25\text{-}\Omega$) stabilizes the quiescent base current.~~



Op-Amp Characteristics

Power Supply Rejection Ratio

O/P stage of MA741

The power supply rejection ratio (PSRR) is a measure of how effective the op-amp is in dealing with variations in supply voltage.

If a supply voltage change of $\Delta V_{cc} = 1 \text{ V}$ causes an input offset of $1 \mu\text{V}$, then the $PSRR = 1 \mu\text{V}/\text{V}$ or 10^{-6}

PSRR is usually expressed in dB, thus PSRR is given by

$$PSRR = 20 \log \frac{\Delta V_s}{\Delta V_{i(0s)}} \text{ dB} \quad (1)$$

$V_{i(0s)}$ → input offset voltage.

PSRR of 100 dB equals a ratio $\frac{1}{100000}$

giving a supply voltage change of (ΔV_s) reduction by a factor of 100000 at the amplifier input.

This is amplified by the circuit closed loop gain, which once again is the non-inverting gain or noise gain.

$$\boxed{\Delta V_o = \frac{\Delta V_s}{PSRR} A_{CL}} \quad \text{--- (2)}$$

$PSRR, CMRR$ decreases with increasing signal frequency.

Problem

A 741 op-amp uses ± 15 V supply with a $2mV$, 120 Hz ripple voltage superimposed. Calculate the amplitude of the output voltage produced by the power supply ripple if the circuit has a non-inverting closed loop gain of 50. Given $PSRR = 96$ dB

$$PSRR = 20 \log \frac{\Delta V_s}{\Delta V_{ios}}$$

$$PSRR = \text{antilog } (96/20) \\ = 63096$$

$$\Delta V_s = 2mV$$

wkt

$$\Delta V_o = \frac{\Delta V_s}{PSRR} A_{CL}$$

$$A_{CL} = 50$$

$$= \frac{2m}{63096} \times 50$$

$$\boxed{\Delta V_o(\text{rip}) = 1.6 \mu V}$$

Input and offset Voltages

Consider the op-amp voltage follower ckt. The differential amplifier & transistors Q_1 and Q_2 has to be perfectly matched so the output voltage exactly has input voltage. The base emitter voltages of the two transistors Q_1, Q_2 are equal $\rightarrow V_{BE1} = V_{BE2}$

If the base-emitter voltages of both transistors are not same, this voltage difference acts as a dc input voltage which is referred to as an input offset voltage (V_{ios}).

$$V_{ios} = V_{BE2} - V_{BE1}$$

Suppose $V_{BE1} = 0.7 \text{ V}$, $V_{BE2} = 0.69 \text{ V}$

$$\therefore V_{ios} = 0.69 - 0.7 = -0.01 \text{ V} = -10 \text{ mV}$$

Thus input V_{in} of ~~voltage~~ voltage follower ckt will be -10 mV the resulting in an output voltage of -10 mV instead of 0V . This is an output offset voltage (V_{os}) and it results in output always being slightly ~~more~~ different from the input voltage.

In case of the amplifier circuit with closed loop gain of A_{cl} , the input offset voltage produces an output offset

$$V_{os} = A_{cl} V_{ios}$$

The o/p offset voltage will be much larger than in case of voltage follower.

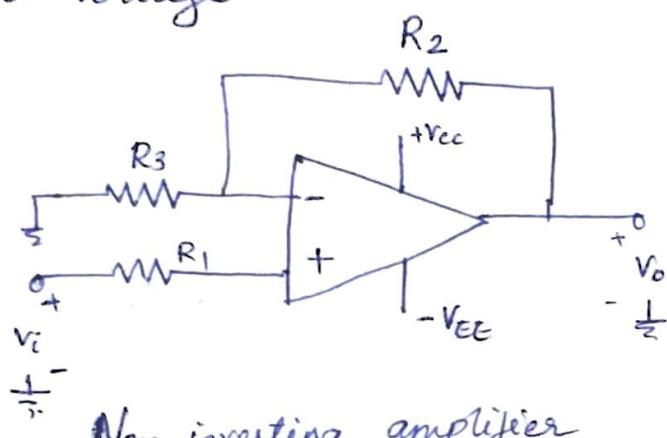
The maximum input offset voltage of UA741 op-amp is 5 mV (as provided in datasheet).

Input Bias Current Effects

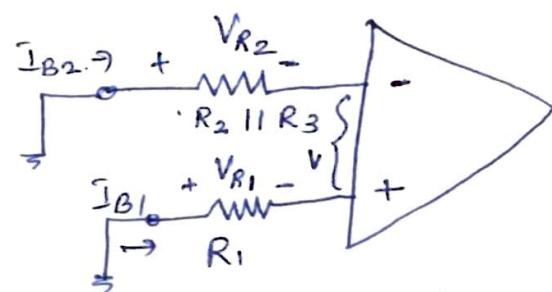
↳ Base currents of the transistors Q_1 and Q_2 (I_{B1} & I_{B2})
 For $\text{MJA741}_{\text{max}}$ Input Bias current = 500nA .

The input bias current has no effect on a simple voltage follower circuit.

This current produces voltage drops across resistors connected in series with each input terminal; where these voltage drops are unequal, the difference behaves like another offset voltage.



Non-inverting amplifier



The input bias currents flow through R_1 and $R_2 \parallel R_3$

Input bias currents to an op-amp produce voltage drops across resistors connected at the input. A difference in the bias currents, known as the input offset current, produces unequal resistor voltage drops resulting in an unwanted input voltage.

Consider the non-inverting amplifier shown in figure.
 The resistance in series with non-inverting terminal is R_1 .
 The resistance in series with inverting terminal is $R_2 \parallel R_3$.

If $R_1 = (R_2 \parallel R_3)$ the voltage drops produced by I_{B1} & I_{B2} will be equal \rightarrow doesn't create any additional input offset voltage.

The resistance looking into each terminal should be equal.

The tolerance of resistors may also play a significant role in input offset voltage i.e. tolerance of resistor also acts a source of input offset voltage.

The V_{tg} levels involved are easily determined by first calculating the maximum and minimum values of resistances in series with each input terminal & then finding the voltage drop across each resistance.

problem

① The non inverting amplifier circuit using MA74 has $R_1 = R_3 = 2.2k\Omega$, $R_2 = 220k\Omega$. Determine the maximum possible output offset V_{tg} due to
 ② the specified input offset V_{tg} ③ input bias current
 Given $V_{i(0s)} = 5mV \text{ max}$ $I_B = 500nA$

$$\text{Solt} @ \text{gain } A_{CL} = 1 + \frac{R_2}{R_3} = 1 + \frac{220k}{2.2k}$$

$$A_{CL} = 101$$

$$\begin{aligned} V_{o(0s)} &= A_{CL} V_{i(0s)} \\ &= 101 \times 5mV \\ V_{o(0s)} &= 505mV \end{aligned}$$

$$\begin{aligned} ④ R &= R_2 \parallel R_3 = 2.2k\Omega \parallel 220k\Omega = 2.18k\Omega \\ \text{difference in input resistance} &= R_1 - R \\ &= 2.2k - 2.18k \end{aligned}$$

$$R_{diff} = 20\Omega$$

$$\begin{aligned} V_{i(0s)} &= I_B R_{diff} \\ &= 500nA \times 20\Omega \\ &= 10\mu V \end{aligned}$$

$$\begin{aligned} V_{o(0s)} &= 10\mu V \times 101 \\ V_{o(0s)} &= 1.01mV \end{aligned}$$

Input offset current

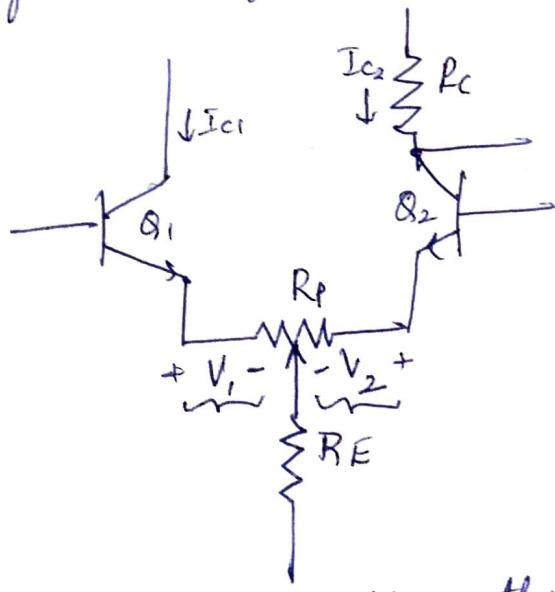
If the base-emitter voltages of the both transistors in D-A are unequal, the dc current gain (hfe) of one transistor may not be exactly equal to that of the other i.e. they both have equal levels of collector currents their base currents may be unequal. The difference in the two input current levels is known as the input offset current (I_{os})

Offset Nulling

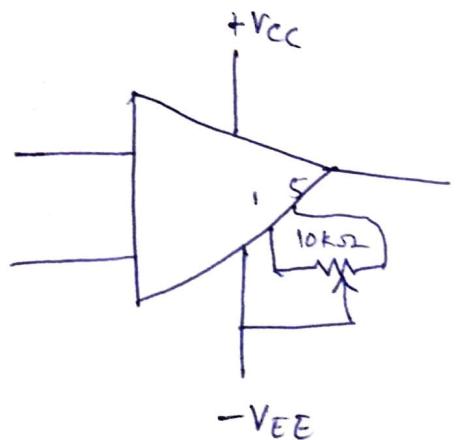
Input offset voltage and current can be dealt by connecting a low-resistance potentiometer (R_p) at the emitters of the input transistors Q_1 & Q_2 .

Adjustment of R_p alters the total voltage drop from base to the common point at the potentiometer moving contact.

→ This adjustment can null the effects of all sources of input offset voltage.



④ Adjustment of R_p alters the balance of V_1 & V_2



⑤ offset nulling for
TAT op-amp

The pin 1 & 5 of UA741 op-amp is reserved for offset null. As shown in fig ⑥ 10k Ω potentiometer is connected b/w the pin 1 & 5 and its moving contact is connected to -ve supply line. The potentiometer is adjusted to null the output offset voltage to zero.

The input offset ~~adjustment~~ adjustment is $\pm 15\text{mV}$ for UA741 op-amp.

The output offset voltage is the o/p voltage obtained when no input is given to the inverting and non-inverting input of the op-amp.

Input Impedance

The typical resistance offered at the input terminals of a J41 op-amp is 2 M Ω .

Input impedance of an op-amp circuit is dependent on the external components

From negative feedback theory, the impedance at the op-amp input terminal for a voltage follower or non-inverting amplifier is $Z_i = R_i(1 + A_{OL}\beta)$

op-amp input resistance without negative feedback.

open loop gain \downarrow feedback factor.

For inverting amplifier $Z_i = R_i$

Output Impedance: Typical output resistance of UA741 is 75 Ω .

The output impedance of an op-amp circuits depends on the negative feedback produced by the external components.

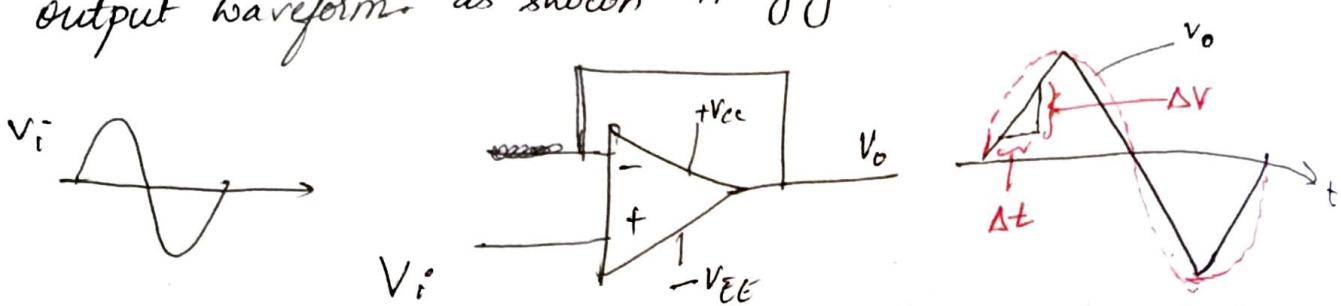
$$Z_o = \frac{R_o}{(1 + A_{OL}\beta)}$$

$R_o \rightarrow$ op-amp output resistance without negative feedback.

Slew rate and Frequency limitations

Slew rate:- The slew rate of an op-amp is the maximum rate at which the output voltage can change. When the slew rate is too slow for the input, distortion results.

Let us consider an example where the sine wave input v_i is given to a voltage follower producing a triangular output waveform as shown in fig.



The triangular wave results because the op-amp output simply cannot move fast enough to follow the sine wave input.

The slew rate defines the maximum rate of change of op-amp output voltage. When the input voltage changes too quickly, when the input voltage changes too quickly, output waveform distortion results.

The typical SR of the 741 op-amp is specified as 0.5 V/μs. → This means that 1 μs is required for the output to change by 0.5 V.

The equation relating SR, output voltage change & time:

$$SR = \frac{\Delta v_o}{t}$$

A 10 V output change from a 741 op-amp requires a minimum time of $t = \frac{\Delta v_o}{SR} = \frac{10}{0.5 \text{ V}/\mu\text{s}} = 20 \mu\text{s}$

Frequency Limitations

Figure 2-21 shows the graph of the open-loop gain (A_{OL}) plotted versus frequency (f) for a 741 op-amp. It can be seen from the graph that A_{OL} is 100 dB when the signal frequency is 1 Hz. At 10 Hz, the gain has fallen below 100 dB, and it continues to fall as the signal frequency increases. Note that frequency is plotted to a logarithmic base and that A_{OL} falls linearly as f increases logarithmically.

$$\text{At } f = 100 \text{ Hz, } A_{OL} \approx 80 \text{ dB}$$

$$\text{At } f = 1 \text{ kHz, } A_{OL} \approx 60 \text{ dB}$$

Thus, A_{OL} falls by 20 dB when f increases from 100 Hz to 1 kHz. The 10 times increase in frequency is termed a *decade*. So, the rate of fall of the gain is said to be *20 dB per decade*. This can also be stated as *6 dB per octave*—a 6 dB reduction in gain each time the frequency is doubled.

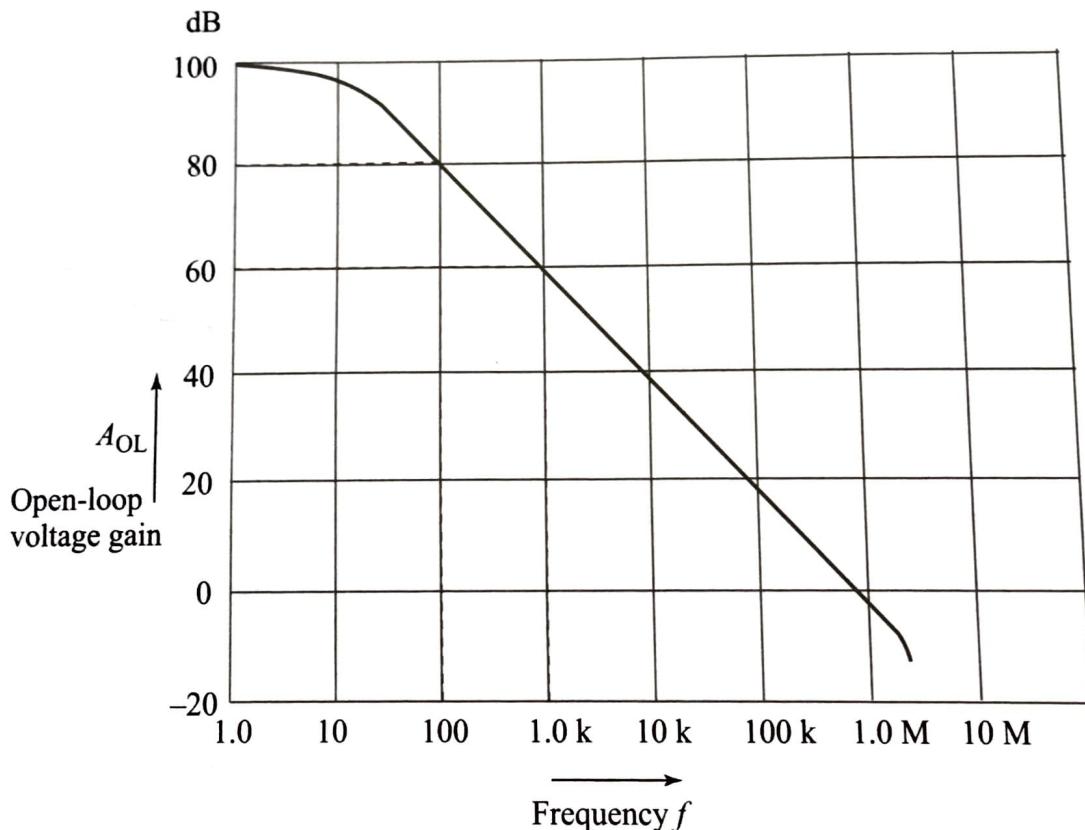


Figure 2-21 Plot of open-loop gain (A_{OL}) versus signal frequency (f) for a 741 op-amp.

The gain/frequency graph in Fig. 2-21 shows that that A_{OL} falls to zero at approximately 800 kHz. Where an internal gain equal to or greater than 80 dB is required for a particular application, it is available with a 741 only for signal frequencies up to approximately 100 Hz. An internal gain greater than 20 dB is possible for signal frequencies up to approximately 90 kHz. Several other op-amps maintain substantial gain to much higher frequencies than the 741. Op-amp frequency response is further investigated in Chapter 5.

Example 2-7

An op-amp circuit is to have a 10 kHz triangular output waveform with a 12 V peak-to-peak amplitude. Calculate the op-amp minimum SR.

Solution

$$t = \frac{1}{2f} = \frac{1}{2 \times 10 \text{ kHz}} = 10\mu\text{s}$$

Eq. 2-10

$$\begin{aligned} \text{SR} &= \frac{\Delta V_o}{t} = \frac{12 \text{ V}}{10\mu\text{s}} \\ &= 1.2 \text{ V}/\mu\text{s} \end{aligned}$$

Practice Problems

- 2-6.1** Calculate the maximum triangular output frequency that can be expected from a LF353 op-amp if the waveform is to have a ± 5 V amplitude.
- 2-6.2** Determine the frequency at which the internal gain of a LF353 falls to
(a) 60 dB and (b) 30 dB.

frequency Limitations

→ Refer David A. Bell.

Problems

- ① An op-amp circuit is to have a 10kHz triangular o/p waveform with a 12 V p-p amplitude. Calculate the op-amp minimum Slew rate

$$SR = \frac{\Delta V_o}{t}$$

$$t = \frac{1}{f} = \frac{1}{10\text{ KHz}} = 0.1\text{ ms} = 100\text{ }\mu\text{s}$$

$$SR = \frac{12}{100} = \underline{\underline{0.12 \text{ V}/\mu\text{s}}}$$

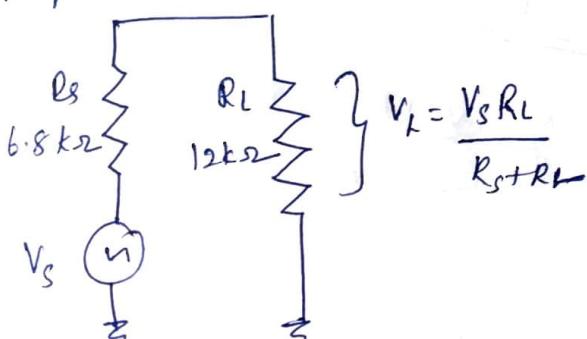
Direct coupled voltage follower

Input & Output impedance of voltage follower

$$Z_i = R_i(1 + A_{OL}\beta)$$

$$Z_o = \frac{R_o}{(1 + A_{OL}\beta)}$$

V-F is normally used to convert a high impedance source to a low o/p impedance → It can be employed as a buffer between the high impedance source and low impedance load. Thus it is also known as buffer amplifier



The fig. shows the signal voltage is divided across R_s and R_L . When directly connected to a load

Part of signal is lost when load is directly connected to source.

Fig shows the voltage follower with high input impedance at the signal source

$Z_i \gg R_s \rightarrow$ no signal loss at Input terminal.

∴ All of V_i appears at the o/p input

Actual o/p voltage from the voltage follower o/p is

$$V_o = V_i - \frac{V_o}{A_{OL}}$$

The output voltage can be thought of it is divided across R_L and the voltage follower output impedance Z_o

$Z_o \ll R_L \rightarrow$ no signal loss.

Virtually all of V_i appears as V_o at the circuit output.

Problems:-

- 1) The voltage follower ckt. has a 1V signal and a $20k\Omega$ load. Calculate the load voltage when
 - a) the load is directly connected to the source and
 - b) the load voltage follower is between the load and the source

Soln :-

$$V_L = V_o \cdot \frac{R_L}{R_s + R_L} = \frac{1 \times 20k\Omega}{20k\Omega + 6.8k\Omega} = \frac{20}{26.8} = 0.746V$$

$$= 746 mV$$

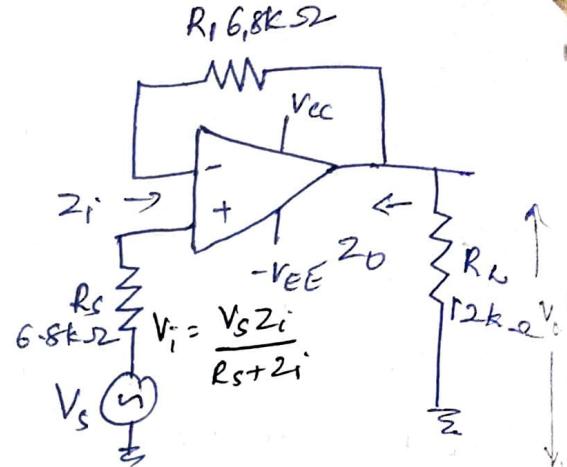
b) $Z_i = R_i(1 + A_{OL}\beta)$ using typical values of A_{OL} op-amp
 $R_i = 2M\Omega$ $A_{OL} = 2 \times 10^5$ $\beta = 1$

$$Z_i = 2 \times 10^5 (1 + 2 \times 10^5 \times 1)$$

$$Z_i = 4 \times 10^{11} \Omega$$

$$V_i = \frac{V_s Z_i}{R_s + Z_i} = 1 \times \frac{1 \times 10^{-11}}{4 \times 10^{11} + 6.8k\Omega} = 1V$$

effectively



Direct coupled non-inverting amplifiers

Gain is given by

$$A_{CL} = 1 + \frac{R_3}{R_2}$$

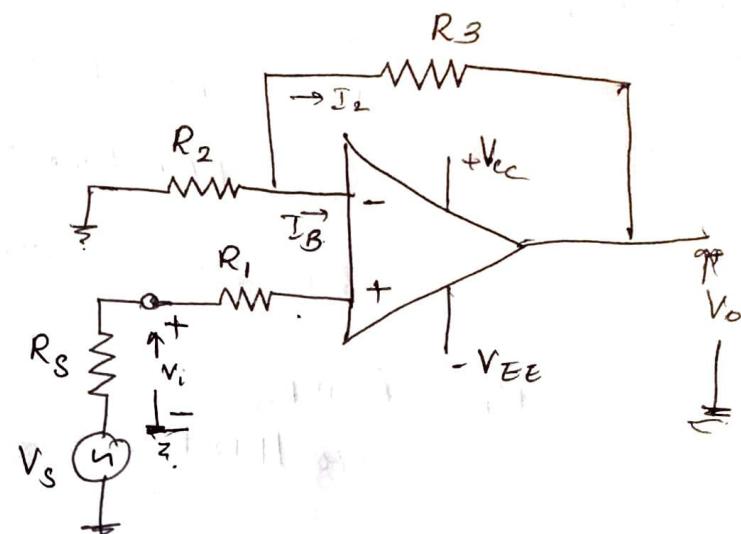
$$I_2 \gg I_{B(\max)}$$

$$R_3 = \frac{V_i}{I_2}$$

The O/p voltage across

$$R_2 + R_3 = \frac{V_o}{I_2}$$

$$R_s + R_1 = R_2 \parallel R_3$$



Designing a non inverting amplifier (using Bipolar op-amp) starts by selecting the voltage divider (I_2) to be much greater than the maximum level of the input bias current (I_B). Then $R_3 = \frac{V_i}{I_2}$
& $R_2 + R_3 = \frac{V_o}{I_2}$

Problem

① Using MA741 op-amp. Design a non inverting amplifier to have a voltage gain of approximately 66. The signal amplitude is to 15 mV. Given $I_B = 500 \mu A$

Select $I_2 = 100 I_B = 100 \times 500 \mu A$

$$\boxed{I_2 = 50 \text{ mA}}$$

$$V_i = 15 \text{ mV}$$

$$R_3 = \frac{V_i}{I_2} = \frac{15 \text{ m}}{50 \mu} = 0.3 \times 10^{-3} = 300 \Omega$$

Choose (std resistance value = 270 Ω)

$$I_2 = \frac{V_i}{R_3} = \frac{15 \text{ mV}}{270 \Omega} = 55.6 \text{ mA}$$

$$V_o = A_{CL} \times V_i = 66 \times 15 \text{ mV} = 0.99 \text{ V} = 990 \text{ mV}$$

$$R_2 + R_3 = \frac{V_o}{I_2} = \frac{990 \text{ m}}{55.6 \text{ mA}}$$

$$R_2 + R_3 = 17.8 \text{ k}\Omega$$

$$R_2 = 17.8 \text{ k}\Omega - 270 = \underline{\underline{17.53 \text{ k}\Omega}}$$

$18 \text{ k}\Omega$ is the std resistance

$$R_1 = R_2 \| R_3$$

$$= 270 \| 18 \text{ k}\Omega = \frac{18 \text{ k} \times 270}{18 \text{ k} + 270} = 26.6$$

$$(R_1 \approx 270 \text{ }\Omega)$$

Draw the opamp non inverting amplifier circuit with the obtained values

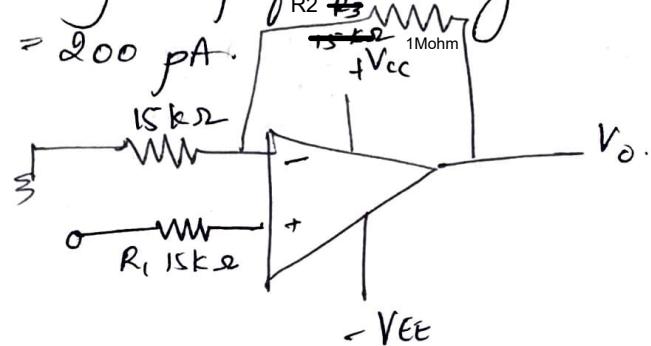
(2) Design the non inverting amplifier using OP-amp. $I_B(\text{max}) = 200 \text{ pA}$

LF353 B_{IFG}

$$A_{CL} = ?$$

$$R_3 = ?$$

$$R_1 = ?$$



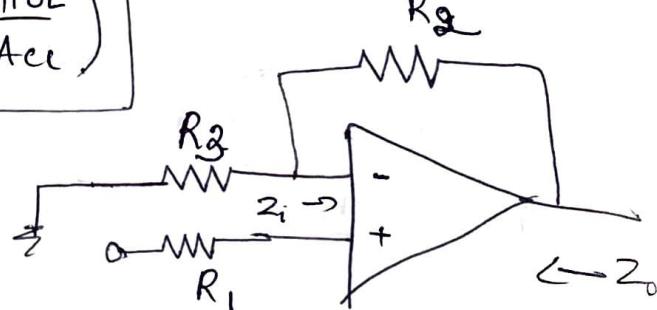
Performance.

$$Z_i = R_i (1 + A_{OL} \beta)$$

$$\beta = \frac{R_2}{R_2 + R_3} = \frac{1}{A_{CL}} \quad (1)$$

$$\boxed{Z_i = R_i \left(1 + \frac{A_{OL}}{A_{CL}} \right)}$$

$$Z_{in} = Z_i + R_1$$



$Z_i \gg R_1$ thus R_1 need not be included

$$Z_o = \frac{R_o}{(1 + A_{OL} \beta)}$$

From (1) $\beta = \frac{1}{A_{CL}}$

$$Z_o = \frac{R_o}{\left(1 + \frac{A_{OL}}{A_{CL}} \right)}$$

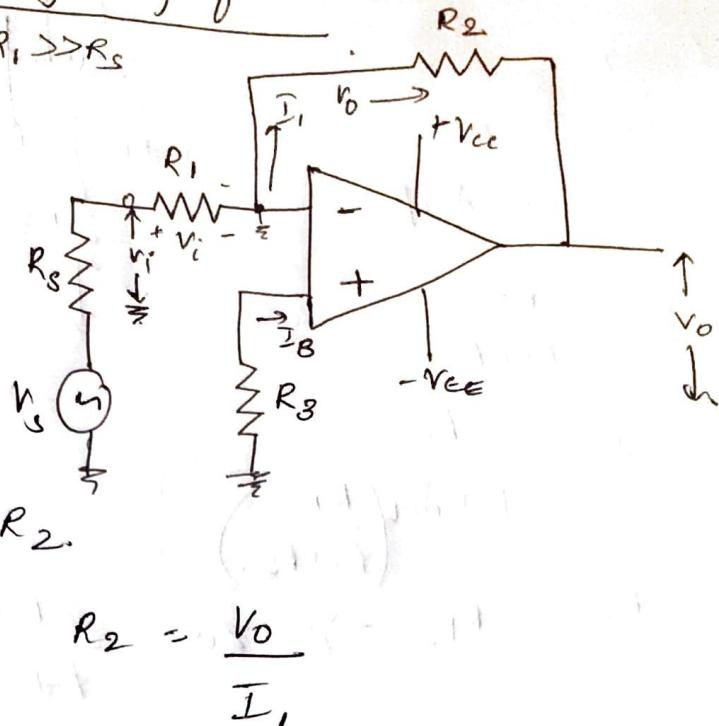
Direct Coupled Inverting Amplifiers

Resistance R_3 when $R_1 \gg R_s$

$$R_3 = R_1 \parallel R_2$$

If R_1 is not much larger than the source resistance (R_s)

$$R_3 = (R_1 + R_s) \parallel R_2.$$



$$R_1 = \frac{V_i}{I_i} \quad R_2 = \frac{V_o}{I_i}$$

Design of an inverting amplifier (using BJT op-amp)

Starts by selecting the voltage divider ~~current~~ current (I_1) to be much greater than the maximum level of the input bias current (I_B). Then $R_1 = \frac{V_i}{I_1}$ and $R_2 = \frac{V_o}{I_1}$ puting

Problem

Design an inverting op-amp amplifier using LM741 op-amp. The voltage gain is to be 50 and the o/p v/g amplitude to be 2.5V, Given $I_B = 500 \text{nA}$ (max)

$$\text{Let } I_1 = 100 I_B = 50 \mu\text{A}$$

$$\frac{V_o}{V_i} = A_{CL}$$

$$V_i = \frac{V_o}{A_{CL}} = \frac{2.5}{50} = \underline{\underline{50 \text{mV}}}$$

$$R_1 = \frac{50 \text{mV}}{50 \mu\text{A}} = 1 \text{k}\Omega \text{ (std value.)}$$

$$R_2 = \frac{2.5}{50 \mu\text{A}} = \frac{V_o}{I_1} = \underline{\underline{50 \text{k}\Omega}}$$

50k Ω is not std resistance \rightarrow Use 47k Ω or 56k Ω
std resistance with a slight variation in gain
To get ~~exact~~ 50k $\Omega \Rightarrow$ 47k Ω resistor in series with 3.3k Ω

$$R_3 = R_1 \parallel R_2 \\ = 1 \text{k}\Omega \parallel 50 \text{k}\Omega \\ R_3 = 1 \text{k}\Omega$$

Performance

$$Z_i = R_1$$

wkt. $Z_o = \frac{R_o}{1 + A_{OL}\beta}$

Q

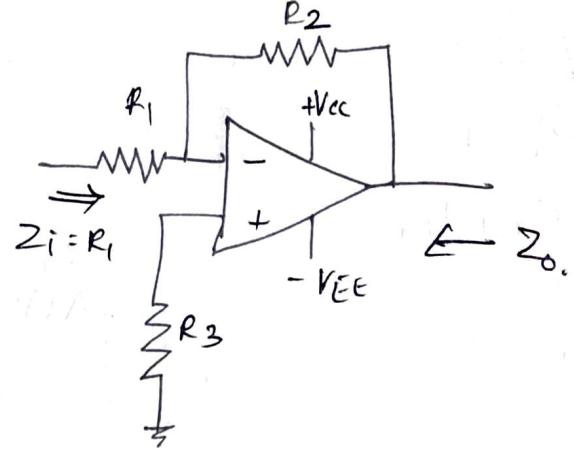
$$\beta = \frac{R_1}{R_1 + R_2}$$

$$Z_o = \frac{R_o}{1 + A_{OL} \left(\frac{R_1}{R_1 + R_2} \right)}$$

When $R_2 \gg R_1 \Rightarrow Z_o = \frac{R_o}{1 + A_{OL} \left(\frac{R_1}{R_2} \right)}$

(i) Similar to a
non inverting amplifier

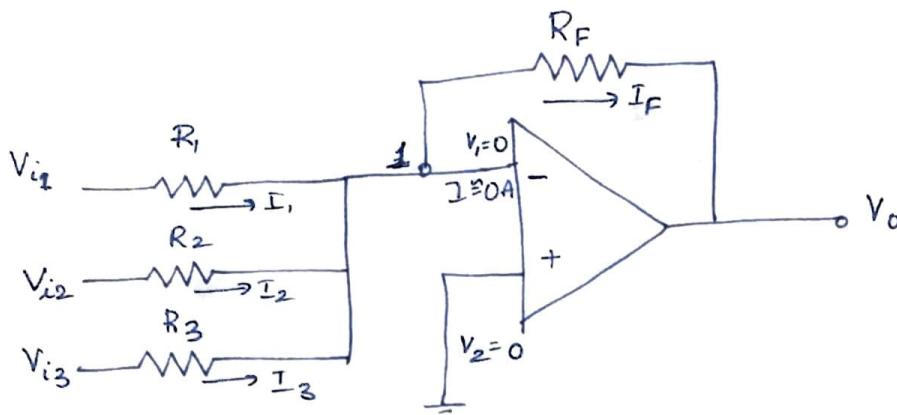
$$Z_o = \frac{R_o}{\left(1 + \frac{A_{OL}}{A_{cc}} \right)}$$



(1)

Summing Amplifiers

Inverting Summing Circuit



Inverting summing circuit

The figure shows the op-amp amplifier with three inputs V_{i1} , V_{i2} and V_{i3} and the output V_o .

$$\text{since } V_2 = 0$$

Due to virtual short in inverting amplifier

$$V_1 = V_2 = 0$$

Due to high input impedance of the op-amp.

$$I \approx 0 \text{ A.}$$

Apply KCL at node V_1

$$I_1 + I_2 + I_3 = I_F \quad \text{--- (1)}$$

$$I_1 = \frac{V_{i1} - V_1}{R_1} \quad I_2 = \frac{V_{i2} - V_1}{R_2} \quad I_3 = \frac{V_{i3} - V_1}{R_3} \quad I_F = \frac{V_1 - V_o}{R_F}$$

$$\text{wkt } V_1 = 0$$

Sub I_1 , I_2 , I_3 and I_F values from above expression by sub.

$$V_1 = 0$$

$$\frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} + \frac{V_{i3}}{R_3} = -\frac{V_o}{R_F}$$

Output Voltage

$$V_o = -\left[\frac{R_F}{R_1} (V_{i1}) + \frac{R_F}{R_2} V_{i2} + \frac{R_F}{R_3} V_{i3} \right]$$

$$V_o = -[aV_{i1} + bV_{i2} + cV_{i3}] \quad \text{--- (2)}$$

$$\text{where } a = R_F/R_1 \quad b = R_F/R_2 \quad c = R_F/R_3$$

Case 1 :- when $a=b=c=1$ Sub in ①

$$V_o = -[V_{i1} + V_{i2} + V_{i3}]$$

This would result in Inverting adder circuit

If $R_1=1k\Omega$ $R_f=R_1=R_2=R_3$

$R_1=R_2=R_3=R_F=1k\Omega$ then the circuit would behave like inverting summer.

Case 2 :- If $a=b=c=\frac{1}{3}$

Sub in ②

$$V_o = -\frac{1}{3}[V_{i1} + V_{i2} + V_{i3}]$$

Inverting averager circuit.

$$R_1 = R_2 = R_3 = 3R_f$$

$$\therefore R_f = \frac{R_1}{3} = \frac{R_2}{3} = \frac{R_3}{3}$$

$$\frac{R_F}{R_1} = \frac{R_F}{R_2} = \frac{R_F}{R_3} = \frac{1}{3}$$

$\boxed{3R_F = R_1}$

$$R_2 = 3R_f$$

$$R_3 = 3R_F$$

For 2 inputs $\Rightarrow a=b=\frac{1}{2}$

For averaging circuit.

For n inputs $\Rightarrow a=b=c\dots\dots\dots=\frac{1}{n}$

Case 3 :- Addition with scaling

If $a \neq b \neq c$ then the circuit performs addition with scaling.

$$V_o = -[aV_{i1} + bV_{i2} + cV_{i3}]$$

$$a=2, b=3, c=+1$$

If $a=b=c$ then the circuit perform addition with scaling

$$V_o = -[aV_{i1} + aV_{i2} + aV_{i3}]$$

$$V_o = -a[V_{i1} + V_{i2} + V_{i3}]$$

For example $a=b=c=2$.

$$V_o = -2[V_{i1} + V_{i2} + V_{i3}]$$

(2)

problem:

1 Design a summing amplifier to give the direct sum of two inputs each ranging from 0.1 to 1 V. Use 741 opamp. Given

$$I_B(\text{max}) = 500 \text{nA}$$

Solu.

$$\begin{aligned} I_2 &= 100 \times I_B(\text{max}) \\ &= 100 \times 500 \text{nA} \end{aligned}$$

$$I_2 = 50 \text{mA}$$

$$R_1 = \frac{V_{1(\text{min})}}{I_1(\text{min})} = \frac{0.1 \text{V}}{50 \text{nA}} = 2 \text{k}\Omega \quad (\text{use } 1.8 \text{k}\Omega \text{ std value})$$

$$R_2 = R_1 = 1.8 \text{k}\Omega$$

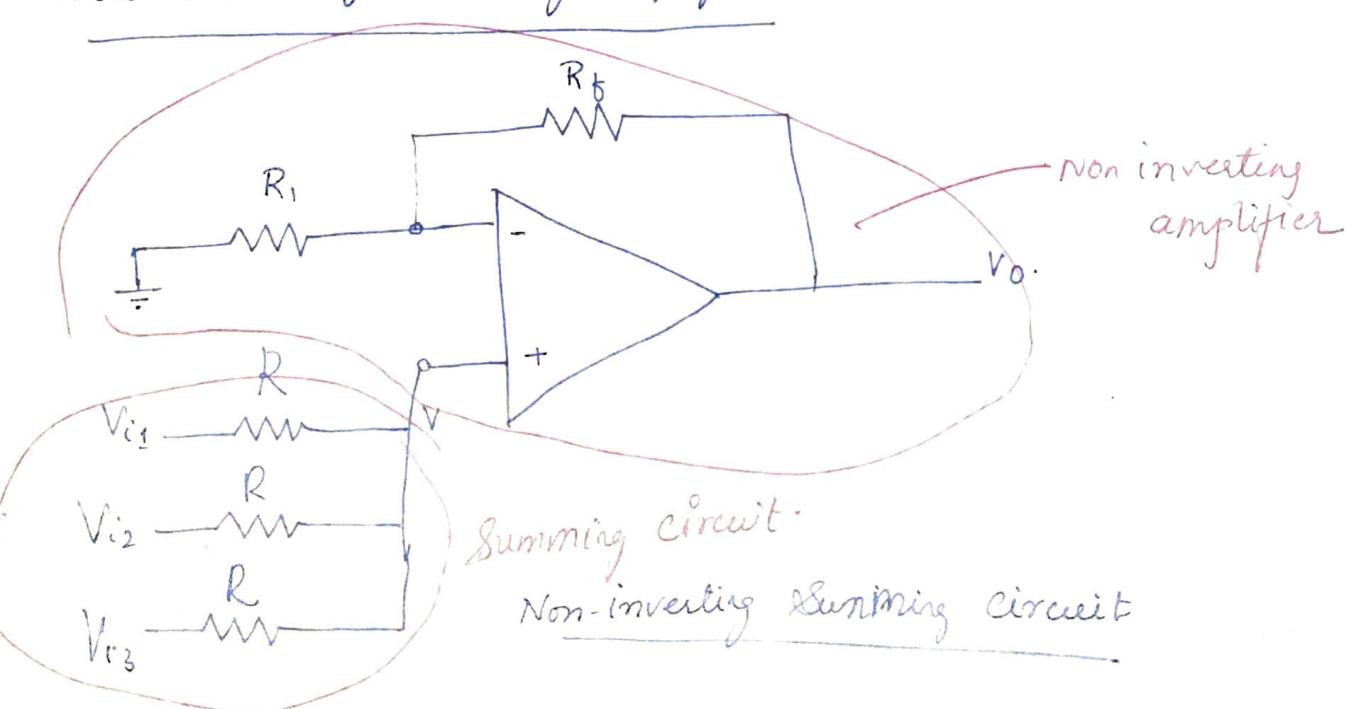
$$\text{and for } A_{\text{cl}} = 1 \quad R_3 = R_1 = 1.8 \text{k}\Omega$$

$$R_4 = R_1 \parallel R_2 \parallel R_3 = 1.8 \text{k}\Omega \parallel 1.8 \text{k}\Omega \parallel 1.8 \text{k}\Omega$$

$$= 600 \Omega \quad (\text{use } 560 \Omega \text{ standard value})$$

Summing Amplifier can function as a multichannel audio mixer for several audio channels.

Non Inverting Summing Amplifier



The circuit shows the non-inverting summing amplifiers where

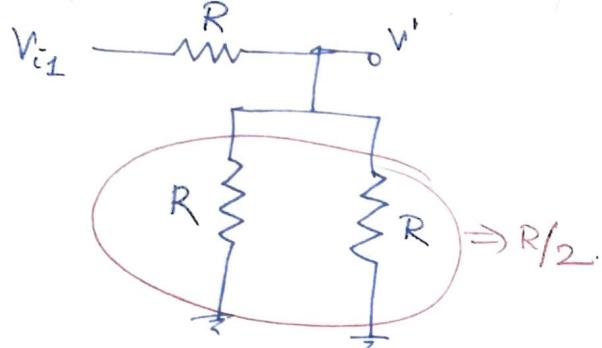
the input voltages are given through non inverting input terminal.

O/P of the non-inverting amplifier is given by

$$V_o = V \left(1 + \frac{R_F}{R_1} \right) \quad \text{--- (1)}$$

Summing circuit:-

V depends on V_{i1} , V_{i2} and V_{i3} . Apply superposition principle to find V



$$V' = \frac{V_{i1} R / 2}{R + R / 2} = \frac{V_{i1} R / 2}{3R / 2}$$

$$\boxed{V' = \frac{V_{i1}}{3}}$$

Similarly $V'' = \frac{V_{i2}}{3}$, $V''' = \frac{V_{i3}}{3}$

$$V = V' + V'' + V'''$$

$$\boxed{V = \frac{1}{3} [V_{i1} + V_{i2} + V_{i3}]} \quad \text{--- (2)}$$

Sub (2) in (1)

$$V_o = \frac{1}{3} (V_{i1} + V_{i2} + V_{i3}) \left(1 + \frac{R_F}{R_1} \right)$$

Case 1: If $1 + \frac{R_F}{R_1} = 3$

then $\boxed{V_o = V_{i1} + V_{i2} + V_{i3}}$

Non-inverting addition

$$\boxed{\frac{R_F}{R_1} = 2}$$

$$R_1 = 1k\Omega \quad R_F = 2k\Omega$$

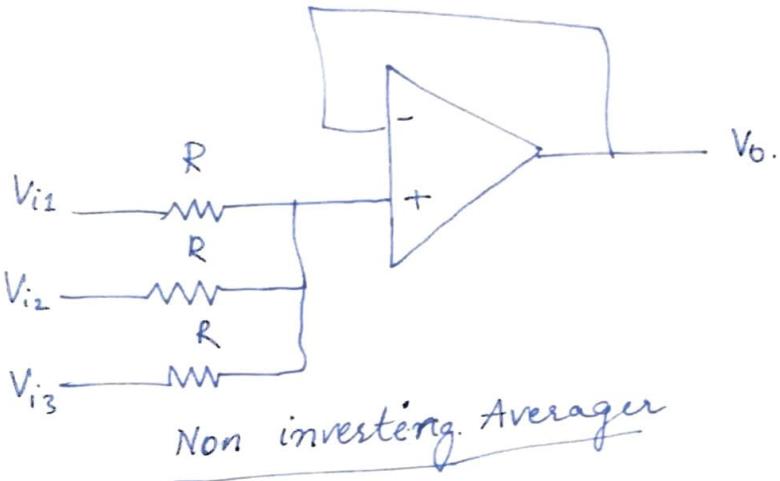
Case 2:-

If $\frac{1+R_F}{R_1} = 1 \Rightarrow$ Voltage follower

$$\frac{R_F}{R_1} = 0$$

$$R_F = 0$$

$$V_o = \frac{1}{3} [V_{i1} + V_{i2} + V_{i3}] \rightarrow \text{Non inverting averager}$$



Difference Amplifier :-

Differential Amplifier with the gain = 1

Instrumentation Amplifier

Introduction

Many industrial and consumer applications require the measurement and control of physical conditions. For example, measurements of temperature and humidity inside a diary plant to accurately maintain product quality, or precise control of the temperature of a plastic furnace to produce a particular grade of plastic, etc.

These changes in physical conditions must be converted to electrical quantities using transducers, and then amplified. Such amplifiers, which are used to amplify signals to measure physical quantities are commonly known as Instrumentation Amplifiers. An instrumentation system is used to measure the output signal produced by a transducer and often to control the physical signal producing it. The block diagram of an instrumentation system is as shown in figure 2.1.

The input to an instrumentation amplifier is the output signal from the transducer. A transducer is a device which converts one form of energy into another. Most of the transducer outputs are of very low-level signals.

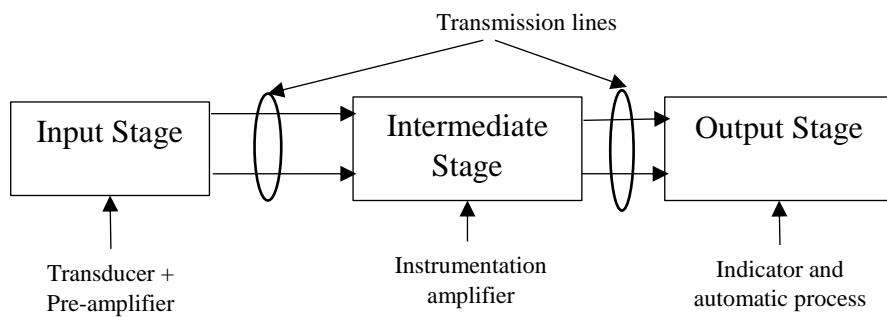


Figure 2.1: Block diagram of an instrumentation system

Hence, before the next stage, it is necessary to amplify the level of the signal, rejecting noise and the interference. The general single ended amplifiers are not suitable for such operations. For the rejection of noise, amplifiers must have high common-mode rejection ratio.

The special amplifier which is used for such low-level amplification with high CMRR, high input impedance to avoid loading is an Instrumentation Amplifier.

The instrumentation amplifier is intended for precise, low-level signal amplification where high input resistance, low noise and accurate closed-loop gain is required. Also, low power consumption, high slew rate and high common-mode rejection ratio are desirable for good performance.

Requirements of a Good Instrumentation Amplifier

An instrumentation amplifier is usually employed to amplify low-level signals, rejecting noise and interference signals. Therefore, a good instrumentation amplifier has to meet the following specifications:

Finite, Accurate and Stable Gain: Since the instrumentation amplifiers are required to amplify very low-level signals from the transducer device, high and finite gain is the basic requirement. The gain also needs to be accurate and the closed-loop gain must be stable.

Easier Gain Adjustment: Apart from a finite and stable gain, variation in the gain factor over a prescribed range of values is also necessary. The gain adjustment must be easier and precise.

High Input Impedance: To avoid the loading of input sources, the input impedance of the instrumentation amplifier must be very high (ideally infinite).

Low Output Impedance: The output impedance of a good instrumentation amplifier must be very low (ideally zero), to avoid loading effect on the immediate next stage.

High CMRR: The output from the transducer usually contains common mode signals, when transmitted over long wires. A good instrumentation amplifier must amplify only the differential input, completely rejecting common mode inputs. Thus, the CMRR of the instrumentation amplifier must be ideally infinite.

High Slew Rate: The slew rate of the instrumentation amplifier must be as high as possible to provide maximum undistorted output voltage swing.

Differential Input/Output Amplifier

The figure 2.2 shows the circuit of an amplifier that accepts a differential input voltage and produces a differential output voltage.

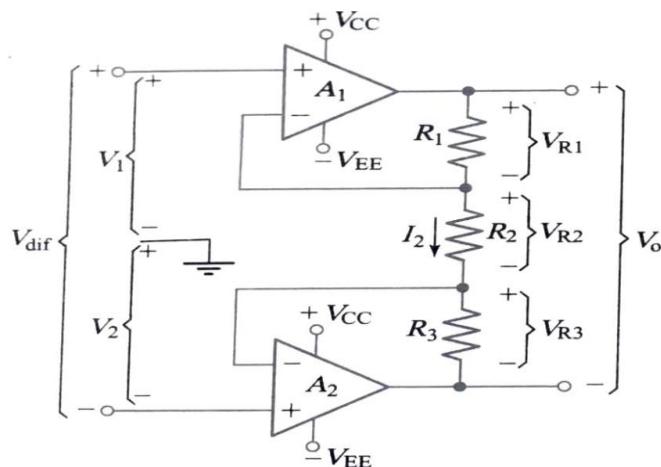


Figure 2.2: A differential input/output amplifier has a differential output voltage as well as a different input

Let us analyse the differential input/output amplifier by assuming the junction of resistors R_2 & R_3 is grounded. Now, the opamp A_1 is a non-inverting amplifier with R_1 as feedback resistor and R_2 as input resistor. The gain of

$$A_1 = 1 + \frac{R_1}{R_2}$$

Similarly if junction of R_2 & R_1 are grounded A_2 is a non-inverting amplifier with R_3 as feedback resistor and R_2 as input resistor. The gain of

$$A_2 = 1 + \frac{R_3}{R_2}$$

The input to the opamp A_1 , A_2 at the junction of R_2 & R_3 is equal to V_1 and A_2 at the junction of R_2 & R_1 is equal to V_2 .

The voltage at the resistance R_2 is given by $V_{R2} = V_1 - V_2 = V_i$

V_{R2} is the differential input to the circuit.

The current flowing in R_2 is given by

$$I_2 = \frac{V_i}{R_2}$$

From the circuit the differential output voltage is

$$V_O = V_{R1} + V_{R2} + V_{R3} = I_2(R_1 + R_2 + R_3)$$

$$V_o = \frac{V_i}{R_2}(R_1 + R_2 + R_3)$$

The closed loop gain of the differential I/O amplifier is given by

$$A_{CL(dif)} = \frac{(R_1 + R_2 + R_3)}{R_2}$$

Normally $R_1 = R_3$

Thus,

$$A_{CL(dif)} = \frac{(2R_1 + R_2)}{R_2}$$

The gain can be altered by adjusting the resistor R_2 .

The common mode gain of the differential I/O amplifier can be analysed by connecting the common mode voltage (V_n) to both the input terminals as shown in figure 2.3.

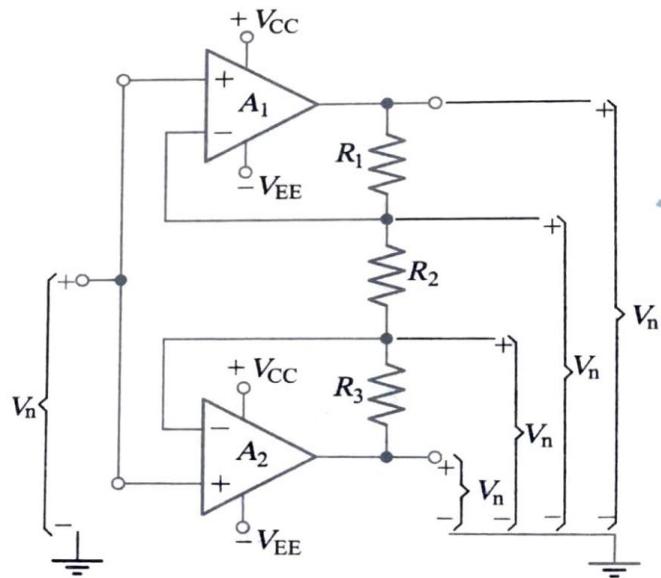


Figure 2.3: A differential input/output amplifier passes common mode inputs without attenuation

The junctions of R_1 , R_2 and R_2 , R_3 will be at the same voltage as the noninverting input terminal of A_1 and A_2 i.e., both the resistor junctions will be at the voltage V_n Volts w.r.t gnd. Thus there

is no current flowing through R_1 , R_2 , or R_3 . Thus the output voltage of each amplifier will be V_n . The common mode gain is $A_{CM} = 1$

Common mode signals are passed but not amplified.

Complete Instrumentation Amplifier (Three Op-amp Instrumentation Amplifier)

The instrumentation amplifier consists of 2 stages one is differential input/output amplifier in stage 1 and difference amplifier in stage 2 as shown in the figure 2.4.

The difference amplifier uses the differential output voltages from the differential input/output amplifier to drive a grounded load.

The differential input/output stage offers a very high input resistance at each input terminal.

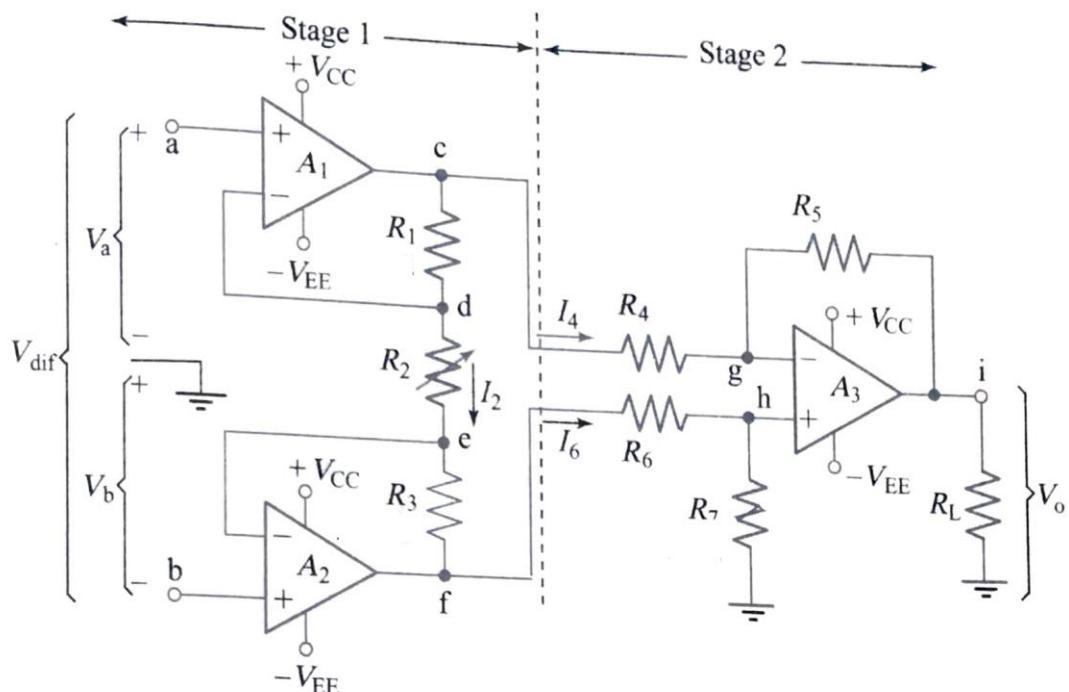


Figure 2.4: Instrumentation amplifier consisting of a differential input/output amplifier and difference amplifier

The voltage gain of the instrumentation amplifier is the

$$A_{CL} = A_{CL1} \times A_{CL2}$$

where A_{CL1} is the voltage gain of stage 1 and A_{CL2} is the stage 2 gain.

The overall gain can be controlled by adjustment of R_2 .

Advantages of Three Op-amp Instrumentation Amplifier

The gain of a three op-amp instrumentation amplifier circuit can be easily varied and controlled by adjusting the value of R_2 without changing the circuit structure.

The gain of the amplifier depends only on the external resistors used. Hence, it is easy to set the gain accurately by choosing the resistor values carefully.

The input impedance of the instrumentation amplifier is dependent on the non-inverting amplifier circuits in the input stage. The input impedance of a non-inverting amplifier is very high.

The output impedance of the instrumentation amplifier is the output impedance of the difference amplifier, which is very low.

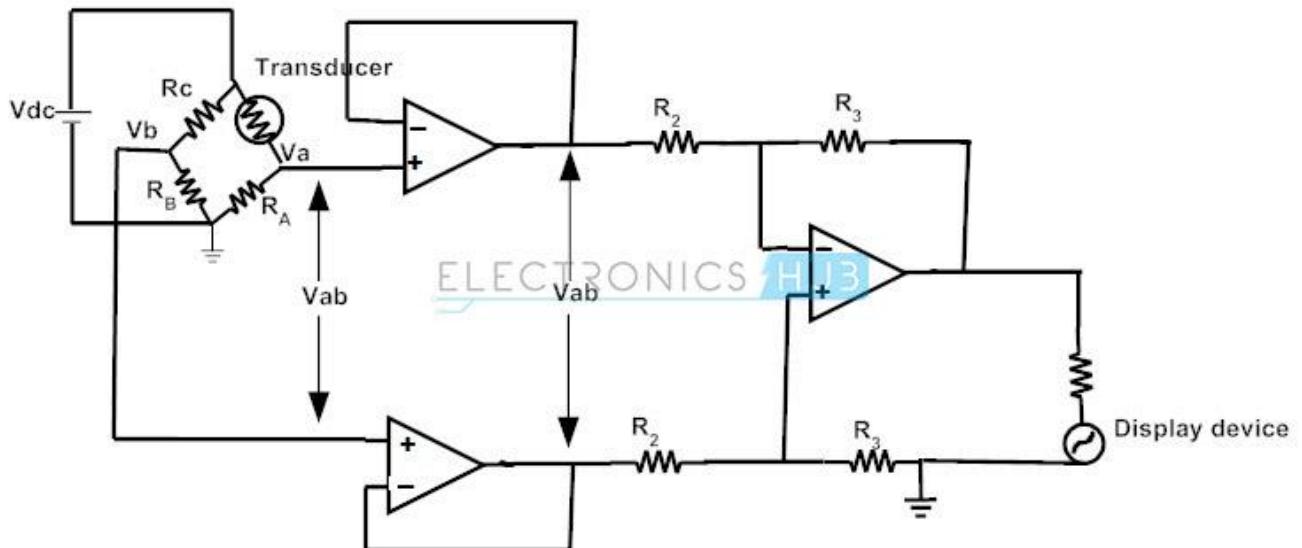
The CMRR of the op-amp $3(A_3)$ is very high and almost all of the common mode signal will be rejected.

SLE Component: Transducer Bridge Instrumentation Amplifier

The resistive transducer bridge is a network of resistors whose resistance varies due to changes in some physical condition. For example, Thermistors change their resistance with temperature and Light Dependent Resistors change their resistance to change in light intensity.

By making such a bridge as a part of the circuit, it is possible to produce an electrical signal proportional to the change in the physical quantity being measured.

Such an electrical signal can be amplified and used to monitor and control the physical process. An instrumentation amplifier can be constructed with a transducer bridge connected to one of its input terminals, as shown in the figure below.



Let the resistance of the transducer device in the resistive bridge be R_T and the change in its resistance be ΔR . The effective resistance of the transducer device is $R_T \pm \Delta R$. The resistive bridge is supplied with a DC voltage, V_{dc} .

When the bridge is balanced, i.e. at some reference condition of the physical quantity being measured, we get,

$$V_a = V_b$$

$$R_A(V_{dc})/(R_A+R_T) = R_B(V_{dc})/(R_B+R_C)$$

Under this condition, the differential input to the instrumentation amplifier is

$$V_{Diff} = V_b - V_a = 0$$

Thus, the output of the amplifier is zero. Consequently, the display device connected at the output displays the reference value of the physical quantity being measured.

The reference condition is generally chosen by the designer and it depends on the device characteristics of the transducer, the type of physical quantity being measured and the type of the application.

When there is a change in the physical quantity being measured, the voltage V_a will no longer be equal to V_b . This is because the resistance of the transducer device changes from R_T to $(R_T \pm \Delta R)$.

This produces a differential input for the instrumentation amplifier and the output of the amplifier will no longer be zero.

The resistances R_B and R_C are constant and hence the voltage V_B remains same as before, i.e.

$$V_b = R_B(V_{dc})/(R_B + R_C)$$

But the voltage V_a changes due to the change in resistance of the transducer device and is now given as,

$$V_a = R_A(V_{dc})/(R_A + R_T + \Delta R)$$

The differential voltage V_{Diff} is,

$$V_{Diff} = V_b - V_a$$

$$V_{Diff} = \{R_B(V_{dc})/(R_B + R_C)\} - \{R_A(V_{dc})/(R_A + R_T + \Delta R)\}$$

If all the resistances in the circuit are chosen to be of same value, i.e. $R_A = R_B = R_C = R_T = R$

$$V_{Diff} = \{R(V_{dc})/(2R)\} - \{R(V_{dc})/(2R + \Delta R)\}$$

$$V_{Diff} = \{RV_{dc}[2R + \Delta R] - R.V_{dc}.2R\}/2R(2R + \Delta R)$$

$$V_{Diff} = \cancel{R}.V_{dc}[\cancel{2R} + \Delta R - \cancel{2R}]/\{2\cancel{R}(2R + \Delta R)\}$$

$$V_{Diff} = \Delta R(V_{dc})/\{2(2R + \Delta R)\}$$

If the value of V_{Diff} is positive, it indicates that V_b is greater than V_a .

The output of the instrumentation amplifier is given as,

$$V_o = (R_3/R_2)V_d$$

$$V_o = (R_3/R_2) [\Delta R(V_{dc})/\{2(2R + \Delta R)\}]$$

As the change in resistance $\Delta R \ll 2R$, V_o can be written as,

$$V_o = (R_3/R_2)[\Delta R/4R](V_{dc})$$

From the above equation, it can be noted that the output depends on the change in the resistance ΔR . The display can be calibrated in terms of the units of the physical quantity being measured.

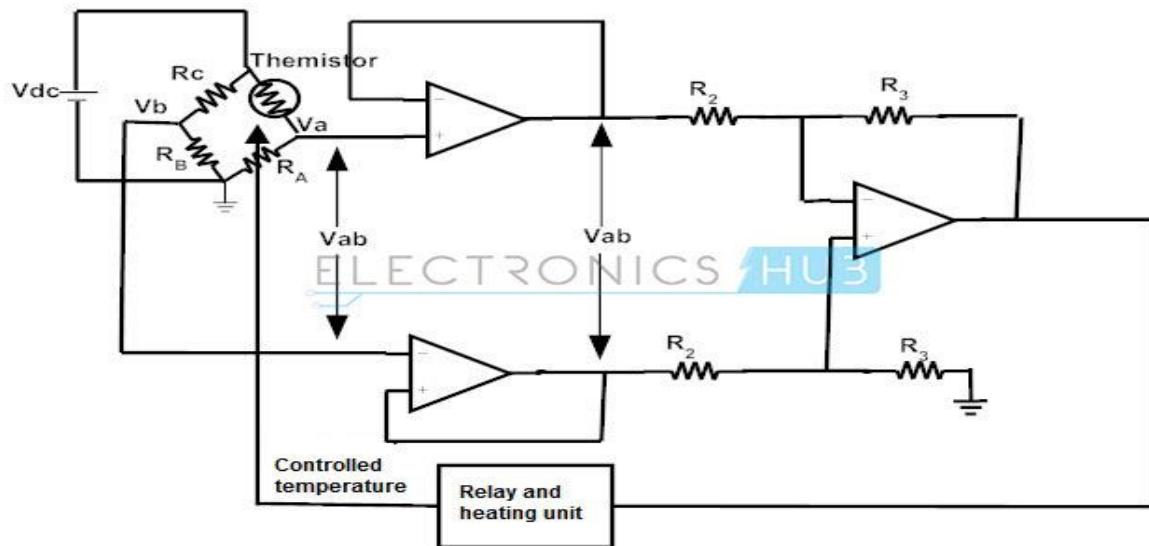
Applications of Instrumentation Amplifier

The instrumentation amplifier, along with a transducer bridge can be used in a wide variety of applications. These applications are generally known as data acquisition systems.

At the input stage, there is a transducer device that converts the change in the physical quantity to an electrical signal.

The electrical signal is fed to an instrumentation amplifier. The amplified signal is then fed to a display device, which is calibrated to detect the change in the quantity being measured.

Temperature Controller



A simple temperature controller system can be constructed using a thermistor as the transducer device, in the resistive bridge, as shown in the figure above.

The resistive bridge is kept balanced for some reference temperature. For any change in this reference temperature, the instrumentation amplifier will produce an output voltage, which drives the Relay which in turn turns ON/OFF the heating unit, thereby controlling the temperature.

Temperature Indicator

The circuit shown for temperature controller can also be used as a temperature indicator. The resistive bridge is kept balanced for a particular reference temperature when $V_o = 0V$.

The temperature indicating meter is calibrated to reference temperature, corresponding to this reference condition.

As temperature changes, the amplifier output also changes. The gain of the amplifier can be appropriately set to indicate the desired range of temperature.

Light Intensity Meter

The same circuit can be used to detect variations in the intensity of light, by replacing the thermistor by a Light Dependent Resistor (LDR). The bridge is set to a balanced condition in darkness.

When light falls on the LDR, its resistance changes and unbalances the bridge. This causes the amplifier to produce a finite output, which in turn drives the meter.

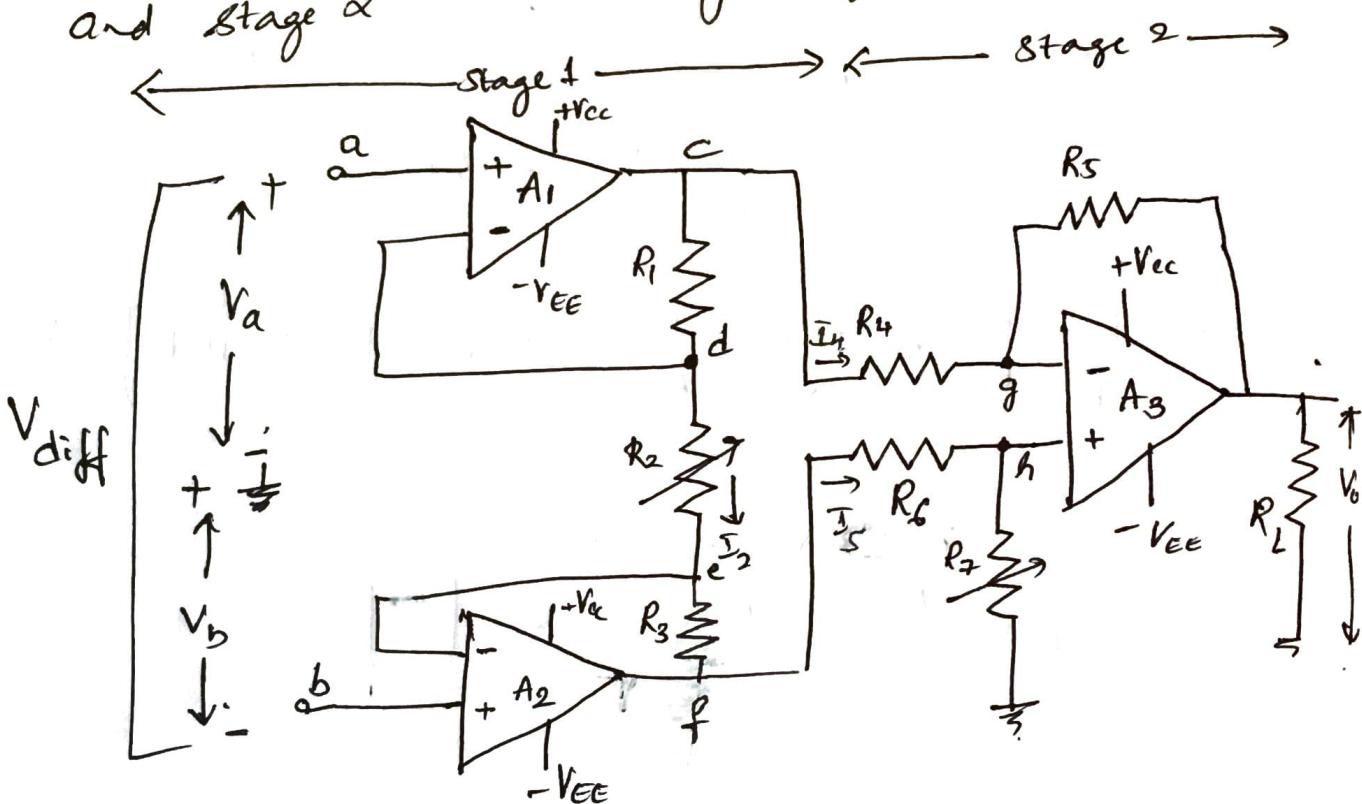
Instrumentation Amplifiers

Problems

- ① Design the instrumentation amplifier shown in figure to use -op-amps with 750 nA maximum input bias current. The circuit is to produce an output ranging from 4V to 8V when the input is 10mV to 20mV.

Soln

Design stage 1 to produce all of the voltage gain and stage 2 to have a gain of 1.



$$I_2 = 100 I_B(\text{max}) \text{ of MA741} \\ = 100 \times 750 \text{nA} = \underline{\underline{75 \mu\text{A}}}$$

$$R_2 = \frac{V_{\text{min}}}{I_2(\text{min})} = \frac{10 \text{mV}}{75 \mu\text{A}} = \frac{133 \Omega}{\text{std resistance}}$$

$$V_o = 4V, \quad V_{R1} = 2V \quad \& \quad V_{R3} = 2V$$

$$R_1 = R_3 = \frac{V_{R1}}{I_{Q(\text{min})}} = \frac{2V}{75\text{mA}}$$

$$R_1 = R_3 = 26.6\text{k}\Omega \quad (\text{use } 27\text{k}\Omega \text{ std value}).$$

When $V_o = 4V$ for the first stage

$$V_C = +2V \quad \text{and} \quad V_F = -2V$$

giving $V_{R6} = V_{R7} = 1V$

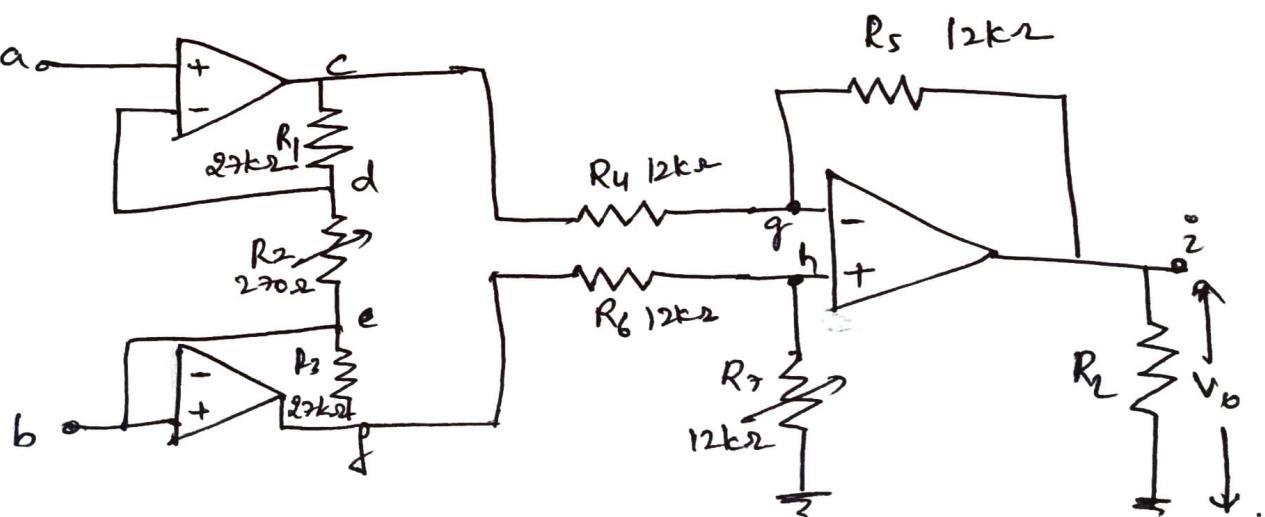
$$R_6 = \frac{V_{R6}}{I_{Q(\text{min})}} = \frac{1V}{75\text{mA}}$$

$$R_6 = 13.3\text{k}\Omega$$

for second stage to have a gain of 1

$$R_4 = R_5 = R_6 = R_7 = 12\text{k}\Omega$$

- (D) Calculate the overall voltage gain for the instrumentation amplifier shown in fig. Also determine the dc voltage levels throughout the circuit when the input a terminals a and b is respectively $+10\text{mV}$ and -10mV and a 1V common mode input is present



V to I and I to V converters

Voltage to Current Converter (Transconductance Amplifier)

The types of circuit to convert a voltage signal to a proportional output current are

① V-I Converter with floating load

② V-I Converter with grounded load.

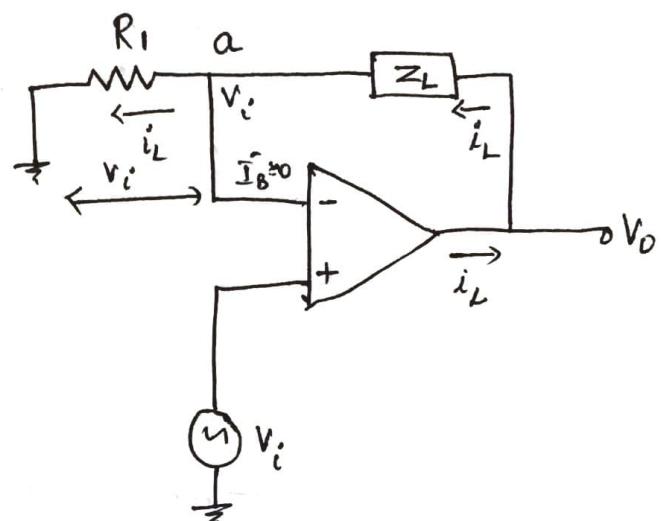
V-I Converter with floating load

The figure shows a V-I converter in which load Z_L is floating.

At node a Voltage = V_i^o

$$\therefore V_i^o = i_L R_1$$

$$i_L = \frac{V_i^o}{R_1} \quad \text{--- (1)}$$



The input voltage V_i is converted into an output current of $\frac{V_i^o}{R_1}$.

Voltage to current converter with floating load

The same current flows through the signal source and load. Thus signal source should be capable of providing this load current.

V-I Converter with grounded load

Let V_a be the voltage at node a

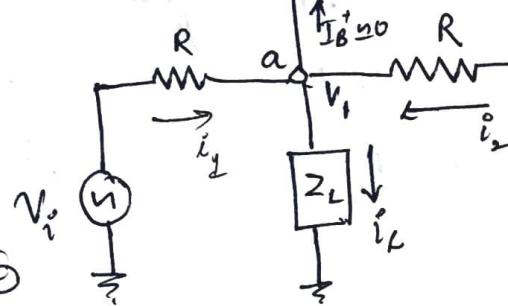
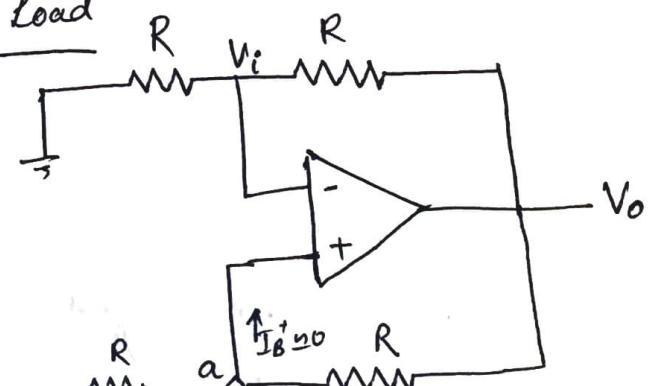
Apply KCL at node V_i , ($V_a = V_i$)

$$i_1 + i_2 = i_L \quad \text{--- (1)}$$

$$\frac{V_i - V_a}{R} + \frac{V_o - V_a}{R} = i_L$$

$$V_i + V_o - 2V_a = i_L R_1$$

$$\therefore V_a = \frac{V_i + V_o - i_L R_1}{2} \quad \text{--- (2)}$$



Op-amp is in non-inverting mode, the gain of circuit.

$$A = 1 + \frac{R_f}{R} = 2$$

∴ The output voltage of the circuit is given by

$$\begin{aligned} V_o &= AV_i \\ &= 2 \left(\frac{V_i + V_o - i_L R}{2} \right) \end{aligned} \quad \text{Solve from (2)}$$

$$V_o = V_i + V_o - i_L R$$

$$\boxed{i_L = \frac{V_i}{R}} \quad \text{--- (3)}$$

As the Input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source.

Applications

low voltage dc and ac voltmeter

LED and Zener diode tester.

Current to Voltage Converter (Transresistance Amplifier)

Photo cell, photo diode and photo voltaic cell give an output current that is proportional to an incident radiant energy or light.

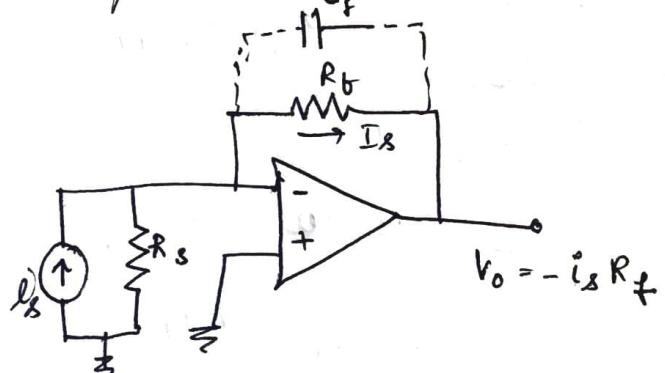
The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light incident on the photo devices can be measured.

→ The figure shows to I-V converter

→ input terminal is a virtual ground

$i_s \rightarrow$ flows through R_f

$$\therefore \boxed{V_o = -i_s R_f}$$



Current to voltage Converter.

The lowest current that this circuit can measure depends on the bias current (I_B) of the op-amp.

For MA 741 $I_B = 3\text{nA}$ can be used to detect lower currents.

→ R_F is shunted with a capacitor C_F to reduce high frequency noise and possibility of oscillations.

- Applications :-
- Photo diode detector
 - Photo FET detector.
 - DAC.

Problem :

① For a V-I converter shown in fig. $V_{in} = 5V$, $R = 10\text{ k}\Omega$. $V_1 = 1\text{ V}$. Find the load current and output voltage V_o . Assume the op-amp is initially nulled.

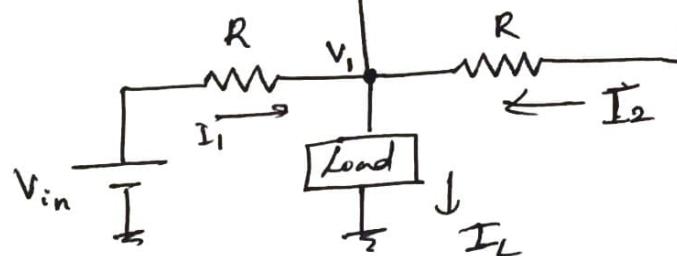
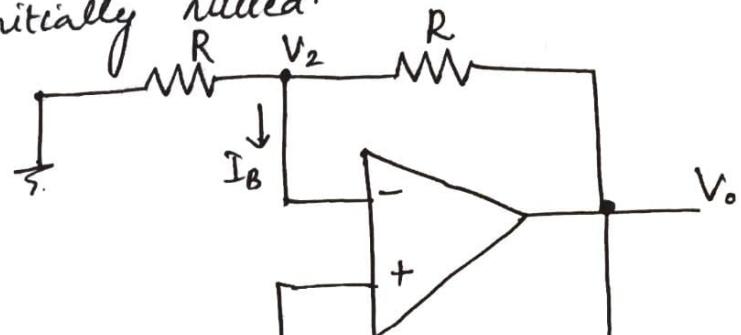
Soln.

Assume $I_B = 0$.

$$I_L = I_1 + I_2$$

$$= \frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R}$$

$$= \frac{V_{in} + V_o - 2V_1}{R} = I_L$$



The gain of the op-amp circuit is

$$A = 1 + \frac{R}{R} = 2$$

$$V_o = 2V_1 \Rightarrow \underline{\underline{2V}}$$

given $V_1 = \underline{\underline{1V}}$

$V_{in} = 5V$

$R = 10\text{ k}\Omega$

$$I_L = \frac{5 + 2 - 2(1)}{10\text{k.}} = \frac{5}{10\text{k.}}$$

$$\boxed{I_L = 0.5\text{mA}}$$

Unit - 2 Op-Amp Linear Applications

Differentiating Circuits

A differentiating circuit produces an output voltage that is proportional to the rate of change of the input voltage.

Consider the OP waveforms illustrated in fig. which shows a ~~exp~~ triangular wave input and the resultant square wave output produced by differentiation.

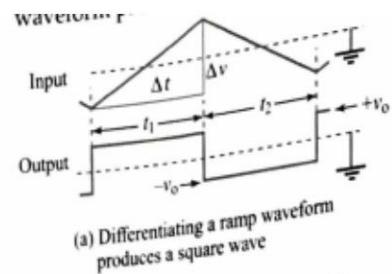
→ At time t_1 the triangular wave is changing at the rate of $\frac{\Delta V}{\Delta t}$

This rate of change is represented by $+V_o$ on the OP waveform.
(constant)

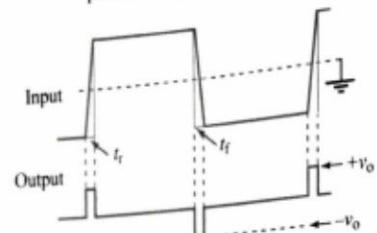
→ At time t_2 the rate of change of I/p is $-\frac{\Delta V}{\Delta t}$ and thus $-V_o$ is the output voltage.

Thus differentiation of Δ ^{lar} wave produces square wave.

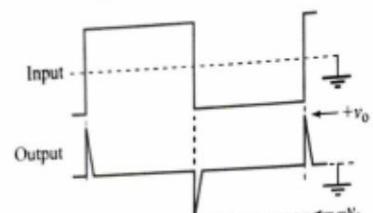
Differentiation of dc I/p is zero.



(a) Differentiating a ramp waveform produces a square wave



(b) Differentiation of a square wave with significant rise and fall times



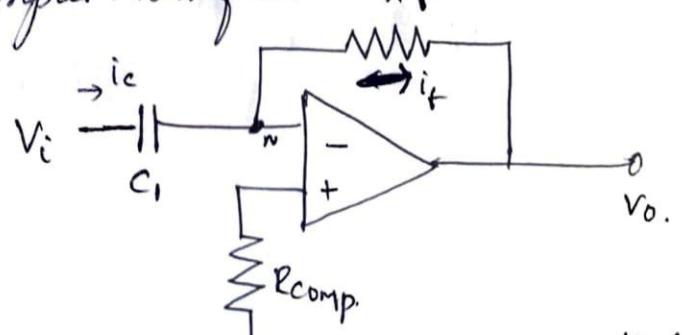
(c) Differentiation of a square wave with fast rise and fall times

Op-amp Differentiator

The circuit performs the mathematical operation of differentiation. i.e., the output waveform is the derivative of the input waveform. R+

Analysis

The node N is at virtual ground $V_N = 0$.



Op-Amp Differentiator

The current i_C through capacitor is

$$i_C = C_1 \frac{d(V_i - V_o)}{dt} = C_1 \frac{dV_i}{dt} \quad \text{--- (1)}$$

The current if through the feedback resistor is
 $i_f = \frac{(V_o - V_o)}{R_f}$ and there is no current entering the opamp.

$$\therefore i_C = i_f$$

$$C_1 \frac{dV_i}{dt} = \frac{V_o - V_o}{R_f}$$

$$C_1 \frac{dV_i}{dt} = -\frac{V_o}{R_f}$$

$$V_o = -R_f C_1 \frac{dV_i}{dt} \quad \text{--- (2)}$$

The output voltage V_o is a constant ($-R_f C_1$) times the derivative of the I/P voltage V_i .
-ve sign indicates a 180° phase shift of the output waveform wrt input signal.

The phasor equivalent $V_o(s) = -R_f C_1 s V_i(s)$

By taking L.T of (2).

where V_o and V_i is the phasor representation of V_o &

In steady state $s = j\omega$

magnitude of Gain of the differential amplifier

$$|A| = \left| \frac{V_o}{V_i} \right|$$

$$= |-j\omega R_f C_1|.$$

$$|A| = \omega R_f C_1 \quad \text{--- (3)}$$

from eqn ③ frequency response of the op-amp differentiator can be drawn.

Eqn ③ can be written

$$|A| = \frac{f}{f_a}$$

where $f_a = \frac{1}{2\pi R_F C_1}$ — 4

At $f = f_a \Rightarrow |A| = 1$ i.e. 0 dB

and the gain increases at the rate of 20 dB/decade. Thus a high frequency differentiator may become unstable and break into oscillations.

~~$|A| = f_a$~~

$$|A| = 2\pi f R_F C_1$$

$$|A| = \frac{f}{\left(\frac{1}{2\pi R_F C_1}\right)} = \frac{f}{f_a}$$

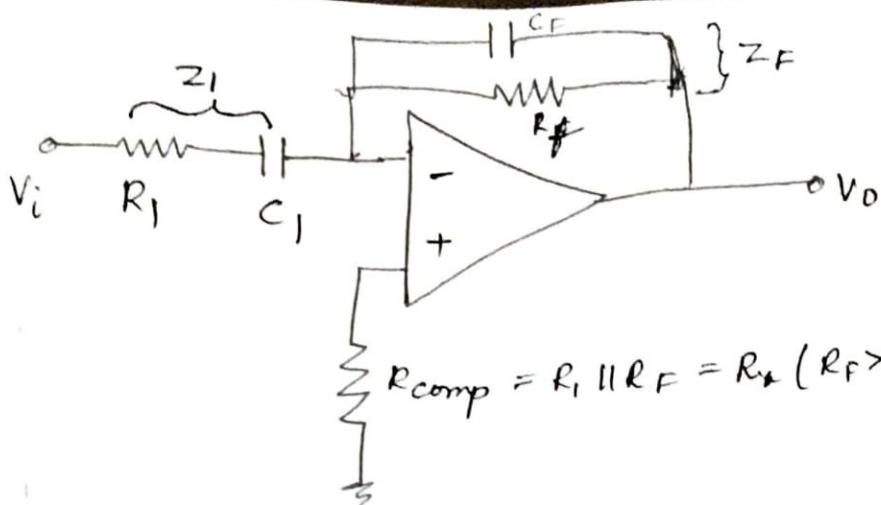
The input impedance of the differentiator circuit is given $Z_i = X_C = \frac{1}{j\omega C}$

∴ The input impedance decreases with the increase in the frequency thereby making the circuit more sensitive to high frequency noise.

Practical Differentiator :-

A practical differentiator shown in fig eliminates the limitations of basic differentiator (i.e. instability and high frequency noise)

Adding Resistance R_1 would maintain high input impedance even at high frequencies.



Practical differentiator.

The transfer function for the ckt.

$$\frac{V_0(s)}{V_i(s)} = \frac{-Z_F}{Z_1}$$

$$Z_1 = (R_1 + X_C) = \left(R_1 + \frac{1}{j\omega C_1} \right) \Rightarrow \frac{1}{j\omega C_1} (1 + R_1 j\omega C_1)$$

$$Z_F = R_f \parallel X_{CF}$$

$$= \frac{R_f X_{CF}}{R_f + X_{CF}} = \frac{\frac{R_f}{j\omega C_F}}{\frac{R_f}{j\omega C_F} + \frac{1}{j\omega C_F}} = \frac{R_f}{1 + j\omega R_f C_f}$$

$$\frac{V_0(s)}{V_i(s)} = -\frac{Z_F}{Z_1} = -\frac{s R_f C_1}{(1 + s R_1 C_1)(1 + s R_f C_f)} \quad \boxed{S = j\omega \text{ at steady state}} \quad \boxed{5}$$

For $R_f C_f = R_1 C_1$

$$\frac{V_0(s)}{V_i(s)} = -\frac{s R_f C_1}{(1 + s R_1 C_1)^2}$$

For steady state $S = j\omega$

$$s R_1 C_1 = j\omega R_1 C_1 = j2\pi f R_1 C_1$$

where $f_b = \frac{1}{2\pi R_1 C_1}$

$$= j\frac{1}{2\pi R_1 C_1} = j\frac{f_b}{2\pi R_1 C_1}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-s R_F C_1}{\left(1 + j \frac{s}{f_b}\right)^2} \quad \textcircled{7}$$

angle $(V_o(s)/V_i(s)) = -90 - 2\text{inv}(\tan f/f_b)$ --- (A)

From equation $\textcircled{7}$ it can be seen that gain increases at $+20 \text{ dB/decade}$ for frequency $f < f_b$
 → decreases -20 dB/decade for $f > f_b$ as shown in fig below.
 This $+40 \text{ dB/decade}$ change in gain is caused by R, C and RF CF factors.

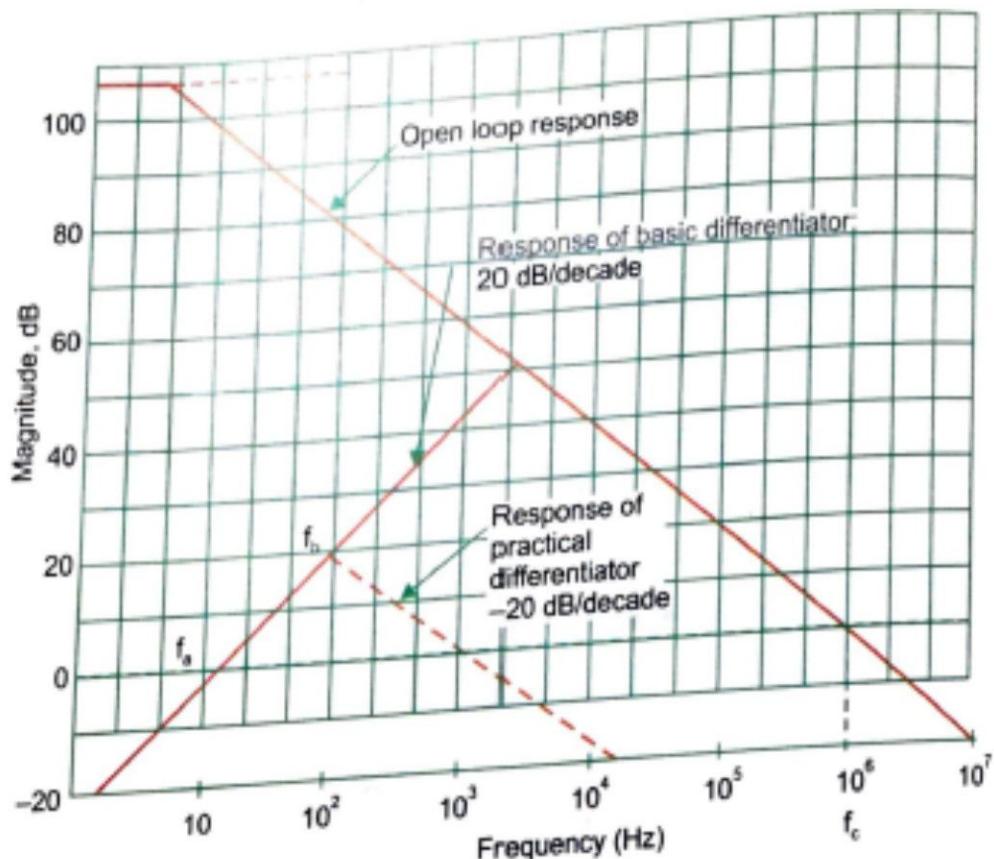


Fig. 4.37 (c) Frequency response

For the basic differentiator circuit the frequency response would have increased continuously at the rate of $+20 \text{ dB/decade}$ even beyond f_b causing stability problem at high frequency.

Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems.

The value of f_b has to be chosen such that
 $f_a < f_b < f_c$

where f_c is the unity gain bandwidth of the opamp in open-loop configuration.

For good differentiation. Time period of the input signal is larger than or equal to $R_f C_1$

$$T \geq R_f C_1$$

If $R_f C_1 \ggg R_i C_1$ or $R_f C_F$ then eqn ⑤. would be reduced to

$$\frac{V_o(s)}{V_i(s)} = -s R_f C_1$$

i.e. the expression for output voltage remains the same as ideal differentiator as

$$V_o = -R_f C_1 \frac{dV_i}{dt}$$

⑧

$R_{comp} = (R_i || R_f) \rightarrow$ to compensate for the input bias current.

A good differentiator may be designed as per the following steps:

① Choose f_a equal to the highest frequency of the input signal. Assume practical value of $C_F (< 1 \text{ MF})$ and calculate R_F

② Choose $f_b = 10 f_a$. Now calculate R_i & C_F so that

$$R_i C_1 = R_F C_F$$

- Problem: design an op-amp differentiator that will differentiate an input signal with $f_{max} = 100 \text{ Hz}$
- i) input signal with $f_{max} = 100 \text{ Hz}$
 - ii) draw the output waveform for a sine wave of 1V peak at 100Hz applied to the differentiator
 - iii) repeat (i) for a square wave input.

Soln: $f_a = f_{max} = 100 \text{ Hz} = \frac{1}{2\pi R_f C_1}$

Let $C_1 = 0.1 \mu\text{F}$

$$R_f = \frac{1}{2\pi(10^3)(10^{-7})} = 15.9 \text{ k}\Omega$$

Now choose $f_b = 10 f_a = 1 \text{ kHz} = \frac{1}{2\pi R_1 C_1}$

$$\therefore R_1 = \frac{1}{2\pi \times 10^3 \times 10^{-7}} = 1.59 \text{ k}\Omega$$

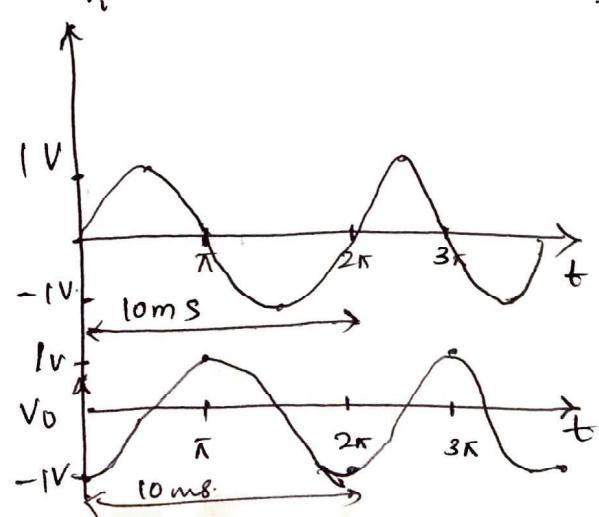
$$R_1 C_1 = R_F C_F$$

$$C_F = \frac{R_1 C_1}{R_F} = \frac{1.59 \times 10^3 \times 0.1 \mu\text{F}}{15.9 \times 10^3 \Omega} = 0.01 \mu\text{F}$$

(i) $V_i = 1.8 \sin(2\pi \times 100 \times t) = 1.8 \sin(2\pi 100t)$

$$\begin{aligned} V_o &= -R_f C_1 \frac{dV_i}{dt} \\ &= (15.9 \text{ k}\Omega)(0.1 \mu\text{F}) \frac{d[\sin 2\pi(10^2)t]}{dt} \\ &= -15.9 \text{ k}\Omega \times 0.1 \mu\text{F} \times 2\pi \times 100 \cos 2\pi(10^2)t \\ &= -0.999 \cos(2\pi(10^2)t) \end{aligned}$$

$$V_o = -1 \cos(2\pi(10^2)t)$$



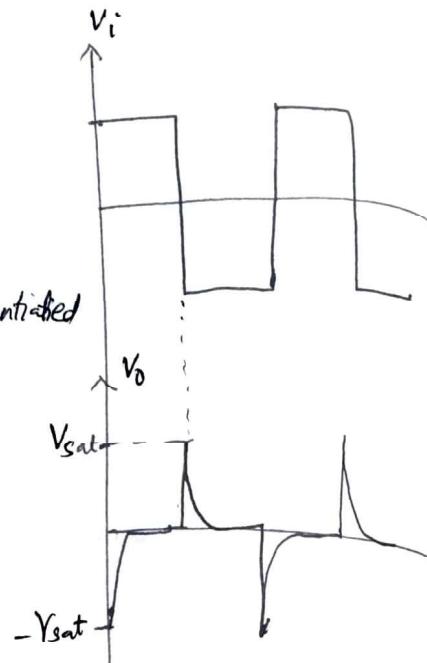
(ii) For square wave input, say 1V peak and 1kHz

The o/p would be positive and negative

Spikes of magnitude V_{sat} with is approximately 13V for $\pm 15V$ op-amp power supply.

→ During the periods for which input is constant at $\pm 1V \Rightarrow$ the differentiated output will be zero.

However when ~~transistor~~ input transits between $\pm 1V$ levels, the slope of the input is infinite for an ideal square wave.



Integrator:-

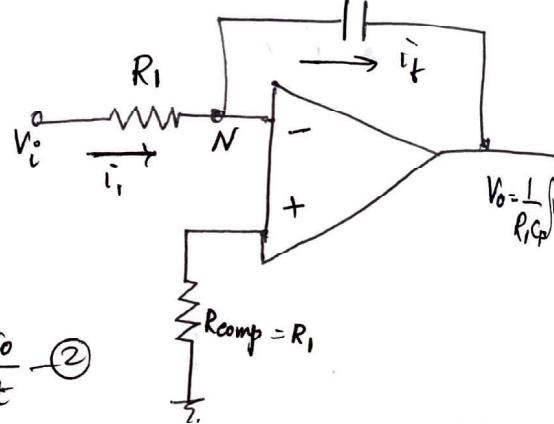
If resistor and capacitor of the differentiator we get the integrator.

$$i_1 = i_F \quad \textcircled{1}$$

$$i_1 = V_i - V_N = \frac{V_i}{R_1} \quad \textcircled{2}$$

$$i_F = -\left(\frac{dV_o}{dt}\right) C_F = -C_F \frac{dV_o}{dt} \quad \textcircled{3}$$

Solve $\textcircled{2}$ & $\textcircled{3}$ in $\textcircled{1}$



Inverting op-amp integrator

$$\frac{V_i - 0}{R_1} = -C_F \frac{dV_o}{dt}$$

$$\frac{dV_o}{dt} = -\frac{V_i}{R_1 C_F} \quad \text{Integrating both sides we get}$$

$$\int_0^t dV_o = -\frac{1}{R_1 C_F} \int_0^t V_i dt$$

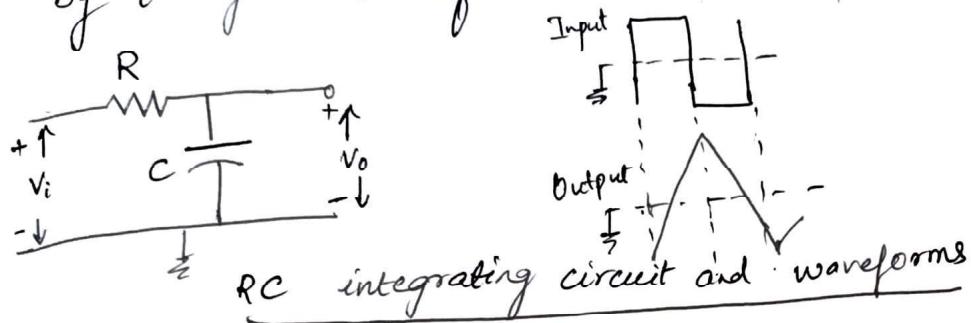
$$V_o(t) = \frac{-1}{R_1 C_F} \int_0^t V_i(t) dt + V_o(0)$$

$V_o(0)$ is the initial output voltage.

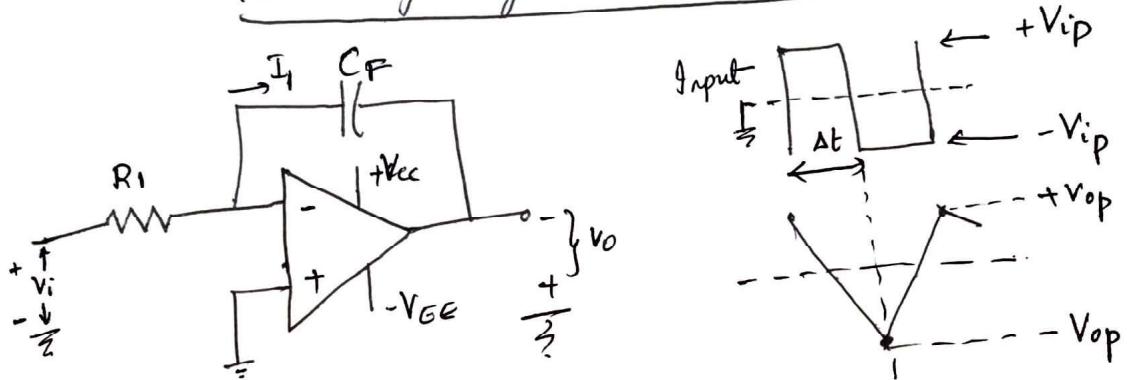
A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires large value R & C.

An integrating circuit produces an output voltage that is proportional to the area under the input voltage waveform (amplitude multiplied by time).

For a square wave input the resultant waveform would be triangular waveform.



RC integrating circuit and waveforms



Basic op-amp integrating circuit and waveforms

- The op-amp integrator shown in fig by Miller's the the effective input capacitance becomes $C_F(1-A_v)$ where A_v is gain of the opamp.

A_v is infinite for an ideal op-amp, so the effective time constant of the op-amp integrator becomes very large which results in perfect integration.

The operation of the integrator can also be studied in the frequency domain. In phasor notation can be written as

$$V_o(s) = -\frac{1}{sR_1C_F} V_i(s)$$

In steady state $s = j\omega$

$$V_o(j\omega) = \frac{-1}{j\omega R_1 C_F} V_i(j\omega)$$

So the magnitude of the gain or integrator transfer function is

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{-1}{j\omega R_1 C_F} \right| = \frac{1}{\omega R_1 C_F}$$

The frequency response of the basic integrator is as shown in fig. The Bode plot is a straight line of slope -6dB/decade
(or -20dB/decade)

Integrator:-

If resistor and capacitor of the differentiator we get the integrator.

$$i_1 = i_F \quad \text{--- (1)}$$

$$i_1 = V_i - V_N = \frac{V_i}{R_1} \quad \text{--- (2)}$$

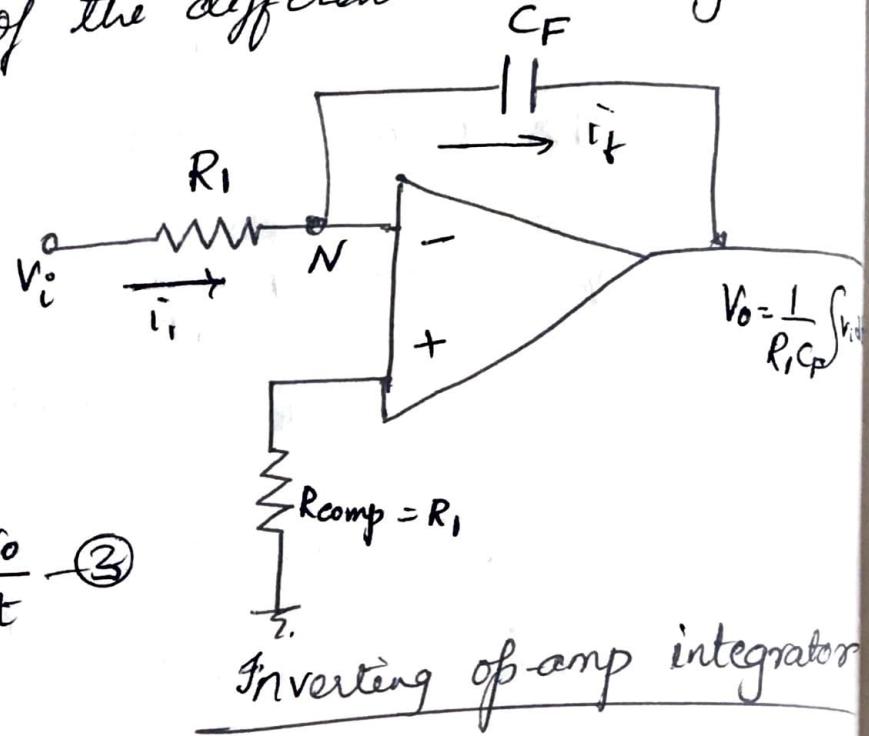
$$i_F = -\left(\frac{dV_o}{dt}\right) C_F = -C_F \frac{dV_o}{dt} \quad \text{--- (3)}$$

Solve (2) & (3) in (1)

$$\frac{V_i - 0}{R_1} = -C_F \frac{dV_o}{dt}$$

$$\frac{dV_o}{dt} = -\frac{V_i}{R_1 C_F}$$

$$\int_0^+ dV_o = -\frac{1}{R_1 C_F} \int_0^+ V_i dt$$



Integrating both sides we get

$$V_o(t) = \frac{-1}{R_1 C_F} \int_0^t V_i(t) dt + V_o(0)$$

(53)

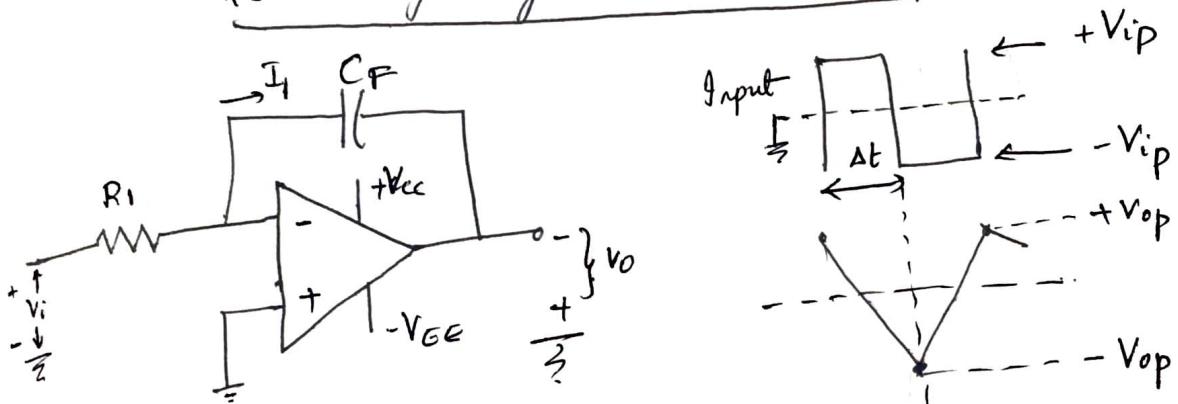
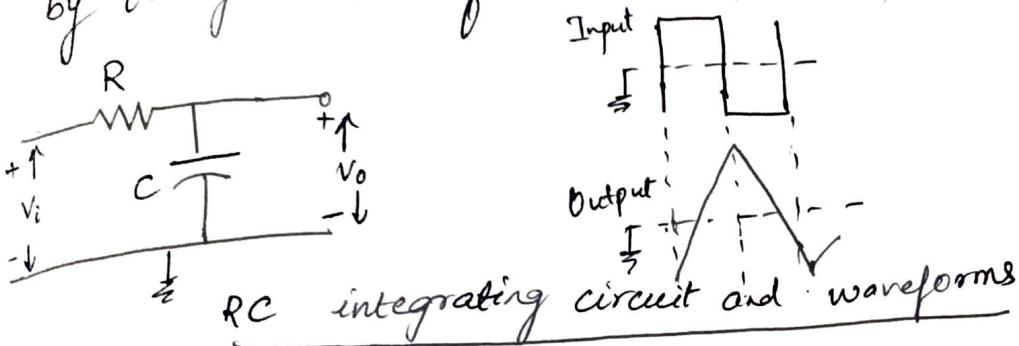
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Basic op-amp integrating circuit and waveforms

The op-amp integrator shown in fig by Miller's theorem, the effective input capacitance becomes $C_F(1+A_v)$ where A_v is gain of the op-amp.

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So The magnitude of the gain or integrator transfer function is

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| \frac{-1}{j\omega R_1 C_F} \right| = \frac{1}{\omega R_1 C_F}$$

The frequency response of this basic integrator is as shown in fig. The Bode plot is a straight line of slope $-20\text{dB}/\text{Octave}$ (or $-20\text{dB}/\text{decade}$)

The frequency (f_b) is the frequency at which the gain of the integrator is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

At $\omega=0 \Rightarrow |A| \rightarrow \infty$

At dc $\Rightarrow C_F$ behaves like an open circuit and there is no negative feedback. The op-amp operates in open loop resulting infinite gain. [for practical op-amp the output remains at saturation voltage V_{sat}]

As frequency increases the gain of the integrator decreases. The integrator circuit does not have any frequency problem as faced in differentiator

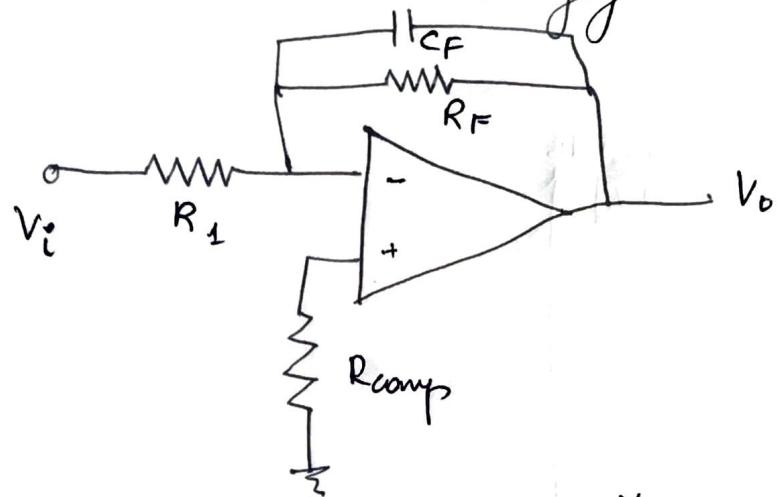
At dc the gain becomes infinite (or saturates) so we

design a practical integrator circuit.

Practical Integrator circuit (Lossy Integrator)

The gain at $\omega=0$ (low frequency) can be controlled by using feedback resistance R_F as shown in figure

The parallel R_F and C_F behaves like a practical capacitor which dissipates power. Hence this circuit is called a loss integrator.



Practical integrator circuit

R_F limits low-frequency gain

$$R_F = -\frac{R_F}{R_1} \quad (\text{usually } R_F = 10R_1)$$

Apply the nodal analysis at the inverting input terminal in s domain

$$\frac{V_i(s)}{R_1} + sC_F V_o(s) + \frac{V_o(s)}{R_F} = 0 \quad (8)$$

from which we have

$$V_o(s) = -\frac{1}{sR_1C_F + R_1/R_F} V_i(s) \quad (9)$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-1}{sR_1C_F + R_1/R_F}$$

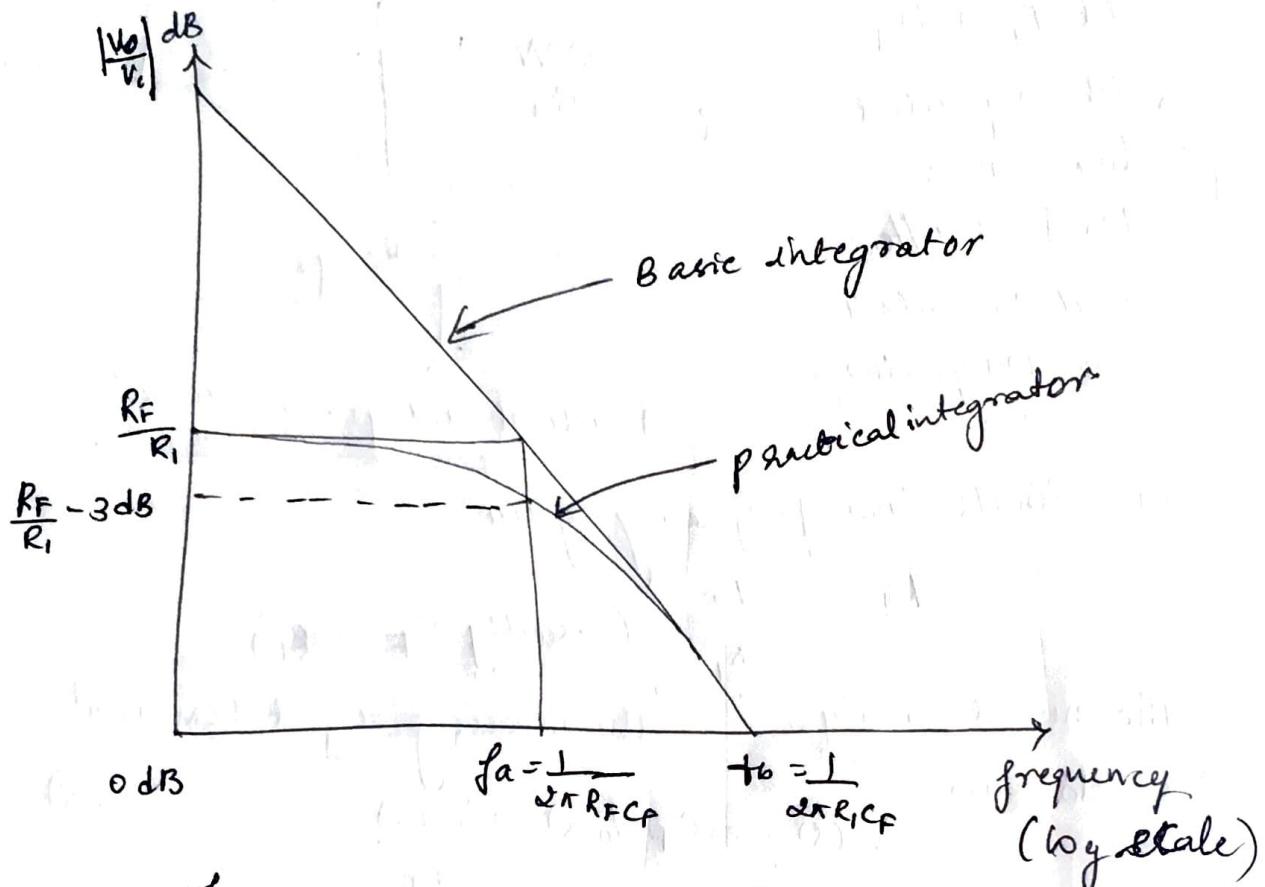
If R_F is large, loss integrator approximates the ideal integrator.

At steady state. $s=j\omega$

The magnitude of the integrator is given by

$$|A| = \sqrt{\frac{V_o}{V_i}} = \frac{1}{\sqrt{\omega^2 R_i^2 C_F^2 + R_i^2 / R_F^2}}$$

$$|A| = \frac{R_F / R_i}{\sqrt{1 + (\omega R_F C_F)^2}} \quad \text{--- (10)}$$



Frequency response of a basic integrator

At the break frequency ($f = f_a$) the gain is $0.707 \times \left(\frac{R_F}{R_i}\right)$ i.e. 3 dB below max gain of $\left(\frac{R_F}{R_i}\right)$

$$|A| = \frac{R_F / R_i}{\sqrt{1 + (\omega R_F C_F)^2}} = \frac{1}{\sqrt{2}}$$

At $f = f_a$

$$\sqrt{1 + (\omega R_F C_F)^2} = \sqrt{2}$$

Solving $\boxed{f_a = \frac{1}{2\pi R_F C_F}}$ --- (11)

(c5)

f_a is the frequency from where integration range starts

If $f < f_a$ this ckt is a simple inverting amplifier.

At $f = f_a \Rightarrow 50\%$ accuracy results.

The practical thumb rule is that if the input frequency is 10 times f_a then 99% accuracy can be obtained.

Problems :-

i) Consider the practical integrator ckt with the component values

$R_f = 10k\Omega$, $R_i = 100k\Omega$, $C_f = 10nF$. Determine the lower frequency limit of integration and study the response for the inputs (i) sine wave (ii) step input (iii) square wave

lower frequency $f_a = \frac{1}{2\pi R_f C_f}$

$$f_a = \frac{1}{2\pi \times 100k \times 10n} = \underline{\underline{159 \text{ Hz}}}$$

For 99% accuracy of at least $\underline{\underline{1.59 \text{ kHz}}}$

Accurate integration can be achieved beyond this frequency.

(i) Sine wave input

For an 1V peak sine wave at 5kHz, the o/p v_o is

$$v_o(t) = -\frac{1}{R_f C_f} \int v_i(t) dt$$

$$= -\frac{1}{10k \times 10n} \int 1 \sin(2\pi 5000t) dt$$

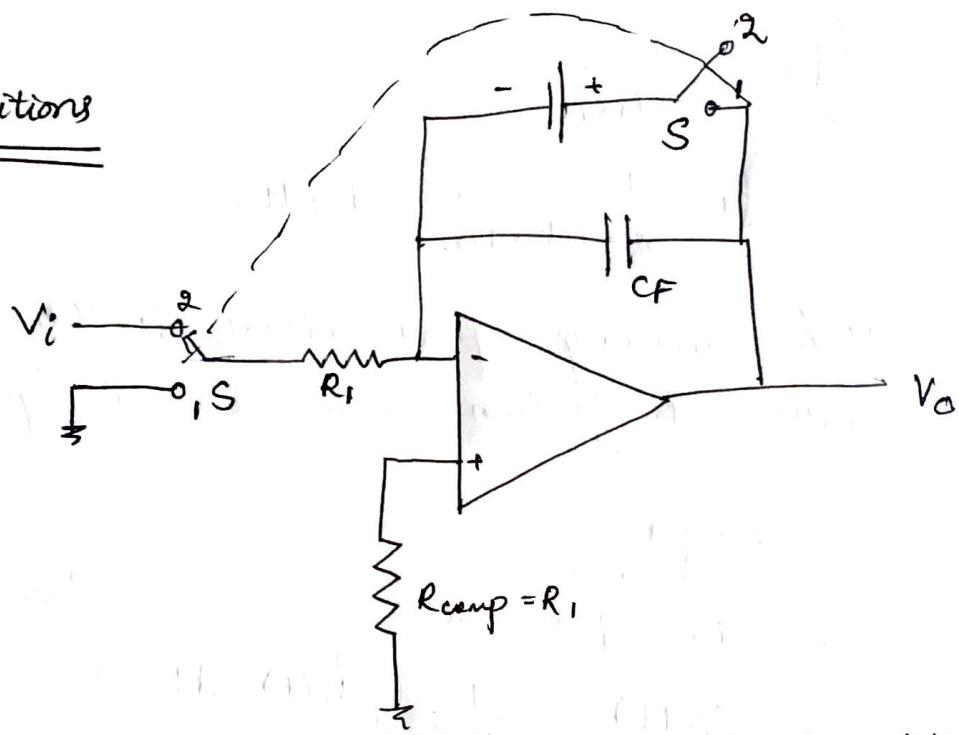
$$= -\frac{10^4}{2\pi 5000} (-\cos 2\pi 5000t)$$

$$v_o(t) = \underline{\underline{0.318 (\cos 2\pi 5000t)}}$$

My solve of step & square wave

- ② Find R_i and R_f in the practical integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $\omega = 10,000 \text{ rad/s}$. Use a capacitance of $0.01 \mu\text{F}$.
- ③ Show that the output of an op-amp integrator to a step input of magnitude V volts is given by
- $$V_o = A_v V \left(1 - e^{-t/R_i C_F} (1 - A_v) \right)$$
- Compare this result with the output obtained from a low pass RC circuit.
- ④ Obtain the expression for the op voltage of non-inverting op-amp integrator circuit.

Initial Conditions



Integrator circuit showing initial conditions

An integrator must also be provided with an external circuit to introduce initial conditions as shown in figure.

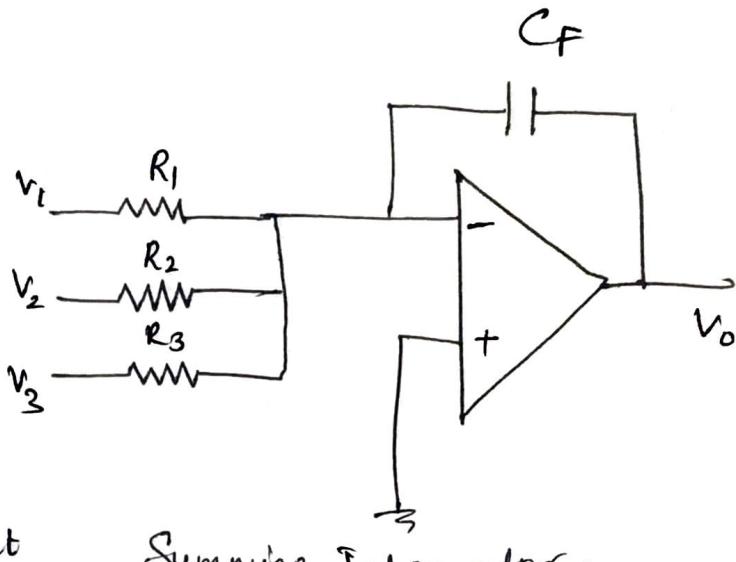
When ganged switch S is in position 1, the input is zero and the capacitor is charged to the voltage V almost instantaneously setting the initial condition $V_o(0) = V$.

(56)

S is in position 2, the amplifier is connected as an integrator and O/P will be V plus + a constant $\frac{1}{R_1 C_F}$ times the integral of the input voltage V_i .

Summing Integrator :-

The output voltage of op-amp summing integrator is given by



$$V_0 = -\frac{1}{C_F} \left[\int \frac{V_1(t)}{R_1} dt + \int \frac{V_2(t)}{R_2} dt + \int \frac{V_3(t)}{R_3} dt \right] + V_0(0).$$

Summing Integrator.

$$V_0 = -\frac{1}{C_F} \left[\frac{1}{R_1} \int V_1(t) dt + \frac{1}{R_2} \int V_2(t) dt + \frac{1}{R_3} \int V_3(t) dt \right] + V_0(0)$$

— (12)

$$\therefore V_0(s) = \frac{-1}{s C_F} \left[\frac{V_1(s)}{R_1} + \frac{V_2(s)}{R_2} + \frac{V_3(s)}{R_3} \right]$$

Active filters

Electric filters are widely used in communication and signal processing and in ^{one} form or another in almost all sophisticated electronic instruments.

→ Such filters can be built from:

(i) passive RLC components

(ii) crystals

(iii) resistors, capacitors and op-amps (active filters)

Active filters

By using passive components filters can be designed but this works well for high frequencies ie Radio frequencies. At audio frequencies, inductors become problematic as the inductors become large, heavy and expensive. This can be overcome by using active filters.

Active filters use the op-amp as the active element and resistors and capacitors as passive elements

The active filters use capacitors in the feedback loop, avoid using inductor.

The advantage of op-amp filters → they provide gain.
→ op-amp is in noninverting configuration

it offers high input impedance and low output impedance.

This increases the load drive capacity & load is isolated from the frequency determining network

Large R_L can be chosen

Limitations of the active filters

① High frequency response is limited by the gain Bandwidth (GBW) product & slew rate of the op-amps.

② High frequency active filters are more expensive than the passive filters. Passive filters in high frequency range is more economic choice.

The most commonly used filters are

Low Pass Filter

High Pass Filter

Band Pass Filter

Band Elimination filter (Band Stop Filter-BSF)

Fall-off Rate

Filters can also be classified by the fall-off rate of their gain/frequency characteristics.

First order filter → has a fall rate (after cut-off frequency f_c) of 20 dB/decade → which is a gain reduction of 20 dB for each frequency increase by a factor of 10 (a decade) i.e 6 dB/octave .

Second order filter → the fall-off rate is 40 dB/decade (12 dB/octave)

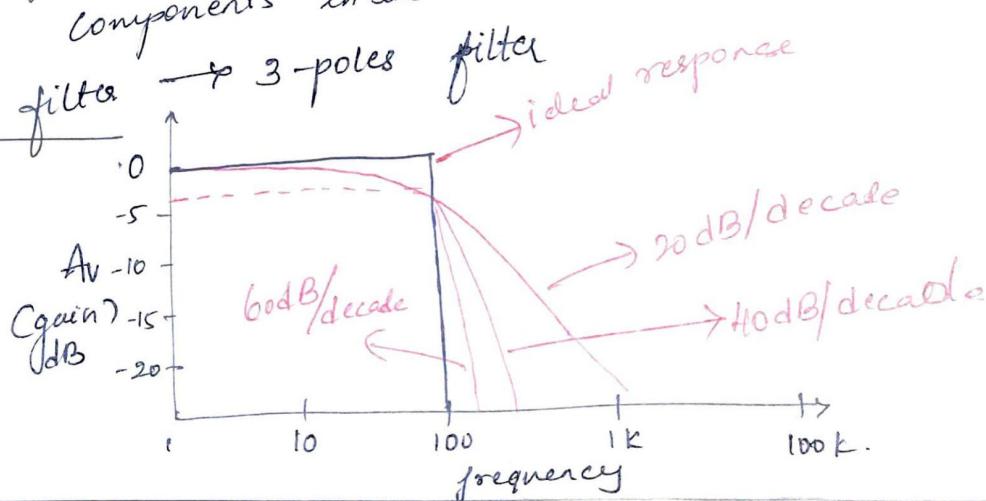
Third order filter → 60 dB/decade (18 dB/octave) fall off rate

A steeper fall-off rate means that the A_v response graph approaches the ideal more closely so that the filter is better at rejecting unwanted frequencies

1st order filter → single pole filter because its circuit has only one reactive component

2nd order filter → two pole filter ∵ it has two reactive components in the circuit.

3rd order filter → 3-poles filter



Filter Design Categories

Major approaches to filter circuit design, which gives different performance characteristics.

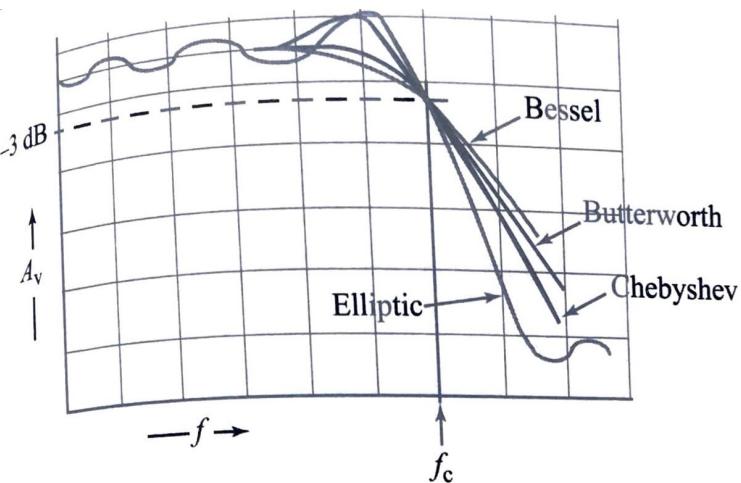
These produce filters that are variously known as Bessel,

Butterworth, Chebyshev and Elliptic (also called Cauer)

The A_v/f graphs illustrates the major differences between the filter types.

Chebyshev and elliptic filter have ripple, or uneven amplitude response within the passband.

Elliptic also has ripple within the stop band.



Frequency response for different types of active filters

phase relationship b/w the component frequencies remains substantially unchanged by the filter.

Active filters are typically specified by the voltage transfer function.

$$H(s) = \frac{V_o(s)}{V_i(s)}$$

Under steady state conditions
(i.e. $s = j\omega$)

$$H(j\omega) = |H(j\omega)| e^{j\phi(\omega)}$$

Transfer function is the ratio of Laplace transform of output / Laplace transform of input.

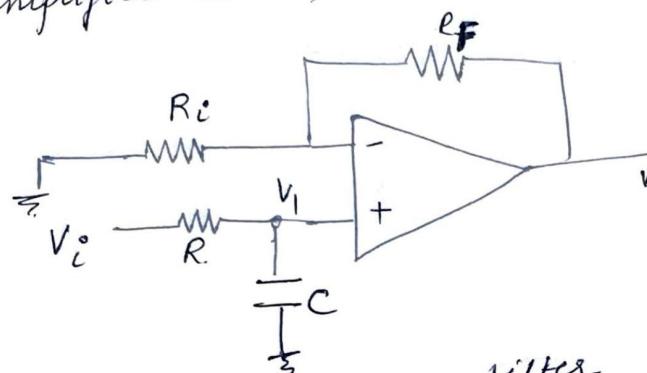
where $|H(j\omega)|$ is the magnitude of the gain function and $\phi(\omega)$ is the phase function

The magnitude response is given in dB as
 $20 \log |H(j\omega)|$

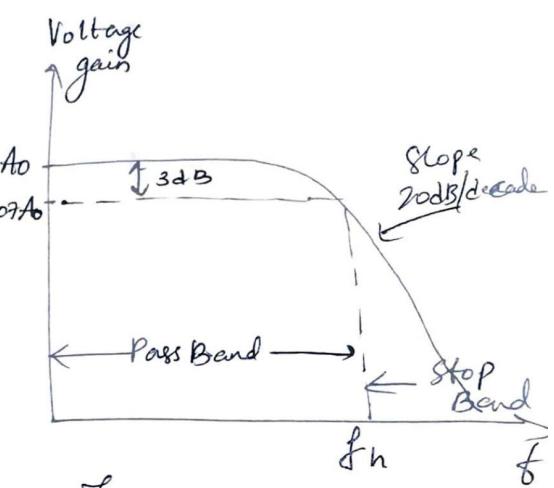
Phase response is given in degrees as
 $-\phi(\omega) \times 57.296$ degrees.

First Order Low Pass filter

1st order LPF consists of a ~~single~~ single RC network connected to the +ve input terminal of non-inverting op-amp amplifier and is shown in fig.



First order low pass filter



Frequency Response

Voltage (V_1) across the capacitor C is obtained by applying voltage divider bias. The voltage V_1 across capacitor in

s domain is

$$V_1(s) = \frac{X_C(s)}{R + X_C(s)} V_i(s) \quad X_{Cs} = \frac{1}{sC}$$

$$= \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

$$\boxed{\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs + 1}} \quad \text{--- } \textcircled{1}$$

The closed loop gain of the opamp is

$$A_o = \frac{V_o(s)}{V_p(s)} = \left(1 + \frac{R_F}{R_i}\right) \quad \text{--- } \textcircled{2}$$

The overall transfer function from ① & ②

$$H_{LP}(s) = \frac{V_o(s)}{V_i(s)} = \underbrace{\frac{V_o(s)}{V_i(s)}}_{A_0} \times \underbrace{\frac{V_i(s)}{V_i(s)}}_{\frac{1}{RCs+1}}$$

$$\boxed{H_{LP}(s) = \frac{A_0}{RCs+1}} = A_0 \left(\frac{1}{RCs+1} \right) \quad \text{--- } ③$$

$$\text{Let } \omega_h = 1/RC$$

$$\therefore H_{LP}(s) = \frac{A_0}{\left(\frac{s}{\omega_h} + 1\right)} = \frac{\omega_h A_0}{(s + \omega_h)} \quad \text{--- } ④$$

This is the standard form of the transfer function of a first order low pass system

To determine the frequency response put $s=j\omega$ in ③

$$\begin{aligned} \therefore H_{LP}(j\omega) &= \frac{A_0}{1+j\omega RC} & \text{where } f_h = \frac{1}{2\pi RC} \\ &= \frac{A_0}{1+j(\omega/f_h)} & f = \frac{\omega}{2\pi} \end{aligned}$$

At low frequency i.e. $f \ll f_h$

$$|H_{LP}(j\omega)| \approx A_0$$

$$\text{At } f = f_h \quad |H_{LP}(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707 A_0.$$

At very high frequency i.e. $f \gg f_h$

$$|H_{LP}(j\omega)| \ll A_0 \approx 0.$$

Max gain at $f = 0 \text{ Hz}$

At $f_h \rightarrow$ gain falls to $0.707 A_0$ (0.707 maximum gain)

frequency range $\rightarrow 0$ to f_h is called the pass band
 $f > f_h$ is called the stop band

Second order LPF [Higher Order high pass filter]

Second order filter can provide -40 dB/decade roll-off rate in the stop band.

To match with the ideal characteristics the roll-off rate should be increased by increasing the order of the filter.

→ Each increase in order will produce a fall-off / roll-off rate of $\sim 20 \text{ dB/decade}$.

→ For the n^{th} order filter the roll off rate will be ~~~ 40~~
 $\sim n \times 20 \text{ dB/decade}$.

→ Higher order filters can be built by cascading a proper number of first and second order filters.

→ The frequency response of n^{th} order filter will be as shown in fig.

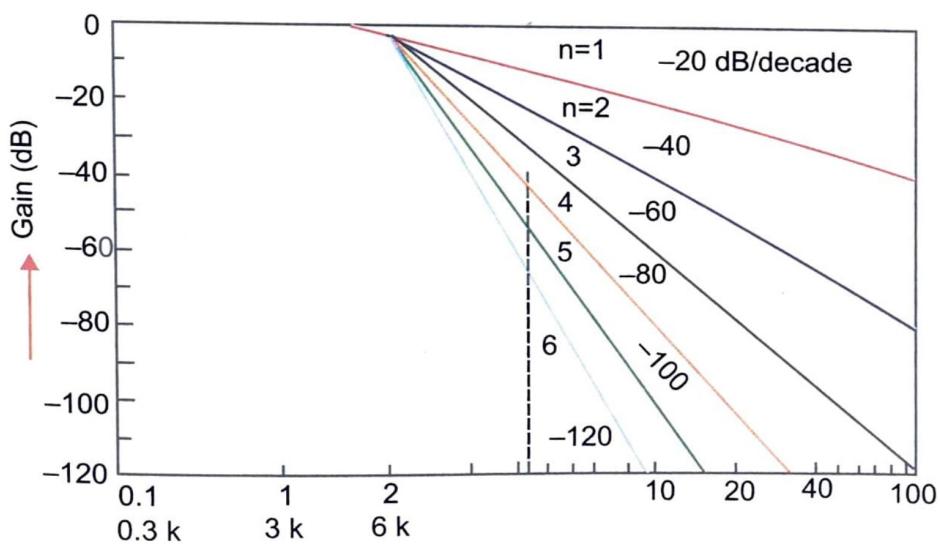
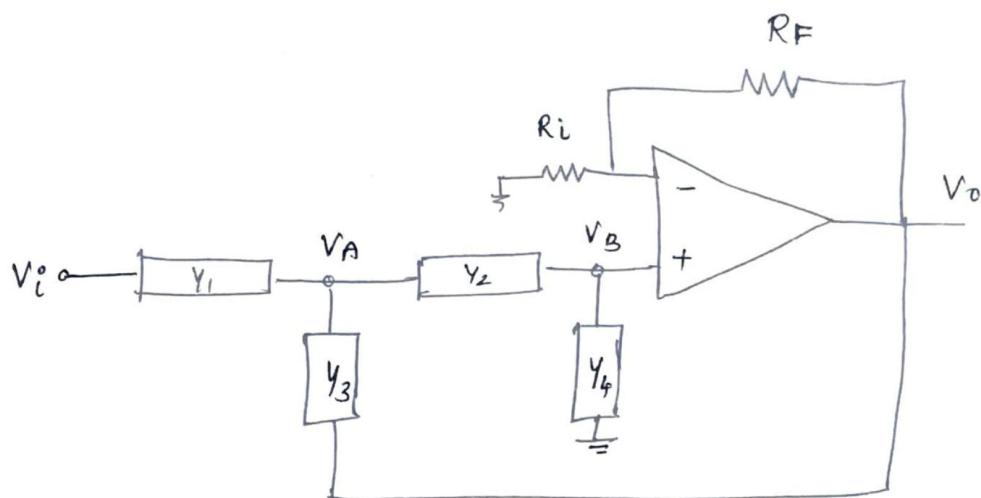


Fig. 7.6 Roll-off rate for different values of n

Example for s^{th} order system

$$H(s) = \frac{A_{01}}{s^n + d_1 s^{n-1} + \dots} \cdot \frac{A_{02}}{s^n + d_2 s^{n-1} + \dots} \cdot \frac{A_0}{s^n + 1}$$

Second order section another second order first order.

General Second Order filter

A general second order filter is shown fig. The results desired here can be used for analyzing low pass and high pass filters.

The output of the op-amp connected as a non-inverting amplifier is given by

$$V_o = \left(1 + \frac{R_F}{R_i}\right) V_B$$

$$\boxed{V_o = A_o V_B} \quad \text{--- (1)}$$

V_B is the voltage at the node B, V_A is the voltage at node A.

Apply KCL at node A.

$$V_i^o Y_1 = V_A (Y_1 + Y_2 + Y_3) - V_o Y_3 - V_B Y_2$$

From (1)

$$V_i^o Y_1 = V_A (Y_1 + Y_2 + Y_3) - V_o Y_3 - \frac{V_o}{A_o} Y_2 \quad \text{--- (2)}$$

Applying KCL at node B.

$$V_A Y_2 = V_B (Y_2 + Y_4) = \frac{V_o}{A_o} (Y_2 + Y_4).$$

$$\therefore V_A = \frac{V_o (Y_2 + Y_4)}{A_o Y_2} \quad \text{--- (3)}$$

Sub (3) in (2)

$$V_i^o Y_1 = \frac{V_o (Y_2 + Y_4) (Y_1 + Y_2 + Y_3)}{A_o Y_2} - V_o Y_3 - \frac{V_o Y_2}{A_o}$$

$$V_i^o Y_1 = \frac{V_0 (Y_2 + Y_4) (Y_1 + Y_2 + Y_3) - V_0 Y_3 A_0 Y_2 - V_0 Y_2 Y_2}{A_0 Y_2}$$

$$A_0 Y_1 Y_2 V_i^o = V_0 [Y_1 Y_2 + Y_1 Y_4 + Y_2^2 + Y_2 Y_4 + Y_4 Y_3 - A_0 Y_3 Y_2 - Y_2^2] + Y_3 Y_2$$

$$A_0 Y_1 Y_2 V_i^o = V_0 [Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_3 Y_2 (1 - A_0)]$$

$$\left. \begin{aligned} \therefore \frac{V_0}{V_i^o} &= \frac{A_0 Y_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_3 Y_2 (1 - A_0)} \end{aligned} \right\} \textcircled{4}$$

To make it a second order LPF

$$Y_1 = Y_2 = 1/R, \quad Y_3 = Y_4 = S.C.$$

Sub in $\textcircled{4}$

Transfer function of second order LPF

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_0}{s^2 C^2 R^2 + s C R (3 - A_0) + 1} \text{ } \textcircled{5}$$

$$H(0) = A_0 \quad \text{for } s=0 \quad \} \text{ configuration is for LPF.}$$

$$H(\infty) = 0 \quad \text{for } s=\infty$$

The minimum dc offset $R_i // R_F = (R + R) = 2R$.

The transfer function of low pass second order system (electrical, mechanical, hydraulic or chemical) can be written as

$$H_{LP}(s) = \frac{A_0 \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2} \text{ } \textcircled{6}$$

$A_0 \rightarrow$ the gain

$\omega_h \rightarrow$ upper cut off frequency in rad/sec

$\alpha \rightarrow$ damping co-efficient

Comparing ⑤ & ⑥ we get

(5)

$$\omega_h = \frac{1}{RC} \quad \text{and} \quad \alpha = (3 - A_0)$$

α is damping co-efficient α for low pass active RC filter can be determined by the value of A_0

Note*

Std second order shm T.F $H(s) = \frac{\omega_h^2}{s^2 + 2\zeta\omega_h s + \omega_h^2}$

$\boxed{\alpha = 2\zeta}$

Putting $s = j\omega$ in ⑥

$$H_{LP}(j\omega) = \frac{A_0}{\left(\frac{j\omega}{\omega_h}\right)^2 + j\alpha\left(\frac{\omega}{\omega_h}\right) + 1}$$

The normalized expression for low pass filter is

$$H_{LP}(j\omega) = \frac{A_0}{s_n^2 + \alpha s_n + 1}$$

where normalized frequency $s_n = j\left(\frac{\omega}{\omega_h}\right)$

The expression of magnitude is dB of the transfer function is

$$20 \log |H(j\omega)| = 20 \log \left| \frac{A_0}{1 + j\alpha \frac{\omega}{\omega_h} + \left(\frac{j\omega}{\omega_h}\right)^2} \right|$$

$$= 20 \log \frac{A_0}{\sqrt{\left(1 - \frac{\omega^2}{\omega_h^2}\right)^2 + \left(\frac{\alpha \omega}{\omega_h}\right)^2}}$$

For $\alpha > 1.7 \rightarrow$ we get heavily damped filter, the response is stable, however the roll off begins very early to the pass band.

α is reduced \rightarrow the response exhibits overshoot & ripples begin to appear at the early stage of pass band

Normalized Butterworth Polynomial.

Order n

Factors of polynomials.

1.

$$S_n + 1$$

2.

$$S_n^2 + 1.414 S_n + 1$$

3.

$$(S_n + 1)(S_n^2 + S_n + 1)$$

4,

$$(S_n^2 + 0.765 S_n + 1)(S_n^2 + 1.848 S_n + 1)$$

5. $(S_n + 1)(S_n^2 + 0.618 S_n + 1)(S_n^2 + 1.618 S_n + 1)$

6, $(S_n^2 + 0.518 S_n + 1)(S_n^2 + 1.414 S_n + 1)(S_n^2 + 1.932 S_n + 1)$

7. $(S_n + 1)(S_n^2 + 0.445 S_n + 1)(S_n^2 + 1.247 S_n + 1)(S_n^2 + 1.809 S_n + 1)$

8, $(S_n^2 + 0.390 S_n + 1)(S_n^2 + 1.111 S_n + 1)(S_n^2 + 1.663 S_n + 1)$
 $(S_n^2 + 1.962 S_n + 1)$

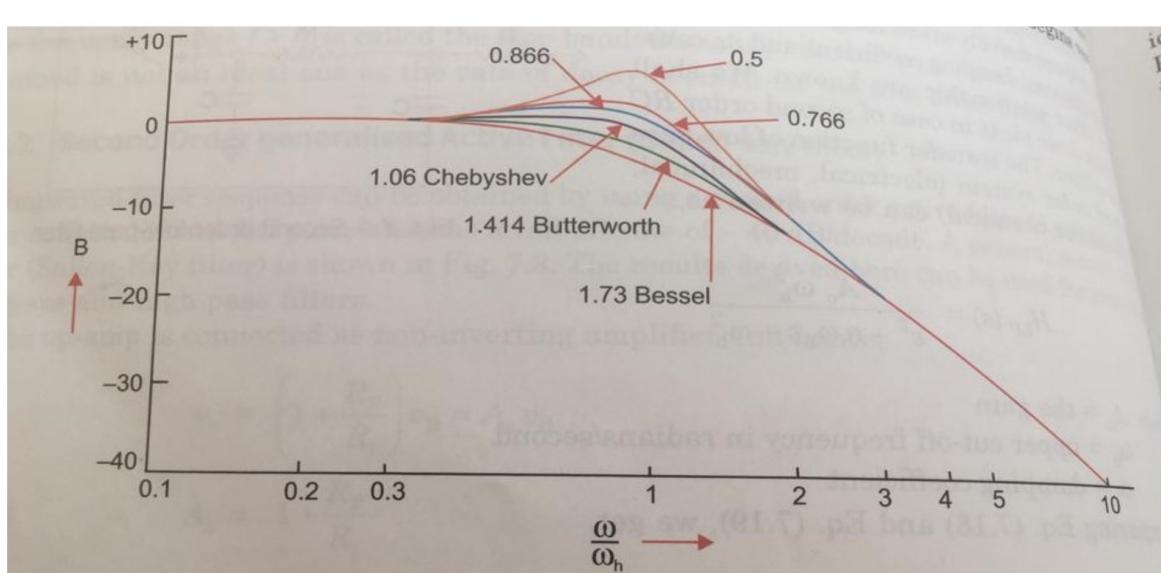


Fig. 7.5 Second order low-pass active filter response for different damping (unity gain $A_0 = 1$)

If α is reduced too much, the filter may become oscillatory
 The flattest pass band occurs for damping co-efficient
 of 1.414. This is called Butterworth filter.

Audio filters are usually butterworth filters

$$\alpha = 1.414 \Rightarrow \alpha = 2\zeta \Rightarrow \zeta = 0.707$$

Sub $\alpha = 1.414$ in eqn ⑦

$$20 \log |H_{LP}(j\omega)| = 20 \log \left| \frac{V_o}{V_i} \right| = 20 \log \left(\frac{A_0}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^4}} \right)$$

For the n^{th} order generalized lowpass Butterworth filter,
 the normalized transfer function for maximally flat filter can
 be written as

$$\boxed{\frac{|H_{LP}(j\omega)|}{A_0} = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^{2n}}}}$$

→ Refer Normalized Butterworth polynomial.

Problem

- ① Design a second order Butterworth low pass filter having upper cut-off frequency 1 kHz. Then determine its frequency response.

Soln

$$f_h = 1 \text{ kHz}$$

$$f_H = \frac{1}{2\pi RC}$$

$$\text{Let } C = 0.1 \mu\text{F}$$

$$R = \frac{1}{2\pi f_h C} = \frac{1}{2\pi \times 1000 \times 0.1 \times 10^{-6}} = 1.6 \text{ k}\Omega$$

For a second order system in the Butterworth polynomial
 table $n = 2 \quad \alpha = 1.414$

$$\therefore \text{The Pass Band gain is } A_0 = 3 - \alpha = 3 - 1.414 = \underline{\underline{1.586}}$$

The transfer function of normalized second order L.P Butterworth filter is

$$H(s) = \frac{A_0}{s_n^2 + \alpha s_n + 1}$$

$$= \frac{1.586}{s_n^2 + 1.414 s_n + 1}$$

$$A_0 = 1 + \frac{R_F}{R_i} = 1.586 = 1 + \frac{R_F}{R_i}$$

$$\text{Let } R_F = 5.86 \text{ k}\Omega$$

$$\frac{R_F}{R_i} = 0.586$$

$$\Rightarrow R_i = 10 \text{ k}\Omega$$

② Design a fourth order Butterworth low pass filter having upper cut-off frequency of 1 kHz.

$$f_h = 1 \text{ kHz} = \frac{1}{2\pi RC}$$

$$\text{Let } C = 0.1 \text{ nF}$$

$$R = 1.6 \text{ k}\Omega$$

From the table factors of polynomial for 4th order Butterworth filter

$$(s_n^2 + 0.765 s_n + 1)(s_n^2 + 1.848 s_n + 1)$$

$$\alpha_1 = 0.765$$

$$\alpha_2 = 1.848$$

$$\alpha = 3 - A_0$$

$$\alpha_1 = 3 - A_{01} \Rightarrow A_{01} = 3 - \alpha_1 = 3 - 0.765 = 2.235$$

$$\alpha_2 = 3 - A_{02} = A_{02} = 3 - \alpha_2 = 3 - 1.848 = 1.152$$

$$T.F = \frac{2.235}{s_n^2 + 0.765 s_n + 1} \cdot \frac{1.152}{s_n^2 + 1.848 s_n + 1}$$

$$A_{01} = 1 + \frac{R_{F1}}{R_{i1}} = 2.235$$

$$\frac{R_{F1}}{R_{i1}} = 1.235 \quad \text{Let } R_{F1} = 12.35 \text{ k}\Omega$$

$$R_{i1} = 10 \text{ k}\Omega$$

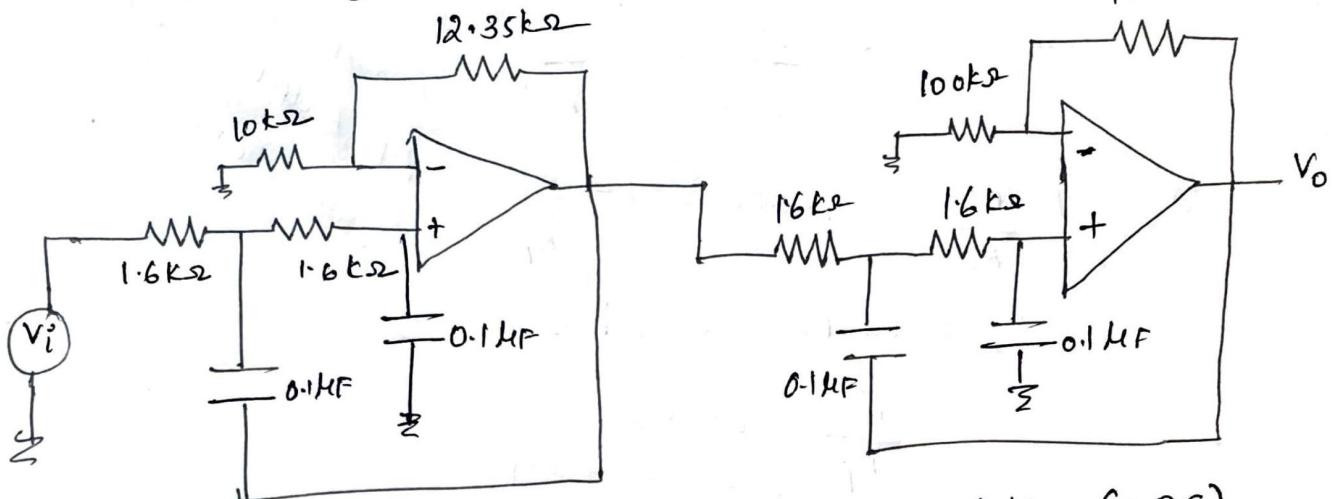
Draw the circuit of 2nd order L.P Butterworth filter with obtained values

Simplifying

$$\therefore 111^{\text{th}} \quad A_{02} = 1.152 = 1 + \frac{R_{F_2}}{R_{i_2}} \Rightarrow 0.152 = \frac{R_{F_2}}{R_{i_2}}$$

$$\text{Let } R_{F_2} = 15.2 \text{ k}\Omega, R_{i_2} = 100 \text{ k}\Omega$$

The circuit realization is as shown in fig. 15.2 k\Omega.

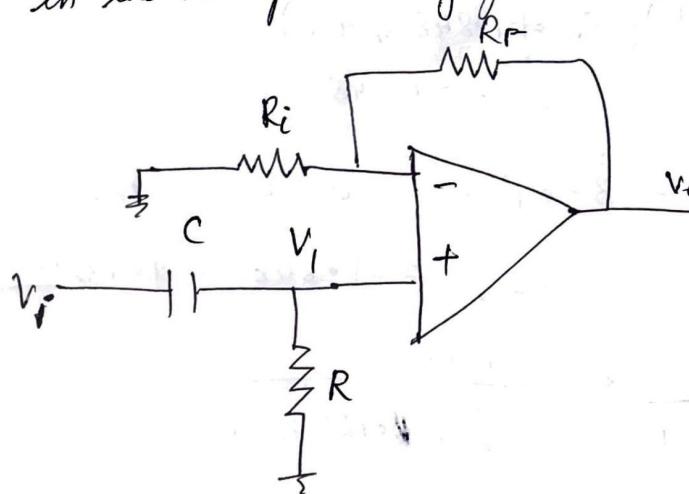


Realization of 4th order Butterworth filter (L.P.F)

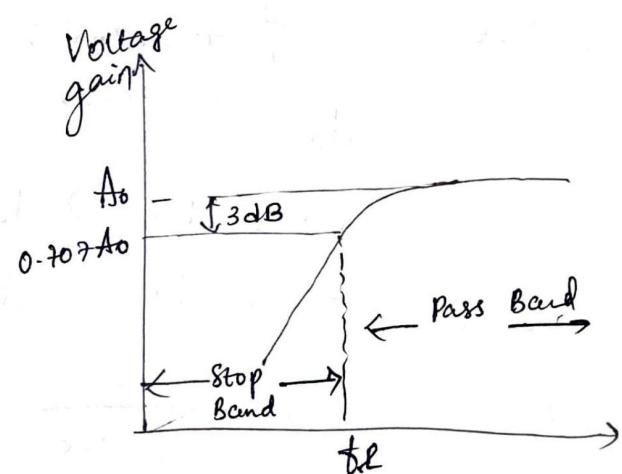
- ③ Determine the order of a low pass Butterworth filter that is to provide 40dB attenuation at $\frac{\omega}{\omega_h} = 2$

High Pass Filter (High Pass Active Filter)

A high pass filter is the complement of the low pass filter and can be obtained simply by interchanging R and C in the low pass configurations.



First order high pass filter



Frequency response

7

Single RC network is connected to non inverting terminal of the opamp. with the gain defined by R_F and R_i .

The voltage V_i appearing at the non inverting terminal is given by

$$V_i(s) = \frac{R}{R + \frac{1}{sC}} V_o(s)$$

$V(s) \rightarrow \text{LT of } v$
in time domain

$$\frac{V_f(s)}{V_i(s)} = \frac{RCs}{1 + RCs} \quad \text{--- (1)}$$

The output voltage v_o is given by

$$V_o(s) = \left(1 + \frac{R_F}{R_i}\right) V_i(s)$$

$$\text{Gain } A_o = \frac{V_o(s)}{V_f(s)} = \left(1 + \frac{R_F}{R_i}\right) \quad \text{--- (2)}$$

The overall transfer function is obtained by

$$\begin{aligned} H(s) &= \frac{V_o(s)}{V_f(s)} = \frac{V_o(s)}{V_i(s)} \cdot \frac{V_i(s)}{V_f(s)} \\ &= \left(1 + \frac{R_F}{R_i}\right) \frac{RCs}{1 + RCs} \\ \boxed{H(s) = \frac{A_o RCs}{1 + RCs}} &\quad \text{--- (3)} \end{aligned}$$

$$H_{HP}(j\omega) = \frac{A_o j f_l / f_e}{1 + j \left(\frac{f}{f_e}\right)} \quad [s = j\omega].$$

where $f_l = \frac{1}{2\pi RC}$

The frequency response of the filter is obtained from the magnitude ie $|H_{HP}(j\omega)| = \left| \frac{V_o}{V_i} \right| = \frac{A_o f_l / f_e}{\sqrt{1 + \left(\frac{f}{f_e}\right)^2}} = \frac{A_o \omega}{\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^2}}$ --- (4)

The frequency response is as shown in fig

$f > f_1$ the gain is constant = A_0

$f < f_1$ the gain rolls-off at the rate of -20 dB/decade

* High pass filter can be obtained from the lowpass filter by applying the transformation.

$$\frac{s}{\omega_0} |_{L.P.} = \frac{\omega_0}{s} |_{H.P.}$$

Thus a low pass filter can be converted to a high pass filter by simply interchanging R and C.

Problems :-

① Design and plot the frequency response of a first order high pass filter for pass band gain of 2 and lower cut-off frequency of $\omega \text{ kHz}$

$$f_L = \omega \text{ kHz}$$

$$f_L = \frac{1}{2\pi RC}$$

$$\text{Let } C = 0.01 \mu F$$

$$f_L = \frac{1}{2\pi R \times 0.01 \mu}$$

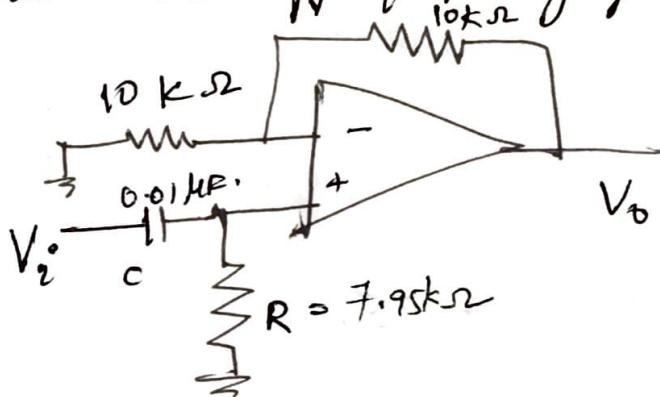
$$R = \frac{1}{2\pi \times \omega \times 0.01 \mu} = \underline{\underline{7.95 \text{ k}\Omega}}$$

$$A_0 = 2.$$

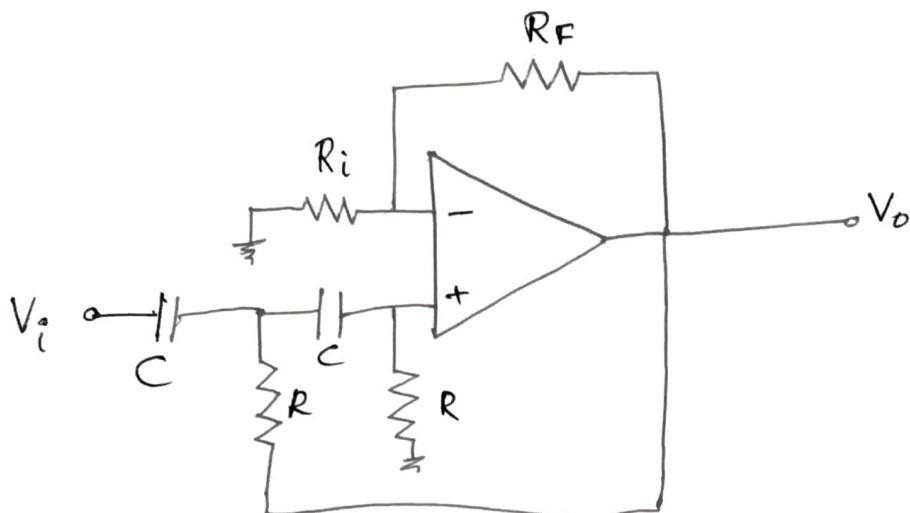
$$A_0 = 1 + \frac{R_F}{R_i}$$

$$\frac{R_F}{R_i} = 1 \Rightarrow R_F = R_i = \underline{\underline{10 \text{ k}\Omega}}$$

Draw the frequency response



Second Order High pass Active filter



Second order high pass filter

HPF is the complement of the low pass filter \Rightarrow it can be obtained simply by interchanging R and C in low pass configuration.

$$\text{wkt } \frac{V_o}{V_i} = \frac{A_0 Y_1 Y_2}{Y_1 Y_2 + Y_u(Y_1 + Y_2 + Y_3) + Y_2 Y_3(1 - A_0)}$$

$$Y_1 = Y_2 = sC, \quad \boxed{Y_3 = Y_u = \frac{1}{R} = G.}$$

$$\begin{aligned} H_{HP}(s) &= \frac{V_o(s)}{V_i(s)} = \frac{A_0 sC sC}{sC sC + \frac{1}{R} (sC + sC + \frac{1}{R}) + \frac{sC}{R} (1 - A_0)} \\ &= \frac{A_0 s^2 C^2}{s^2 C^2 + \frac{sC}{R} + \frac{sC}{R} + \frac{1}{R} + \frac{sC(1 - A_0)}{R}} \end{aligned}$$

$$H_{HP}(s) = \frac{A_0 s^2}{s^2 + (3 - A_0) \omega_L s + \omega_L^2} \quad (5) \quad \omega_L = \frac{1}{RC}$$

$$H_{HP}(s) = \frac{A_0}{1 + \left(\frac{\omega_L}{s}\right)(3 - A_0) + \left(\frac{\omega_L}{s}\right)^2} \quad (6)$$

From ⑥

$$\text{if } \omega = 0 \Rightarrow H = 0$$

if $\omega = \infty$ we get $H_{HP} = A_0 \rightarrow$ the circuit acts like a high pass filter

Lower cut-off frequency. $f_L = f_{3dB} = \frac{1}{2\pi RC}$

Put $s = j\omega$ in ⑥

$$H_{HP}(j\omega) = \frac{A_0}{1 + \frac{\omega_L}{j\omega} (3 - A_0) + \left(\frac{\omega_L}{j\omega}\right)^2}$$

$3 - A_0 = 1.414$ for a Butterworth filter

The voltage gain magnitude equation of the second order Butterworth high pass filter

$$|H_{HP}(j\omega)| = \left| \frac{V_o}{V_i} \right| = \frac{A_0}{\sqrt{1 + \left(\frac{f_L}{\omega}\right)^4}}$$

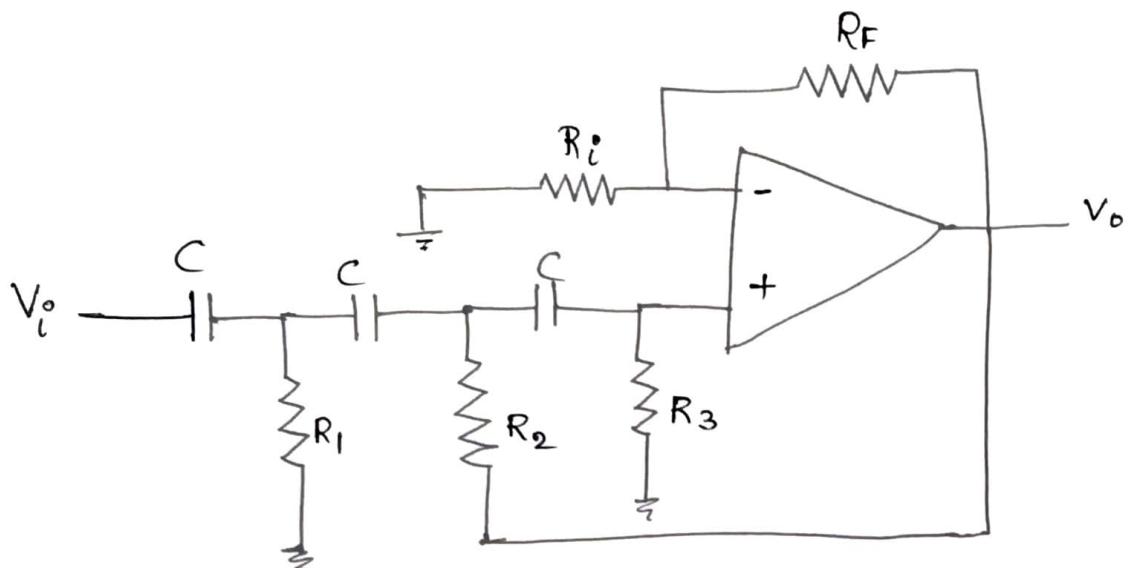
$$\left| \frac{H_{HP}(j\omega)}{A_0} \right| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{\omega}\right)^4}}$$

Higher-order high pass filters

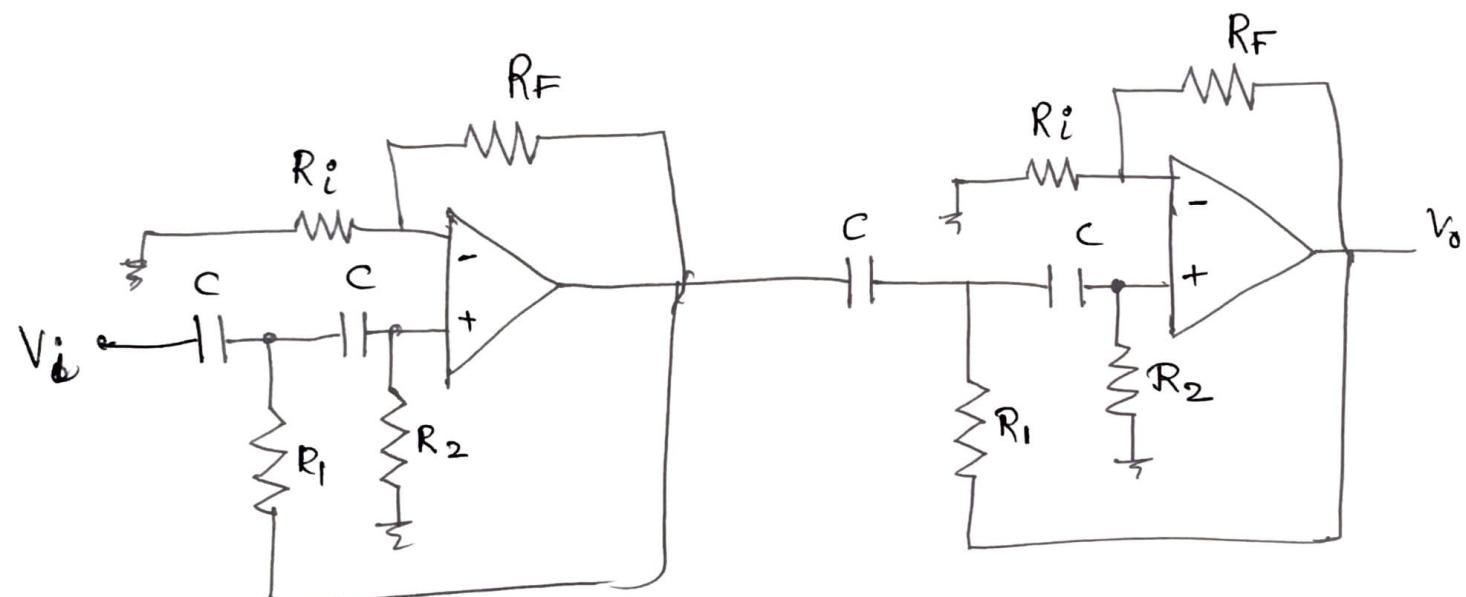
The magnitude of the voltage transfer function for the n^{th} order Butterworth high-pass filter is given by

$$\left| H_{HP}(j\omega) \right| = \frac{1}{\sqrt{1 + \left(\frac{f_L}{\omega}\right)^{2n}}}$$

Higher order filters can be designed by adding additional RC networks i.e. by cascading a required no. of first and second order filters.



Third order Butterworth High pass filter



Fourth order Butterworth High pass filter

Problem

- 1) Design a second order Butterworth high pass filter having lower cut-off frequency of 1 kHz.

Band Pass filter :-

There are types of Band Pass filters which are classified as per the figure of merit or quality factor (Q)

(i) Narrow band pass filter ($Q > 10$)

(ii) Wide band pass filter ($Q < 10$)

The following relationships are important

$$Q = f_0/BW = f_0(f_h - f_l)$$

$$f_0 = \sqrt{f_h f_l}$$

where $f_h \Rightarrow$ upper cut-off frequency

$f_l \Rightarrow$ lower cut-off frequency

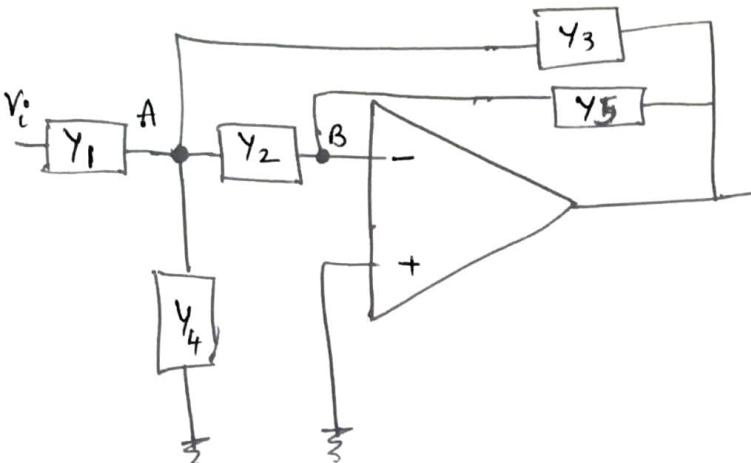
$f_0 \Rightarrow$ the central frequency

Narrow Band Pass Filters

The important parameters of a band pass filter (BPF) are

upper cut-off frequency	f_h
lower cut-off frequency	f_l
Bandwidth	BW
Central frequency	f_0
Central frequency gain	A_0
Selectivity	Q

Consider the Band Pass filter circuit as shown in fig.
The circuit has two feedback paths and the op-amp is used
in inverting mode of operation.



Consider the fig (a)

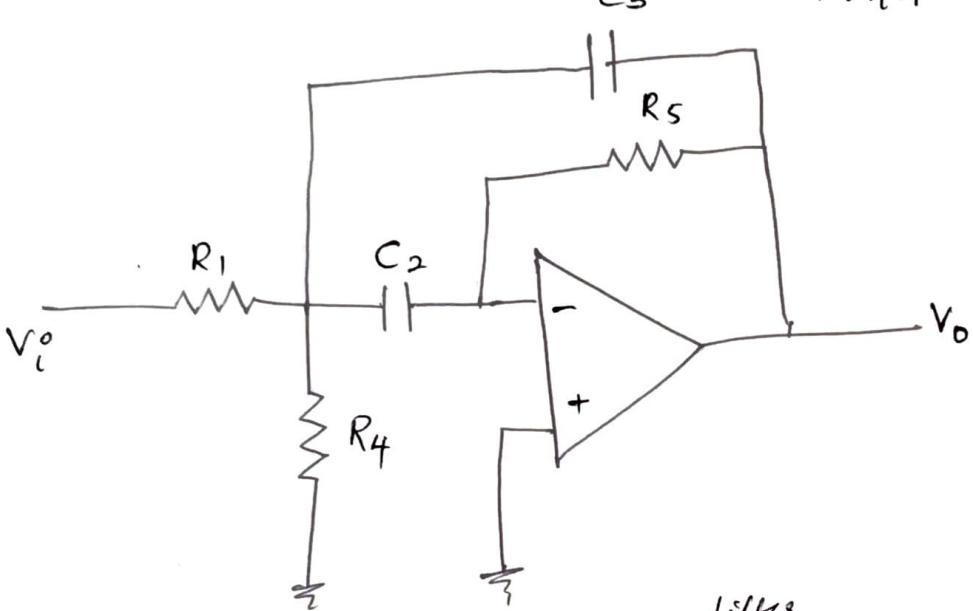
The node voltage eqn at node A is

$$V_i \cdot (V_A - V_i) Y_1 + (V_A - V_B) Y_2 + V_A Y_4 + (V_A - V_o) Y_3 = 0$$

$$V_i Y_1 + V_o Y_3 = V_A Y_1 + V_A Y_2 - V_B Y_2 + V_A Y_4 + V_A Y_3$$

$V_B = 0$ (virtual ground)

$$\therefore V_i Y_1 + V_o Y_3 = V_A (Y_1 + Y_2 + Y_3 + Y_4) \quad \text{--- (1)}$$



(b) Second order band pass filter

The node voltage equation at node B.

$$V_2 (V_B - V_A) + (V_B - V_o) Y_5 = 0$$

wkt $V_B = 0$

$$-V_A Y_2 - V_o Y_5 = 0$$

$$V_A Y_2 = -V_o Y_5$$

$$V_A = -V_o \left(\frac{Y_5}{Y_2} \right) \quad \text{--- (2)}$$

Sub (2) in (1)

$$V_i Y_1 + V_o Y_3 = -V_o \left(\frac{Y_5}{Y_2} \right) (Y_1 + Y_2 + Y_3 + Y_4)$$

$$V_i Y_1 = -V_o \left(\frac{Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5 + Y_3 Y_2}{Y_2} \right)$$

$$\frac{V_o}{V_i} = - \frac{Y_1 Y_2}{Y_2 Y_3 + Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_4 Y_5} \quad \textcircled{3}$$

For this circuit to be band pass filter

put $Y_1 = G_1, Y_2 = sC_2, Y_3 = sC_3, Y_4 = G_u, Y_5 = G_s -$
as shown in fig \textcircled{b}

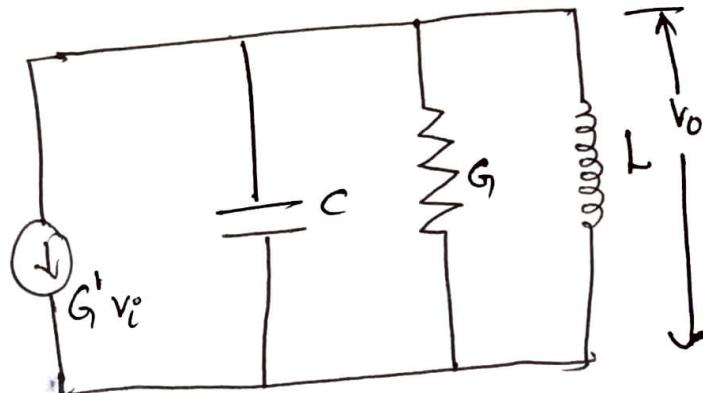
∴ Transfer function

$$H(s) = - \frac{G_1 s C_2}{s^2 C_2 C_3 + G_1 G_5 + s C_2 G_5 + s C_3 G_5 + G_u G_5}$$

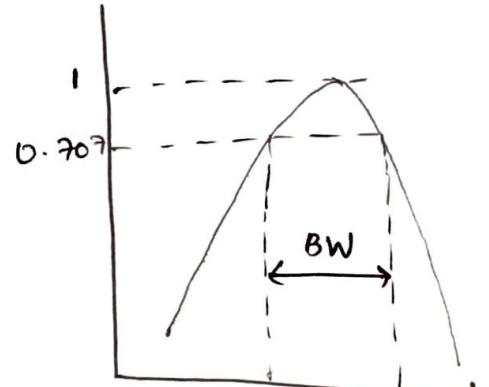
$$H(s) = \frac{-s G_1 C_2}{s^2 C_2 C_3 + s(C_2 + C_3) G_5 + G_5(G_1 + G_u)} \quad \textcircled{4}$$

$$H(s) = \frac{-G_1}{s C_3 + \frac{(C_2 + C_3) G_5}{C_2} + \frac{(G_1 + G_u) G_5}{s C_2}} \quad \textcircled{5}$$

The transfer function in $\textcircled{4}$ is equivalent to the gain expression of a parallel RLC circuit driven by a current source $G^1 v_i$ and with band pass characteristics as shown below. The gain expression is $\frac{V_o(s)}{V_i(s)} = -\frac{G^1}{Y} = -\frac{G^1}{sC + G + \frac{1}{sL}}$ $\textcircled{6}$



(2a) Parallel RLC circuit



Band Pass Characteristics

Comparing the gain expression in ⑤ and ⑥. we get

$$G' = G_1$$

$$L = \frac{C_2}{(G_1 + G_4) G_5}$$

$$G = \frac{G_5 (C_2 + C_3)}{C_2}$$

$$C = C_3$$

At resonance the circuit of ②a has unity power factor i.e. imaginary part is zero which gives the resonant frequency

$$\omega_0^2 = \frac{1}{LC} = \frac{G_5 (G_1 + G_4)}{C_2 C_3} \quad \text{--- } ③$$

The gain at resonance is given by

$$\left. \frac{V_o}{V_i} \right|_{w=\omega_0} = -\frac{G'}{G} = -\frac{(G_1/G_5) C_2}{C_2 + C_3} \quad \text{from } ④$$

$$\left. \frac{V_o}{V_i} \right|_{w=\omega_0} = -\frac{(R_5/R_1) C_2}{C_2 + C_3} \quad \text{--- } ⑦$$

The Q-factor at resonance is given by

$$Q_0 = \frac{\omega_0 L}{R} = \omega_0 R C = \frac{\omega_0 C}{G} \quad \text{from } ④$$

$$Q_0 = \frac{\omega_0 C_2 C_3}{(C_2 + C_3) G_5} \quad \text{--- } ⑧$$

The Bandwidth BW is given by

$$BW = f_h - f_l = \frac{f_0}{Q_0} = \frac{\omega_0}{2\pi Q_0} = \frac{\omega_0}{2\pi R \omega_0 C}$$

$$BW = \frac{1}{2\pi RC} = \frac{G}{2\pi C} = \frac{G_5 (C_2 + C_3)}{2\pi C_2 C_3} \quad \text{--- } ⑨$$

from ④.

and centre frequency $f_0 = \sqrt{f_h f_l}$.

If $C_2 = C_3 = C$, the gain at resonant frequency from (7) is

$$\left| \frac{V_o}{V_i} \right|_{\omega=\omega_0} = -\frac{R_S}{2R_1} = -A_0. \quad \text{--- (10)}$$

Resonant frequency $\omega_0 = \frac{\sqrt{G_5(G_1+G_4)}}{C}$ --- (11)

$$BW = \frac{G_5(2C)}{2\pi C^2} = \frac{G_5}{\pi C} = \frac{1}{\pi R_S C} \quad \text{--- (12)}$$

Design parameters

- $\boxed{ }$ gain at resonance
- $\boxed{ }$ resonant frequency
- $\boxed{ }$ Bandwidth.

Using (10), (11) & (12) in eqn (5)

The standard transfer function of a bandpass filter is obtained as

$$H(s) = \frac{-A_0(\omega_0/\zeta)s}{s^2 + (\omega_0/\zeta)s + \omega_0^2} = -\frac{A_0 \alpha \omega_0 s}{s^2 + \omega_0 \alpha s + \omega_0^2} \quad \text{--- (13)}$$

Magnitude in dB

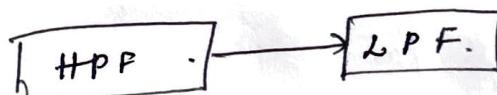
$$20 \log |H(s)| = 20 \log \left| \frac{A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2} \right| \quad \text{--- (14)}$$

where the damping factor $\alpha = \frac{1}{\zeta}$

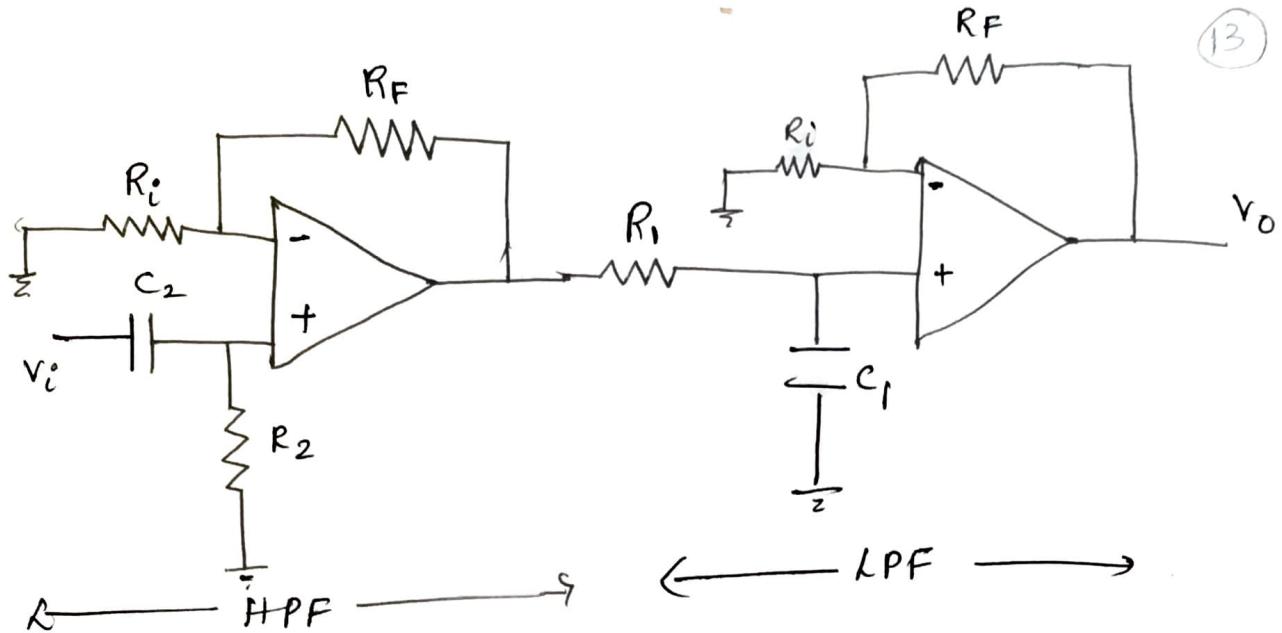
From eqn (13) $w \ll \omega_0$ & $w \gg \omega_0$ the gain is zero
and for $w = \omega_0$ the gain is A_0 . A_0 is negative.

Wide Band Pass Filter

A wide band-pass filter can be formed by cascading HPF and LPF section.



If HPF and LPF are of first order then the Band pass filter (BPF) will have a roll-off rate of 20 dB/decade



First order Band-pass filter

For the high pass section, The magnitude of gain is

$$|H_{HP}| = \left| \left(1 + \frac{R_F}{R_i} \right) \frac{j 2\pi f R_2 C_2}{1 + j 2\pi f R_2 C_2} \right| = \left| A_{01} \frac{j f/f_L}{1 + j(f/f_L)} \right|$$

$$\left[H_{HP} \right] = \frac{A_{01} \left(\frac{f}{f_L} \right)}{\sqrt{1 + \left(\frac{f}{f_L} \right)^2}} \quad \text{--- (1)}$$

$$f_L = \frac{1}{2\pi R_2 C_2} \quad \text{--- (2)}$$

Similarly for the low pass section, The magnitude of the gain is

$$\left[H_{LP} \right] = \frac{A_{02}}{\sqrt{1 + \left(\frac{f}{f_H} \right)^2}} \quad \text{--- (3)}$$

$$\text{where } f_H = \frac{1}{2\pi R_1 C_1} \quad \text{--- (4)}$$

The voltage gain magnitude of the wide band pass filter is the product of that of LPF & HPF \therefore The frequency response of wide BPF is obtained by

$$\left| \frac{V_o}{V_i} \right| = \left| \frac{A_{01} \left(\frac{f}{f_L} \right)}{\sqrt{1 + \left(\frac{f}{f_L} \right)^2} \sqrt{1 + \left(\frac{f}{f_H} \right)^2}} \right| \quad \text{--- (5)}$$

Total Pass Band gain $A_0 = A_{01} \times A_{02}$.

W^{hy} to obtain BPF with -4dB/decade fall-off rate Second order HPF & LPF can be cascaded.

Problems

① Design a wide-band pass filter having $f_L = 400\text{Hz}$, $f_H = 2\text{kHz}$ and pass band gain of 4. Find the value of Q of the filter.

Soln $f_0 = \sqrt{f_H f_L} = \sqrt{400 \times 2\text{k}} = 894.4 \text{ Hz}$

$$Q = \frac{f_0}{BW} = \frac{894.4}{2\text{k} - 400} = \frac{894.4}{1600} = 0.56$$

Since $Q < 10 \rightarrow$ wide Band pass filter.

pass band gain $= A_0 = 4$

$A_0 = A_{01} \times A_{02}$
 \Rightarrow Let us consider the gain of Both HPF &

HPF $A_{01} = Q$ \quad $\text{LPF} = 2$
 $A_{01} = 1 + \frac{R_F}{R_i}$

LPF $A_{02} = 2$ \quad $Q = 1 + \frac{R_F}{R_i}$

$$\boxed{R_F = R_i} \quad = 10 \text{ k}\Omega$$

W^{hy} $A_{02} = 1 + \frac{R_F}{R_i} \cdot$

$$2 = 1 + \frac{R_F}{R_i}$$

$$\boxed{R_F = R_i = 10 \text{ k}\Omega}$$

$$f_L = \frac{1}{2\pi R_2 C_2} \Rightarrow 400 = \frac{1}{2\pi R_2 C_2} \quad \text{let } C_1 = C_2 = 0.01 \mu F$$

$$R_2 = \frac{1}{800\pi C_2} = 39.8 \text{ k}\Omega$$

$$f_H = \frac{1}{2\pi R_1 C_1} \Rightarrow 2k = \frac{1}{2\pi R_1 C_1} \quad = 7.9 \text{ k}\Omega$$

$$R_1 = \frac{1}{2k \times 2\pi \cdot 0.01 \mu}$$

The resonant frequency f_0 of a BPF is 1 kHz and its BW is 3 kHz. Find Q, f_L and f_H

Soln

$$Q = \frac{f_0}{BW} = \frac{1 \text{ kHz}}{3 \text{ kHz}} = 0.33$$

$Q < 10 \Rightarrow$ wide Band filter.

$$Q = \frac{f_0}{f_H - f_L} = \frac{f_0}{BW}$$

$$f_0 = \sqrt{f_H} \Rightarrow f_L f_H = f_0^2 \Rightarrow f_H = \frac{f_0^2}{f_L}$$

$$Q = \frac{f_0}{\frac{f_0^2 - f_L^2}{f_L}} \Rightarrow \frac{f_0 f_L}{f_0^2 - f_L^2}$$

$$Q = \frac{f_0}{BW} = \frac{\sqrt{f_H f_L}}{BW}$$

Solve for $f_L \& f_H$

$$f_L = \sqrt{\frac{BW^2}{4} + f_0^2} - \frac{B}{2}$$

$$f_H \Rightarrow f_H = f_L + BW$$

$$f_L = 302.77 \text{ Hz}$$

$$f_H = 3302.77 \text{ Hz}$$

Band Reject Filter (Band Elimination Filter) \rightarrow Band Stop filter

[Narrow Band Reject Filter \rightarrow notch filter]

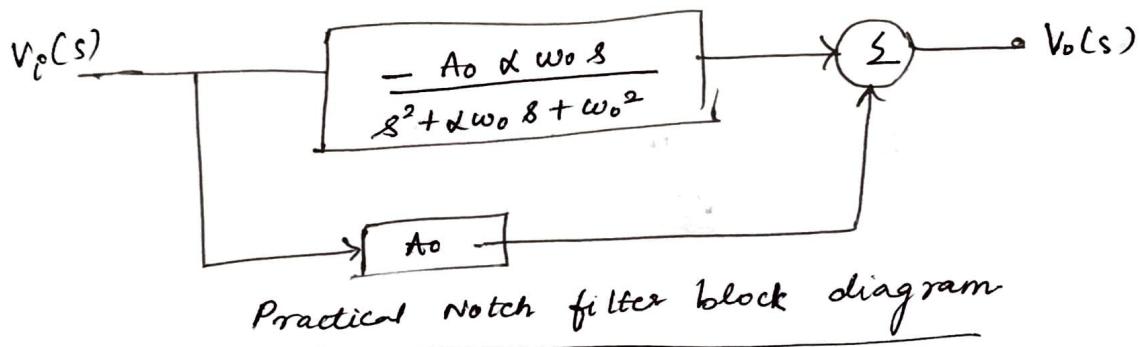
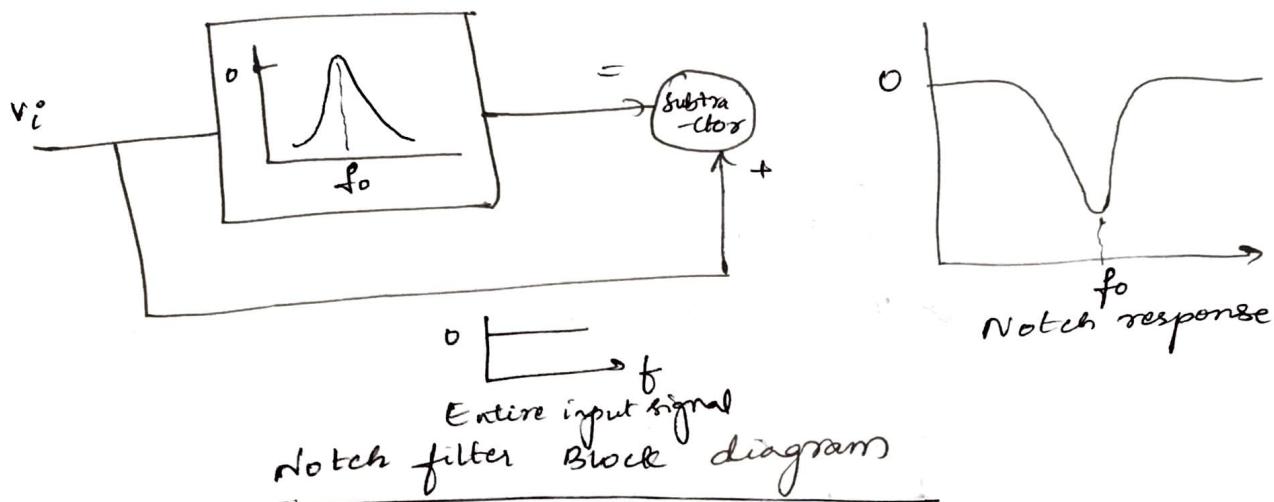
[Wide Band Reject Filter]

Notch filter is useful for the rejection of a single frequency such as 50 Hz power line frequency hum.

One simple technique to design a notch filter is to subtract the band pass filter output from input.

Band Pass filter discussed earlier has an inverted output as the gain or transfer function is negative \therefore We must use a summer instead of a subtractor.

BPF gain = $A_0 \Rightarrow$ O/P at the centre frequency = $-A_0 V_i$



To completely subtract this output, the input of summer must be precisely $A_0 V_i$ \therefore a gain A_0 must be added between the input and summer. as shown in fig.

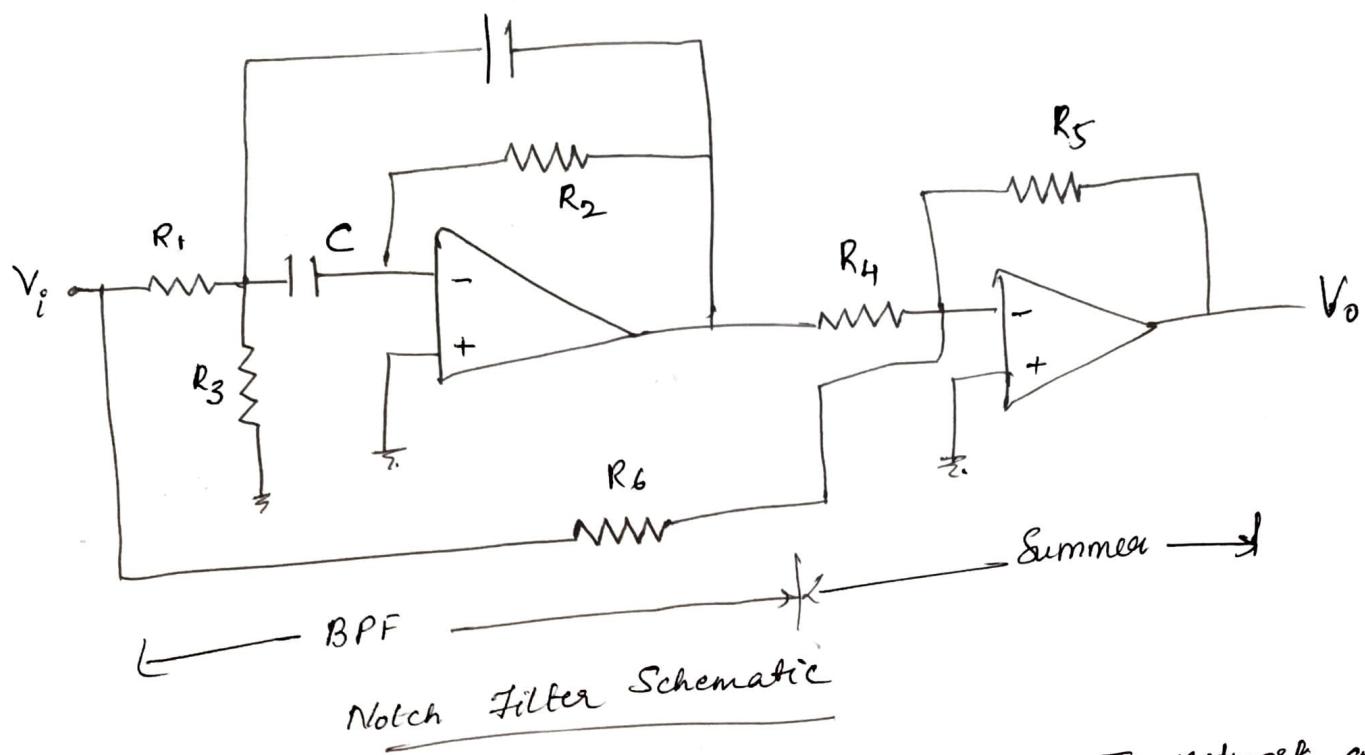
The output of the circuit in the s -domain is given by

$$V_o(s) = A_0 V_i(s) + \left(\frac{-A_0 \alpha \omega_0 s V_i(s)}{s^2 + \alpha \omega_0 s + \omega_0^2} \right) \quad \text{--- (1)}$$

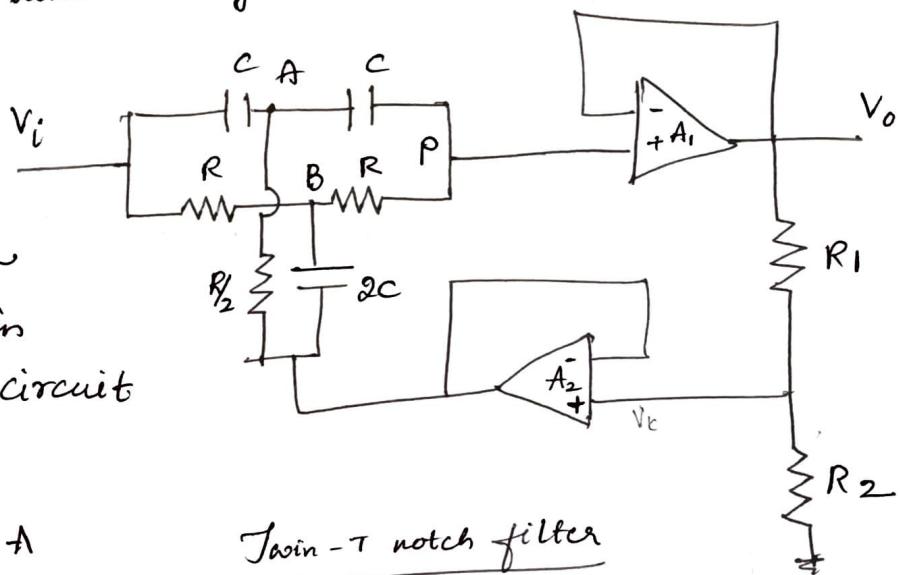
$$= A_0 V_i(s) \left(1 - \frac{\alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2} \right)$$

$$\boxed{\frac{V_o(s)}{V_i(s)} = \frac{A_0 (s^2 + \omega_0^2)}{s^2 + \alpha \omega_0 s + \omega_0^2}} \quad \text{--- (2)}$$

Eqn ② gives the transfer function for a second order notch filter.
 The circuit schematic is as shown in figure below



Another commonly used notch filter is the twin T-network as shown in fig.



Applying the KCL in s-domain for the active filter circuit

Apply KCL at node A

Twin-T notch filter

$$(V_A - V_i) sC + (V_A - V_p) sC + \frac{(V_A - KV_0)}{(R/2)} = 0$$

$$\text{where } K = \frac{R_2}{R_1 + R_2}$$

$$-sCV_i + sCV_A + \underline{sCV_p} - sCV_p + 2VAG - 2KV_0G = 0$$

$$sV_A sC + 2VAG = sCV_i + sCV_p + 2KV_0G$$

$$2V_A(sC + G) = sCV_i + sCV_p + 2KV_0G$$

$$2V_A(sC + G) = sCV_i + (sC + 2KG)V_0$$

$$G = 1/R$$

$$\frac{2}{R} = 2G$$

$$V_p = V_0$$

[∴ voltage follower]

(1)

At node B.

$$(V_B - V_i)G + (V_B - V_p)G + (V_B - KV_o)2sC = 0$$

$$V_p = V_o \quad K = \frac{R_2}{R_2 + R_3}$$

$$V_B G - V_i G + G V_B - V_o G + 2sC V_B - 2K V_o sC = 0$$

$$V_i G + V_o (G + 2K sC) = 2 V_B G + 2sC V_B$$

$$V_i G + V_o (G + 2K sC) = 2(G + sC) V_B \quad \boxed{\quad} \quad (2)$$

Apply KCL at Node P

$$(V_p - V_A) sC + (V_p - V_B) G = 0$$

$$V_p = V_o$$

$$-V_A sC + V_o sC + V_o G - V_B G = 0$$

$$\boxed{sC V_A + V_B G = (G + sC) V_o} \quad \boxed{3}$$

From ①, ② & ③ obtain the transfer function of filter

$$H(s) = \frac{V_o}{V_i} = \frac{G^2 + s^2 C^2}{G^2 + s^2 C^2 + 4(1-K)sCG}$$

$$H(s) = \frac{s^2 + (G/C)^2}{s^2 + (G/C)^2 + 4(1-K)s(G/C)} \quad \boxed{4}$$

In the steady state $s = j\omega$

$$H(j\omega) = \frac{\omega^2 - \omega_0^2}{\omega^2 - \omega_0^2 - j4(1-K)\omega\omega_0} \quad \boxed{5}$$

where $\omega_0 = \frac{G}{C}$
 $\omega_0 = \frac{1}{RC}$

$$\omega_0 = \frac{G}{C} = \frac{1}{RC}$$

$$f_0 = \frac{1}{2\pi RC} \quad \text{--- (6)}$$

Now $\omega = \omega_0 \Rightarrow H(j\omega) = 0$
 $\omega << \omega_0$ and $\omega >> \omega_0 \quad H(j\omega) = \text{unity} = 1$
 At 3 dB points $|H| = \frac{1}{\sqrt{2}}$

$$\omega^2 - \omega_0^2 = \pm 4(1-k)\omega\omega_0$$

$$\text{or} \quad \left(\frac{\omega}{\omega_0}\right)^2 \pm 4(1-k)\frac{\omega}{\omega_0} - 1 = 0 \quad \text{--- (7)}$$

Solving we get

$$f_h = f_0 \left[\sqrt{1 + 4(1-k)^2} + 2(1-k) \right]$$

$$f_l = f_0 \left[\sqrt{1 + 4(1-k)^2} - 2(1-k) \right]$$

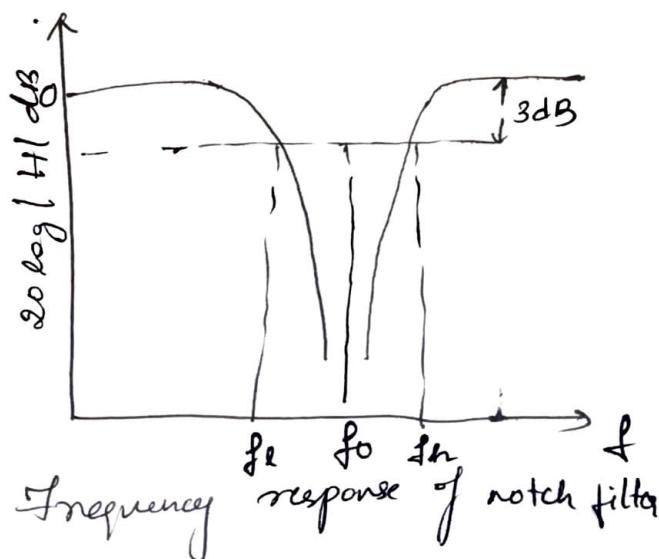
The 3 dB bandwidth

$$BW = f_h - f_l$$

$$BW = 4(1-k)f_0$$

$$Q = \frac{f_0}{BW} = \frac{1}{4(1-k)} \quad \text{--- (9)}$$

As k approaches unity
 Q becomes large.
 BW approaches 0



Problem

① Design a 50Hz active notch filter.

$$f_0 = 50\text{Hz}$$

$$\text{Let } C = 0.1 \mu\text{F}$$

$$\text{wkt. } f_0 = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi f_0 C} = 31.8 \text{ k}\Omega$$

For $R/2$ take 2 $31.8 \text{ k}\Omega$ resistors in parallel.

For $2C$ take 2 $0.1 \mu\text{F}$ capacitors in parallel.

Wide Band Reject filter

A wide band reject filter ($Q < 10$) can be made using a LPF, HPF and a summer. To design

(i) $f_L >> f_H$ (LPF)

(HPF)

(ii) The pass band gain of LPF and HPF should be same

Problem :-

① Design a wide Band reject filter having $f_h = 400\text{Hz}$ and $f_L = 2\text{kHz}$ having pass band gain as 2

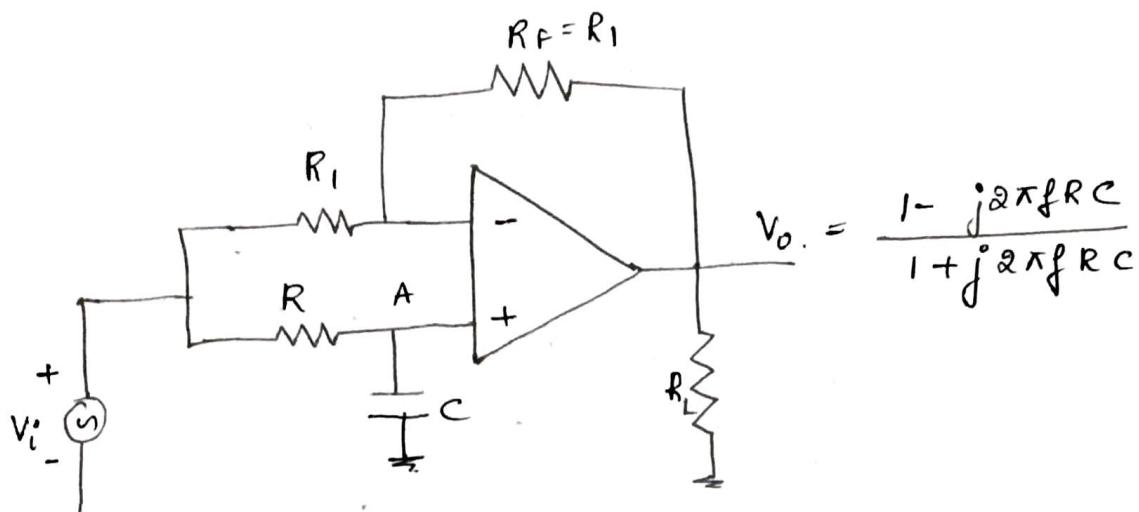
All Pass Filter

An all pass filters passes all frequency components of the input signal without any attenuation & provides desired phase shifts at different frequencies of the input signal.

→ When signals are transmitted over transmission lines, such as telephone wires, they undergo change in phase. These phase changes can be compensated by all-pass filters.

⇒ thus all pass filters are also called delay equalizers or phase correctors.

The figure shows an all-pass filter where $R_F = R_1$. 7



All pass filter

The output voltage V_o is obtained by using Superposition theorem:-

$$V_o = -\frac{R_F}{R_1} V_i + \left(1 + \frac{R_F}{R_1}\right) V_a \quad \dots \dots \textcircled{1}$$

where V_a is the voltage at node A.

Since $R_F = R_1$ eqn $\textcircled{1}$ becomes

$$V_o = -V_i + 2V_a \quad \textcircled{2}$$

Apply Voltage $V_a = \frac{-jX_C}{R-jX_C} \times V_i$ \textcircled{3}
divider bias.

Sub $\textcircled{3}$ in $\textcircled{2}$

$$\begin{aligned} V_o &= -V_i + 2 \frac{-jX_C}{R-jX_C} V_i \\ &= V_i \left(-1 - \frac{2jX_C}{R-jX_C} \right) \\ &= V_i \left(-1 - \frac{2}{1+j2\pi f RC} \right) \end{aligned}$$

$$\boxed{\frac{V_o}{V_i} = \frac{1 - j2\pi f RC}{1 + j2\pi f RC}} \quad \textcircled{4}$$

$$X_C = \frac{1}{2\pi f C}$$

$$\text{The magnitude of } \left| \frac{V_o}{V_i} \right| = \frac{\sqrt{1 + (2\pi f RC)^2}}{\sqrt{1 + (2\pi f RC)^2}} \quad (5)$$

$$|V_o| = |V_i|$$

It can be seen that $|V_o| = |V_i|$ throughout the frequency range. The phase shift ϕ between V_o and V_i

is given by

$$\phi = -\tan^{-1}(2\pi f RC) - \tan(2\pi f RC)$$

$$\boxed{\phi = -2\tan^{-1}(2\pi f RC)} \quad (6)$$

Phase shift ϕ can be varied with frequency for given R and C from 0 to -180° as frequency is varied from 0 to ∞ .

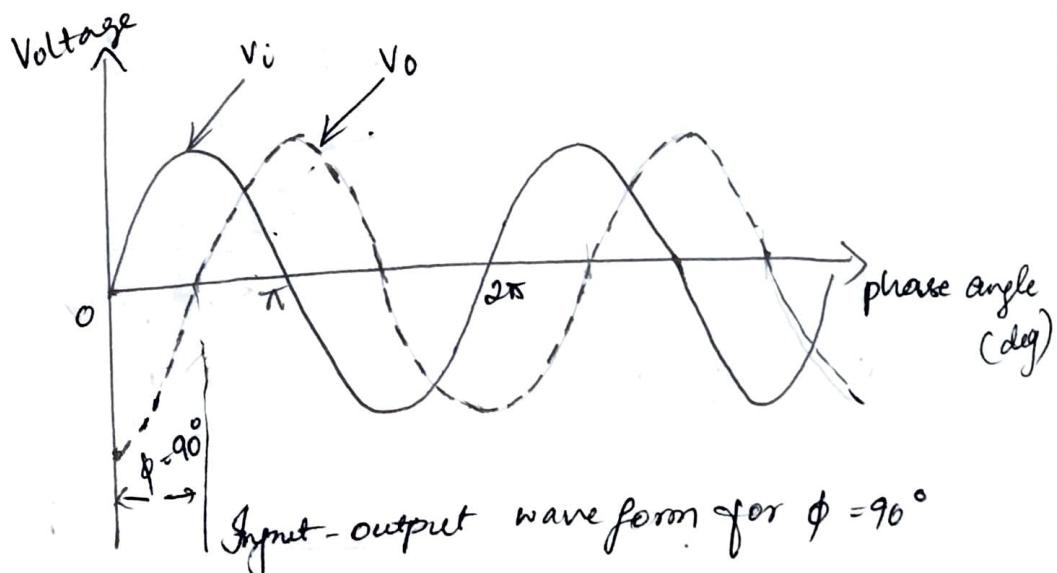
→ Phase shift is negative → the output V_o lags V_{in}

→ Phase shift can be made positive by interchanging R and C .

If $R_F = R_F = 10 k\Omega$
 $R = 15.9 k\Omega$ $C = 0.01 \mu F$

$$\phi = -90^\circ$$

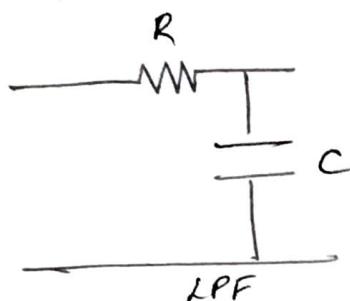
∴ The output voltage V_o will have the same frequency as the input but lags V_i by 90° as shown below.



Filter Transformations :-

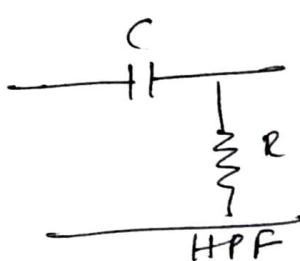
Let us normalize the frequency such that the cut-off frequency of the low pass function is unity. Let ' p ' be the frequency domain of the low pass and $S \rightarrow$ frequency domain.

Low pass to High pass Transformation



$$A(s)_{LPF} = \left| \frac{H(s)}{A_0} \right| = \frac{1}{1 + \frac{s}{w_n}} = \frac{1}{1 + S_n} \quad \text{--- (1)}$$

$S_n \rightarrow$ normalized frequency ' P



$$A(s)_{HPF} = \left| \frac{H(s)}{A_0} \right| = \frac{RCs}{1 + SRC} = \frac{S_n}{1 + S_n}$$

L.PF \rightarrow H.PF

$$A(s)|_{LPF} \neq S_n \rightarrow \frac{1}{S_n} \text{ we get } A(s)|_{HPF}$$

$$\text{Sub } S_n = \frac{1}{s_n} \neq$$

$$A(s)_{LPF} = \frac{1}{1 + \frac{1}{S_n}} = \frac{S_n}{S_n + 1} = A(s)|_{HPF}$$

For example a third order butterworth filter low pass transfer function in p -domain given as

$$H(p) = \frac{A_0}{p^3 + 2p^2 + 2p + 1}$$

can be transformed to HPF by simply Applying the transformation $P = \frac{1}{S}$

$$H(s) = \frac{A_0 s^3}{s^3 + 2s^2 + 2s + 1}$$

Low pass - Band Pass transformation

Consider a first order Butterworth low-pass transfer function in p-domain as

$$H(p) = \frac{A_0}{p+1} \quad \text{--- (1)}$$

Let the transformation by $p = \frac{s^2 + \omega_0^2}{(\omega_h - \omega_e)s}$

In order to normalize put $s_n = \frac{s}{\omega_0}$

$$\& Q = \frac{\omega_0}{\omega_h - \omega_e}$$

$$\therefore p = \frac{Q(s_n^2 + 1)}{s_n}$$

Sub p in (1)

$$H(s_n) = \frac{(A_0/Q) s_n}{s_n^2 + (1/Q) s_n + 1}$$

Low pass to Band Reject Transformation

$$p = \frac{(\omega_h - \omega_e)s}{s^2 + \omega_0^2} = \frac{s_n}{Q(s_n^2 + 1)}$$

where $s_n = s/\omega_0$

∴ Band Reject transfer function is given by

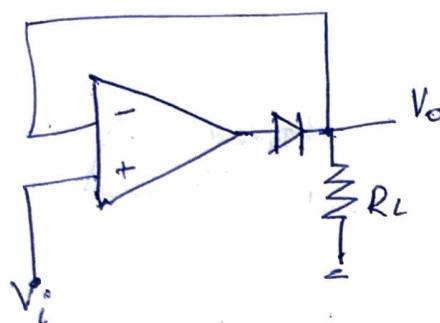
$$H(s_n) = \frac{A_0(s_n^2 + 1)}{s_n^2 + (1/Q)s_n + 1}$$

Note $s_n = j1$ $|H(j1)| = 0 \rightarrow$ notch filters.

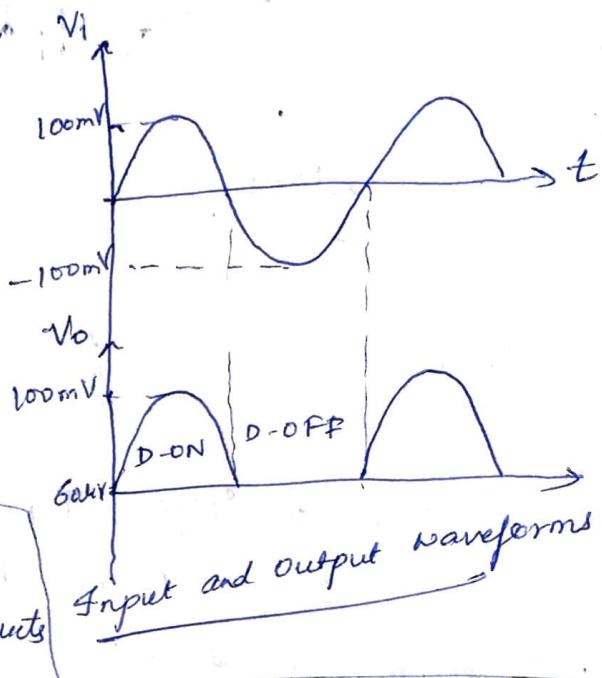
Op-Amp Circuits Using Diodes

The major limitation of ordinary diode is that it cannot rectify voltages below V_r (no. 6V) cut-in voltage of the diode.

Precision diodes are the diodes which acts like an ~~ideal~~ ideal diode.



Precision diode



When $\frac{V_o}{A_{OL}} > V_r$ then $V_o > V_r$
and the diode Conducts

This circuit is a voltage follower for $V_i > \frac{V_r}{A_{OL}}$ $V_o = V_i$ for
the half cycle

when $V_i < \frac{V_r}{A_{OL}}$ \rightarrow Diode is off \rightarrow no ~~current~~ current flows
in the load except reverse
saturation current

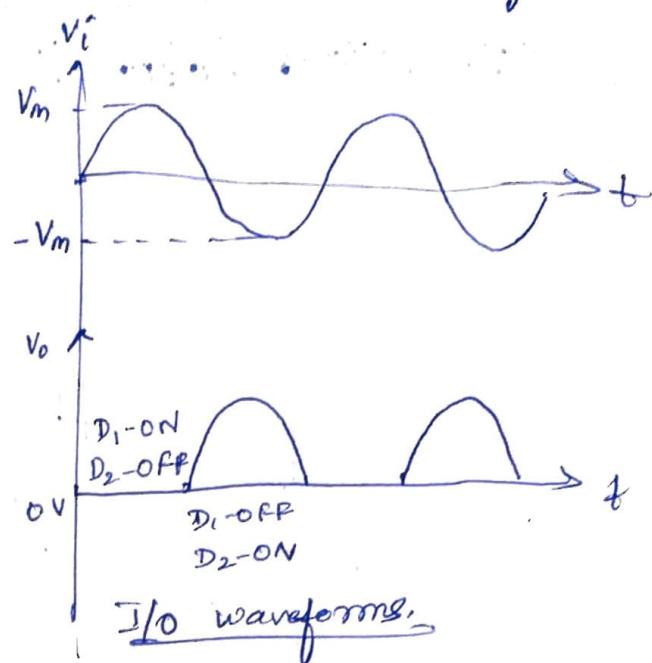
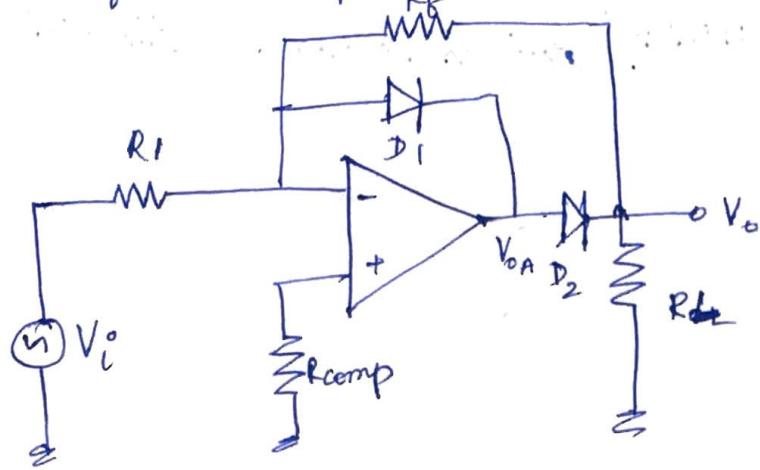
This circuit is called the precision diode and is capable of rectifying input signals of the order of millivolts.

Typical Applications of precision diode are

- Half wave rectifier
- Full wave rectifier
- Peak value detector
- Clippers
- Clampers

Precision Half wave rectifier

An ~~ideal~~ inverting amplifier can be converted into an ideal half wave rectifier by adding two diodes as shown in fig



Ideal half wave rectifier

When V_i is positive, D_1 conducts causing V_{OA} is negative $\therefore D_2$ is reverse Biased $\Rightarrow V_o = 0$ \because no current flows through R_f & the input current flows through \cancel{D}_1

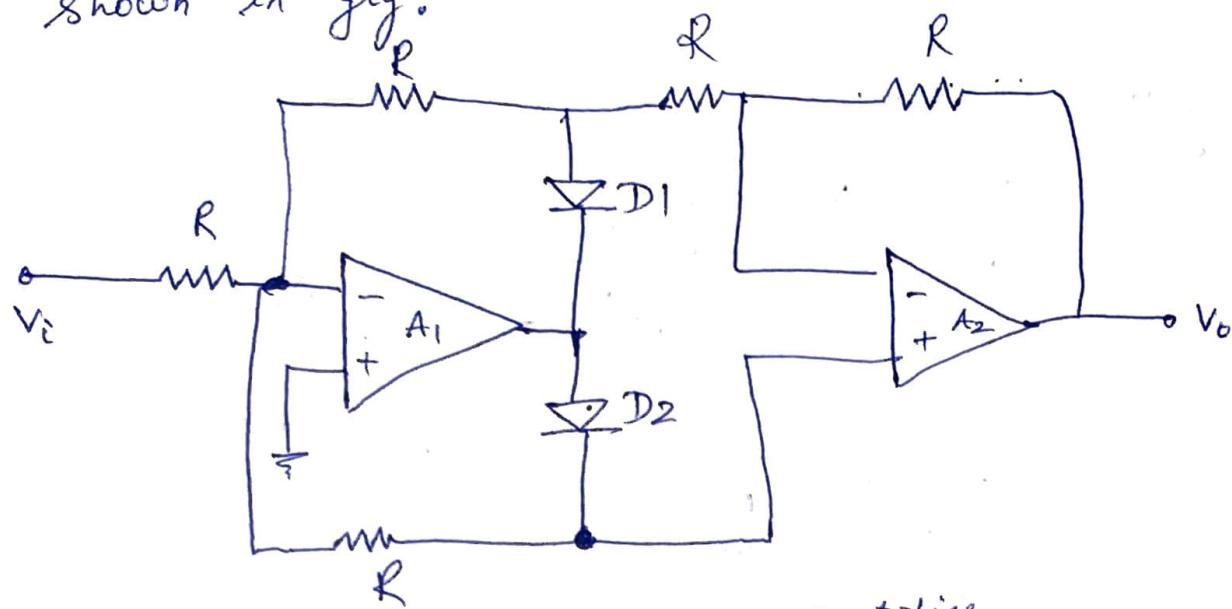
When V_i is negative $V_i < 0$ D_2 conducts & D_1 is off
-ve V_i forces V_{OA} to positive thus D_2 conducts
Now the circuit behaves like an ~~ideal~~ inverting amplifier
(If $R_i = R_f$ the circuit behaves like inverter)
 $\therefore V_o$ becomes positive.

The op-amp must be a high speed op-amp since it alternates between open loop and closed loop operations.
 \rightarrow Slew Rate is the limitation.

\Rightarrow If both diodes are reversed ~~then~~ then only positive signal is transmitted and gets inverted. The circuit then provides a negative output.

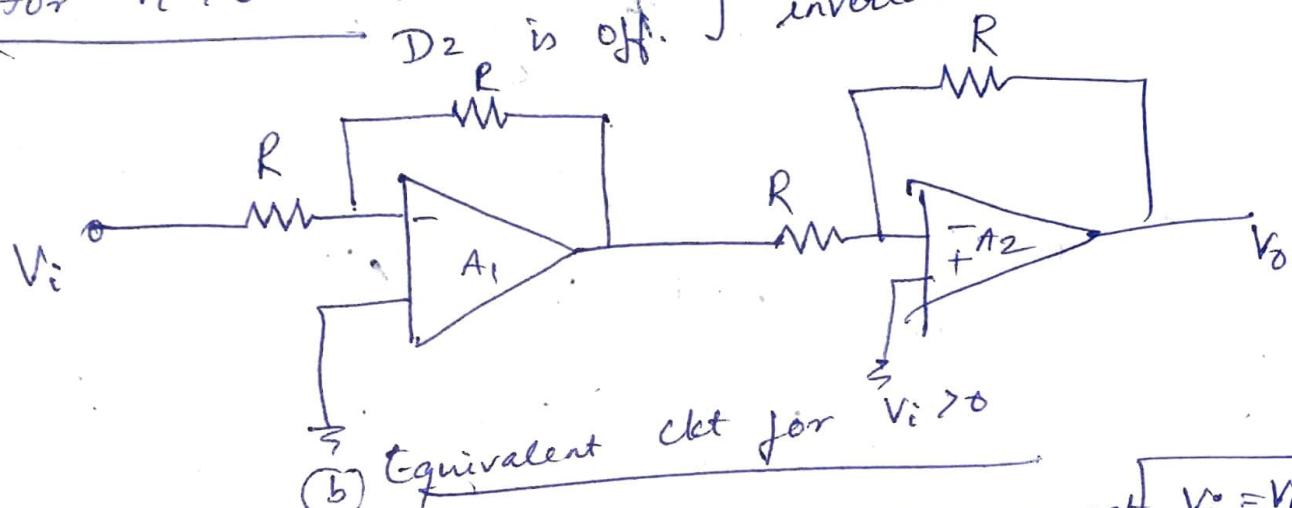
Precision Full wave Rectifier

A full wave rectifier or absolute value ckt is as shown in fig.



(a) Precision full wave rectifier

For $V_i > 0 \rightarrow D_1$ is ON }
 D_2 is off. } Both A_1 & A_2 acts as inverter

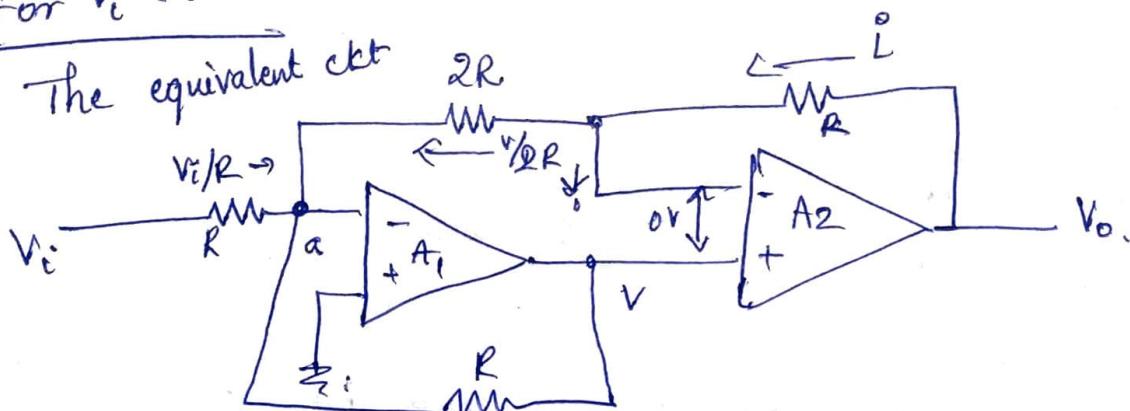


(b) Equivalent ckt for $V_i > 0$

when A_1 & A_2 both are inverter we get $V_i = V_0$

For $V_i < 0 \rightarrow D_1$ is off, D_2 is ON.

The equivalent ckt



(c) Equivalent ckt for $V_i < 0$

Let the output voltage of A₁ be V

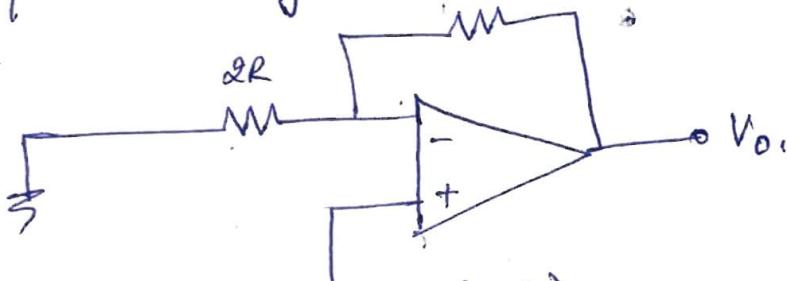
From the ckt the differential I/P to A₂ = 0 V [\therefore both the terminals are at potential V]

Apply KCL at node a

$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

$$V = -\frac{2}{3} V_i \quad \text{--- (1)}$$

The equivalent ckt of $V_i < 0$ can be written as shown below:-



$$V = \left(-\frac{2}{3} V_i\right)$$

Equivalent ckt. of (1)

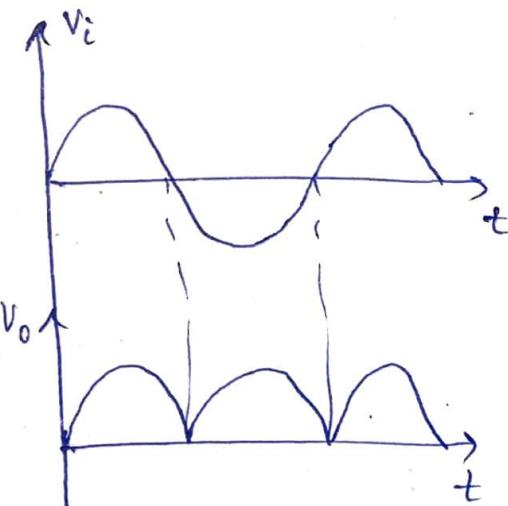
This ckt is a non-inverting amplifier. The o/p voltage will be

$$\Rightarrow V_o = \left(1 + \frac{R}{2R}\right) V$$

$$= \left(1 + \frac{1}{2}\right) \left(-\frac{2}{3} V_i\right)$$

$$= \frac{3}{2} \times -\frac{2}{3} V_i$$

$$V_o = -V_i$$



\therefore When $V_i < 0$ the output is positive

This circuit is also called absolute value circuit as output is positive even when I/P is -ve.

It is possible to obtain negative outputs by simply reversing the diodes.

Peak Detectors :-

(3)

→ The function of a peak detector is to compute the peak value of the input.

→ The circuit follows the voltage peaks of a signal and stores the highest value on a capacitor

→ If a higher peak signal is detected new value is stored and it remains till the capacitor is discharged

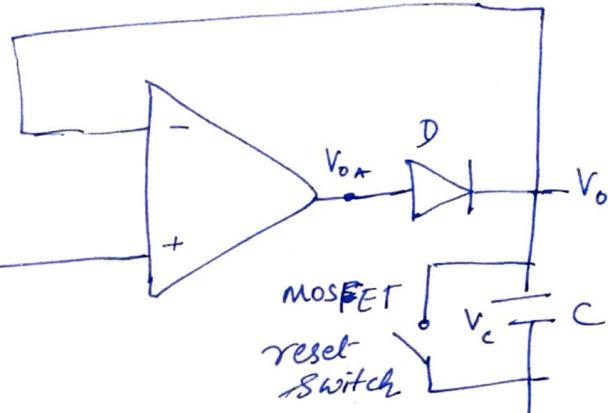
when $V_i > V_c \Rightarrow D$ is forward biased, the circuit behaves like a voltage follower $\therefore V_o$ follows V_i till V_i exceeds V_c

When $V_i < V_c \rightarrow D$ is reverse biased and capacitor holds the charge till input voltage again attains a value $> V_c$.

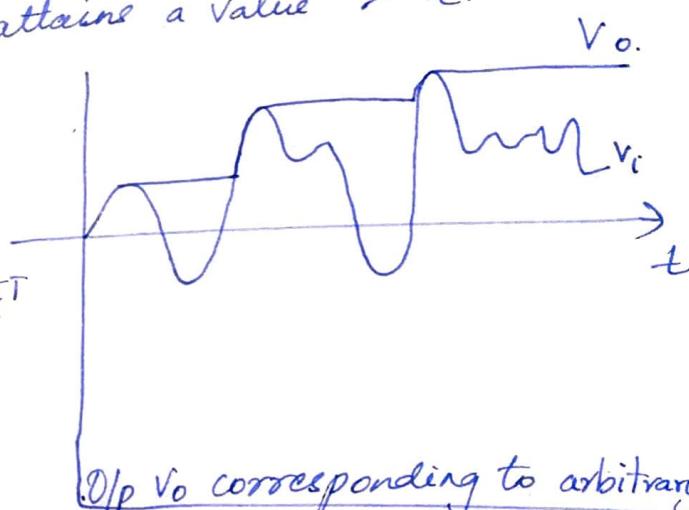
→ The circuit can be reset, i.e. capacitor V_c can be made zero by connecting a low leakage MOSFET switch across capacitor.

⇒ If the diode is reversed the ckt can detect the lowest or the most negative voltage.

⇒ Applications



Positive peak detector



O/p V_o corresponding to arbitrary input V_i

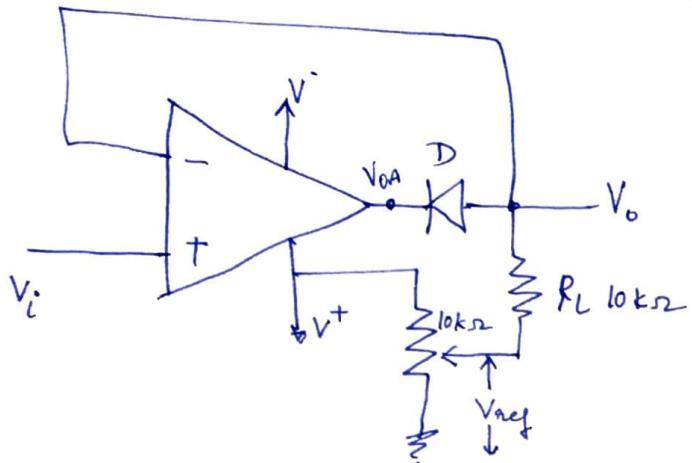
Test and measurement instrumentation

Amplitude modulation Communication.

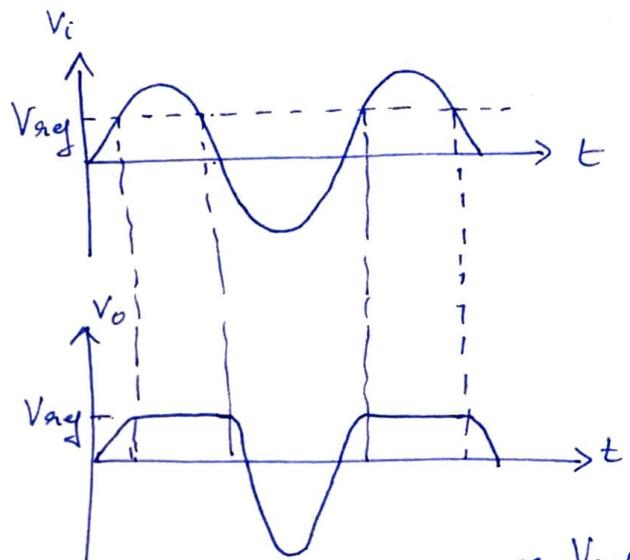
Clippers.

A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired output waveform.

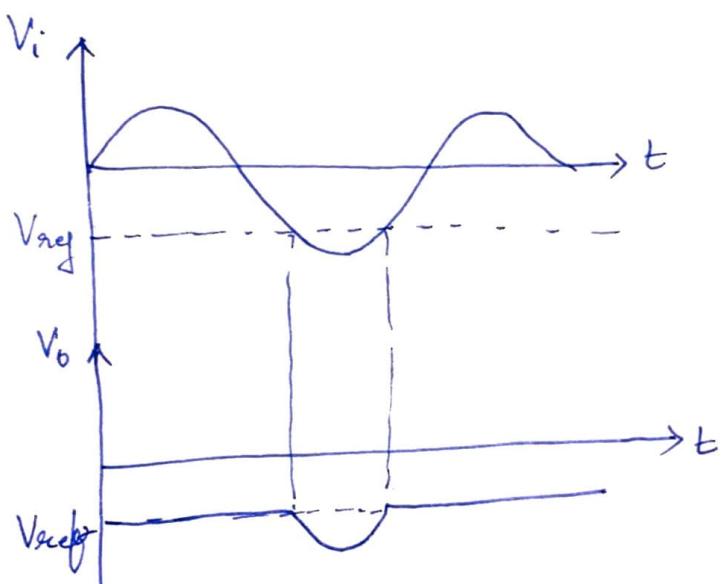
Positive clipper



Positive clipper circuit



I/O waveform for +ve Vref



I/O waveform for -ve Vref

The clipping level is determined by the reference voltage V_{ref} and could be obtained from the +ve ~~neg~~ supply voltage V^+ .

for $V_i > V_{ref}$ are clipped off

For input voltage $V_i < V_{ref}$ diode D conducts
op-amp works as voltage follower

$$V_o = V_i$$

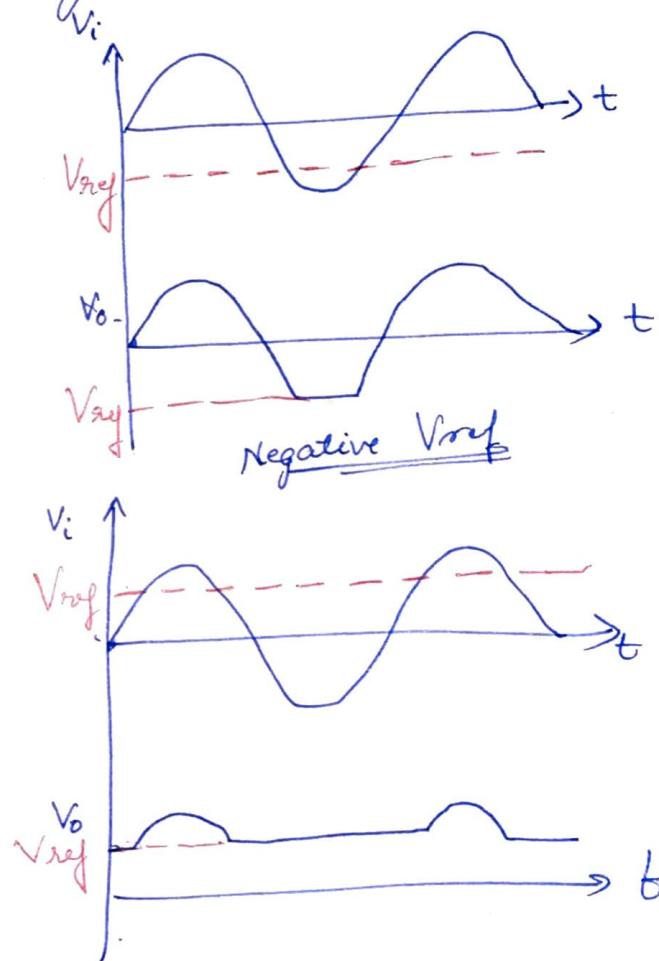
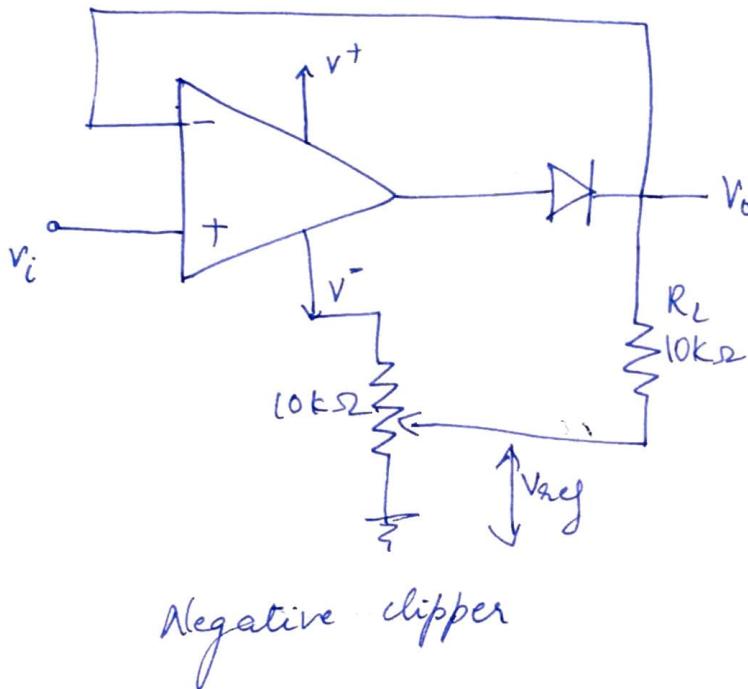
when $V_i \geq V_{ref}$ D is OFF \Rightarrow the op-amp V_{OA} is not enough to drive the Diode.

Thus the op-amp voltage $V_o = V_{ref}$

If V_{ref} is -ve. Then o/p waveform above V_{ref} will be clipped off as shown in fig. (4)

Negative Clipper :-

- Positive clipper can be converted to a negative ~~converter~~ clipper by simply reversing the diode and changing the polarity of the reference voltage V_{ref} .
- circuit diagram & expected graphs are shown below.

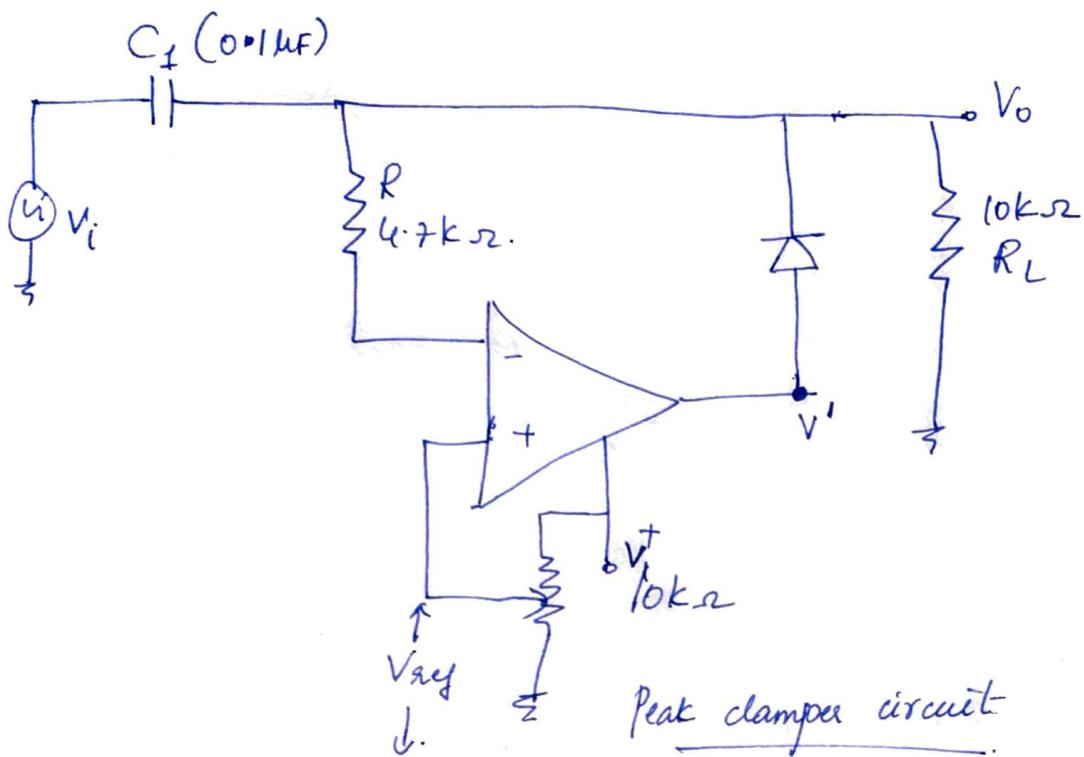


Positive V_{ref}

Clampers

- The clampers are also known as dc inserter or restorer.
- Adds desired dc level to the output voltage.
 - o/p is clamped to a desired dc level.

- If dc level is positive it is positive clumper
- If dc level is negative → negative clumper.



- Clammer circuit with a variable dc voltage applied at non inverting input terminal is as shown in fig.
- This circuit clamps the ~~peak~~ of peak of the I/p waveform and ∴ it is also called as peak clammer.

→ O/p contains both ac & dc. Since ~~but~~ the inverting terminal is applied with ac voltage and non inverting terminal with dc V_g .

Let us consider
 → When V_{ref} is +ve V' is also +ve → D is ON. ∴ $V_o = +V_{ref}$

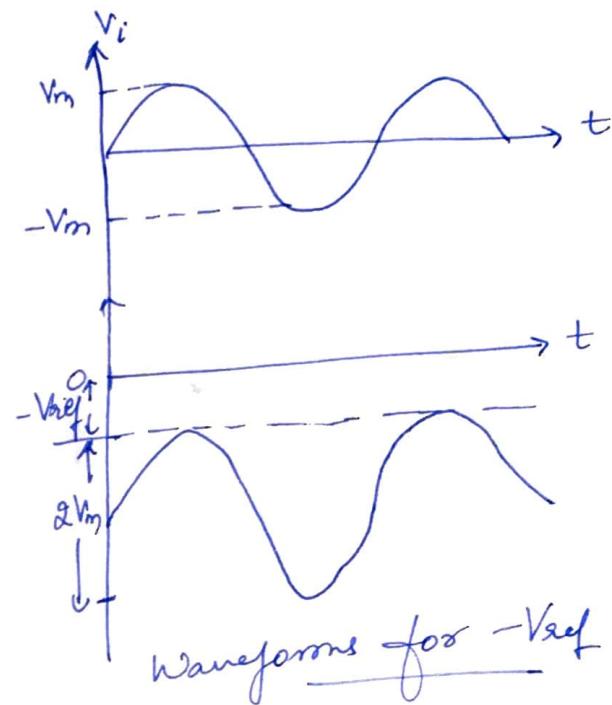
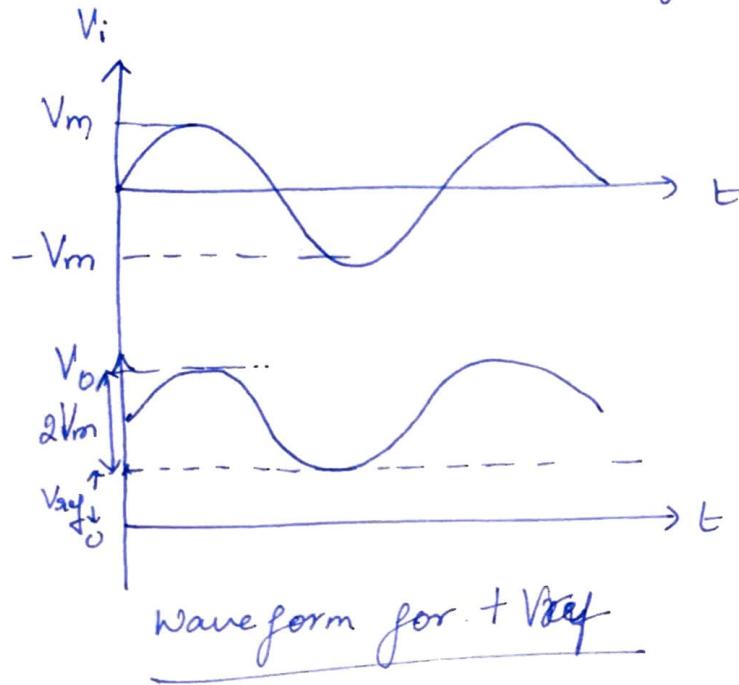
→ Now consider ac input $V_i = V_m \sin \omega t$ applied at inverting terminal
In -ve half cycle diode conducts, thus Capacitor C_1 charges through diode (D) to -ve peak V_g V_m

In +ve half cycle → diode is reverse biased → capacitor retains the voltage charged (V_m)

(5)

This V_m is in series with the ac input signal,
 $\therefore \text{O/p } V_{\text{tg}} = \underline{V_m + V_i}$

Let us examine the o/p voltage when both V_{ref} & V_i are applied
 The total o/p voltage $V_o = \underline{V_{\text{ref}} + V_m + V_i}$



Negative Peak Clamping can be obtained by simply reversing the diode and using a -ve reference voltage ($-V_{\text{ref}}$)

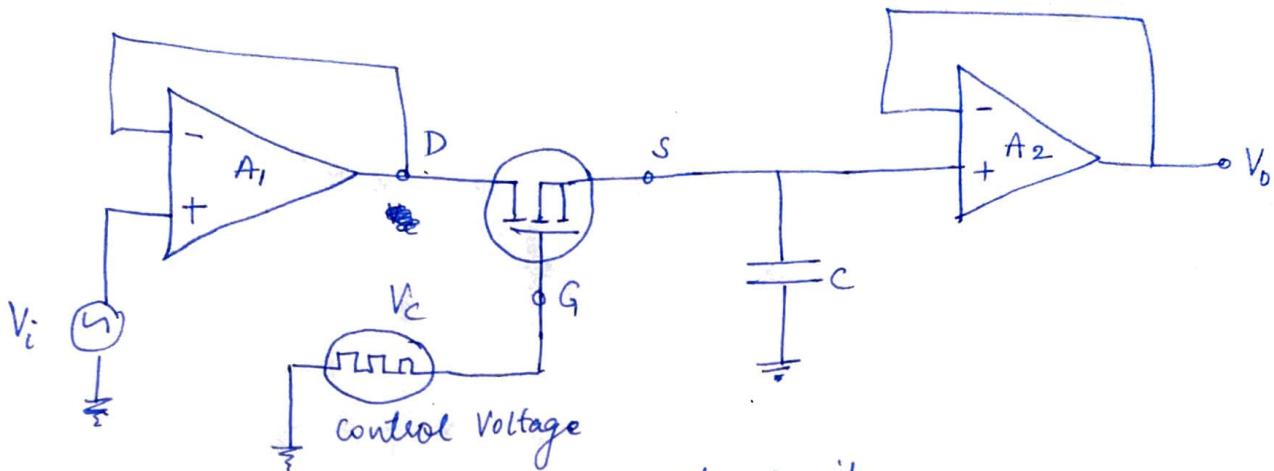
\Rightarrow The resistor R is used for protecting the op-amp against excessive discharge currents from capacitor C_1 especially when dc supply V_{gs} are switched off.

Sample and Hold Circuit

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again.

Application of this circuit

- digital interfacing
- analog to digital modulation techniques
- pulse code modulation techniques

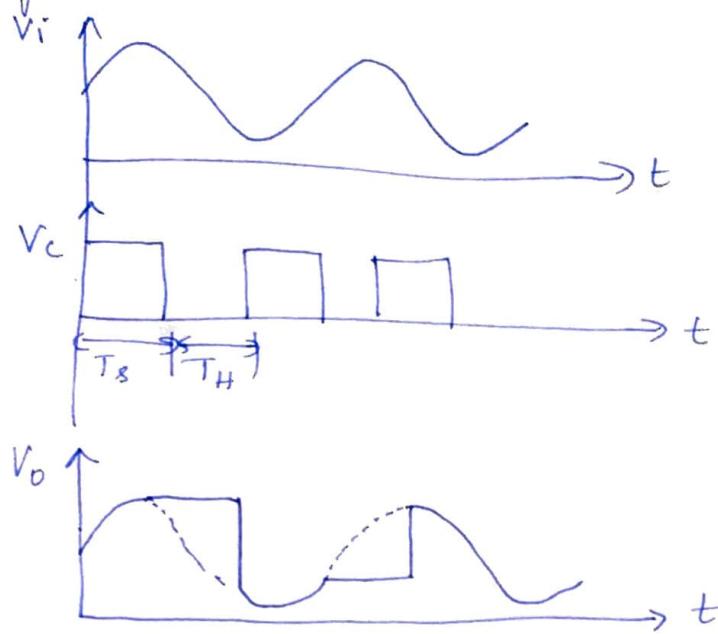


Sample and hold circuit

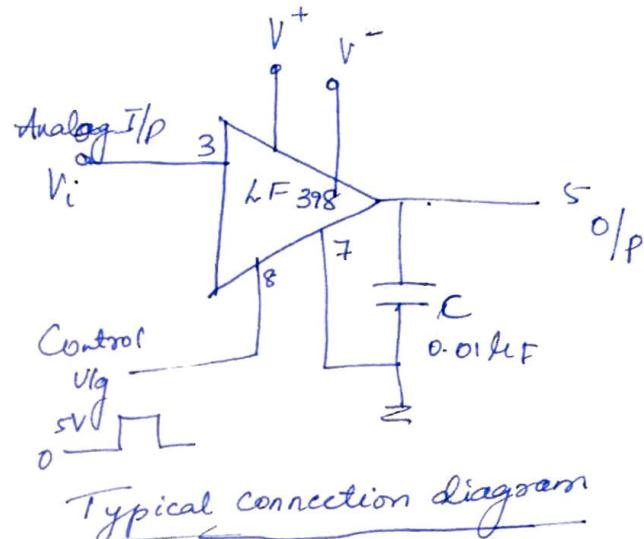
→ The simplest practical sample and hold circuit configuration as shown above.

- n-channel enhancement mode MOSFET works as a switch and is controlled by the control voltage V_c .
- Capacitor stores the charge.
- Drain of e-mosfet is applied with analog signal V_i to be sampled
- The control v/g V_c is applied to the gate
- When V_c is positive e-mosfet is ON capacitor charges to the instantaneous value of input V_i with a time constant $[R_o + r_{DS(on)}]C$.
 $R_o \rightarrow$ output resistance of the op-amp. A_1 (Voltage follower A_1)
 $\neq r_{DS(on)}$ → resistance of the MOSFET when on.
- V_i appears across the capacitor C and at the o/p of voltage follower A_2 .
- When mosfet is OFF (ie when $V_c = 0$) → The capacitor ~~here~~ is facing high input impedance of the voltage follower A_2 .
∴ Capacitor cannot discharge. it holds the charged value.
- The time period T_s is the time during which voltage across the capacitor is equal to the input V_g . is called the sample period.

The time period T_H during which the voltage across the capacitor is held constant is called hold period



I/O waveform



Typical connection diagram

(at least twice)

- The control voltage frequency should be higher than the input signal frequency, so that the input can be retrieved from the output.
- A low leakage capacitor should be used to retain the stored charge.
- Several sample and hold IC's are available of make Harris Semiconductor HA2420, National Semiconductor such as LF198, LF398.
- The typical diagram of LF398 is as shown in fig.

11

D-A AND A-D CONVERTERS

11.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superim-position of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variables in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 11.1 highlights a typical application within which A/D and D/A conversion is used. Figure 11.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

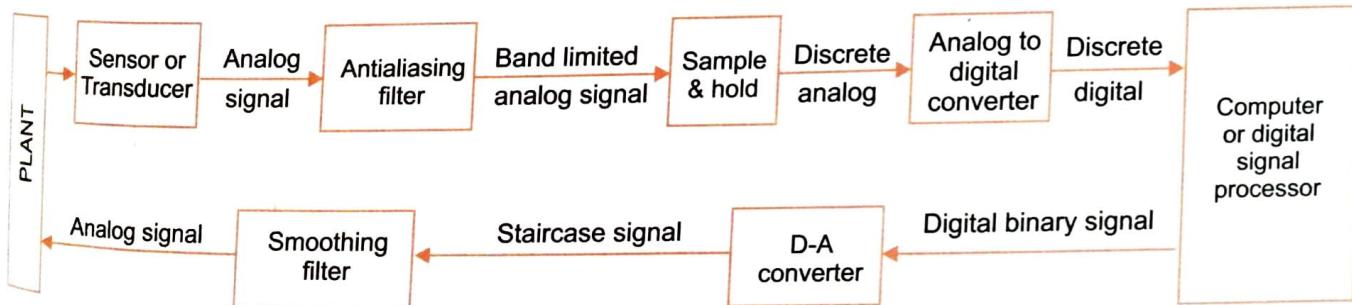


Fig. 11.1 Circuit showing application of A/D and D/A converter

The scheme given in Fig. 11.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

11.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 11.2. The input is an n -bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K V_{FS} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}) \quad (11.1)$$

where, V_o = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

d_1, d_2, \dots, d_n = n -bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

There are various ways to implement Eq. (11.1). Here we shall discuss the following resistive techniques only:

Weighted resistor DAC

R-2R ladder

Inverted R-2R ladder

11.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 11.3 (a) uses a summing amplifier with a binary weighted resistor network. It has n -electronic switches d_1, d_2, \dots, d_n controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 11.3 (a), the output current I_o for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \dots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n R} d_n$$

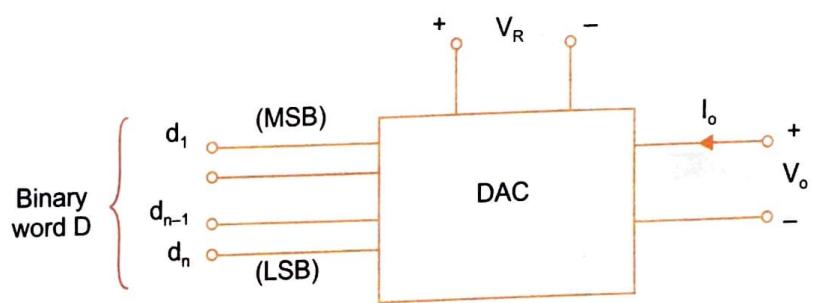


Fig. 11.2 Schematic of a DAC

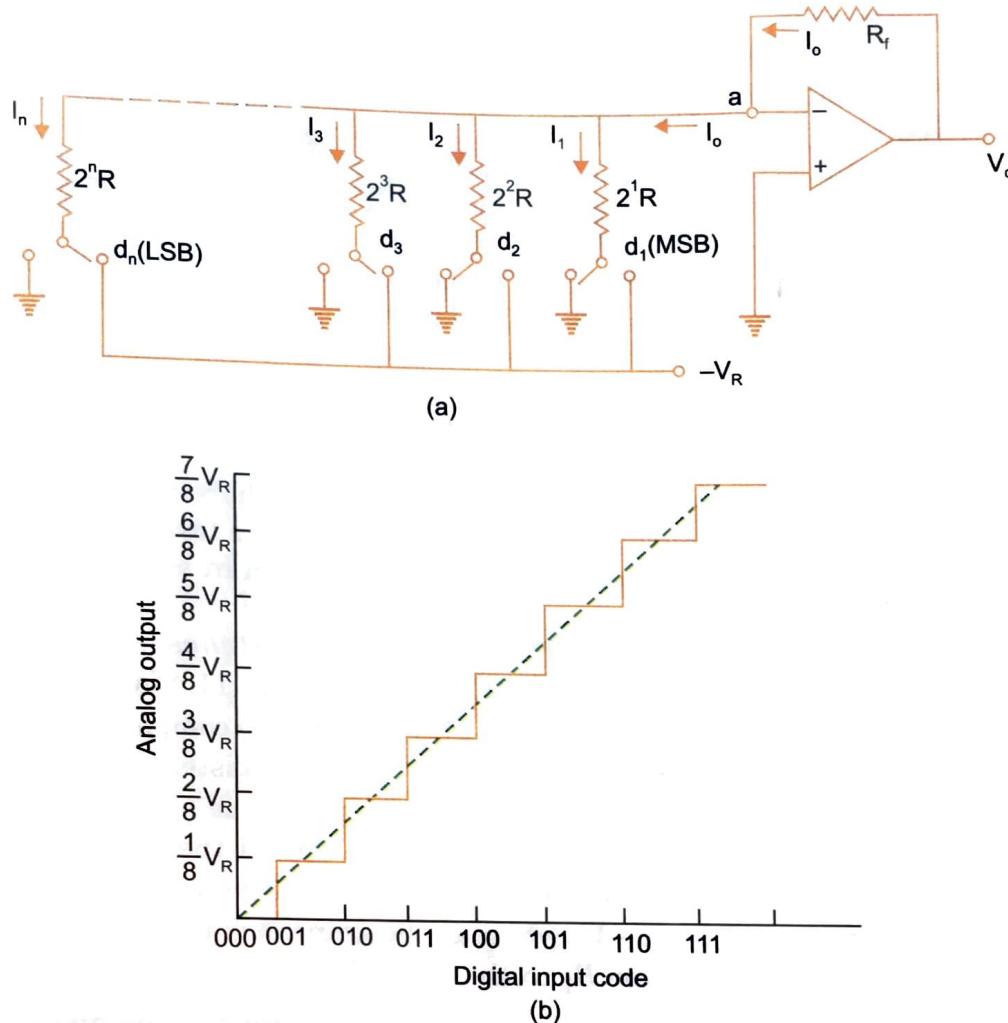


Fig. 11.3 (a) A simple weighted resistor DAC, **(b)** Transfer characteristics of a 3-bit DAC

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n}) \quad (11.2)$$

Comparing Eq. (11.1) with Eq. (11.2), it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 11.3 (a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 11.3 (b) for a 3-bit weighted resistor DAC. It may be noted that

- (i) Although the op-amp in Fig. 11.3 (a) is connected in inverting mode, it can also be connected in non-inverting mode.
- (ii) The op-amp is simply working as a current to voltage converter.
- (iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be $+5\text{ V}$ and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are $2^0 R, 2^1 R, 2^2 R, \dots, 2^7 R$. The largest resistor increases. For 8-bit DAC, the resistors required are $2^0 R, 2^1 R, 2^2 R, \dots, 2^7 R$. The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is $5.12 \text{ M}\Omega$ if the smallest is $2.5 \text{ k}\Omega$. The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as $2.5 \text{ k}\Omega$ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 11.3 (a) are in series with resistors and therefore, their **on** resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

Different types of **digitally controlled SPDT electronic switches** are available of which two are shown in Fig. 11.4. A totem-pole MOSFET driver in Fig. 11.4 (a) feeds each resistor connected to the inverting input terminal 'a' of Fig. 11.3 (a). The two complementary gate inputs Q and \bar{Q} come from MOSFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i.e. logic '1' corresponds to -10 V and logic '0' corresponds to zero volt. If there is '1' in the bit line, $S = 1$ and $R = 0$ so that $Q = 1$ and $\bar{Q} = 0$. This drives the transistor Q_1 **on**, thus connecting the resistor R_1 to the reference voltage $-V_R$ whereas the transistor Q_2 remains **off**. Similarly a '0' at the bit line connects the resistor R_1 to the ground terminal.

Another SPDT switch of Fig. 11.4(b) consists of CMOS inverter feeding an op-amp voltage follower which drives R_1 from a very low output resistance. The circuit is using a positive logic with $V(1) = V_R = +5 \text{ V}$ and $V(0) = 0 \text{ V}$. The complement \bar{Q} of the bit under consideration is applied at the input. Thus $\bar{Q} = 0$ makes transistor Q_1 **off** and Q_2 **on**. The output of the CMOS inverter is at logic 1, that is, 5 V is applied to resistor R_1 through the voltage follower. And if $\bar{Q} = 1$ the output of the CMOS inverter is 0 V connecting the resistance R_1 to ground.

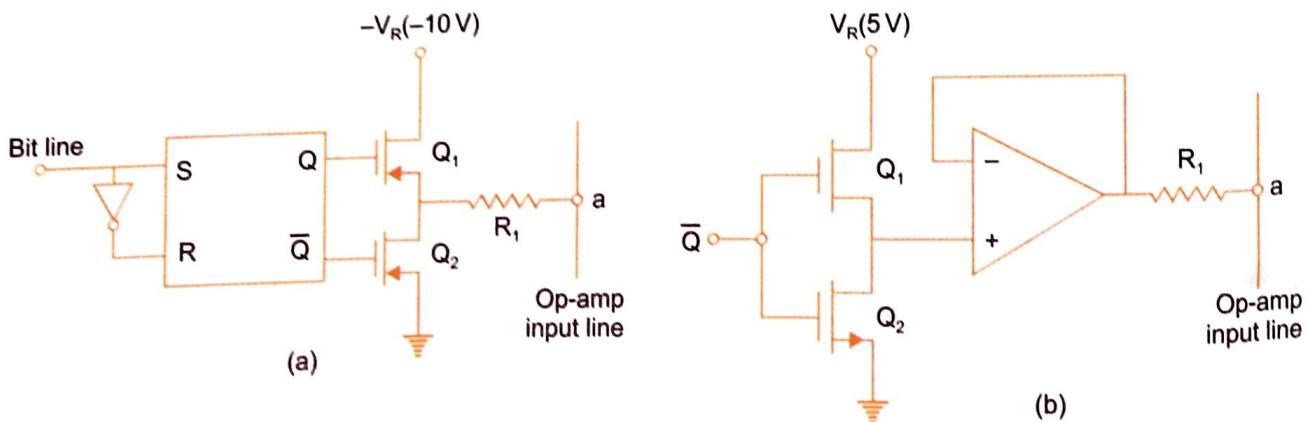


Fig. 11.4 (a) A totem pole MOSFET switch **(b)** CMOS inverter as switch

11.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from $2.5 \text{ k}\Omega$ to $10 \text{ k}\Omega$.

For simplicity, consider a 3-bit DAC as shown in Fig. 11.5 (a), where the switch position $d_1 d_2 d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 11.5 (b) and finally to Fig. 11.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R \left(\frac{2}{3}R \right)}{2R + \frac{2}{3}R} = -\frac{V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R} \left(-\frac{V_R}{4} \right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

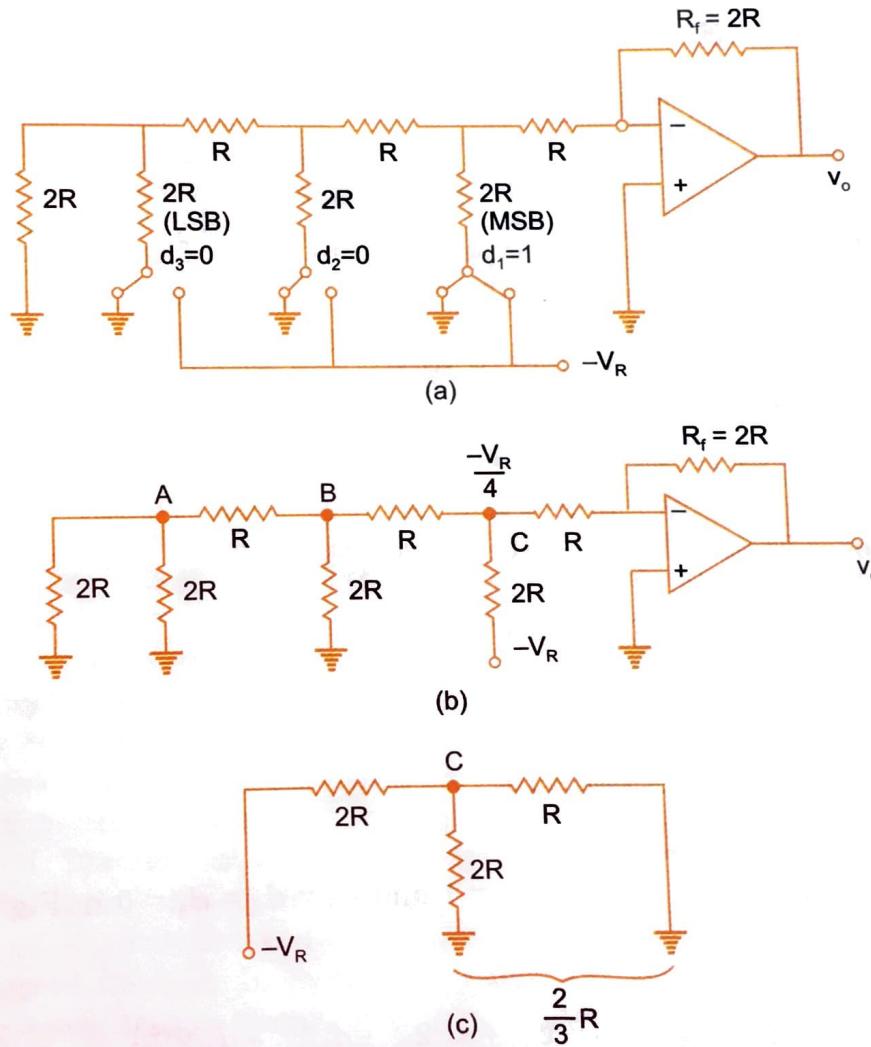


Fig. 11.5 (a) R-2R ladder DAC, **(b)** Equivalent circuit of (a), **(c)** Equivalent circuit of (b)

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 11.6 (a). The circuit can be simplified to the equivalent form of Fig. 11.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_o = \left(-\frac{2R}{R} \right) \left(-\frac{V_R}{16} \right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

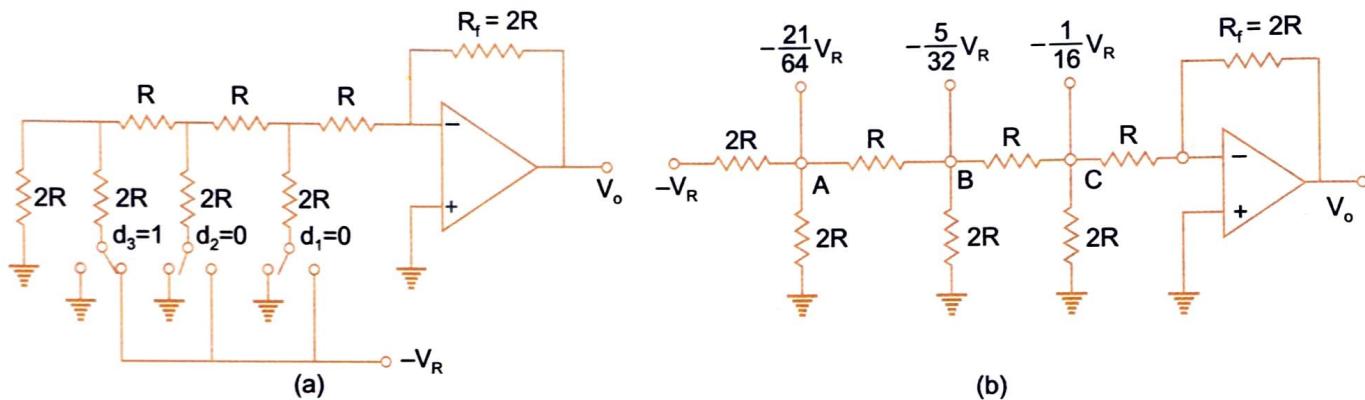


Fig. 11.6 (a) R-2R ladder DAC for switch positions 001, **(b)** Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

Example 11.1

Consider a 4 bit $R-2R$ ladder DAC of the type shown in Fig 11.5 (a). Given $R = 10 \text{ k}\Omega$ and $V_R = 10 \text{ V}$. Determine the value of the feedback resistance R_f for the following output conditions.

- (i) value of 1 LSB at the output is 0.5V
- (ii) analog output is 6V for a binary input of 1000
- (iii) full scale output voltage is 10 V

Solution

- (i) Given $R = 10 \text{ k}\Omega$, $V_R = 10 \text{ V}$ and $n = 4$

The resolution of a $R - 2R$ ladder DAC is given by

$$\text{Resolution, } V = \frac{1}{2^n} \times \frac{V_R}{R} \times R_f$$

$$\text{Thus } 0.5V = \frac{1 \times 10V \times R_f}{2^4 \times 10 \times 10^3}$$

or

$$R_f = 8 \text{ k}\Omega$$

- (ii) For binary digital input 1000, setting $d_1 = 1$ and $d_2 = d_3 = d_4 = 0$ in Fig 11.3(a), we can write

$$V_o = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + d_4 2^{-4})$$

$$6 = \frac{R_f \times 10V \times 2^{-1}}{10 \times 10^3} \text{ (as } d_2 = d_3 = d_4 = 0\text{)}$$

Therefore,

$$R_f = 12 \text{ K}\Omega$$

(iii) Now $d_1 = d_2 = d_3 = d_4 = 1$. Thus for getting the full scale voltage of 10V,

$$R_f \times \frac{10}{10 \times 10^3} (2^{-1} + 2^{-2} + 2^{-3} + 2^{-4}) = 10$$

Thus

$$R_f = 10.667 \text{ K}\Omega$$

11.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 11.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 11.7 (a), when switch d_i is at logical '0' i.e., to the left, the current through $2R$ resistor flows to the ground and when the switch d_i is at logical '1' i.e., to the right, the current through $2R$ sinks to the virtual ground. The circuit has the important property that the current divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly $2R$. The division of the current is shown in Fig. 11.7 (b). Consider a reference current of 2 mA . Just to the right of node A , the equivalent resistor is $2R$. Thus 2 mA of reference input current divides equally to value 1 mA at node A . Similarly to the right of node B , the equivalent resistor is $2R$. Thus 1 mA of current further divides to value 0.5 mA at node B . Similarly, current divides equally at node C to 0.25 mA . The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 11.7 (a) are the SPDT switches discussed earlier. According to bit d_i , the corresponding switch gets connected either to ground for $d_i = 0$ or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for $d_i = 1$ and from ground to $-V_R$ for $d_i = 0$. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 11.7(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 11.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

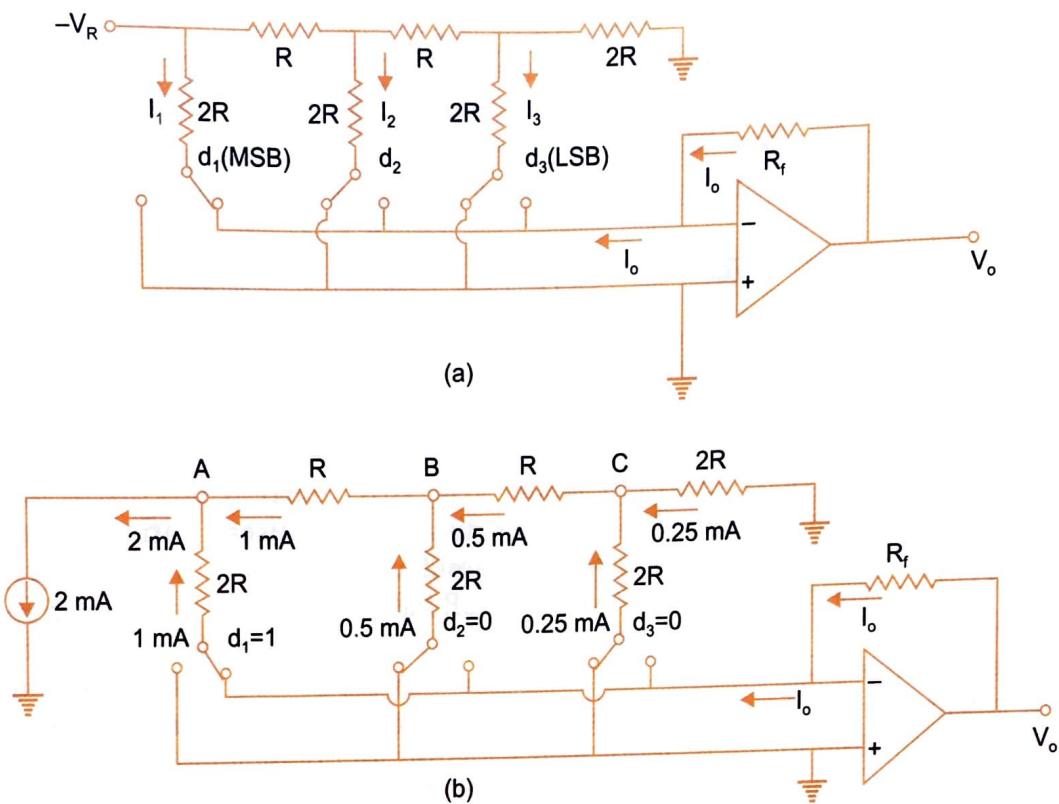


Fig. 11.7 (a) Inverted $R - 2R$ ladder DAC, (b) Inverted $R - 2R$ ladder DAC showing division of current for digital input word 001

Example 11.2

Consider the inverted $R - 2R$ ladder DAC shown in Fig 11.7 (a) Given $R = R_f = 10 \text{ k}\Omega$ and $V_R = 10\text{V}$. Calculate the output voltage for the binary input of 1110.

Solution

In Fig 11.7 (a),

$$I_1 = \frac{V_R}{2R} = \frac{10\text{V}}{2 \times 10 \times 10^3} = 0.5 \text{ mA}$$

$$I_2 = \frac{I_1}{2} = 0.25 \text{ mA}$$

$$I_3 = \frac{I_2}{2} = 0.125 \text{ mA}$$

and

Therefore, current

$$\begin{aligned} I_o &= I_1 + I_2 + I_3 \\ &= 0.5 + 0.25 + 0.125 \text{ mA} \\ &= 0.875 \text{ mA} \end{aligned}$$

The output voltage,

$$\begin{aligned} V_o &= I_o \times R_f \\ &= 0.875 \times 10^{-3} \times 10 \times 10^3 \\ &= 8.75 \text{ V} \end{aligned}$$

11.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage V_R is called a multiplying D/A converter (MDAC). Thus if in the Eq. (11.1), the reference voltage v_R is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

$$\text{Then, } v_o(t) = V_{om} \cos (2\pi ft + 180^\circ)$$

where V_{om} will vary from 0V to $(1-2^{-n}) V_{im}$ depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output V_o is a fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

11.2.5 Monolithic DAC : 1408 DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 11.8 (a). It has eight input data lines d_1 (MSB) through d_8 (LSB). It requires 2 mA reference current for full scale input and two power supplies $V_{CC} = +5$ V and $V_{EE} = -5$ V (V_{EE} can range from -5 V to -15 V). The total reference current source is determined by resistor R_{14} and voltage reference V_R and is equal to $V_R/R_{14} = 5$ V/ 2.5 k Ω = 2 mA. The resistor $R_{15} = R_{14}$ match the input impedance of the reference source. The output current I_o is calculated as

$$I_o = \frac{V_R}{R_{14}} \left(\sum_{i=1}^8 d_i 2^{-i} \right); d_i = 0 \text{ or } 1$$

For full scale input (i.e. d_8 through $d_1 = 1$)

$$I_o = \frac{5 \text{ V}}{2.5 \text{ k}\Omega} \left(\sum_{i=1}^8 1 \times 2^{-i} \right) = 2 \text{ mA } (255/256) = 1.992 \text{ mA}$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage V_o for the full scale input is

$$V_o = 2 \text{ mA } (255/256) \times 5 \text{ k}\Omega = 9.961 \text{ V}$$

In general, the output voltage V_o is given by

$$V_o = \frac{V_R}{R_{14}} R_f \left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \dots + \frac{d_8}{256} \right]$$

The 1408 DAC can be calibrated for bipolar range from -5 V to $+5$ V by adding resistor R_B (5 k Ω) between V_R and output pin 4 as shown in Fig. 11.8 (b). The resistor R_B supplies 1 mA ($= V_R/R_B$) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation I'_o is

$$I'_o = I_o - (V_R/R_B) = (V_R/R_{14}) \left(\sum_{i=1}^8 d_i 2^{-i} \right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

$$V_o = I'_o R_f = (I_o - V_R/R_B) R_f = (0 - 5 \text{ V}/5 \text{ k}\Omega) \times 5 \text{ k}\Omega = -5 \text{ V}$$

For binary input word = 10000000, output V_o becomes

$$\begin{aligned} V_o &= (I_o - V_R/R_B) R_f = [(V_R/R_{14}) (d_1/2) - (V_R/R_B)] R_f \\ &= [(5 \text{ V}/2.5 \text{ k}\Omega) (1/2) - (5 \text{ V}/5 \text{ k}\Omega)] 5 \text{ k}\Omega = (1 \text{ mA} - 1 \text{ mA}) \times 5 \text{ k}\Omega = 0 \text{ V} \end{aligned}$$

For binary input word = 11111111, output V_o becomes

$$\begin{aligned} V_o &= [(V_R/R_{14}) (255/256) - (V_R/R_B)] R_f = (1.992 \text{ mA} - 1 \text{ mA}) \times 5 \text{ k}\Omega \\ &= 0.992 \text{ mA} \times 5 \text{ k}\Omega = +4.960 \text{ V} \end{aligned}$$

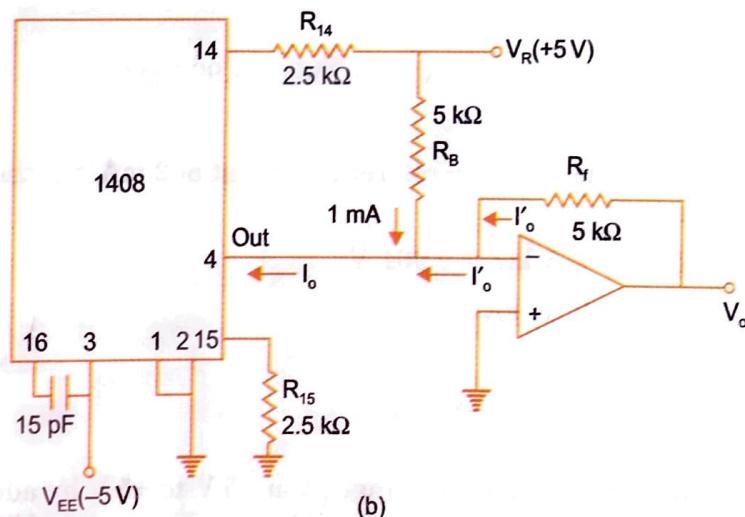
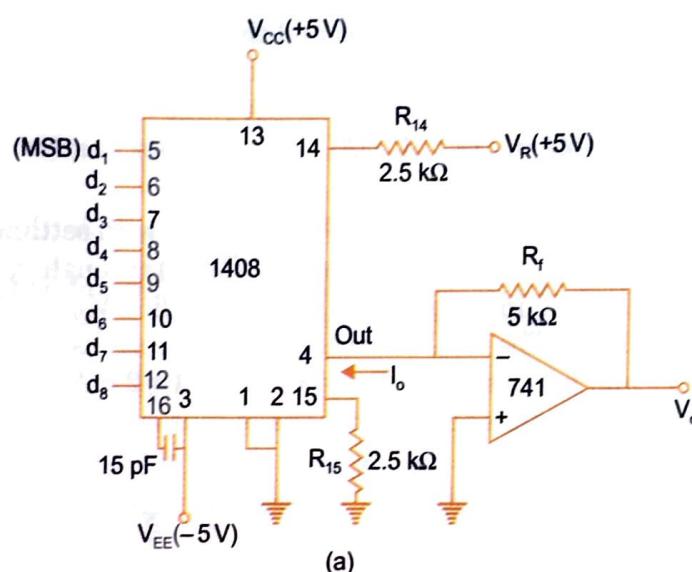


Fig. 11.8 1408 D/A converter (a) Voltage output in unipolar range (b) Modified circuit for bipolar output

Example 11.3

The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111?

Solution

The output voltage for input 101101111 is

$$= 10.3 \text{ mV} (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0) \\ = 10.3 \text{ mV} (367) = 3.78 \text{ V}$$

Example 11.4

Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 V range.

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

$$\text{For } 10 \text{ V range, } \text{LSB} = \frac{10 \text{ V}}{256} = 39 \text{ mV}$$

and

$$\text{MSB} = \left(\frac{1}{2}\right) \text{ full scale} = 5 \text{ V}$$

$$\begin{aligned} \text{Full scale output} &= (\text{Full scale voltage} - 1 \text{ LSB}) \\ &= 10 \text{ V} - 0.039 \text{ V} = 9.961 \text{ V} \end{aligned}$$

Example 11.5

What output voltage would be produced by a D/A converter whose output range is 0 to 10 V and whose input binary number is

- (i) 10 (for a 2-bit D/A converter)
- (ii) 0110 (for a 4-bit DAC)
- (iii) 10111100 (for a 8-bit DAC)

Solution

$$(i) V_o = 10 \text{ V} \left(1 \times \frac{1}{2} + 0 \times \frac{1}{4}\right) = 5 \text{ V}$$

$$\begin{aligned} (ii) V_o &= 10 \text{ V} \left(0 \times \frac{1}{2} + 1 \times \frac{1}{2^2} + 1 \times \frac{1}{2^3} + 0 \times \frac{1}{2^4}\right) \\ &= 10 \left(\frac{1}{4} + \frac{1}{8}\right) = 3.75 \text{ V} \end{aligned}$$

$$\begin{aligned} (iii) V_o &= 10 \text{ V} (1 \times 1/2 + 0 \times 1/2^2 + 1 \times 1/2^3 + 1 \times 1/2^4 + 1 \times 1/2^5 \\ &\quad + 1 \times 1/2^6 + 0 \times 1/2^7 + 0 \times 1/2^8) \\ &= 10 \text{ V} (1/2 + 1/8 + 1/16 + 1/32 + 1/64) = 7.34 \text{ V} \end{aligned}$$

11.3 A-D CONVERTERS

The block schematic of ADC shown in Fig. 11.9 provides the function just opposite to that of a DAC. It accepts an analog input voltage V_a and produces an output binary word $d_1 d_2 \dots d_n$ of

functional value D , so that

$$D = d_1 2^{-1} + d_2 2^{-2} + \dots + d_n 2^{-n} \quad (11.3)$$

where d_1 is the most significant bit and d_n is the least significant bit. An ADC usually has two additional control lines: the **START** input to tell the ADC when to start the conversion and the **EOC** (end of conversion) output to announce when the conversion is complete. Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays.

ADCs are classified broadly into two groups according to their conversion technique. Direct type ADCs and Integrating type ADCs. Direct type ADCs compare a given analog signal with the internally generated equivalent signal. This group includes

- Flash (comparator) type converter
- Counter type converter
- Tracking or servo converter
- Successive approximation type converter

Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are:

- (i) Charge balancing ADC
- (ii) Dual slope ADC

The most commonly used ADCs are **successive approximation** and **the integrator type**. The successive approximation ADCs are used in applications such as data loggers and instrumentation where conversion speed is important. The successive approximation and comparator type are faster but generally less accurate than integrating type converters. The flash (comparator) type is expensive for high degree of accuracy. The integrating type converter is used in applications such as digital meter, panel meter and monitoring systems where the conversion accuracy is critical.

DIRECT TYPE ADCs

11.3.1 The Parallel Comparator (Flash) A/D Converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure 11.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 11.10 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 11.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table for the flash type AD converter is shown in Fig. 11.10 (c). The circuit has the advantage of high speed as the

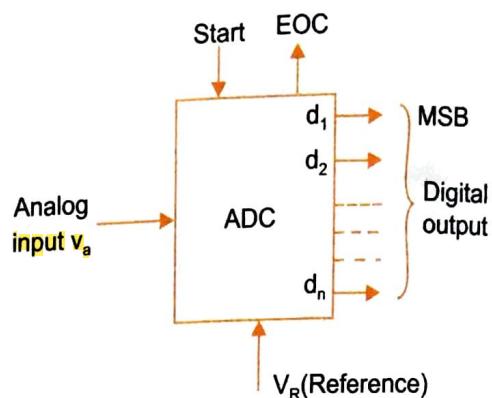


Fig. 11.9 Functional diagram of ADC

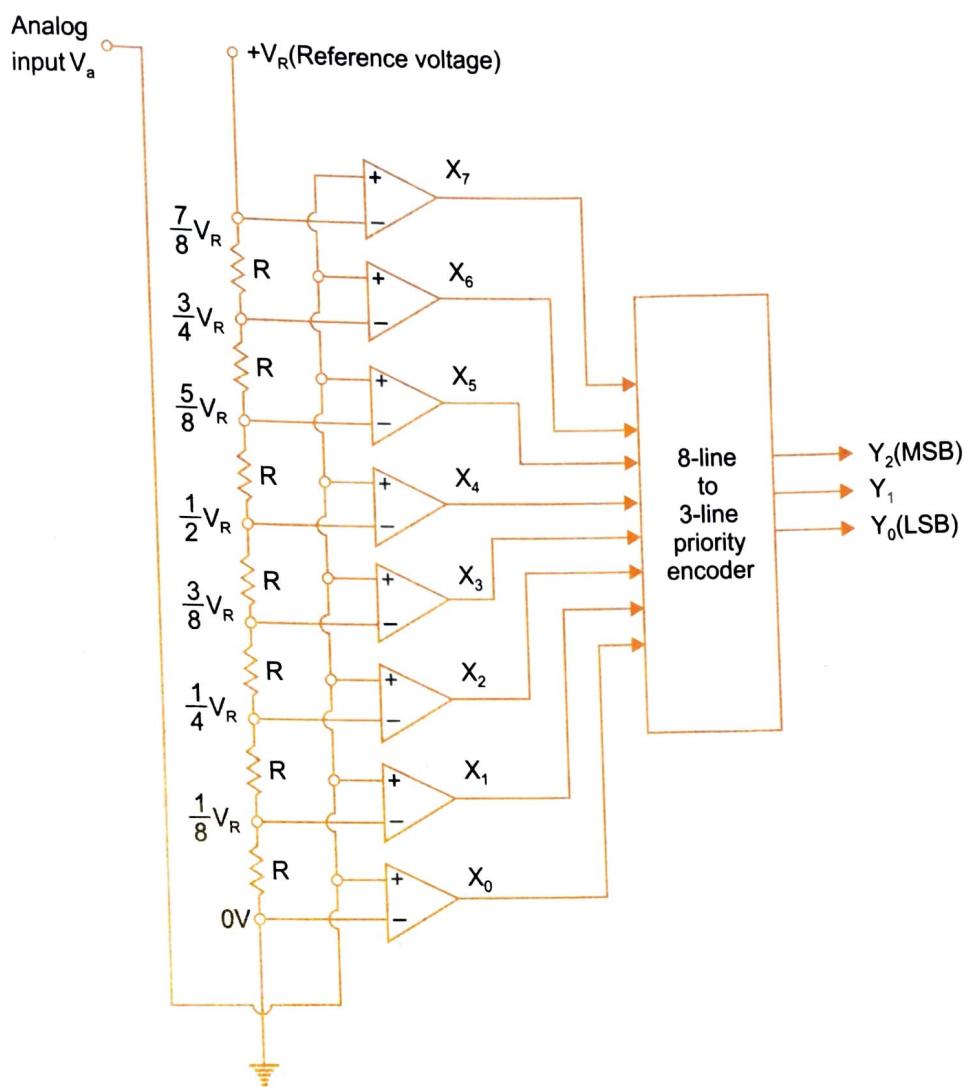


Fig. 11.10 (a) Basic circuit of a flash type A/D converter

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

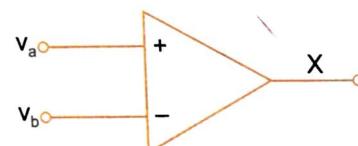


Fig. 11.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to $3 V_R/8$	0	0	0	0	0	1	1	1	0	1	0
$3 V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to $5 V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5 V_R/8$ to $3 V_R/4$	0	0	1	1	1	1	1	1	1	0	1
$3 V_R/4$ to $7 V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7 V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 11.10 (c) Truth table for a flash type A/D converter

conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are $2^n - 1$ where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n , the more complex is the priority encoder.

11.3.2 The Counter Type A/D Converter

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within $\pm (1/2)$ LSB to the analog input V_a which is to be converted to binary digital form. Thus in addition to the DAC, we need suitable logic circuitry to perform the code search and a comparator of adequate quality to announce when the DAC output has come within $\pm (1/2)$ LSB to V_a .

A 3-bit counting ADC based upon the above principle is shown in Fig. 11.11 (a). The counter is reset to zero count by the reset pulse. Upon the release of RESET, the clock pulses are counted by the binary counter. These pulses go through the AND gate which is enabled by the voltage comparator high output. The number of pulses counted increase with time. The binary word representing this count is used as the input of a D/A converter whose output is a staircase of the type shown in Fig. 11.11 (b). The analog output V_d of DAC is compared to the analog input V_a by the comparator. If $V_a > V_d$, the output of the comparator becomes high and the AND gate is enabled to allow the transmission of the clock pulses to the counter. When $V_a < V_d$, the output of the comparator becomes low and the AND gate is disabled. This stops the counting at the time $V_a \leq V_d$ and the digital output of the counter represents the analog input voltage V_a . For a new value of analog input V_a , a second reset pulse is applied to clear the counter. Upon the end of the reset, the counting begins again as shown in Fig. 11.11 (b). The counter frequency must be low enough to give sufficient time

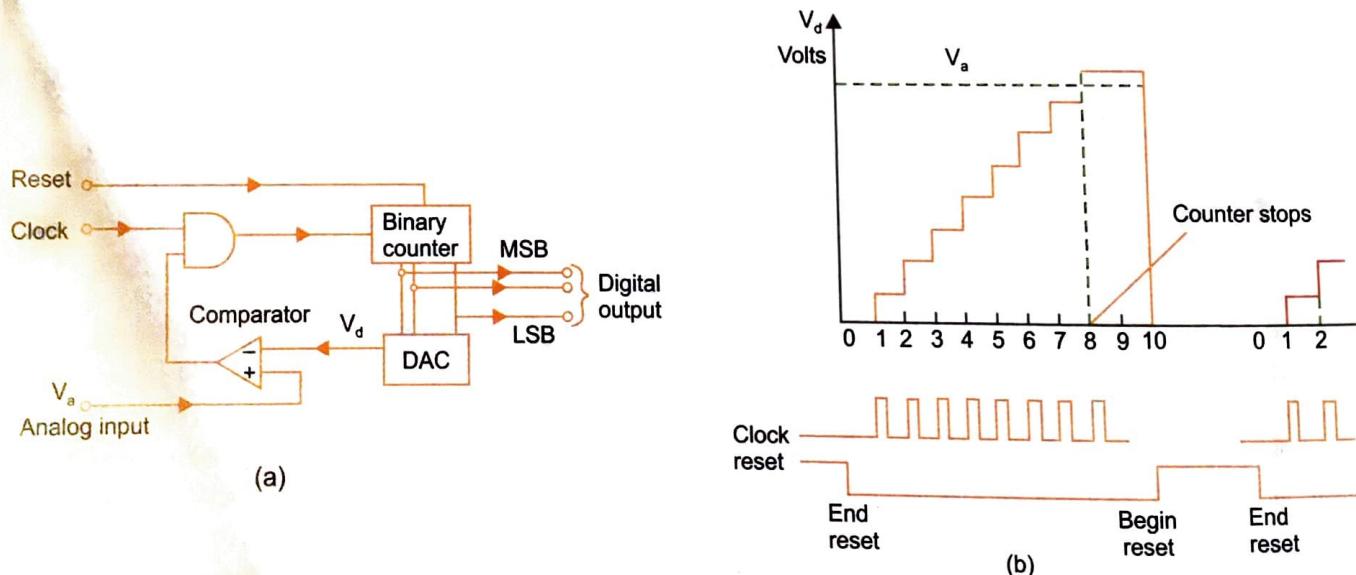


Fig. 11.11 (a) A counter type A/D converter, (b) D/A output staircase waveform

for the DAC to settle and for the comparator to respond. Low speed is the most serious drawback of this method. The conversion time can be as long as $(2^n - 1)$ clock periods depending upon the magnitude of input voltage V_a . For instance, a 12-bit system with 1 MHz clock frequency, the counter will take $(2^{12} - 1) \mu s = 4.095 \text{ ms}$ to convert a full scale input.

If the analog input voltage varies with time, the input signal is sampled, using a sample and hold circuit before it is applied to the comparator. If the maximum value of the analog voltage is represented by n -pulses and if the clock period is T seconds, the minimum interval between samples is nT seconds.

11.3.3 Servo Tracking A/D Converter

An improved version of counting ADC is the tracking or a servo converter shown in Fig. 11.12 (a). The circuit consists of an up/down counter with the comparator controlling the direction of the count. The analog output of the DAC is V_d and is compared with the analog input V_a . If the input V_a is greater than the DAC output signal, the output of the comparator goes high and the counter is caused to count up. The DAC output increases with each incoming clock pulse and when it becomes more than V_a , the counter reverses the direction and counts down (but only by one count, LSB). This causes the control to count up and the count increases by 1 LSB. The process goes on being repeated and the digital output changes back and forth by ± 1 LSB around the correct value. As long as the analog input changes slowly, the tracking A/D will be within one LSB of the correct value. However, when the analog input changes rapidly, the tracking A/D cannot keep up with the change and error occurs as shown in Fig. 11.12 (b).

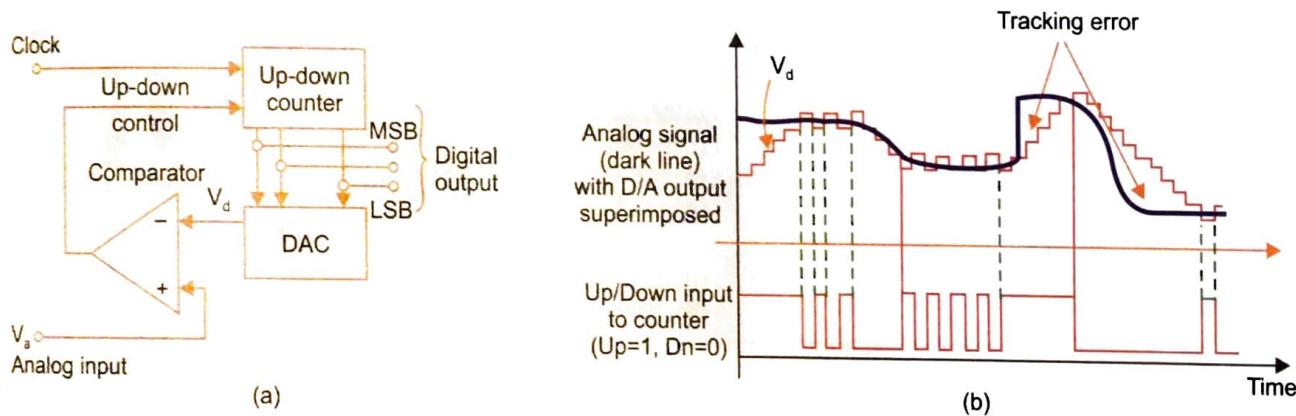


Fig. 11.12 (a) A tracking A/D converter, (b) Waveforms associated with a tracking A/D converter

The tracking ADC has the advantage of being simple. The disadvantage, however, is the time needed to stabilize as a new conversion value is directly proportional to the rate at which the analog signal changes.

11.3.4 Successive Approximation Converter

The successive approximation technique uses a very efficient code search strategy to complete n -bit conversion in just n -clock periods. An eight bit converter would require eight clock pulses to obtain a digital output. Figure 11.13 shows an eight bit converter. The circuit uses a

successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows. With the arrival of the START command, the SAR sets the MSB $d_1 = 1$ with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now compared with analog input V_a . If V_a is greater than the DAC output V_d then 10000000 is less than the correct digital representation. The MSB is left at '1' and the next lower significant bit is made '1' and further tested.

However, if V_a is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bit positions have been tested. Whenever the DAC output crosses V_a , the comparator changes state and this can be taken as the **end of conversion** (EOC) command. Figure 11.14 (a) shows a typical conversion sequence and Fig. 11.14 (b).

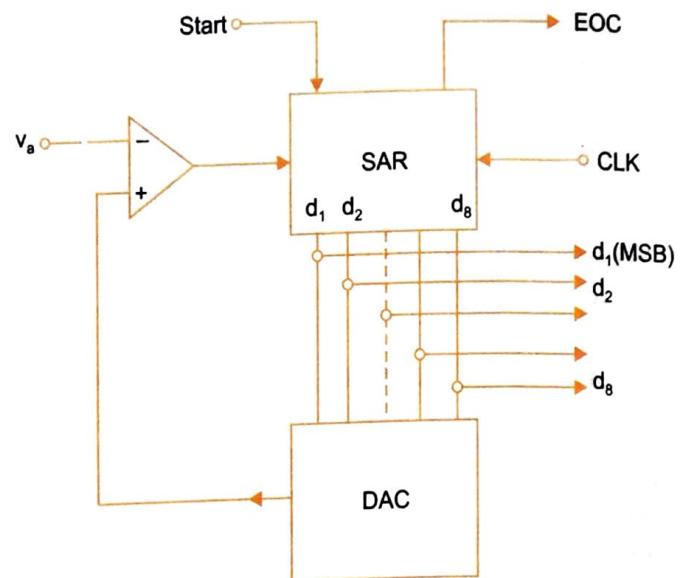


Fig. 11.13 Functional diagram of the successive approximation ADC

Correct digital representation	Successive approximation register output V_d at different stages in conversion	Comparator output
11010100	10000000	1 (initial output)
	11000000	1
	11100000	0
	11010000	1
	11011000	0
	11010100	1
	11010110	0
	11010101	0
	11010100	

Fig. 11.14 (a) Successive approximation conversion sequence for a typical analog input

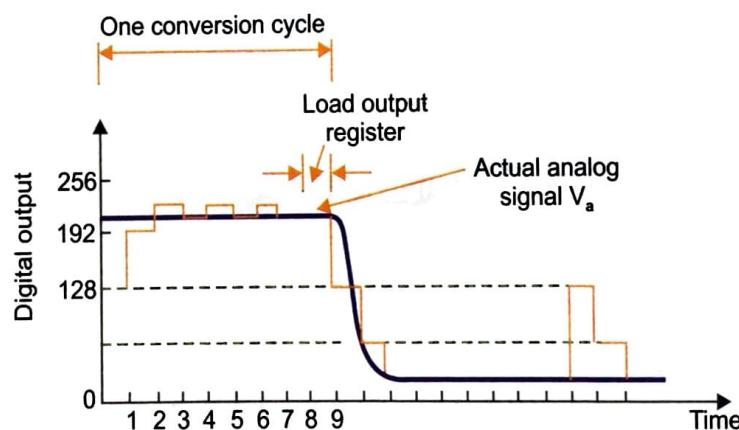


Fig. 11.14 (b) The D/A output voltage is seen to become successively closer to the actual analog input voltage

shows the associated wave forms. It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in Fig. 11.15. Given the same clock frequency, we see that the tracking circuit is faster only for small changes in the input. In general, the successive approximation technique is more versatile and superior to all other circuits discussed so far.

Successive approximation ADCs are available as self contained ICs. The AD7592 (Analog Devices Co.) a 28-pin dual-in-line CMOS package is a 12-bit A/D converter using successive approximation technique.

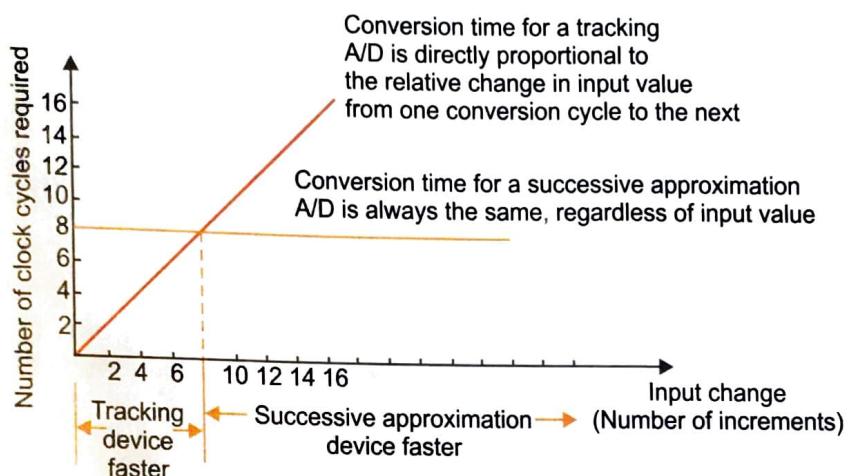


Fig. 11.15 Comparison of conversion times for tracking and successive approximation A/D devices

Example 11.6

An 8-bit A/D converter is used for converting 0 to 10V input voltage. Determine :

- input voltage required to change by 1 LSB
- input voltage required to generate all 1's at the output
- the digital output for an input voltage of 4.8V

Solution

$$(i) 1 \text{ LSB} = \frac{10V}{2^8} = 39.1 \text{ mV}$$

- Since digital output starts from 0 in a A/D converter, therefore the maximum full-scale input voltage will produce output less by 1 LSB for all digital output 1's.

Thus, $V_{iFS} = 10V - 39.1 \text{ mV} = 9.961 \text{ V}$.

- The digital output for an input voltage of 4.8V is given by

$$D = \frac{4.8V}{39.1 \text{ mV}} = 122.76$$

$$= 123$$

Converting this to binary gives the digital output as 01111011.

Example 11.7

The conversion rate of a 8-bit ADC is $9 \mu\text{s}$. Find the maximum frequency of the input sine wave that can be digitized.

Solution

The maximum frequency is given by

$$f_{\max} = \frac{1}{2\pi(T_C)2^n}$$

$$= \frac{1}{2\pi \times 9 \times 10^{-6} \times 2^8}$$

$$= 69.07 \text{ Hz.}$$

Comparators

An operational amplifier in the open-loop configuration operates in a non linear manner

Some of the op-amp non-linear applications are Comparators

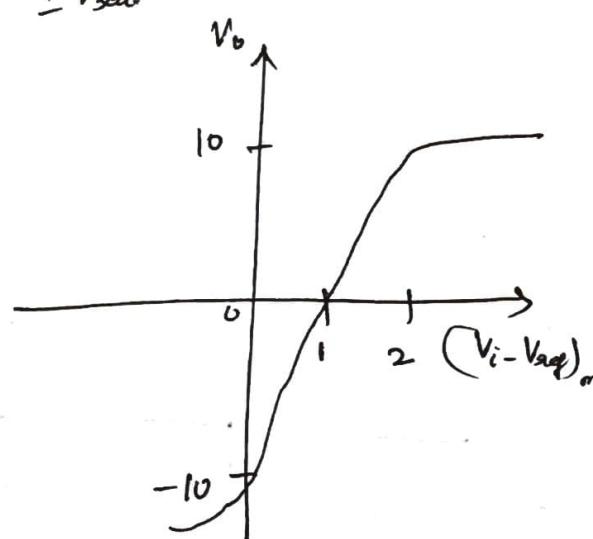
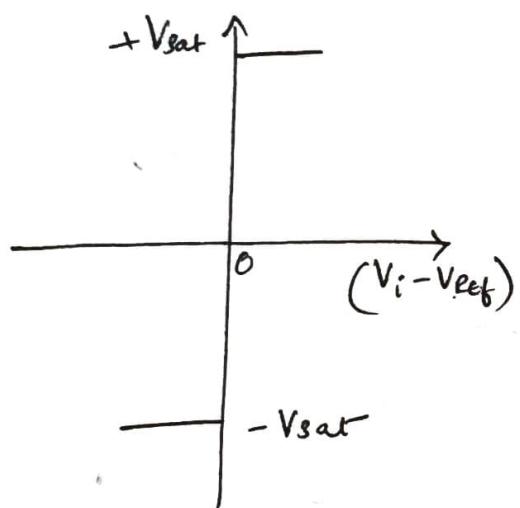
- Detectors

- Limiters

Digital Interfacing devices
namely Converters

A Comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input.

→ Open loop opamp with $V_{out} = \pm V_{sat}$



The transfer characteristics of Ideal Comparator

Transfer characteristics of Practical comparator

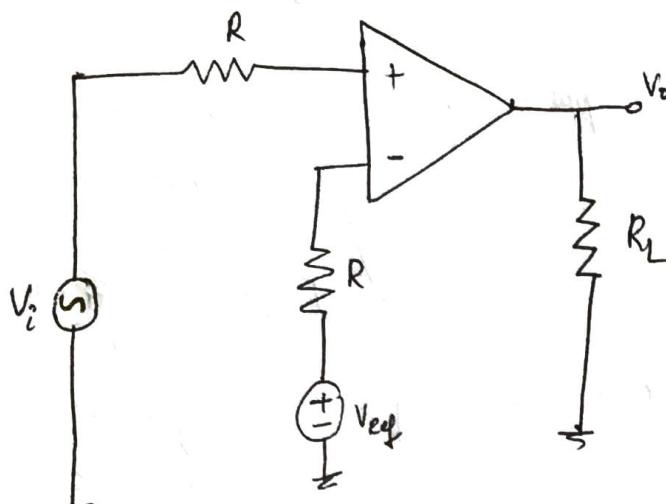
In the practical comparator change in the output state takes place with an increment in input V_i of $\sim 2mV \Rightarrow$ uncertainty region because output cannot be directly defined.

Two types of comparators are

[Inverting Comparator

Non-inverting Comparator

Non-inverting comparator



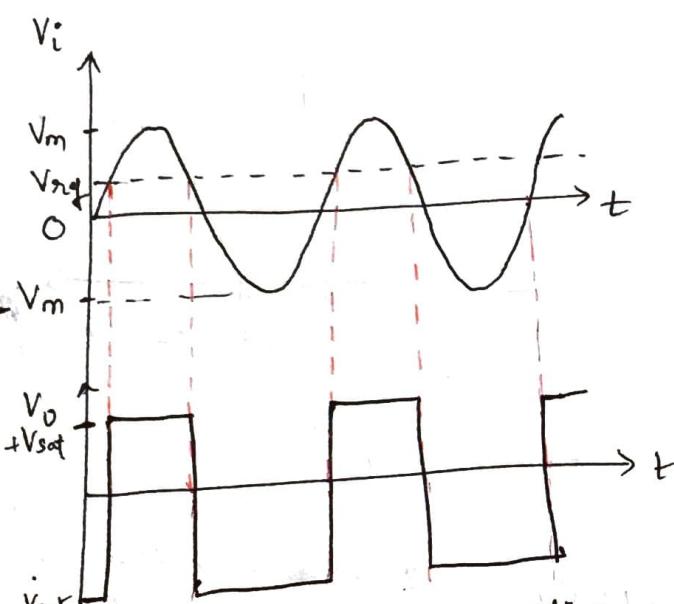
→ A fixed reference voltage V_{ref} is applied to -ve input terminal.

→ Analog signal (a time varying signal) is applied to non-inverting terminal.

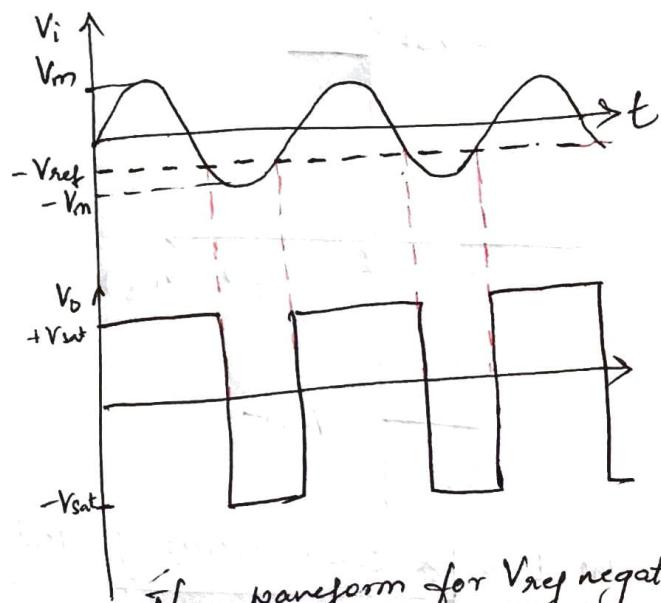
→ When $V_i > V_{ref} \Rightarrow V_{out} = +V_{sat}$

→ When $V_i < V_{ref} \Rightarrow V_{out} = -V_{sat}$

Non-inverting comparator



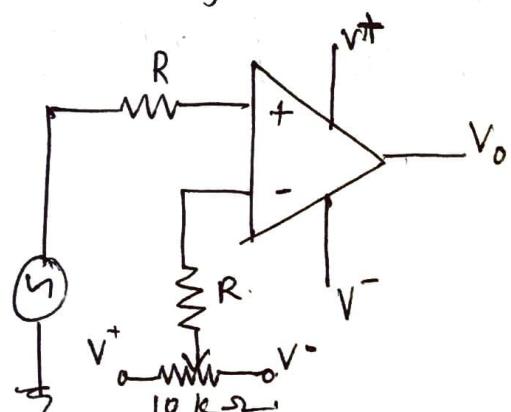
I/O waveform for V_{ref} positive



I/O waveform for V_{ref} negative

In a practical circuit V_{ref} is obtained by using a $10k\Omega$ potentiometer which forms a voltage divider with supply voltages V^+ and V^- with the wiper connected to inverting terminal.

By adjusting the potentiometer desired V_{ref} can be obtained.

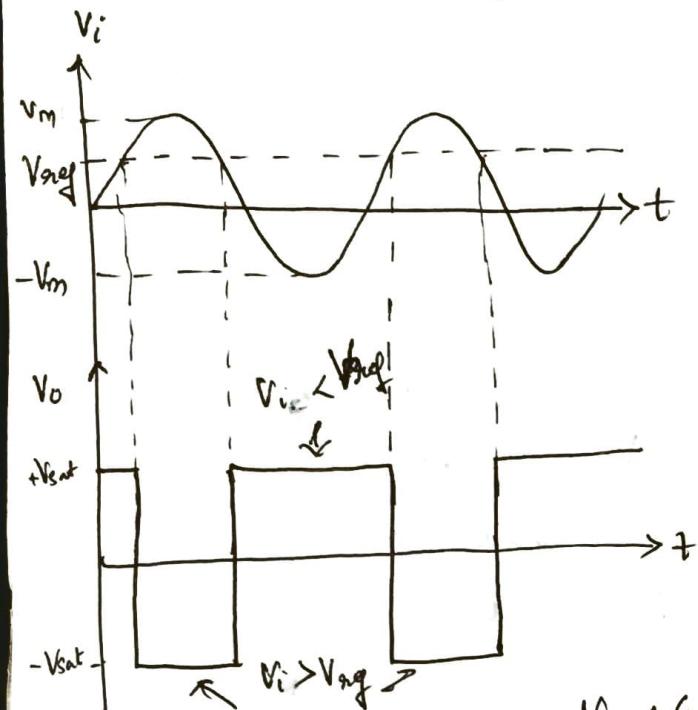


Inverting Comparator

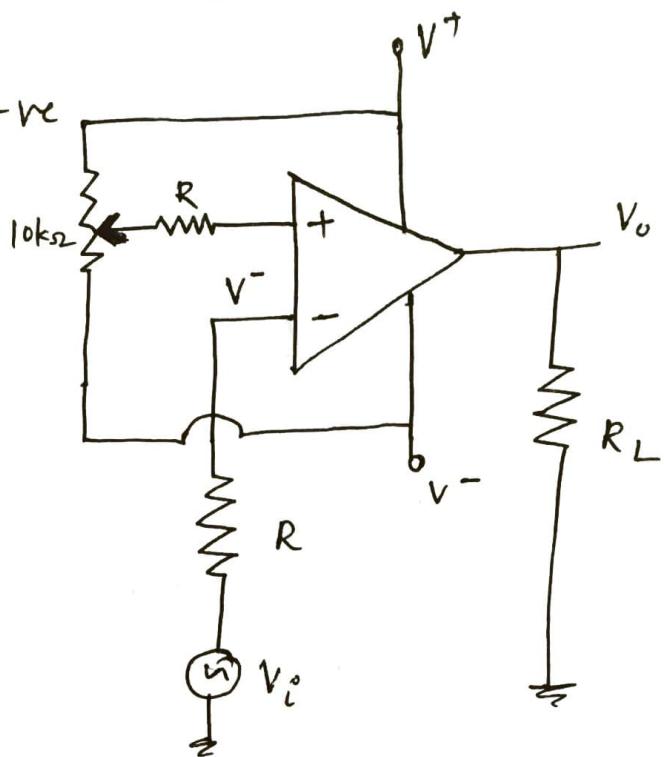
Practical Inverting comparator with $V_{ref} \rightarrow$ non inverting terminal

& V_i to inverting terminal.

I/O waveforms for $V_{ref} > 0$ & $-V_{ref}$ are as shown in fig below.



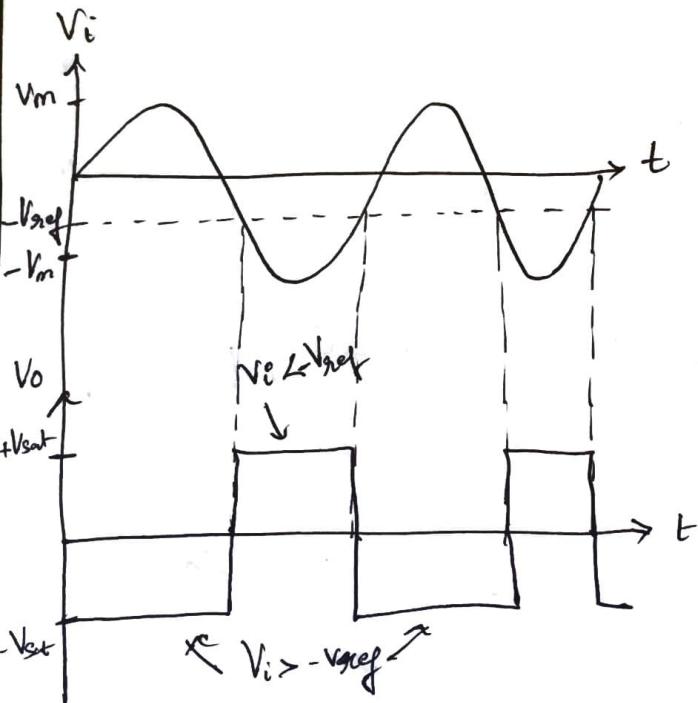
I/O waveform for +ve V_{ref} ($V_{ref} > 0$)



Inverting Comparator

when $V_i < V_{ref} \Rightarrow V_{out} = +V_{sat}$

when $V_i > V_{ref} \Rightarrow V_{out} = -V_{sat}$

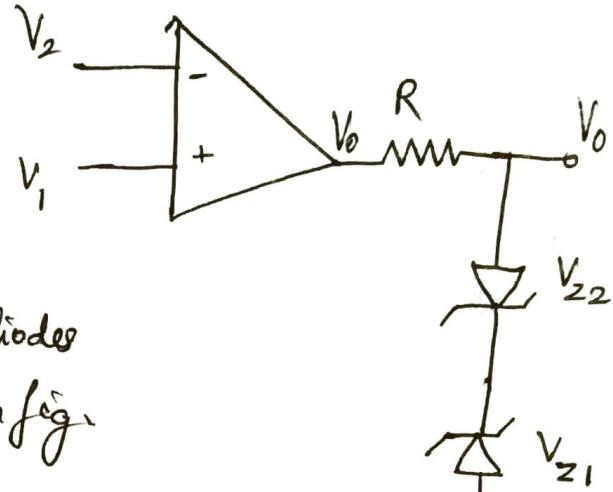


The output voltages are dependent on the power supply voltages.

I/O waveform when $V_{ref} < 0$

O/p voltage of the Comparator
can be made independent of power
Supply voltages by using resistance

R and $\&$ back to back zener diodes
at the opamp output as shown in fig.



Resistance R is chosen so that
Zener diodes operate at the recommended current.

\therefore The o/p voltage will be $V_0 = (V_{21} + V_D)$

$$V_0 = -(V_{22} + V_D)$$

where $V_Z \rightarrow$ Zener voltage

$V_D \rightarrow$ diode voltage. (0.7V in forward bias),

In practical circuits the switching time is noticeable (i.e.
the o/p doesn't change instantaneously).

- Actual waveform will exhibit slant edges as well as delays at the point of input threshold crossing.
- At high frequency o/p switching times are comparable or even longer than the input period.
- ∴ There is an upper limit in the operating frequency of any comparator.

→ Slew rate of the opamp determines the limitation
In M7741 → the internally compensated op-amp is used

as the comparator

Slew rate of M7741 is $0.5\text{V}/\mu\text{s}$ it takes $2 \times 13/0.5 \cong 50\mu\text{s}$
 $(\pm 13\text{V} \text{ for } 13\mu\text{s})$ to swing from one saturation level to the other.

In many applications settle time is too long. To decrease the response we must use uncompensated opamp as 301 for Comparator applications.

Applications of Comparator

- Zero Crossing Detectors
- Window Detector
- Time Marker Generator
- Phase meter.

5.2.1 Applications of Comparator

Some important applications of comparator are:

- Zero crossing detector
- Window detector
- Time marker generator
- Phase meter.

Zero Crossing Detector

The basic comparators of Figs. 5.2 (a) and 5.3 (a) can be used as a zero crossing detector provided that V_{ref} is set to zero. An inverting zero-crossing detector is shown in Fig. 5.4 (a) and the output waveform for a sinusoidal input signal is shown in Fig. 5.4 (b). The circuit is also called a sine to square wave generator.

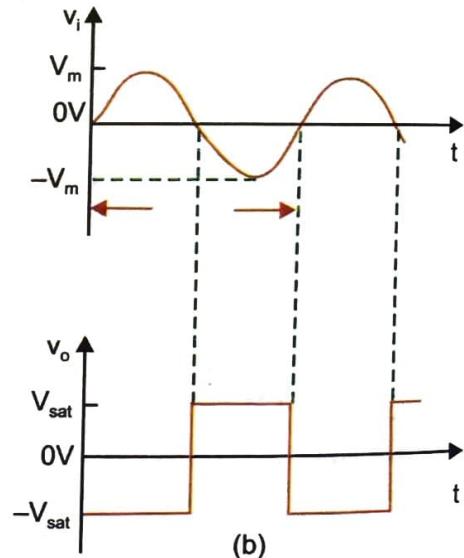
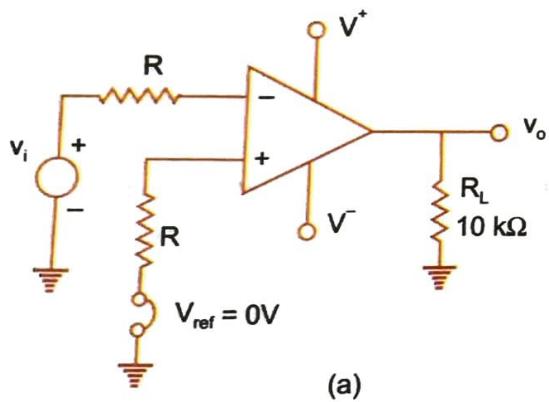


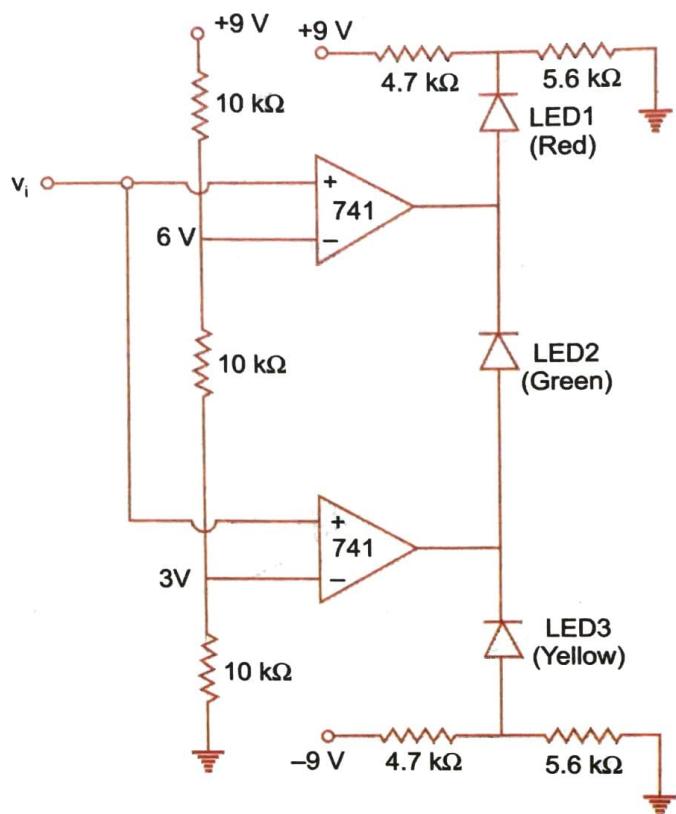
Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

Window Detector

Sometimes one may like to mark the instant at which an unknown input is between two threshold levels. This can be achieved by a circuit called window detector. Figure 5.5 shows a three level detector with indicator circuit. There are three indicators: Yellow (LED 3) for input too low (<3 V), Green (LED 2) for safe input (3 – 6 V) and Red (LED 1) for high input (>6 V). They are turned **on** and **off** as indicated in Table 5.1.

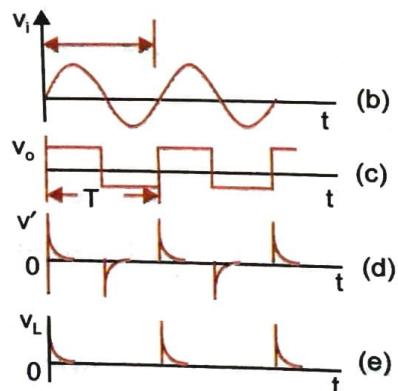
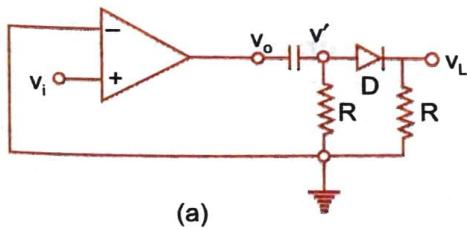
Table 5.1 Three level comparator LED specifications

<i>Input (volts)</i>	<i>Yellow LED 3</i>	<i>Green LED 2</i>	<i>Red LED 1</i>
Less than 3 V	On	Off	Off
Between 3 V and 6 V	Off	On	Off
Greater than 6 V	Off	Off	On

**Fig. 5.5** Three level comparator with LED indicator

Time Marker Generator

The circuit is shown in Fig. 5.6 (a). The output of the zero-crossing detector is differentiated by an RC circuit ($RC \ll T$), so that the voltage v' is a series of positive and negative pulses

**Fig. 5.6** (a) Time marker circuit (b) Input waveform (c) Output v_o
(d) Differentiated output v' (e) Output pulses

as shown in Fig. 5.6 (d). The negative portion is clipped off after passing through the diode D and the waveform v_L is as shown in Fig. 5.6 (e). So, with the help of this circuit, the sinusoid has been converted into a train of positive pulses of spacing T and may be used for triggering the monoshots, SCR, sweep voltage of CRT etc.

Phase Detector

The phase angle between two voltages can also be measured using the circuit of Fig. 5.6 (a). Both voltages are converted into spikes and the time interval between the pulse spikes of one input and that of the other is measured. The time interval is proportional to the phase difference. One can measure phase angles from 0° to 360° with such a circuit.

Example 5.1

- For the comparator shown in Fig. 5.7 (a) plot the transfer curve if the op-amp is an ideal one and $V_{Z1} = V_{Z2} = 9\text{ V}$.
- Repeat part (a) if the open loop gain of op-amp is 50,000.

Solution

- Since $A_{OL} = \infty$, even a small positive or negative voltage at the input drives the output to $\pm V_{sat}$. This causes V_{Z1} or V_{Z2} to break down, giving output voltage $v_o = \pm (V_Z + V_D) = \pm 9.7\text{ V}$. The transfer curve is shown in Fig. 5.7 (b).

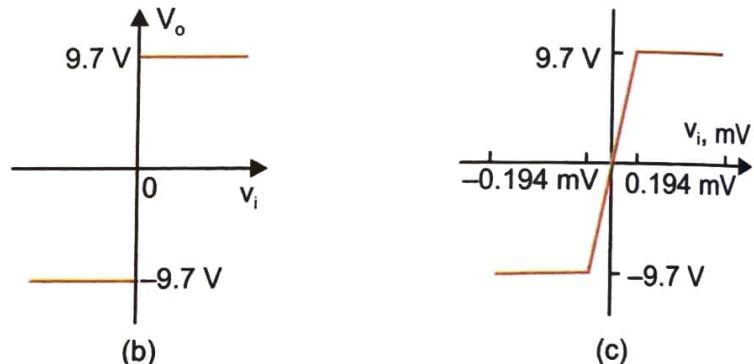
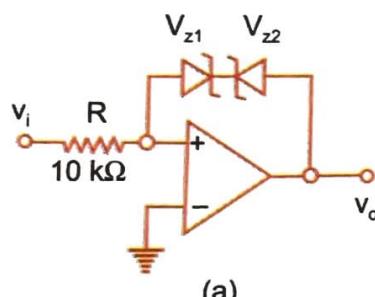


Fig. 5.7 (a) Circuit of Example 5.1 (b) Transfer curve for Example 5.1 (a).
(c) Transfer curve for Example 5.1 (b)

- Now $A_{OL} = 50,000$, so $\Delta v_i = \frac{9.7}{A_{OL}} = 0.194\text{ mV}$. The zeners break down after $\pm 0.194\text{ mV}$

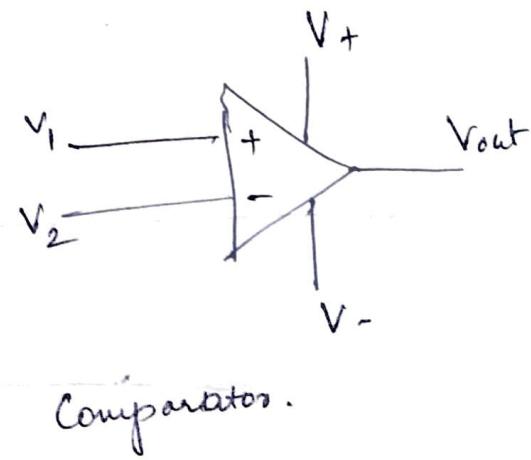
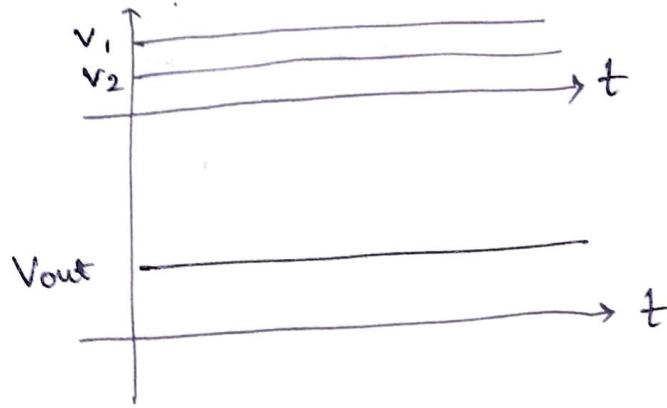
as shown in the transfer curve of Fig. 5.7 (c).

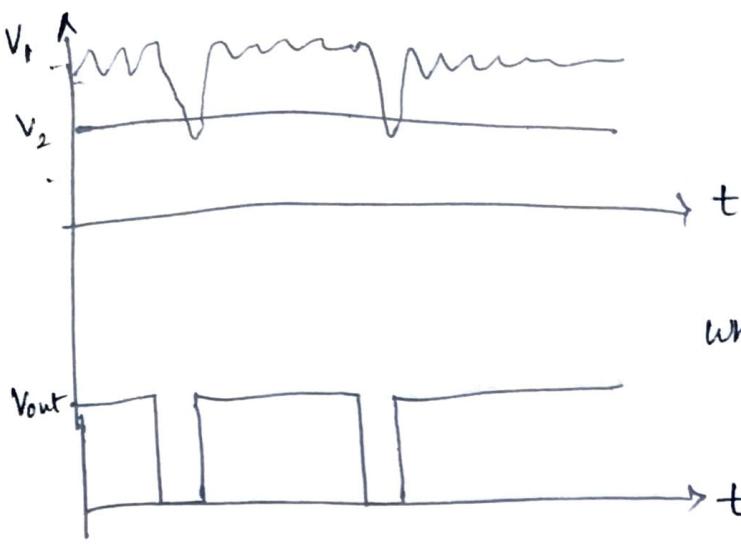
Schmitt Trigger Circuits

Comparators used to compare two input signals. But the limitation is ~~is~~ if I/P is noisy desired output is not obtained. A Schmitt trigger circuit is a fast-operating voltage level detector.

A positive feedback is added to the comparator circuit to obtain Schmitt trigger. Schmitt trigger can be defined as a regenerative comparator; it converts sinusoidal or triangular input into a square wave output. The output of Schmitt trigger swings at upper and lower threshold voltages which are the reference voltages of the input waveforms.

- The input voltage (V_i) triggers the output (V_o) every time it exceeds certain voltage levels.
- The voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}) which are also referred as Upper trigger point (UTP) and lower triggering point (LTP) respectively.
- The Schmitt triggers exhibit a phenomenon called hysteresis. Hysteresis width is the difference between these two threshold voltages (i.e. $V_{UT} - V_{LT}$)



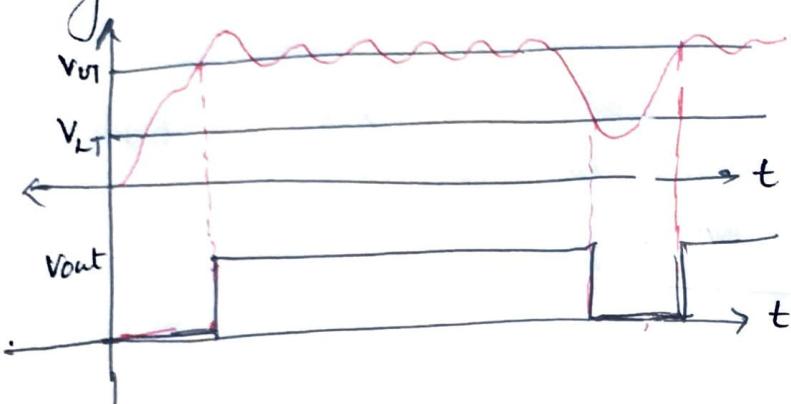


If we observe here V_1 is a noisy signal.

When the noise in V_1 reaches V_2 , the output will be altered / modified. (ie, undesired output will be obtained.)

This can be avoided with Schmitt trigger ckt.

→ We can say that Schmitt trigger is a comparator with hysteresis.



op. of the schmitt trigger.

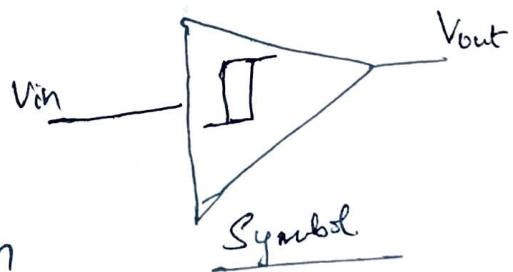
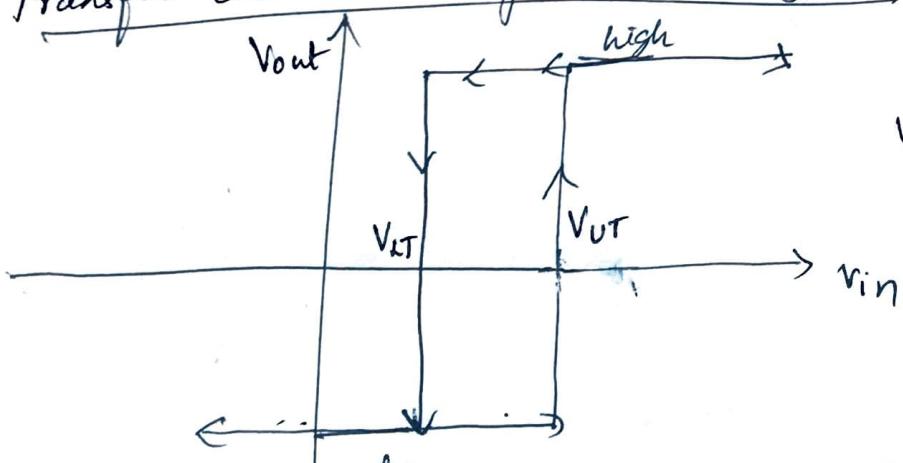
OPR are constant.
Thus introduce noise immunity for the schmitt trigger circuit.

The hysteresis voltage determines the noise immunity of Schmitt trigger circuit.

Four parameters of schmitt trigger are.

⇒ Higher & low OPR voltages, V_{LT} & V_{UT}

Transfer characteristic of Schmitt Trigger



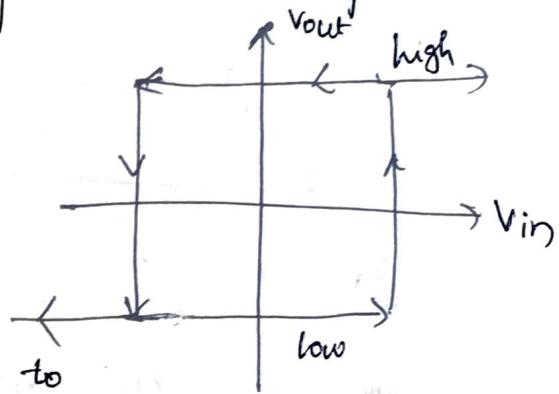
Non Inverting Schmitt trigger Transfer Characteristic

When the input voltage is below threshold the V_o remains at low voltage, when the input V_{in} passes through the V_{UT} the output voltage changes from low to high and it remains high till the input voltage comes below V_{LT} .

As the input V_{in} reaches V_{LT} the off voltage changes from high to low and it remains in low voltage till the I/P increases beyond V_{UT} . This gives the working of a non-inverting schmitt trigger circuit.

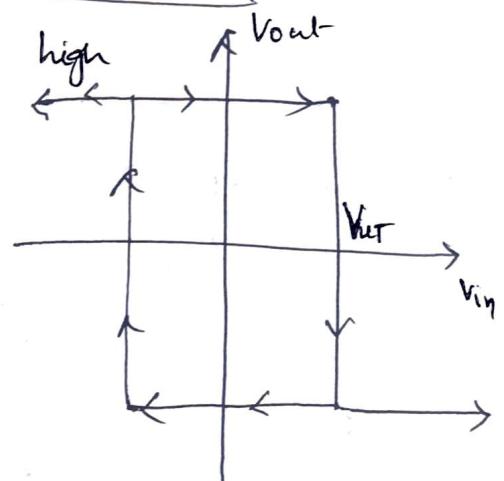
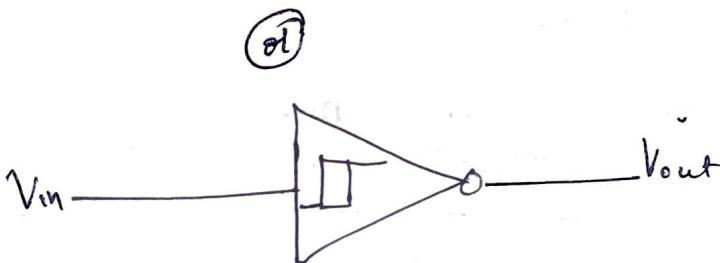
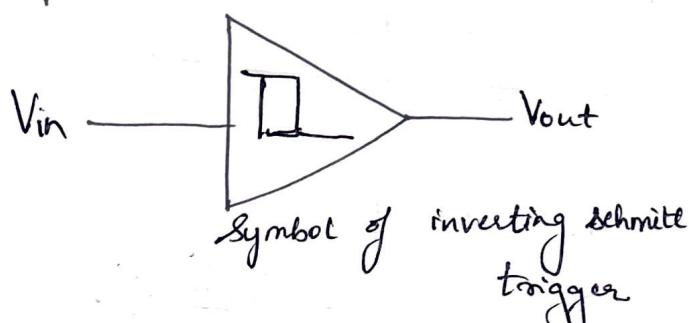
If V_H & V_L are equal and opposite in polarity then the hysteresis curve would be symmetric with respect to y -axis (V_{out} -axis).

The figure shows the hysteresis curve for the same.



By providing the reference voltage to the circuit the curve can be shifted to left or right.

Transfer Characteristics of Inverting Schmitt trigger:-



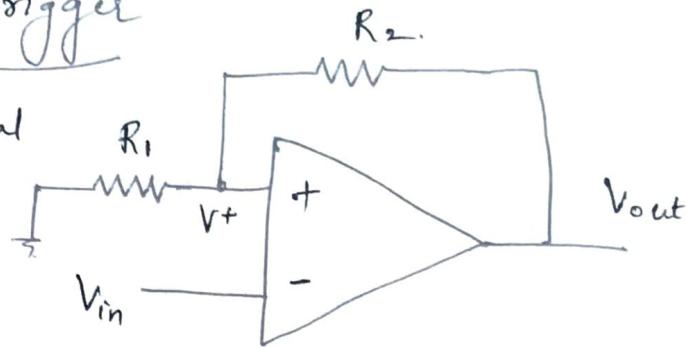
Inverting schmitt trigger hysteresis

Design of inverting Schmitt trigger

V^+ is v/g at non inverting terminal

If $V_{in} > V^+$, $V_{out} = V_L$

If $V_{in} < V^+$ then $V_{out} = V_H$



Applying KCL at V_+

Circuit diagram.

$$\frac{V^+ - 0}{R_1} + \frac{V^+ - V_{out}}{R_2} = 0$$

$$V^+ \left(\frac{1}{R_1} + \frac{1}{R_2} \right) = \frac{V_{out}}{R_2} \Rightarrow V^+ \frac{R_1 + R_2}{R_1 R_2} = \frac{V_{out}}{R_2}$$

$$V^+ = \frac{R_1}{R_1 + R_2} V_{out}$$

—— ①

Initially o/p $= V_H$ Let $V^+ = V_I$

$$V_I = \frac{R_1}{R_1 + R_2} V_H$$

$\therefore V_I \Rightarrow$ Upper threshold voltage $V_T \Rightarrow$

$$V_{UT} = \frac{R_1}{R_1 + R_2} V_H$$

—— ②

When $V_{in} > V_I$, the $V_{out} = V_L$

thus Sub $V_{out} = V_L$ in ①

$$V^+ = \frac{R_1}{R_1 + R_2} \cdot V_L = V_2$$

$V_{in} < V_2 \Rightarrow V_{out} = V_H$, thus we get $V_2 = V_{LT}$

$$V_{LT} = \frac{R_1}{R_1 + R_2} V_L$$

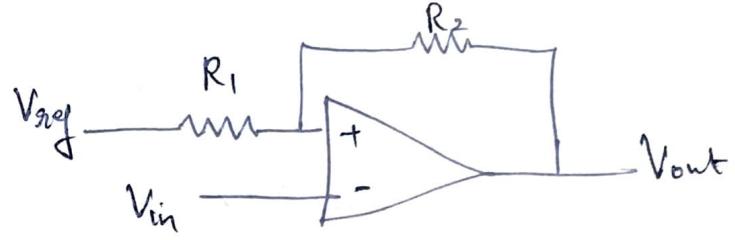
—— ③

$$V_H = V_{UT} - V_{LT}$$

—— ④

Hysteresis
Voltage

By providing V_{ref} the hysteresis curve can be shifted.



Non Inverting Schmitt Trigger

$$V^+ > 0 \Rightarrow V_{out} = V_H$$

$$V^+ < 0 \Rightarrow V_{out} = V_L$$

Applying KCL at node V^+

$$\frac{V^+ - V_{in}}{R_1} + \frac{V^+ - V_{out}}{R_2} = 0$$

$$V^+ \left[\frac{1}{R_1} + \frac{1}{R_2} \right] = \frac{V_{in}}{R_1} + \frac{V_{out}}{R_2}$$

$$\boxed{V^+ = \frac{R_2}{R_1+R_2} V_{in} + \frac{R_1}{R_1+R_2} V_{out}} \quad (1)$$

Let us assume op-amp output is low voltage V_L

$$V_1 = \frac{R_2}{R_1+R_2} V_{in} + \frac{R_1}{R_1+R_2} V_L$$

If $V_1 > 0 \Rightarrow V_{out} = V_H$

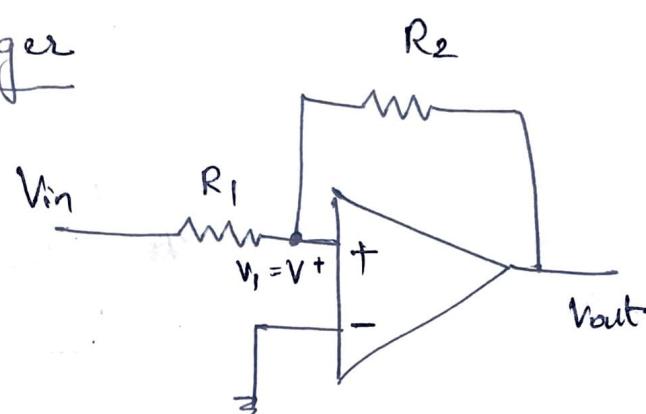
$$\frac{R_2}{R_1+R_2} V_{in} > -V_L \frac{R_1}{R_1+R_2}$$

$$\boxed{V_{in} > -\frac{R_1}{R_2} V_L} \rightarrow \text{The op-amp o/p becomes high i.e. } V_H$$

$$\therefore \boxed{V_{ur} = -\frac{R_1}{R_2} V_L} \quad (2)$$

If $V_{out} = V_H, V^+ = V_2$

$$V_2 = \frac{R_2}{R_1+R_2} V_{in} + \frac{R_1}{R_1+R_2} V_H$$



when $V_2 < 0 \Rightarrow V_{out} = V_L$

$$\frac{R_2}{R_1+R_2} > V_{in} < \frac{-R_1 V_H}{R_1+R_2}$$

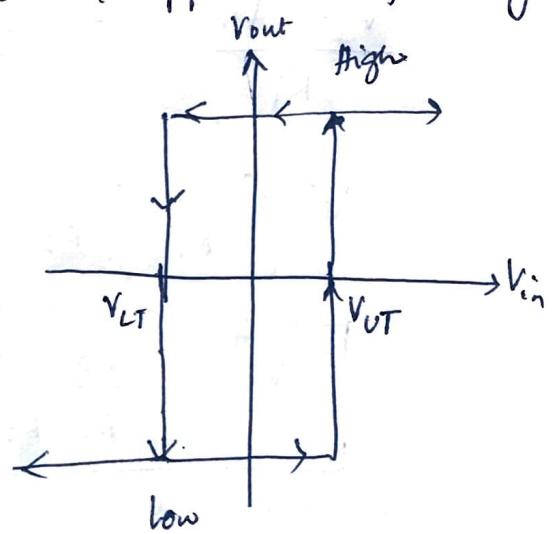
$$V_{in} < \frac{-R_1}{R_2} V_H$$

o/p changes to low voltage

$$V_{LT} = -\frac{R_1}{R_2} V_H$$

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Assuming V_H & V_L are equal & opposite in polarity.



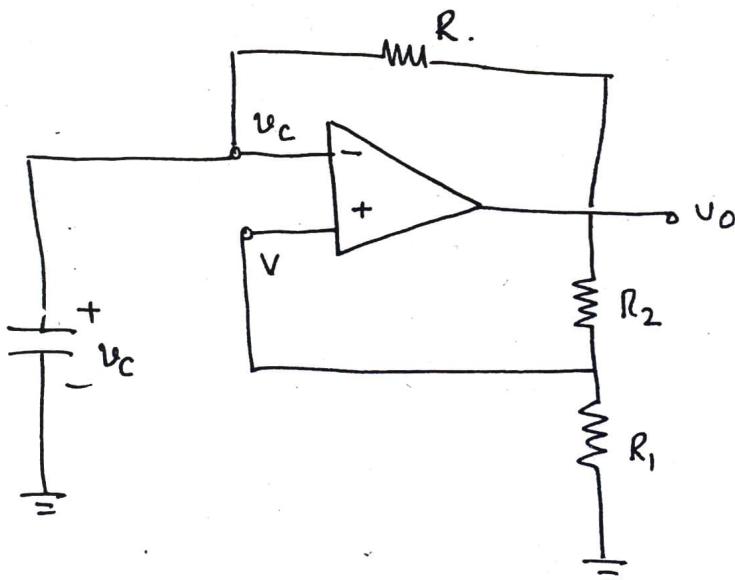
Wave form Generators

- Square wave Generator — AStable multivibrator
- triangle wave Generator
- pulse Generator — Mono shot — MonoStable multivibrator.

Square wave Generator / AStable multivibrator /

Free running oscillator

- Contains \swarrow OP-Amp with the FB
Timing Ckt — RC. nlw.



Fig(A)

$R_1 = R_2$: +ve FB = nlw

R-C : Timing nlw.

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• Due to the. Fls clc is unstable.

$\therefore V_0$ is at $+V_{sat}$ or $-V_{sat}$.

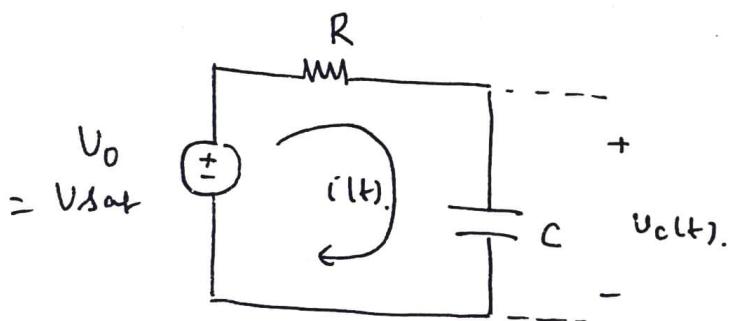
Let $V_0 = V_{sat}$.

Using Vg division rule

$$V = \frac{V_{sat} R_1}{R_1 + R_2} = \beta V_{sat}$$

$$\beta = \frac{R_1}{R_1 + R_2} = \text{Fls fact.}$$

Capacitor gets charged towards V_{sat} via R .



When Cap. vs $V_c(t)$ became equal to, $V = \beta V_{sat}$

and exceeds βV_{sat} ,

$$V_c(t) > V$$

Opf switches to $-V_{sat}$ (Compensate action)

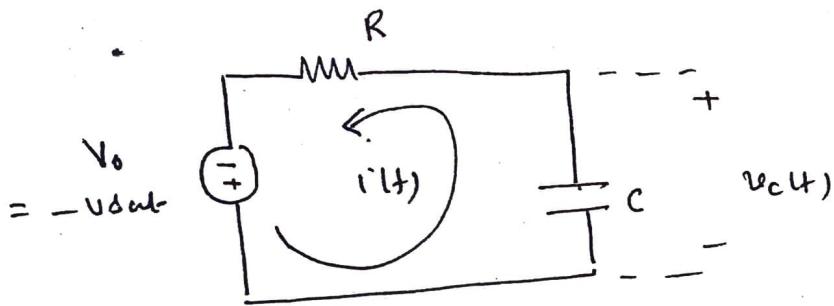
Now $V_0 = -V_{sat}$

$$\& V = -\beta V_{sat}$$

Now Capacitor charges towards $-V_{sat}$

(02)

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When $V_o = -V_{sat}$ became equal to, $V = -\beta V_{sat}$
and goes below $-V_{sat}$

$$V_c(t) < V$$

Op-amp switches to $+V_{sat}$

$$\text{Now } V_o = +V_{sat}$$

$$V = \beta V_{sat}$$

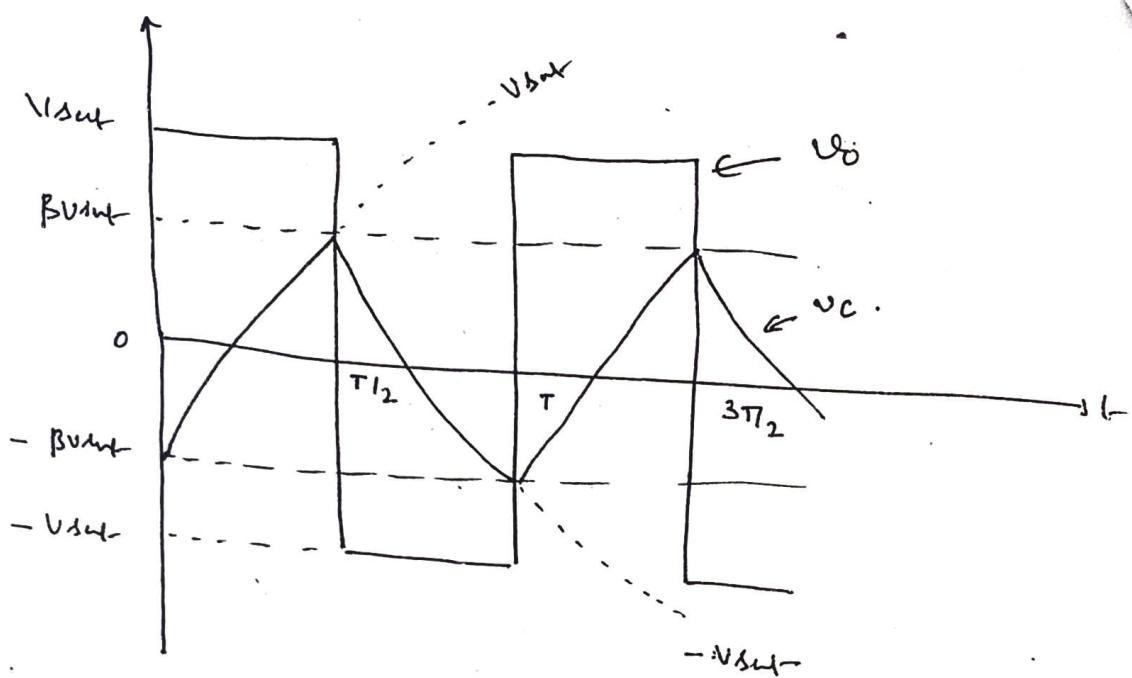
Now the Cap gets charged towards V_{sat} cycle of opw
as before and the same repeat.

Note that,

$$V_o \text{ switches b/w } \pm V_{sat}$$

$$V_c(t) \text{ charged b/w } \pm \beta V_{sat}.$$

wave forms of v_o and v_c .



Expression for frequency of oscillations.

Consider the interval $0 < t < T/2$

Cap is getting charged via R toward $V_{o\text{max}}$.
The general eqn is

$$v_c(t) = v_f + (v_i - v_f) e^{-t/RC} \quad (A)$$

v_f = Final v_o to which cap can charge
if allowed to charge.

v_i = Initial v_o in cap.
From fig

$$v_i = -BV_{d\text{max}}$$

$$v_f = V_{o\text{max}}$$

Substitut in τ_{sw} (A)

$$V_C(t) = V_{SUT} + (-\beta V_{SUT} - V_{SUT}) e^{t/\tau_{RC}} \quad - (K)$$

$$\text{Also at } t = \tau_{T2}, \quad V_C(t) = \beta V_{SUT}$$

$$\beta V_{SUT} = V_{SUT} - (1+\beta) V_{SUT} e^{-\tau_{T2} \tau_{RC}}$$

$$\beta = 1 - (1+\beta) e^{-\tau_{T2} \tau_{RC}}$$

$$(1+\beta) e^{-\tau_{T2} \tau_{RC}} = (1-\beta)$$

$$e^{-\tau_{T2} \tau_{RC}} = \frac{1-\beta}{1+\beta}$$

$$e^{\tau_{T2} \tau_{RC}} = \frac{1+\beta}{1-\beta}$$

$$\ln e^x = x$$

$$\ln(e^{\tau_{T2} \tau_{RC}}) = \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\frac{\tau}{2\tau_{RC}} = \ln\left(\frac{1+\beta}{1-\beta}\right)$$

$$\frac{\tau}{2} = R_C \ln\left(\frac{1+\beta}{1-\beta}\right) \quad (B-1)$$

$$\tau = 2 R_C \ln\left(\frac{1+\beta}{1-\beta}\right) \quad - (C)$$

$$f = \frac{1}{\tau} = \frac{1}{2 R_C \ln\left(\frac{1+\beta}{1-\beta}\right)} \quad - (D)$$

If $\beta = 0.5$

$$\ln\left(\frac{1+\beta}{1-\beta}\right) = \ln(3) \approx 1$$

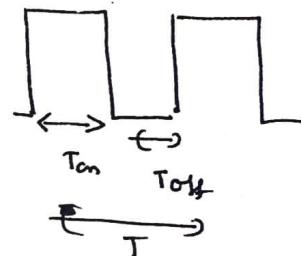
$$\therefore T = 1.2RC \quad \text{--- (E)}$$

$$f = 1/2RC \quad \text{--- (F)}$$

The wave form generated is a symmetrical square wave since charge time = discharge time.
 (T_{on}) (T_{off})

Duty cycle

$$D = \frac{T_{on}}{T}$$



$$\text{In this case, } T_{on} = T_{off} = \frac{\pi}{2}$$

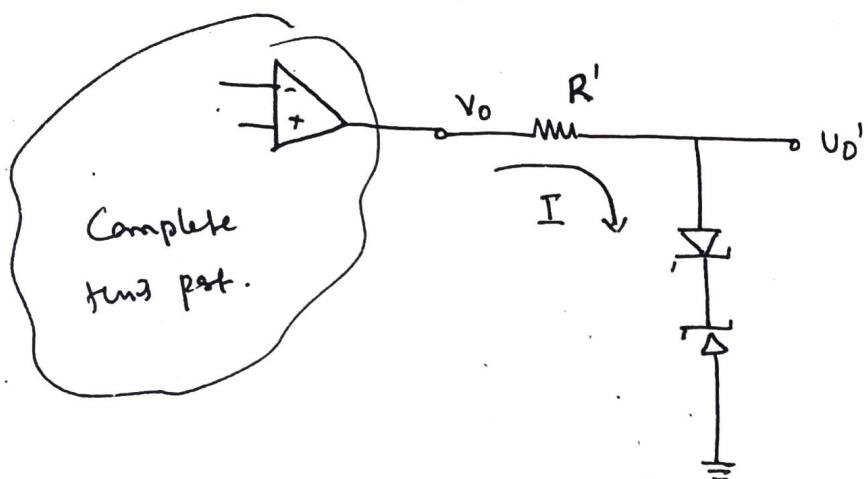
$$\therefore D = \frac{\pi/2}{T} = 0.5 \approx 50\%$$

Why name 1) A stable: Both states of op-amp if
 $\pm V_{out}$ are unstable.

2) Free runnng: Op-amp switches between $\pm V_{out}$ without any external trigger.

Op Amp Amplitude limiter

Ref Fig (A)



$$\text{Then } V_o = V_{\text{sat}}$$

upper diode : forward biased. (V_f) ; $V_f = 0.7V$

lower diode : Reverse break down. (V_z)

$$\therefore V_o' = (V_f + V_z)$$

$$\text{Similar when } V_o = -V_{\text{sat}}$$

$$V_o' = - (V_f + V_z)$$

$$\therefore V_o = \pm V_{\text{sat}} \Rightarrow V_o' = \pm (V_f + V_z)$$

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$$I = \frac{V_0 - V_0'}{R_1}$$

$$\text{i.e. } I = \frac{V_{Sut} - (V_f + V_Z)}{R_1} \quad \text{--- (G)}$$

$$I > I_{Zt}$$

$$I < I_{Zmax}$$

$$\Rightarrow I_{Zt} < I < I_{Zmax}$$

Atlo $I < I_{0(\text{max}) \text{ or } \text{dyn.}} (= 20\text{mA})$

I_{Zt} : Min. Current required in Zener
to initiate break down phenomenon.

I_{Zmax} : Max. Allowable Zener Current.

$$I_{Zmax} = \frac{P_{Zmax}}{V_Z}$$

P_{Zmax} : Allowable power dissipation in Zener.

Illustration

$$\text{Let } V_{CC} = 15\text{V} \Rightarrow V_{int} = 0.9V_{CC} = 13.5\text{V}$$

$$V_Z = 5.1\text{V}$$

$$P_{Zmax} = 0.5\text{W}$$

$$I_{Zt} = 5\text{mA}$$

$$I_{2\max} = \frac{P_{2\max}}{V_Z} = \frac{0.5W}{5.1V} \approx 100mA$$

$$\Rightarrow 5mA < I < 100mA$$

Choose $I = 10mA$

$$R' = \frac{V_{out} - (V_T + V_Z)}{I}$$

$$= \frac{13.5V - (0.7 + 5.1)V}{10mA}$$

$$= \dots$$

Problem

- ① Design a Sq. wave generator using op-Amp with the following specifications.

$$f = 2kHz$$

$$\text{Op amp amplitude: } \pm \frac{6V}{\cancel{5.8V}}$$

$$\pm V_{cc} : \pm 15V$$

Duty cycle: 50%

Feedback factor $\beta: 0.5$

Ans

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Since $\beta = 0.5$

$$T = \frac{1}{f} = 2RC$$

choose $C = 0.1 \text{ HF}$

Find R.

$$\beta = \frac{R_1}{R_1 + R_2} = 0.5$$

$$\Rightarrow R_1 = R_2$$

choose $R_1 = R_2 = 10 \text{ k}\Omega$

$$V_o' = \pm 6V = \pm (V_f + V_z)$$

$$V_f + V_z = 6V$$

$$V_z = 5.3V$$

Select 5.1V Zener with

$$P_{Z \max} = 0.5W$$

Calculated R' using Eqn (a).

Draw the AC circuit and incorporate Component Values.

(2)

Repeat previous problem with $\beta = 0.75$
Other data remain unchanged.

(06)

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Hint: Since $\beta \neq 0.5$

$$T = \frac{1}{f} = 2RC \ln \left(\frac{1+\beta}{1-\beta} \right)$$

$$\beta = \frac{3}{4} = \frac{R_1}{R_1 + R_2}$$

Assume R_1 , Find R_2

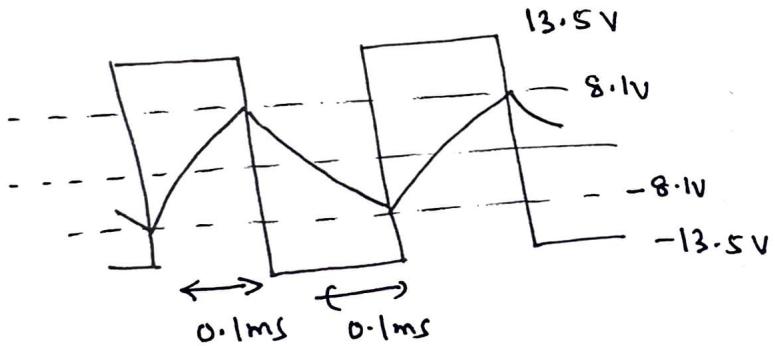
Take $C = 0.1 \mu F$

Find R .

Amplitude limited clc designs

is same as before.

(3)



Take $V_{CC} = 15V$

op-amp Amplitude to be limited to $\pm 6V$.

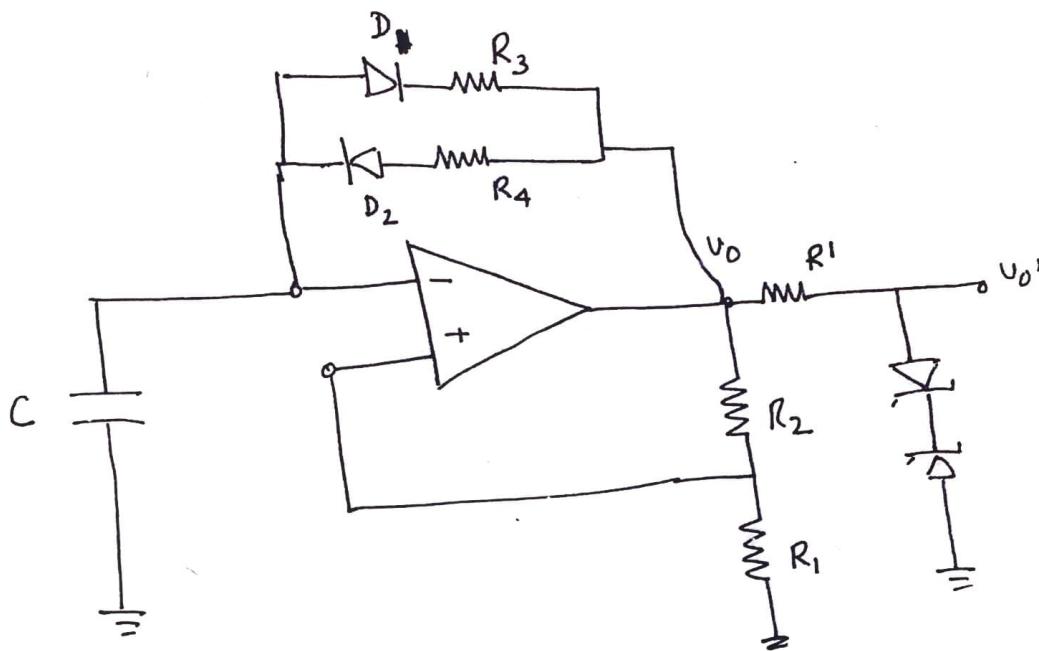
Hint: $T/2 = 0.1ms \Rightarrow T = 0.2ms$

$$f = 5 \text{ kHz}$$

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$$\beta_{V8\text{mL}} = 8.1V$$

$$\beta = \frac{8.1V}{13.5V} = 0.6$$



When $V_0 = V_{sat}$

D_2 conducts. charging of cap takes place via
 D_2 and R_3 .

Ref eqn (B-1)

Replace TI_2 by Ton.

$$Ton = R_4 C \ln \left(\frac{1+\beta}{1-\beta} \right) - (H)$$

When $V_0 = -V_{sat}$

D_1 conducts. charging of cap takes place via
 $D_1 \& R_3$

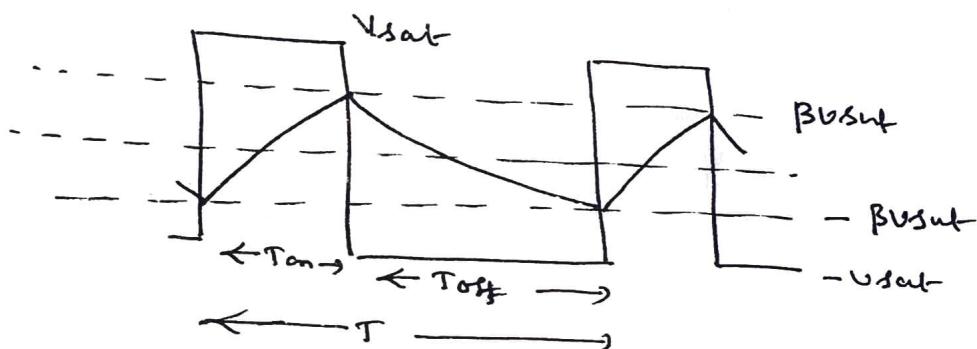
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$$T_{off} = R_3 C \ln \left(\frac{1+\beta}{1-\beta} \right) - (I)$$

$$T = T_{on} + T_{off} = (R_3 + R_4) C \ln \left(\frac{1+\beta}{1-\beta} \right) - (J)$$

$$f = 1/T$$

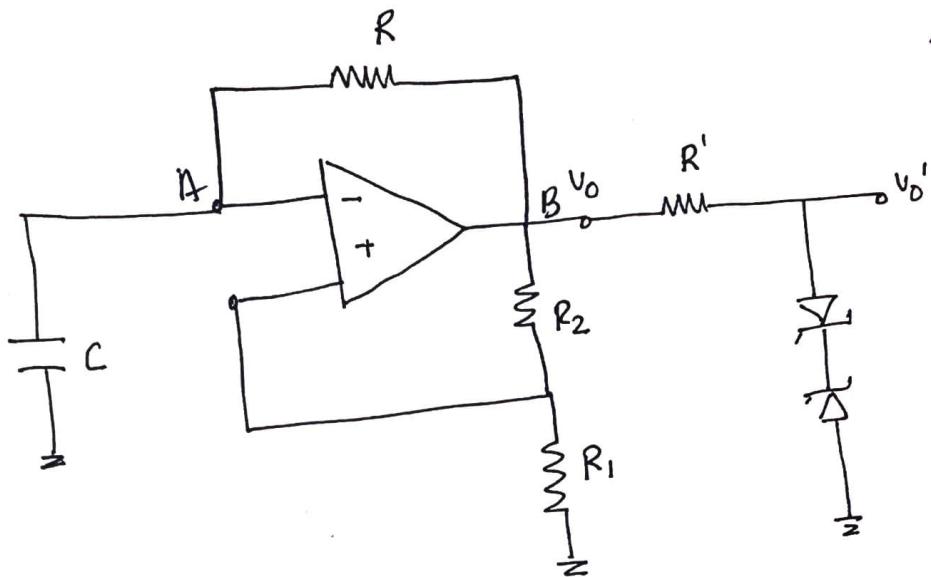
Duty cycle = $D = \frac{T_{on}}{T} = \frac{R_4}{R_3 + R_4} - (K)$



Note:

Students are advised to derive eqns
(H) & (J) ~~using the~~ in same way
as eqns (B-1) & (C) are derived.

Sq. wave Generator



$$T_{on} = T_{off} = \frac{I}{2} = R C \ln \left[\frac{1+\beta}{1-\beta} \right]$$

$$T = 2 R C \ln \left[\frac{1+\beta}{1-\beta} \right]$$

$$\beta = \frac{R_1}{R_1 + R_2}$$

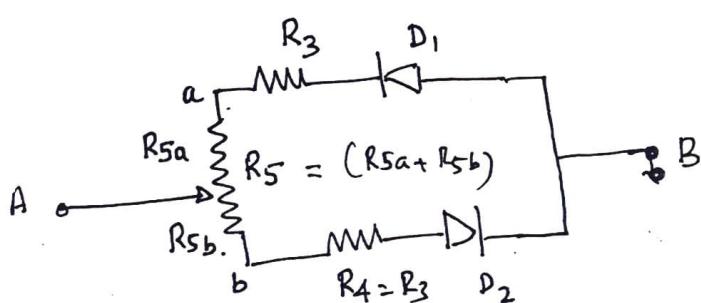
If $\beta = 0.5$, $\ln \left[\frac{1+\beta}{1-\beta} \right] \approx 1$

$$T_{on} = T_{off} = RC$$

$$T = 2RC.$$

Duty cycle 50%.

Duty cycle Adjustment at constant frequency



$$T_m = (R_3 + R_{5a}) C \quad (\beta=0.5)$$

$$T_{off} = (R_3 + R_{5b}) C$$

$$T = (2R_3 + R_5) C \quad (\because R_5 = R_{5a} + R_{5b})$$

$$D = \frac{T_m}{T} = \frac{R_3 + R_{5a}}{2R_3 + R_5}$$

When the wiper is at a

$$R_{5a} = 0$$

$$D = \frac{R_3}{2R_3 + R_5} \rightarrow \text{Minimum.}$$

When the wiper is at b

$$R_{5b} = R_5$$

$$D = \frac{R_3 + R_5}{2R_3 + R_5} \rightarrow \text{Maxin.}$$

When the wiper is at the Centre

$$R_{5a} = R_{5b}/2$$

$$D = \frac{R_3 + R_{5b}/2}{2R_3 + R_5} = 0.5.$$

Duty cycle can be varied from min to max at a constant frequency.

problem

1. Sq. wave Generator

$$f = 2 \text{ kHz}$$

$$D = 0.75$$

$$\beta = 0.5$$

$$V_{CC} = 15 \text{ V}$$

old Amplitude: $\pm 6 \text{ V}$

Hint

$$\beta = \frac{R_1}{R_1 + R_2} = 0.5$$

$$\Rightarrow R_1 = R_2 = 10 \text{ k}\Omega$$

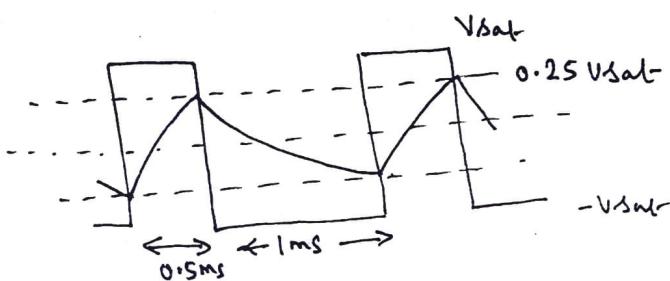
$$D = 3/4 = \frac{R_4}{R_3 + R_4}$$

Assume R_4 and find R_3 .

Find C from $T_{QW}(J)$

Draw the C_{di} and incorporate Compt values.

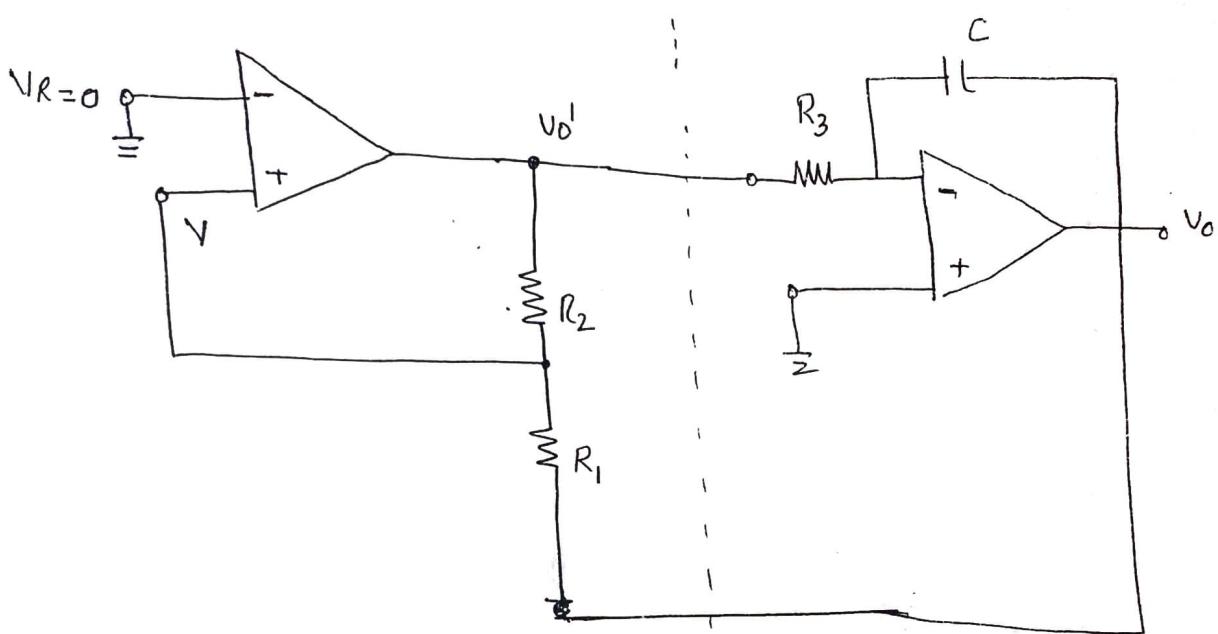
2.



$$V_{CC} = 15 \text{ V}$$

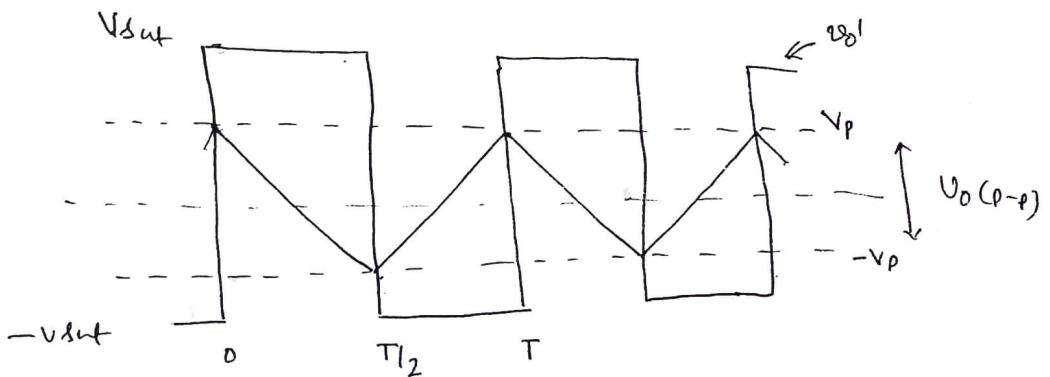
Triangular waveform Generator

Square wave $\xrightarrow{\text{Integrate}}$ Triangular wave.



Non-inverting
Schmitt trigger
with $V_L = 0$.

Integrator.



$$\text{Then } V_0' = V_{\text{out}}$$

$$V_0 = - \frac{1}{R_3 C} \int V_{\text{out}} dt = - \frac{V_{\text{out}}}{R_3 C} t$$

\Rightarrow negative going ramp.

$$\text{When } V_0' = -V_{\text{sat}}$$

V_0 is a +ve going ramp.

V is compared with $V_R = 0$

Applying superposition principle

$$V = \frac{V_0' R_1}{R_1 + n_2} \Big|_{V_0=0} + \frac{V_0 n_2}{R_1 + n_2} \Big|_{V_0'=0} \quad \dots (1)$$

$$\text{When } V_0' = V_{\text{sat}}$$

V_0 is a -ve going ramp.

$$V \rightarrow 0 \quad \text{When } V_0 \rightarrow -V_p.$$

$$\therefore 0 = \frac{V_{\text{sat}} R_1}{R_1 + n_2} + \frac{(-V_p) n_2}{R_1 + n_2}$$

$$V_p = \frac{V_{\text{sat}} R_1}{n_2} \quad \dots (2)$$

Consider the interval $0 < t < T_{l_2}$

$$-\frac{1}{R_3 C} \int_0^{T_{l_2}} V_{\text{sat}} dt = \Delta V_0 = \text{change in } V_0$$

$$-\frac{V_{\text{sat}}}{R_3 C} (t)_{0}^{T_{l_2}} = -V_p (-V_p)$$

$$-\frac{V_{\text{sat}} T}{2 R_3 C} = -2 V_p$$

$$V_p = \frac{V_{\text{sat}}}{2 f R_3 C} \quad \dots (3)$$

Here $f = 0.5$

Combining (2) & (3)

$$\frac{V_{out} M}{\pi_2} = \frac{V_{out}}{\frac{4 + \pi_3 C}{R_2 / R_1}} \Rightarrow 4 + \pi_2 \pi_3 C \approx \pi_2$$
$$f = \frac{R_2 / R_1}{4 \pi_3 C} - (4)$$

$$f = \frac{R_2}{4 R_1 R_3 C}$$

Example Design a triangular wave generator

$$f = 2 \text{ kHz}$$

$$V_o(1-p) = 6V$$

$$V_{CC} = 15V$$

$$2V_p = 6V \Rightarrow V_p = 3V$$

$$V_p = \frac{V_{out} M}{\pi_2}$$

$$3V = 13.5 \times \frac{R_1}{\pi_2}$$

Assume R_1 & Find π_2

$$f = \frac{R_2 / R_1}{4 \pi_3 C}$$

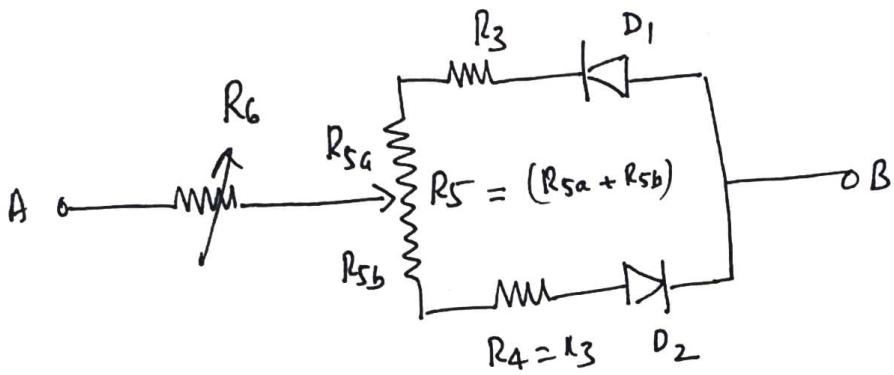
$$\text{choose } C = 0.1 \mu F$$

Find π_3 .

Additivity

Cine out ask them to find

and duty cycle.
frequency adjustment



$$T_{on} = (R_3 + R_{5a} + R_6) C$$

$$T_{off} = (R_3 + R_{5b} + R_6) C$$

$$T = (2R_3 + 2R_6 + R_5) C$$

$$D = \frac{R_3 + R_{5a} + R_6}{2R_3 + 2R_6 + R_5}$$

By adjusting R_6 , frequency of oscillations

can be changed.

problem

Design a square wave generator using OP-amp with the following specifications.

OP-amp $f: 200\text{Hz}$ to 2kHz

D: 20% to 80% .

$\pm V_{CC}: \pm 15\text{V}$

Output amplitude: $\pm 6\text{V}$.

Procedure

frequency is max. when $R_6 = 0$.

with $R_6 = 0$

$$T = (2R_3 + R_5)C \quad [\beta = 0.5 \text{ i.e. } R_4 = k_2]$$

$$f = 1/T = 2000 \text{ Hz}$$

$$2R_3 + R_5 = \frac{T}{C} = \frac{1}{f_C} =$$

$$\text{Take } C = 0.01 \mu\text{F}$$

$$2R_3 + R_5 = 50 \text{ k}\Omega \quad - \textcircled{1}$$

$$D = \frac{R_3 + R_{5a}}{2R_3 + R_5}$$

D is minimum when $R_{5a} = 0$ i.e. $R_{5b} = R_5$ -

$$0.2 = \frac{R_3}{2R_3 + R_5}$$

$$\Rightarrow R_5 = 3R_3 \quad - \textcircled{2}$$

put $\textcircled{2}$ in $\textcircled{1}$

$$2R_3 + 3R_3 = 50 \text{ k}\Omega$$

$$R_3 = 10 \text{ k}\Omega$$

$$R_5 = 30 \text{ k}\Omega$$

(05)

frequency is min when R_6 is fully included.

$$T = \frac{1}{f} = (2R_3 + 2R_6 + R_5)C = \frac{1}{200}$$

$$\Rightarrow 2R_3 + 2R_6 + R_5 = 500\text{k}\Omega$$

$$2R_6 = 500\text{k}\Omega - 2R_3 - R_5 = 450\text{k}\Omega$$

$$\boxed{R_6 = 225\text{k}\Omega}$$

Design amplitude limiting circuit.

Log and Antilog Amplifier

- Antilog ~~and~~ computations may require functions such as $\ln x$, $\log x$ or $\sinh x$. These can be performed continuously with log-amps.
- We can obtain direct dB display on digital voltmeter and spectrum analyzer
- these functions can be performed by log-amplifiers
- Log amp can be used to compress the dynamic range of a signal.

Log Amplifier

Log amplifier gives an output voltage which is proportional to the natural log of the input voltage. Fig (6) shows the circuit of fundamental log-Amp circuit.

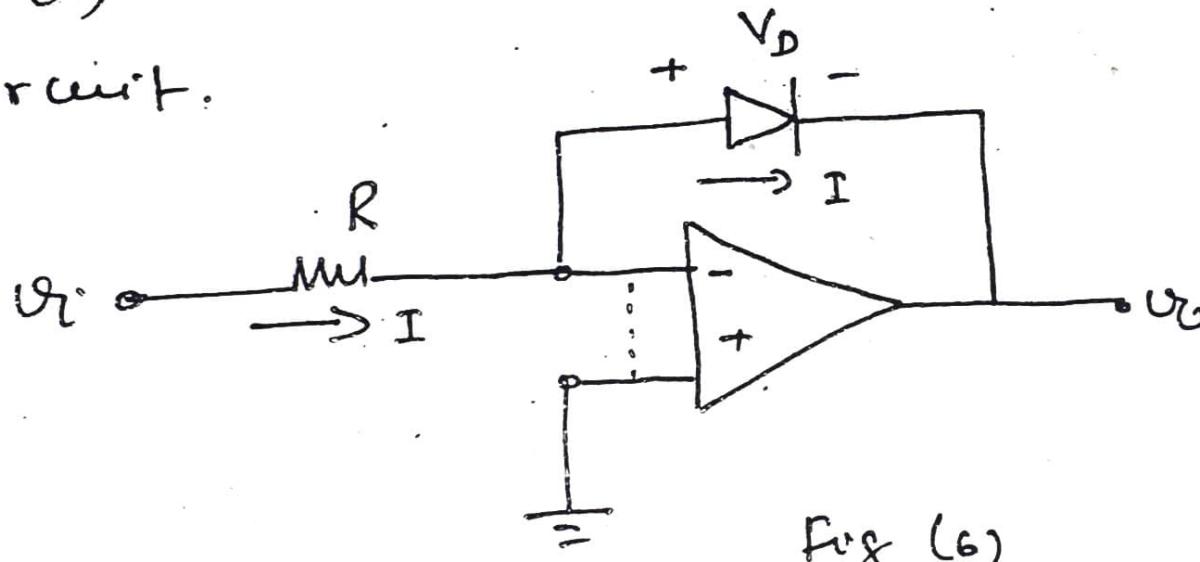


Fig (6)

$$I = \frac{V_i}{R} \quad \text{--- (1)}$$

(B) (2)

$$\text{Also, } I = I_s [e^{qV_D/kT} - 1] \quad \text{--- (2)}$$

$$\text{and } V_0 = -V_D \quad \text{--- (3)}$$

Combining (2) and (3) we have

$$I_s = I_s [e^{-qV_0/kT} - 1]$$

$$\frac{I}{I_s} = e^{-qV_0/kT} - 1$$

$$e^{-qV_0/kT} = \frac{I}{I_s} + 1 \approx \frac{I}{I_s} \quad [\text{Since } I_s \ll I]$$

$$\ln [e^{-qV_0/kT}] = \ln [I/I_s]$$

Substituting for I , from equation (1) we have

$$-\frac{qV_0}{kT} = \ln \left[\frac{V_i}{R I_s} \right]$$

$$V_0 = -\frac{kT}{q} \ln \left[\frac{V_i}{R I_s} \right]$$

Taking $V_{ref} = R I_s$ we have

$$V_0 = -\frac{kT}{q} \ln \left[\frac{V_i}{V_{ref}} \right] \quad \text{--- (4)}$$

Note that, V_0 is proportional to the natural log of $\frac{V_i}{V_{ref}}$

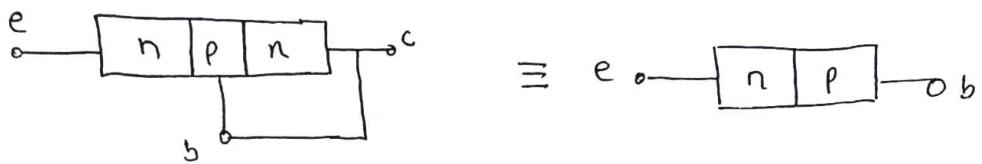
Draw backs of basic log Amplifier (Continued)

In the basic log Amplifier

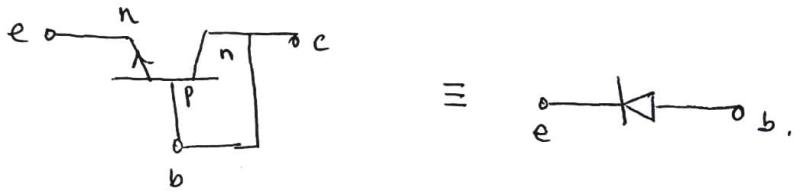
$$V_o = -V_T \ln(V_i/R_{I_s})$$

V_T and I_s are both temperature dependent hence V_o

Note



In a transistor if base is shorted to collector it works as a diode.



The basic log amplifier with diode implemented using transistors is shown in Fig (1).

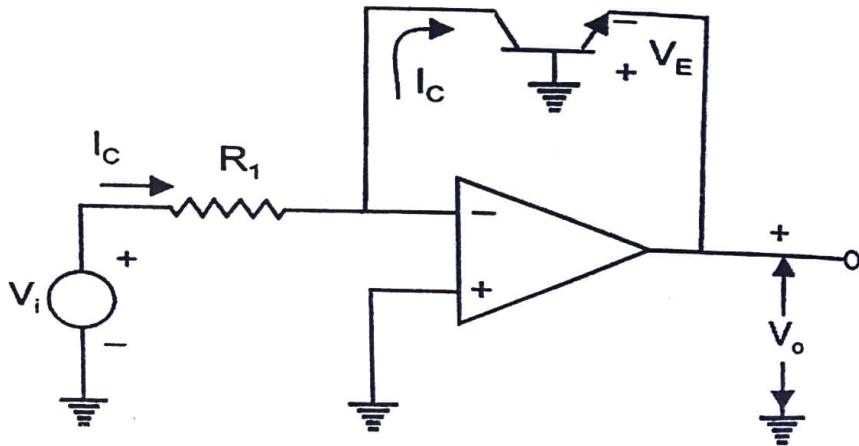


Fig (1)

02

Log Amplifier with Compensation for Saturation Current and Temperature

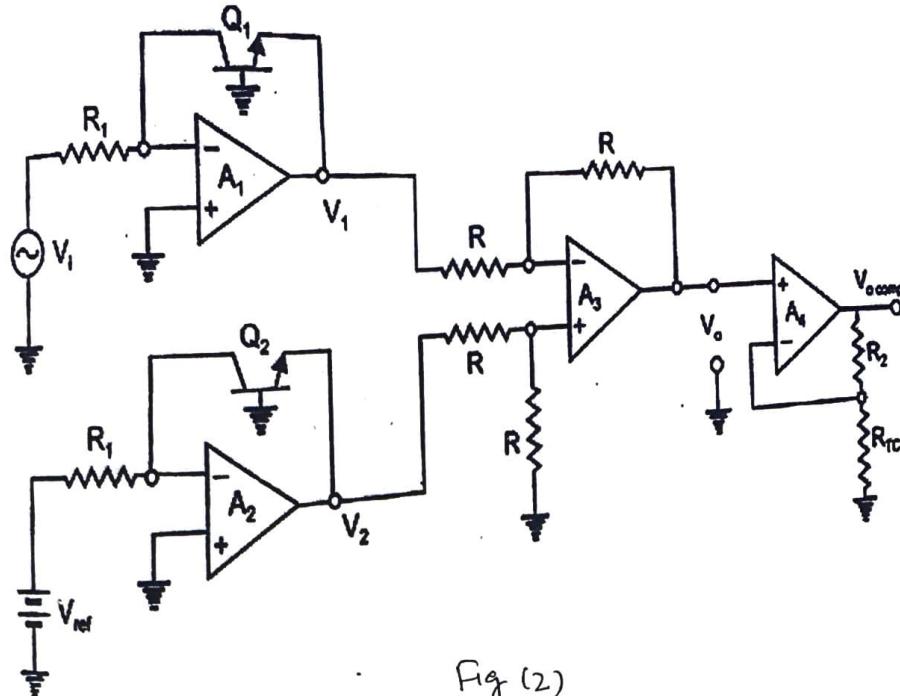


Fig (2)

$\therefore A_1$ and A_2 are basic log amplifiers with inputs V_i and V_{ref} respectively

Assuming Q_1 and Q_2 to be identical, we have

$$I_{S1} = I_{S2} = I_S.$$

$$V_1 = -V_T \ln \left[\frac{V_i}{R_1 I_S} \right]$$

$$V_2 = -V_T \ln \left[\frac{V_{ref}}{R_1 I_S} \right]$$

$\therefore A_3$ is configured as Subtractor.

$$\therefore V_o = V_2 - V_1$$

$$V_o = -V_T \ln \left[\frac{V_{ref}}{R_1 I_S} \right] + V_T \ln \left[\frac{V_i}{R_1 I_S} \right]$$

$$V_o = V_T \ln \left\{ \frac{V_i / R_1 I_S}{V_{ref} / R_1 I_S} \right\}$$

$$V_o = V_T \ln \left[\frac{V_i}{V_{ref}} \right]$$

A₄ is configured as non-inverting amplifier.

$$V_o (\text{comp}) = \left[1 + \frac{R_2}{R_{TC}} \right] V_o$$

$$V_o (\text{comp}) = \left[1 + \frac{R_2}{R_{TC}} \right] V_T \ln \left[\frac{V_i}{V_{ref}} \right]$$

R_{TC} is a sensistor which has ^{Coefficient of} \propto temperature.

Thus the ratio $\left[1 + \frac{R_2}{R_{TC}} \right] V_T$ remains constant even when temperature varies.

A Log Amplifier

Fig (7) shows the circuit of A Log amplifier.

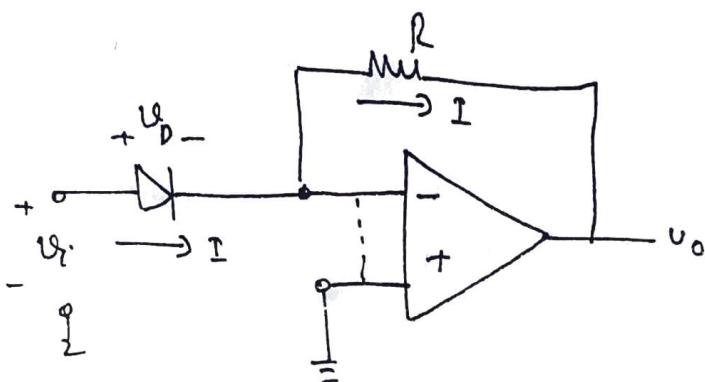


Fig (7)

$$v_i = v_D \quad \text{--- (1)}$$

$$I = -v_o/R \quad \text{--- (2)}$$

$$I = I_s \left[e^{\frac{qv_D}{kT}} - 1 \right]$$

$$\frac{I}{I_s} \approx e^{\frac{qv_i}{kT}}$$

$$-\frac{v_o}{R I_s} = e^{\frac{qv_i}{kT}}$$

$$v_o = -R I_s e^{\frac{qv_i}{kT}} \quad \text{--- (3)}$$

From Eq (3) we find that v_o is proportional to the ALog of v_i .

Antilog Amplifier

The fig. ③ shows the antilog amp. ~~with~~ The input V_i for the antilog-amp is fed into the compensating voltage divider R_2 and R_{TC} and then to the base of Q_2 .
 $I_{C_1} = I_s e^{\frac{V_{BE_1}}{V_T}}$ (Diode current eqn)

$$\Rightarrow V_{BE_1} = V_T \ln \left(\frac{I_{C_1}}{I_s} \right)$$

$$\text{Similarly } V_{BE_2} = V_T \ln \left(\frac{I_{C_2}}{I_s} \right)$$

$$I_{C_1} = V_o / R_1 \quad \therefore V_{BE_1} = V_T \ln \left(\frac{V_o}{R_1 I_s} \right)$$

$$I_{C_2} = V_{ref} / R_2 \quad \& \quad V_{BE_2} = V_T \ln \left(\frac{V_{ref}}{R_2 I_s} \right)$$

The output V_o of the anti-log amp is feedback to the inverting input of A through the resistor R_1

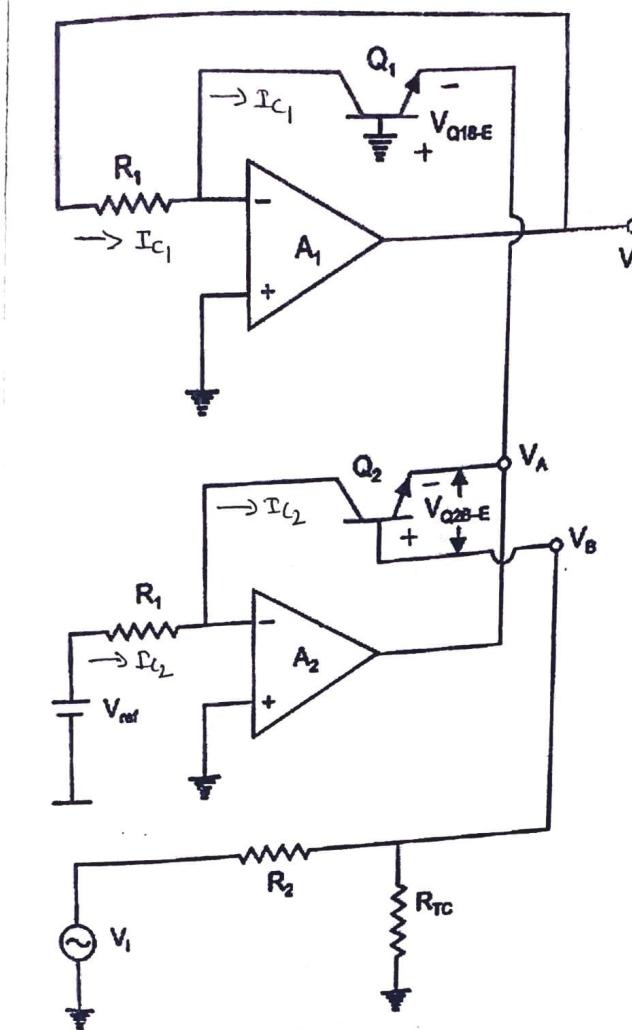


Fig 3

$$V_{Q1BE} \equiv V_{BE1}$$

$$V_{Q2BE} = V_{BE2}$$

$$V_{BE1} = 0 - V_A \Rightarrow V_A = -V_{BE1}$$

$$V_{BE2} = V_B - V_A - (A)$$

$$V_B = \frac{V_i \cdot R_{TC}}{R_2 + R_{TC}}$$

~~For~~ Consider eqn (A)

$$V_T \ln \left(\frac{V_{ref}}{R_1 I_S} \right) = \frac{V_i \cdot R_{TC}}{I_2 + I_{TC}} + V_T \ln \left(\frac{V_o}{R_1 I_S} \right)$$

$$V_T \ln \left(\frac{V_o}{R_1 I_S} \right) - V_T \ln \left(\frac{V_{ref}}{R_1 I_S} \right) = - \frac{V_i \cdot R_{TC}}{R_2 + R_{TC}}$$

$$V_T \ln \left(\frac{V_o / R_1 I_S}{V_{ref} / R_1 I_S} \right) = - V_i \cdot R_{TC} / I_2 + I_{TC}$$

$$\ln \left(\frac{V_0}{V_{ref}} \right) = - \frac{V_T R_{TC}}{V_T (\lambda_2 + \lambda_{TC})}$$

$$V_0 = V_{ref} \ln^{-1} \left[\frac{-V_T \lambda_{TC}}{V_T (\lambda_2 + \lambda_{TC})} \right]$$

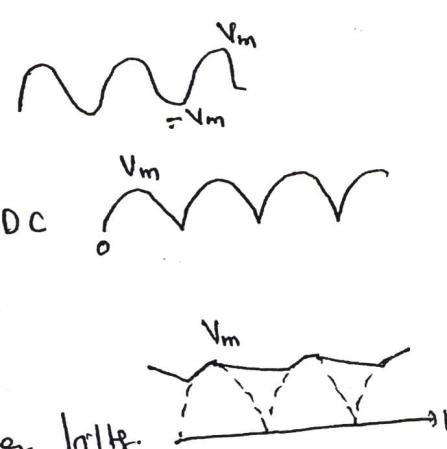
Voltage Regulator

- A Voltage regulator is an electronic circuit that provides a stable dc voltage independent of
 - Load current
 - Temperature
 - AC line voltage variations.

Need for Voltage regulators

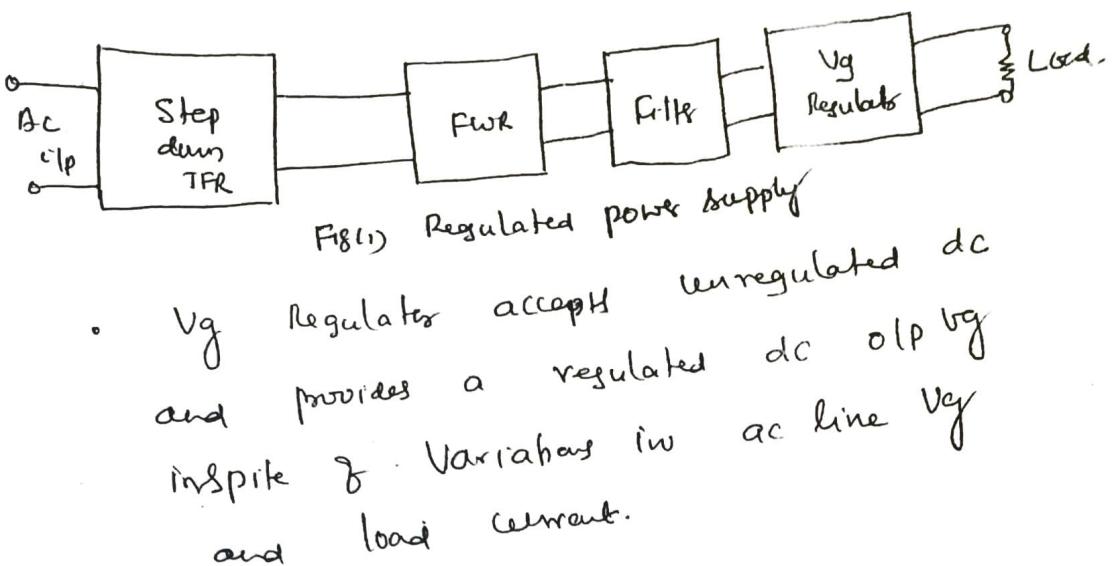
All electronic equipments require a stable dc voltage for their proper operation.

How do we get DC Voltage

- Available source is AC
 - If it is rectified to obtain DC
 - This dc has ripple
 - Ripple is removed using filter.
- Observe that Variation in filter o/p is small \Rightarrow less ripple.
- 

The o/p of filter is unregulated dc since the dc V_o varies with load current and AC line V_o .

Block diagram of regulated power supply



- V_g Regulator accepts unregulated dc and provides a regulated dc o/p V_g inspite of variations in ac line V_g and load current.

Classification of Voltage Regulators

- Linear Voltage Regulator (Series Regulator)
- Switching Voltage Regulator (Switching Regulator)
- In linear Voltage Regulator the control element (BJT / FET) is operated in the active region or linear region
- In switching regulator the control element is operated as a switch (on/off) at high frequency.
- Switching Regulators are compact and efficient compared to linear V_g Regulators.

Linear Voltage Regulator

The circuit consists of Reference voltage circuit, Error amplifier, Series pass transistor, feedback network

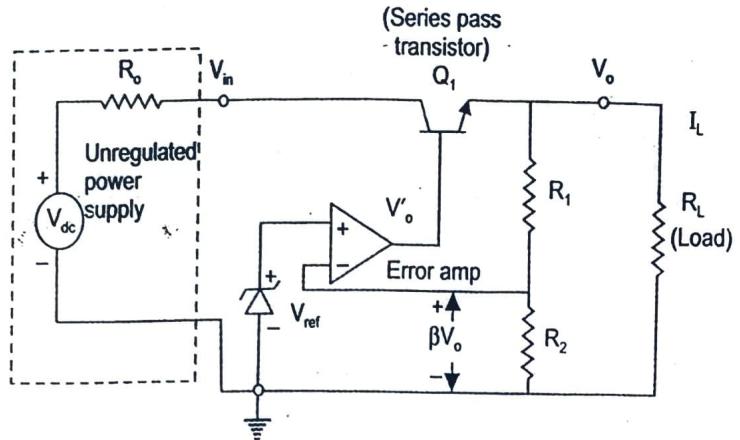


Fig 2. Linear Voltage regulator

- The Control element is Q_1 , which is in series with the load
 \Rightarrow Series bg Regulator.
- The error amplifier output controls the conduction of Q_1 to regulate the o/p bg V_o

feed back bg $V_f = V_o \left(\frac{R_2}{R_1 + R_2} \right) = \beta V_o$

Error Amplifier o/p, $V_o' \propto (V_{ref} - V_f)$

- Q_1 transistor is also connected as an emitter follower and therefore provides the sufficient current gain to drive the load

Regulating Action

Regulation against Variation in I_L

If $I_L \uparrow$

- $V_o \uparrow$
- $V_f = \beta V_o \uparrow$
- $V_o' \propto (V_{ref} - V_f) \downarrow$
- $I_{B1}, I_r \downarrow$
- $I_{C1}, I_{E1} \downarrow$
- $I_L \downarrow$
- $V_o \downarrow$ \rightarrow thus the increase in V_o is nullified.

If $I_L \downarrow$

Regulation against Variation in V_{in}

If $V_{in} \uparrow$

- $V_{C1} \uparrow$
- $I_{C1}, I_{E1} \uparrow$
- $I_L \uparrow$

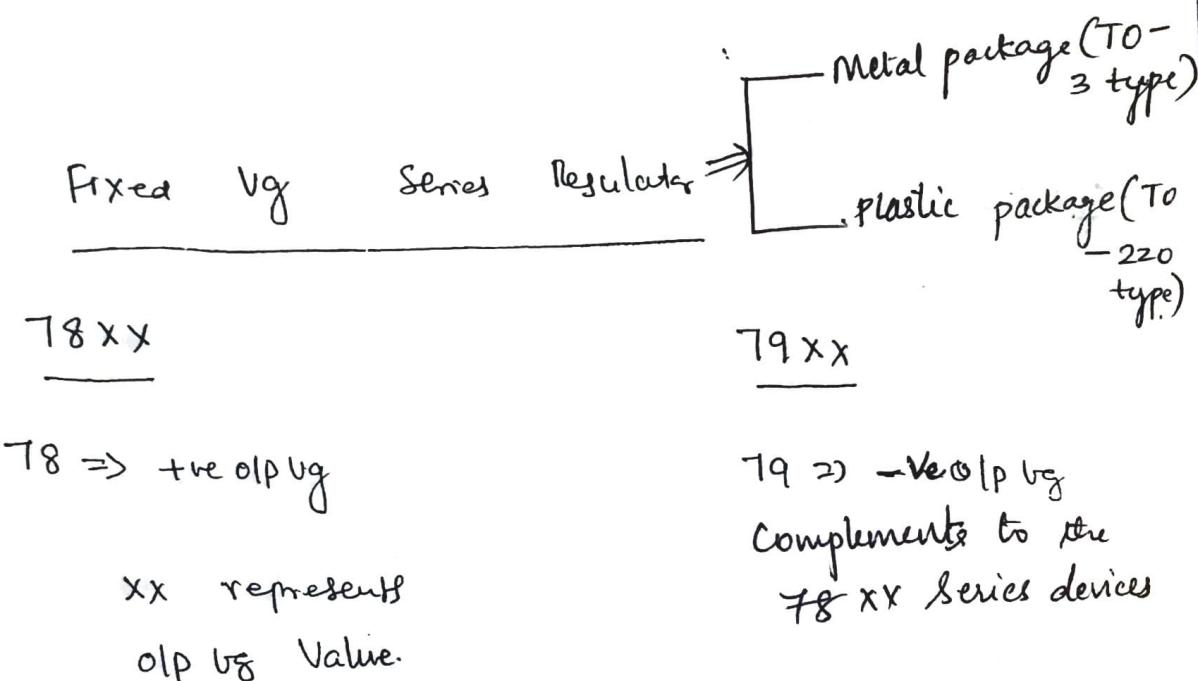
$V_o \uparrow$

If $V_{in} \downarrow$

- $V_o \downarrow$

IC Voltage Regulators

- With advances in microelectronics it became possible to incorporate the regulator circuit on a monolithic silicon chip.
- Examples of monolithic regulators are 78XX/79XX series. This results in general purpose regulators.
- low cost
- High reliability
- Reduction in size
- Excellent performance.



V_o options available

5, 6, 8, 12, 15, 18, 24V

Ex: 7805, 7812, 7824

indicates a 12V regulator

Both are three terminal Regulators.

Same as in 78XX with two extra pins -2V & -5.2V.

Ex 7905, 7902, 7914 ...

(06)

Three terminal positive V_g regulator

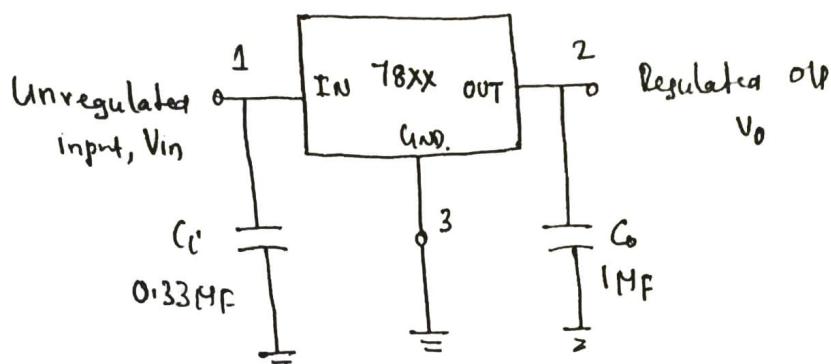


Fig 3. Three terminal regulator

- C_1 is connected between pin 1 & ground to cancel the inductive effects due to long distribution lead
- C_0 improves transient response.

$V_{in(\max)}$: 35V for 5 to 18V Regulators

40V for 24V Regulators.

$V_{in(\min)}$: $2V + |V_o|$ Regulated

↑
dropout V_g

For ex : For 7805

$$|V_o|_{Reg} = 5V$$

$$V_{in(\min)} = 2 + 5 = 7V. \quad V_{in(\max)} = 35V,$$

$$I_o(\max) = 1A.$$

Characteristics

(6a)

There are four characteristics of a three terminal IC regulators

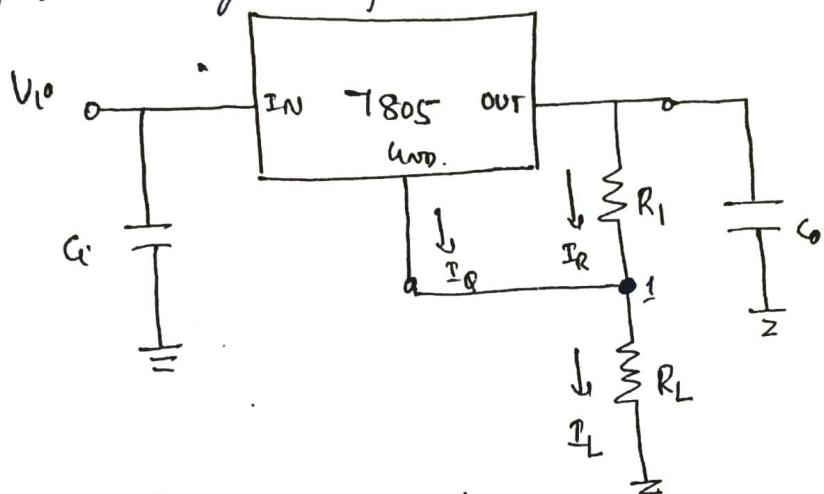
- (1) V_o : The regulated output voltage is fixed at a value as specified by the manufacturer.
- (2) $|V_{in}| \geq |V_o| + 2V$: The unregulated input voltage must be atleast $2V$ more than the regulated output voltage.
Ex:- If $V_o = 5V$ then $V_{in} = V_o + 2V = 7V$
 \uparrow
drop out voltage
- (3) $I_{o\ max}$:- the load current may vary from 0 to rated maximum output current. (~~1A~~). The IC is usually provided with a heat sink.
- (4) Thermal shutdown :- The IC has a temperature sensor built in which turns off the IC when it becomes too hot (usually $125^\circ C$ to $150^\circ C$). The output current will drop and remains there until the IC has cooled significantly.

Line / Input Regulation :- It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the o/p voltage. The typical value of line regulation for 7805 is $3mV$

Load Regulation It is defined as the change in output voltage for a change in load current and is also expressed in mV or as a percentage of V_o . The typical value of load regulation for 7805 is $15mV$ for $5mA < I_o < 1.5A$.

Current Source using 78xx

The three terminal fixed voltage regulator can be used as a current source. Figure(4) shows the circuit when 7805 has been wired to supply a current of 1 ampere to a 10Ω , 10 watt load.



Fig(4). Current source

Given across $R_1 = I_L \cdot R_1 = 5V$
Apply KCL at node ①

$$I_L = I_Q + I_R$$

I_Q = Quiescent current.

$$= 4.2mA \text{ for } 7805$$

$$I_Q \ll I_L$$

$$\Rightarrow I_L \approx I_R = \frac{5V}{R_1}$$

$$\text{If } I_L = 1A, \quad R_1 = 5\Omega$$

~~But~~ $R_L = 10\Omega$

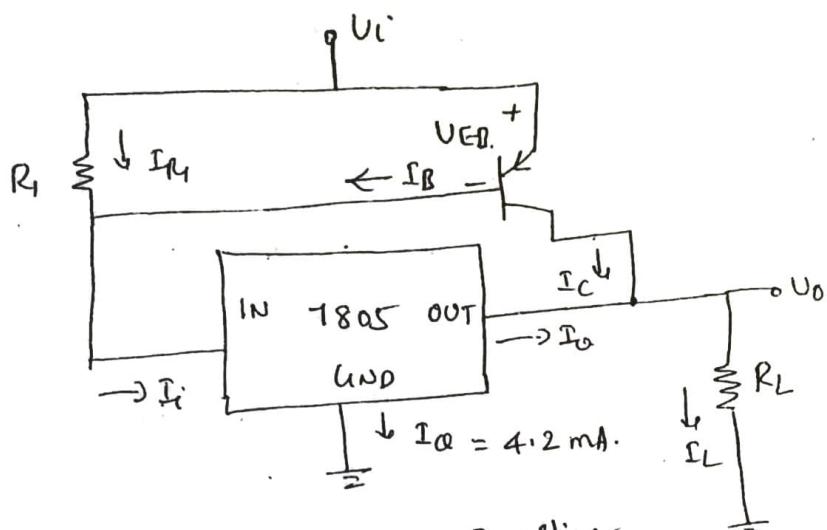
I_L is independent of R_L .

How much V_{10} is needed?

Ex: Try with 7812 for a load current of 0.5A into 10Ω load.

Cu. Boosting in 78xx and 79xx

08/20



Fig(5) Current Boosting

* For the regulator, $I_i = I_o + I_B \approx I_o$.

$$* I_{R_1} + I_B = I_i \Rightarrow I_{R_1} \approx I_i \approx I_o.$$

$$* U_{EB} = I_{R_1} R_1 = I_o R_1 \quad \text{--- (1)}$$

For the transistor to turn on

$$I_{DN} \geq 0.7V$$

* Let us limit I_o to 100 mA.

$$R_1 = \frac{0.7V}{0.1A} = 7\Omega$$

* For $I_L < I_o$, α is off

For $I_L > I_o$, α is on

$$I_L = I_o + I_C$$

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(09)

If the load demands current $> 100mA$,

If comes from the T_{Xr} .

Applying KCL at V_o node

$$I_L = I_C + I_0 \quad \text{--- (2)}$$

~~Also~~

$$I_C = \beta I_B$$

$$I_L = \beta I_B + I_0 \quad \text{--- (4)}$$

$$I_0 \approx I_{L0}$$

$$I_B = I_i - I_R$$

$$I_B = I_0 - \frac{V_{BE}}{R_L} \quad \text{--- (3)}$$

Sub (3) in (4)

$$I_L = \beta \left[I_0 - \frac{V_{BE}}{R_L} \right] + I_0$$

$$I_L = (1 + \beta) I_0 - \beta \frac{V_{BE(\text{cm})}}{R_L}$$

For 7805, $I_{out} = 1A$

$$V_{BE(\text{cm})} = 1V$$

$$\text{If } \beta = 15$$

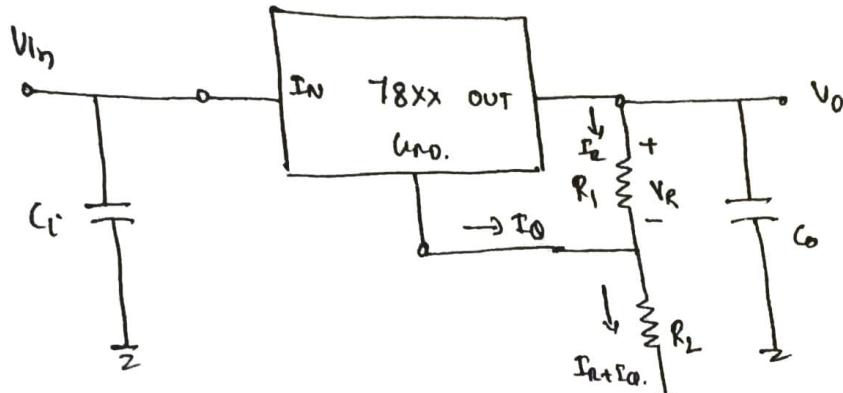
$$I_L = 13.8 A.$$

~~Output~~ ~~current~~.

Problem

- Q For the fig(3). Let $V_{BE(\text{cm})} = 1V$, $\beta = 15$, calculate the output current coming from 7805 and I_C coming from transistor Q₁ for loads 100Ω , 5Ω , 1Ω

Variable V_{QF} using 78xx



Fig(6) Variable Voltage using fixed V_Q
regulator
7805 gives 5V o/p

7806 gives 6V o/p.

How to obtain a V_Q between 5 & 6V?

$$V_O = I_R R_1 + (I_R + I_Q) R_2$$

Neglecting I_Q .

$$V_O = I_R (R_1 + R_2)$$

$$I_R = \frac{V_R}{R_1}$$

$$\Rightarrow V_O = V_R [1 + R_2/R_1]$$

Ex: To obtain 5.4V using 7805

$$5.4 = 5 (1 + R_2/R_1) = I_R (R_1 + R_2)$$

Choose $I_R \gg I_Q$

~~$R_2/R_1 \approx 0$~~

Let $I_R = 25\text{mA}$

At this R_2 and final I_2 . \checkmark

$$I_R = \frac{V_R}{R_1}$$

$$R_1 = ?$$

Dual power Supply

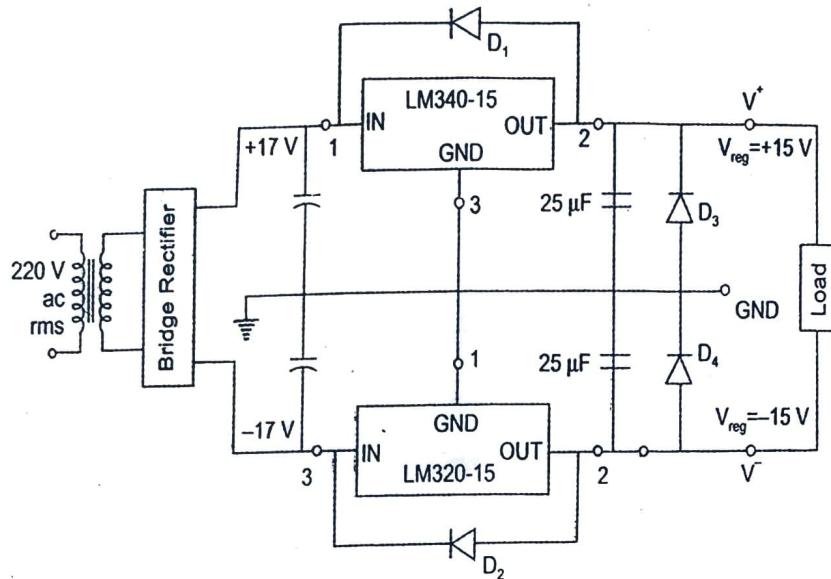


Fig (7) Dual power supply

- Many discrete and IC Circuits require dual power supply. Ex: Op-Amp.
- LM340-15 is a +15V o/p Regulator
- LM320-15 is a -15V o/p Regulator.
- We can also use 7815 and 7915 ICs.
- D₁ and D₂ protect the regulator against short circuit occurring ~~between the two~~ at its input terminals.
- D₃ & D₄ provide protection against the situation when both the regulators may not turn on simultaneously.

- If there is a load between the two outputs, the faster one will try to reverse the polarity of the other and cause it to latch up unless it is properly clamped.
- The clamping function is done by the diodes under normal operating conditions, both diodes will be reverse biased and will no longer have any effect on the circuit.
- LM325H is a dual tracking $\pm 15V$ supply and can furnish current upto 100mA.
- An op-amp draws less than 5mA current.
Hence LM325H can drive the circuit consisting of 20 op-amps.

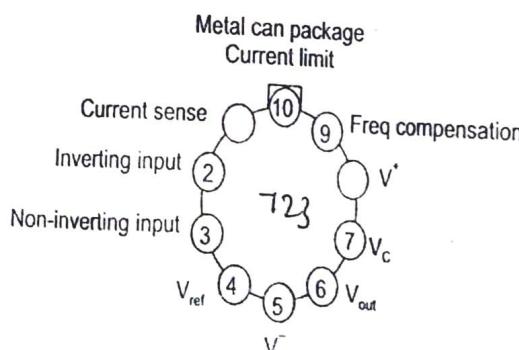
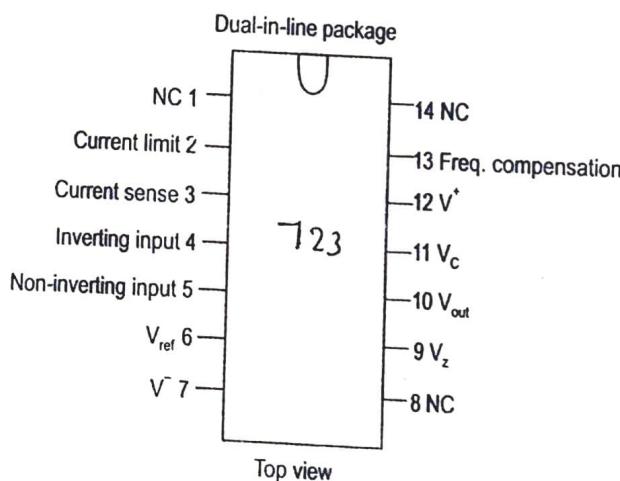
Limitations of three terminal regulators

- No short circuit protection.
 - output V_{G} is fixed.
- These limitations ~~are~~ have been overcome in the 723 general purpose regulator.

723 General purpose Regulators

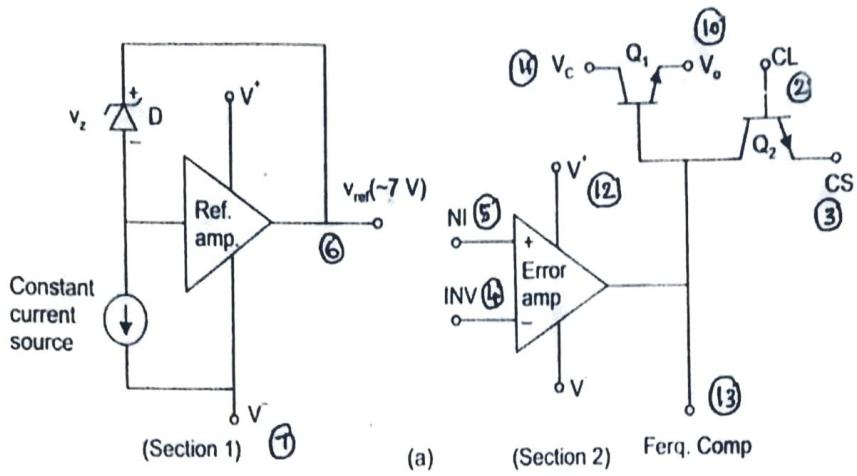
13

- Output voltage can be adjusted over a wide range of both +ve or -ve regulated V_{out} .
- $V_o : 2 \text{ to } 7V \rightarrow$ low voltage regulator
- $V_o : 7 \text{ to } 37V \rightarrow$ High voltage regulator
- $I_o (\text{max}) : 150 \text{ mA}$
- Externally boosted up to 5 Amp.
- Internal ref. $V_{\text{ref}} : 7.15V$
- $V_{\text{in}} (\text{max}) : 40V$
- Available as 14 pin DIP & 10 pin metal can.



(e) Fig (8) 723 I.C packages

Fenchannel Block diagram



Fig(9) Fenchannel Block diagrams 9/723

Section (1)

- Zener Diode, Constant current source and reference amplifier produces a fixed V_g of $7.15V$ at pin 6

The Constant current source forces the zener diode to operate at a fixed point. So that the zener outputs a fixed V_g .

Section (2)

- Error amplifier compares a part or full V_g of op-amp at inverting input with V_{ref} applied at non inverting input
- Op-amp of Error amplifier controls the conduction of series pass transistor Q_1

Low voltage regulator using 723

15

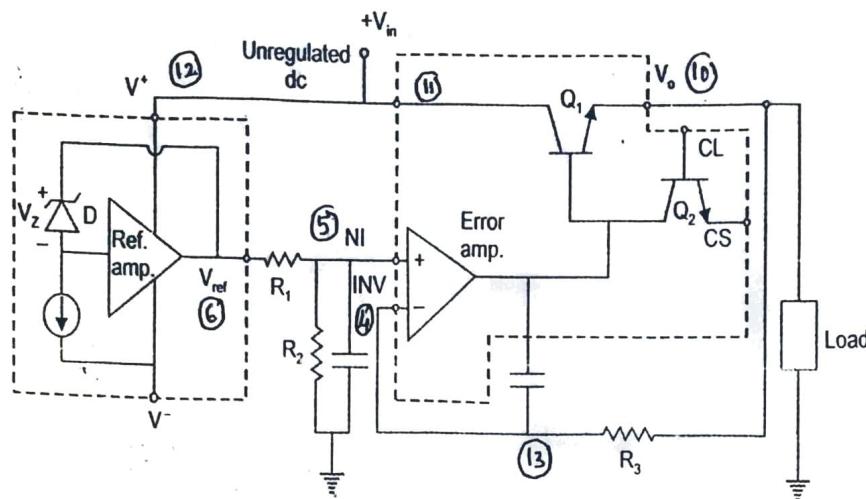


Fig (I) 723 low vg regulator. functional diagram.

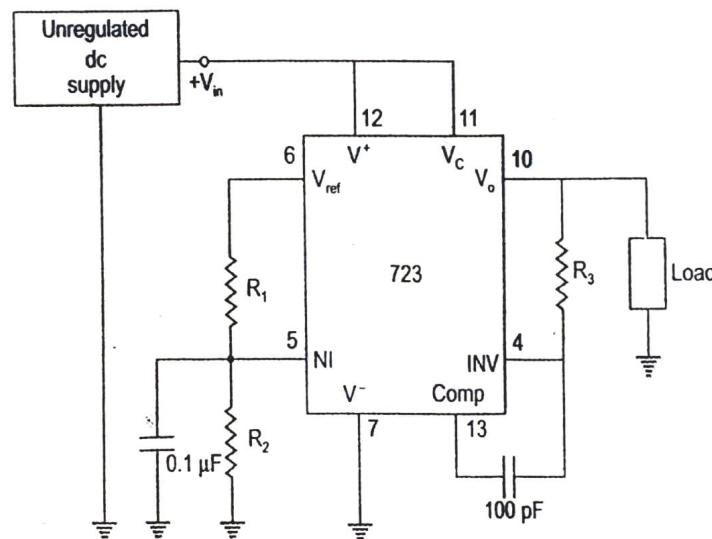
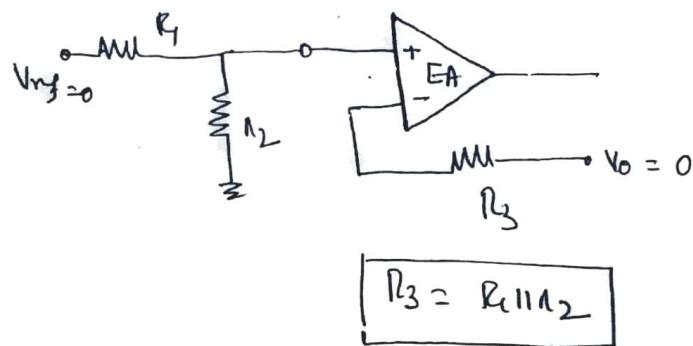


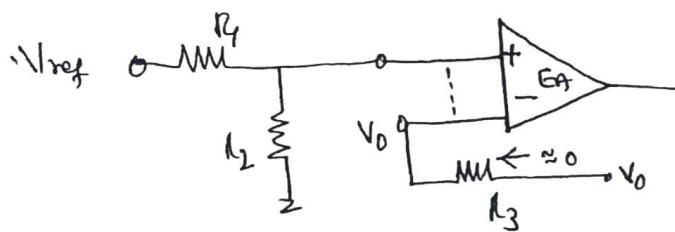
Fig (II) Ckt of low vg regulator using 723.

- A loop filter capacitor is recommended between pin 4 and 13 for stability purpose.
- A 0.1MF capacitor is recommended between pin 5 and ground for suppression of noise by

- V_{ref} is divided using V_g divider into R₁ and R₂ and the V_g across R₂ is applied to N1 terminal of Error amplifier.
- Entire A_{op} is applied to INV 111 via R₃.
- R₃ is used to obtain minimum drift due to offset current effect.



Expression for Regulated op-amp V_g V₀



Due to Virtual short at the input of EA

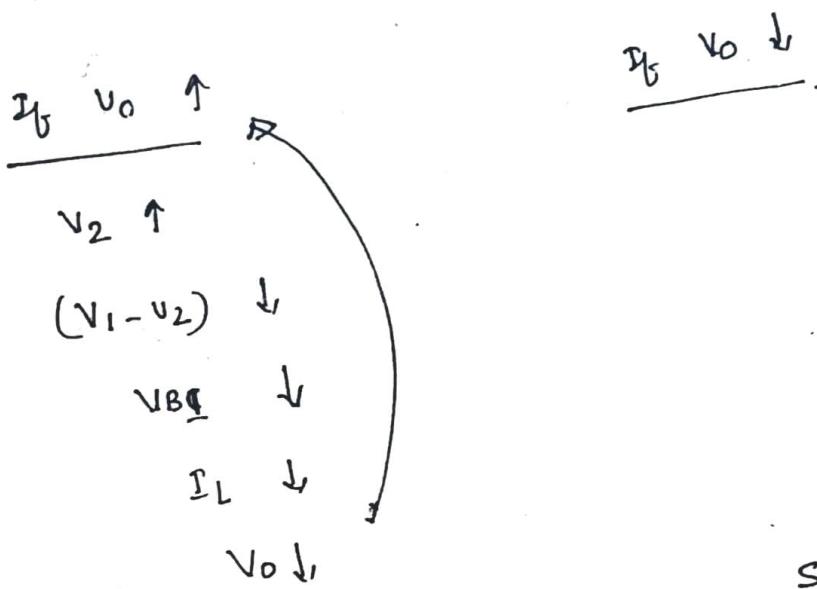
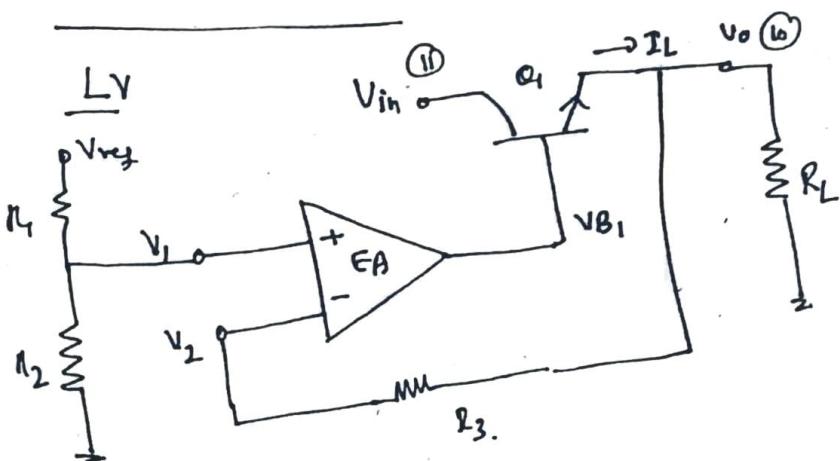
$$V_0 = V_{ref} \frac{R_2}{R_1 + R_2}$$

$$V_0 = 7.15 \left[\frac{R_2}{R_1 + R_2} \right]$$

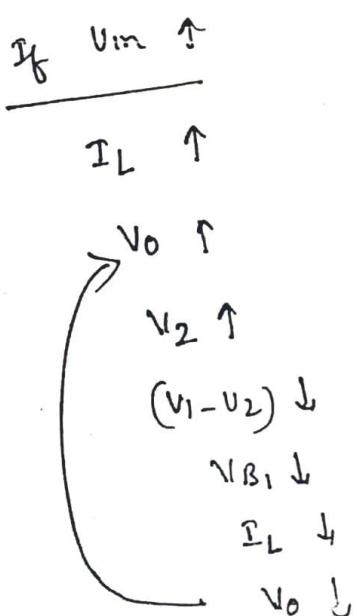
Note that $V_0 < 7.15\text{V}$

Hence low I_{o} - regulator.

Regulating Action



Similar explain
for HV.



Higher Voltage Regulator

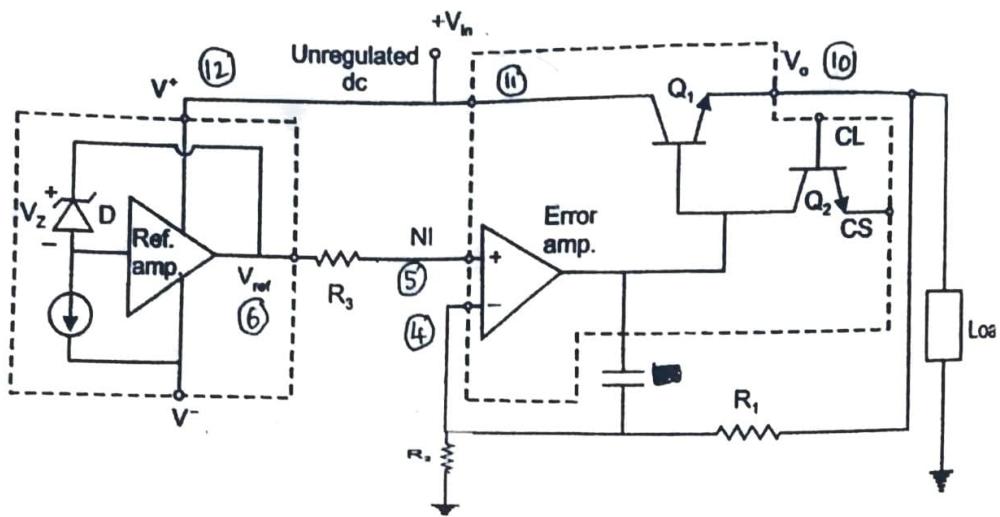
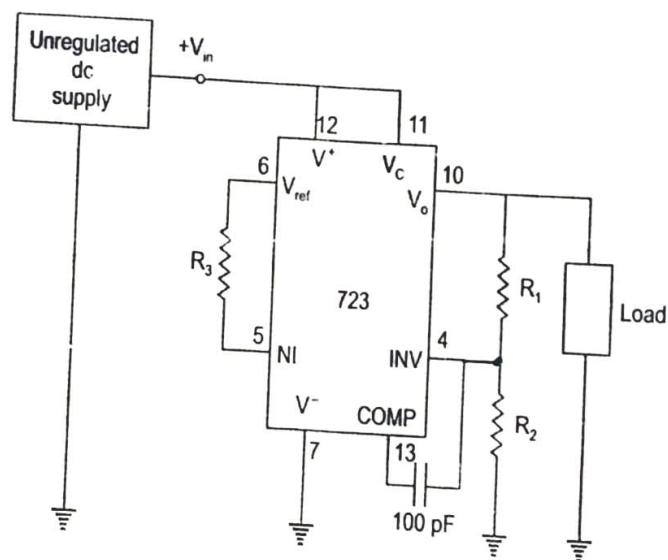


Fig (12) High voltage regulator using
two channel diagram.



Fig(13) Circuit diagram of high voltage
regulator

to 4710 7004 V7500

- potential divider $R_1 - R_2$ is connected between output pin (10) and ground. V_g across R_2 is applied to Inv chip.
- R_3 is used for minimum drift between pin 5 and 6. $R_3 = R_1 \parallel R_2$.
- Due to virtual short at the input of EA

$$V_{ref} = V_o \frac{R_2}{R_1 + R_2}$$

$$V_o = V_{ref} \left[1 + \frac{R_1}{R_2} \right]$$

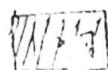
$$V_o = 7.15 \left[1 + 1/(R_2) \right]$$

Note that $V_o > 7.15V$

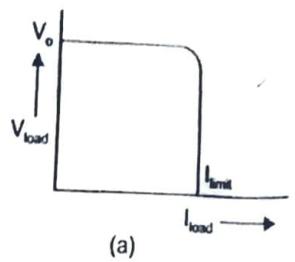
Hence high V_g regulator.

Current limit protection

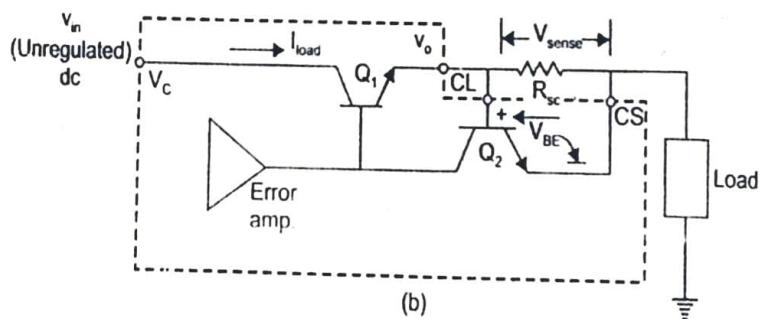
- The ICs of LV and HV regulators have no protection.
- If the load demands more current, the IC tries to provide it at a constant old V_g
- As a result the IC gets hotter and ultimately burn out.



- Current limiting refers to the ability of a Cuk to prevent the load current from increasing above a preset value.
- In a current limited power supply the output voltage remains constant for a load current below I_{limit} .
- As current approaches I_{limit} the op-amp voltage drops thus reducing power dissipation



Current limit protection circuit



Fig(14) current limit protection
circuit

The current limit I_{limit} is set by connecting an external resistor R_{sc} between the terminals C_L and C_S .

$$V_{\text{sense}} = I_L R_{\text{sc}}$$

For $V_{\text{sense}} < 0.5 \text{ V}$

Q_2 is off \Rightarrow no current limit action.

R_{sc} is selected such that

$$I_{\text{limit}} \cdot R_{\text{sc}} = 0.5 \text{ V}$$

• When $I_L > I_{limit}$

• when $I_L > I_{limit}$

$$I_L R_{sc} > 0.5V$$

Q_2 turns ON

• $V_{C2} \downarrow \Rightarrow V_{B1} \downarrow$

• $I_{B1} \downarrow, I_{E1}, I_{C1}, I_L \downarrow$

$$I_L R_{sc} < 0.5V$$

• Q_2 goes OFF

Thus load current cannot exceed I_{limit} .

Low Voltage Regulator with Current limit Protection

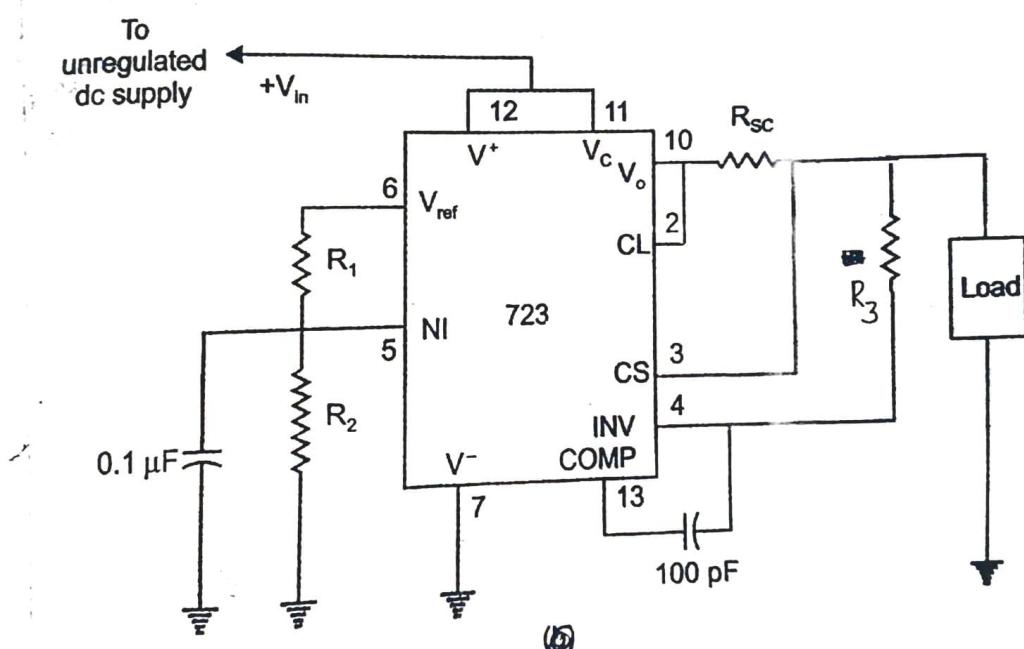


Fig 15. Circuit of low voltage regulator with current limit protection.

(25)

Design equations for low voltage regulators

- $V_o = V_{ref} \left[\frac{R_2}{R_1 + R_2} \right]$

- $V_{ref} = 7.15V$

- $R_3 = R_1 \parallel R_2$

$V_{in} > 7.15V$ for LV regulator

$V_{in} > V_o$ for HV regulator.

- $R_{SC} = \frac{V_{sense}}{I_{limit}} = \frac{0.5V}{I_{limit}}$

- Wattage of $R_{SC} > (I_{limit})^2 \cdot R_{SC}$

- Loop FF Cap between 13 & 4 for stability

- 0.1 HF Cap across R_2 for noise suppression.

High Voltage Regulator with current limit protection

$$V_o = V_{ref} [1 + R_1/R_2]; \text{ other equations remain the same.}$$

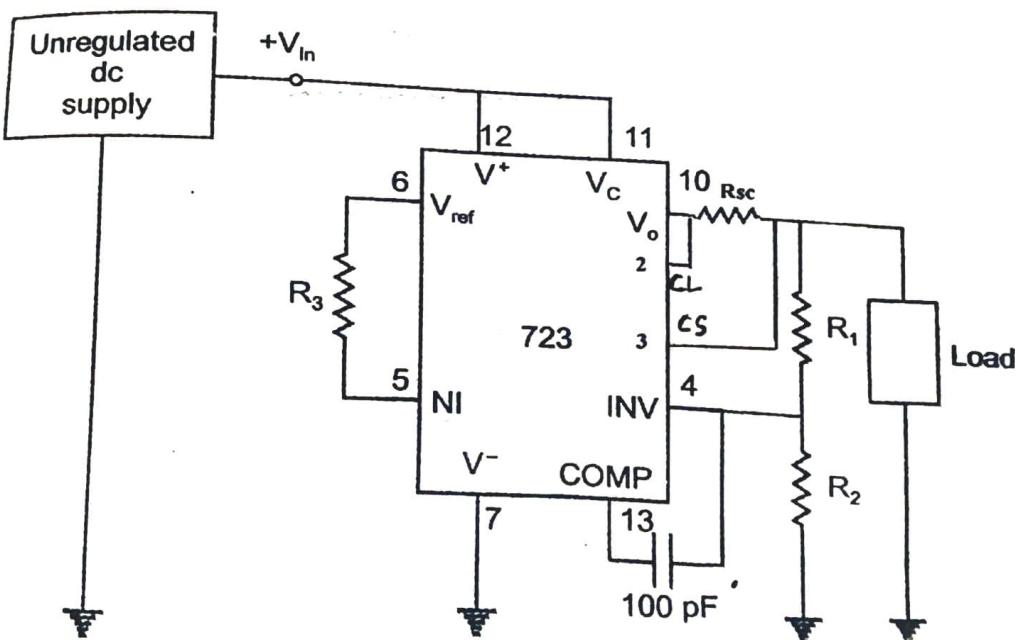


Fig 16. Circuit of high voltage regulator with current limit protection

(24)

Ex:1 Design a VG regulator using 723 to meet the following specifications.

$$V_0 = 5V$$

$$I_L = 120mA$$

The circuit must be short cut protected.

Suggest a suitable V_{1^o} .

Ex2 Ref the circuit of Fig 15.

$$R_1 = 10k\Omega \quad R_2 = 5k\Omega$$

a) Calculate V_0

b) Find R_L for $I_L = 130mA$

c) Calculate R_3

d) Find R_{BC} and the wattage to limit the load current at $130mA$

e) Suggest a suitable V_{1^o} .

Ex3 Repeat Ex1 for $V_0 = 15V$.

Ex4 Repeat Ex2 for the circuit of Fig 16.

(25)

Current Boosted in low voltage regulator

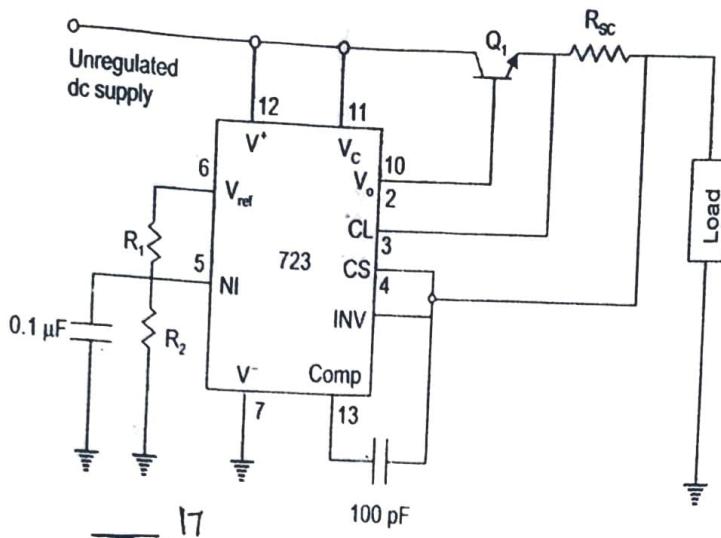


Fig. 25.1 Current boosted low voltage regulator

- Max current o/p from 723 is 140mA.
- For applications requiring load current greater than 140mA, current boosting is necessary. This is done using an external transistor Q_{ext} .
- The base current for Q_{ext} is o/p current of 723.
- $I_L = I_E(ext) = \beta \times I_o(723)$

If $\beta = 25$ and $I_o(723)$ is limited to 100mA then

$$I_L = 25 \times 0.1A = 2.5A$$

~~Design choice~~

Ex 5

Ref. the circuit of Fig 17.

$$R_f = R_2 = 10\text{k}\Omega$$

(a) Calculate V_o

(b) Find R_L and its voltage for a load current of 2A.

(c) Choose suitable R_{SC} such that $I_0(723)$ is limited to 100 mA and I_L is limited to 2A.

(d) Suggest a suitable V_i

Hint (c)

$$\beta = \frac{I_{Limit}}{I_0(723)} = \frac{2\text{A}}{0.1\text{A}} = 20$$

choose tx with $\beta = 25$

$$R_{SC} = \frac{0.5\text{V}}{I_{Limit}} = \frac{0.5\text{V}}{2\text{A}} = 0.25\Omega$$

Voltage of $R_{SC} > (I_{Limit})^2 \times R_{SC}$.

Additional

- Draw the circuit of HV regulator with current boosting.

Ex 6

Repeat examples for HV regulator with current boosting.

Current fold back.

(27)

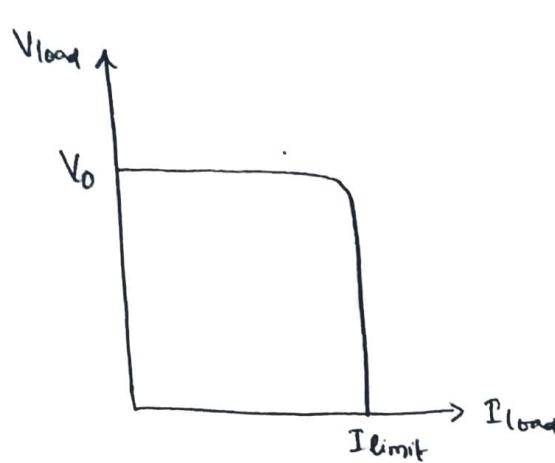
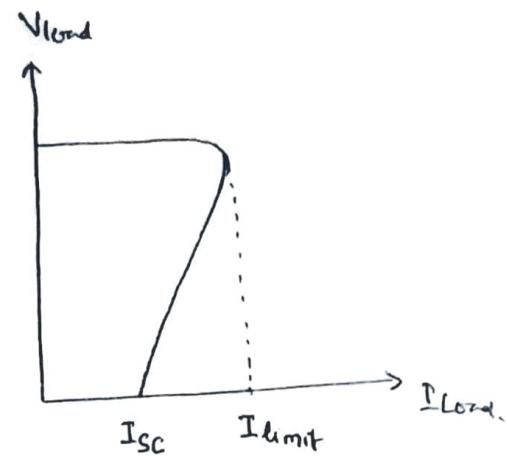


Fig 18 (a) current limiting



(b) current fold back.

- In current limiting technique, the load current is maintained at a preset value and when the over load condition occurs, the o/p v_o drops to zero.
- If the regulator is short circuited, the regulator has to carry maximum current.
- To protect the regulator current fold back is used.
- In fold back current limiting both o/p v_o and o/p current decreases when the load current exceeds a preset level I_{limit}.
- When the load is short circuited $V_o \rightarrow 0$
- $I_{Load} \rightarrow I_{SC}$
- Note that $I_{SC} < I_{limit}$.

Low voltage regulator using current fold back.

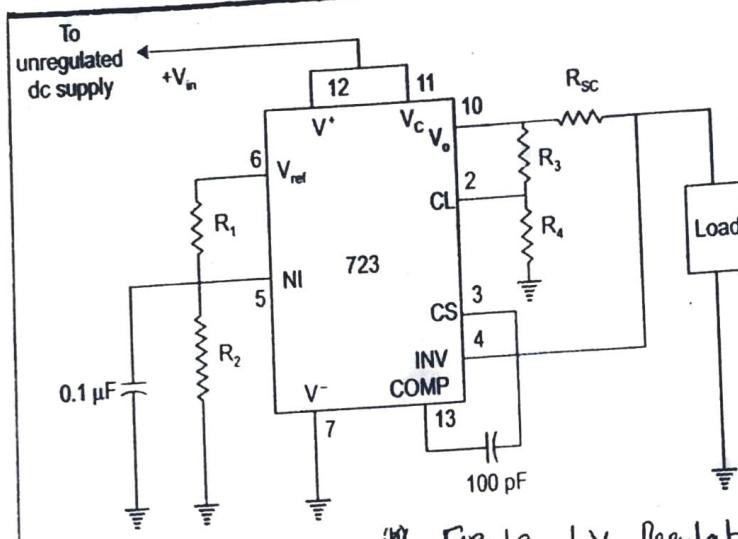


Fig 19 LV Regulates Using
Current fold back

$$I = \frac{V_A}{R_3 + R_4} ; \quad V_{B2} = \frac{V_A R_4}{R_3 + R_4} = K V_A$$

$$K = \frac{R_4}{R_3 + R_4} ; \quad V_A = I_L R_{SC} + V_0$$

$$\therefore V_{B2} = K [I_L R_{SC} + V_0]$$

$$V_{BE2} = V_{B2} - V_0 = K I_L R_{SC} + (K-1) V_0$$

$$I_L = \frac{V_{BE2}}{K R_{SC}} + \frac{(1-K) V_0}{K R_{SC}}$$

when Load is short circuited, $V_0 \rightarrow 0$

$$I_L = \frac{V_{BE2}}{K R_{SC}} = I_{SC}$$

$$\therefore I_L = I_{SC} + \frac{(1-K) V_0}{K R_{SC}} > I_{SC}$$

K is selected such that I_{limit} is 2 to 3 times I_{SC} .

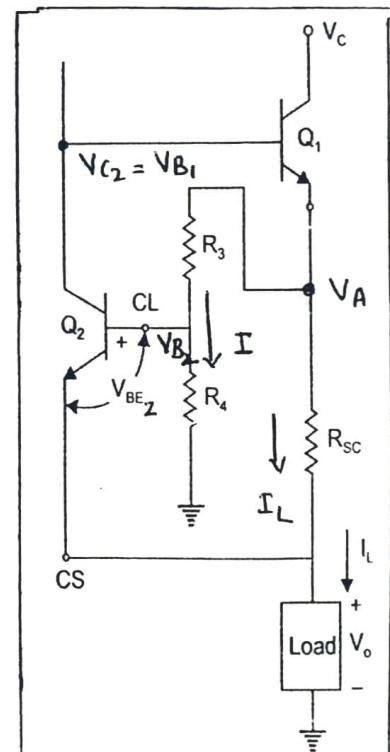


Fig (20) Current fold back circuit.

Working of current limiting circuit

- When the load current increases to a large value
 - $V_A \uparrow \Rightarrow V_{B_2} \uparrow, V_{BE_2} \uparrow$
 - When V_{BE_2} becomes 0.5V, Q_2 starts conducting.
 - $V_{C_2} \downarrow, V_{B_1} \downarrow$
 - Conduction of $Q_1 \downarrow$
 - $I_L \downarrow, V_o \downarrow, V_B \downarrow$
 - $V_{B_2} = k [V_A] \quad V_{B_2} \downarrow$ by a small amount
Compared to V_o
 - $V_{BE_2} = V_{B_2} - V_o \uparrow$
 - Conduction of $Q_2 \uparrow$
 - Conduction of $Q_1 \downarrow$
 - $I_L \downarrow, V_o \downarrow$
 - This process continues until $V_o \rightarrow 0$
and V_A is large enough to keep
0.5V between C_L and C_S terminals.

Switching Regulators

Linear Regulator vs Switching Regulator

Linear Regulator

- Input Stepdown transformer is bulky and expensive since as because of low frequency (50Hz)

- Large values of filter capacitors are required to filter low frequency ripple.

$$r = \frac{1}{4f_3 R_L C}$$

- The pass transistors operate in its linear region to provide a controlled voltage drop across it with a steady dc current flow.

$$P_C = V_{CE} I_C$$

Continuous power loss

$$n \downarrow$$

$$\eta_{max} = 50\% \text{ Typically}$$

Switching Regulator

- In switching regulators transformer size is less due to high frequency switching.

- Size of filter capacitors is small due to high frequency ripple.

- The pass transistors is operated as a controlled switch.
OFF : $I_C = 0 \Rightarrow P_C = 0$
ON : $V_{CE} = 0 \Rightarrow P_C = 0$ min power loss

$$n \uparrow$$

$$\eta_{max} = 90 - 95\%$$

Typically

Block diagram of Switching Regulator

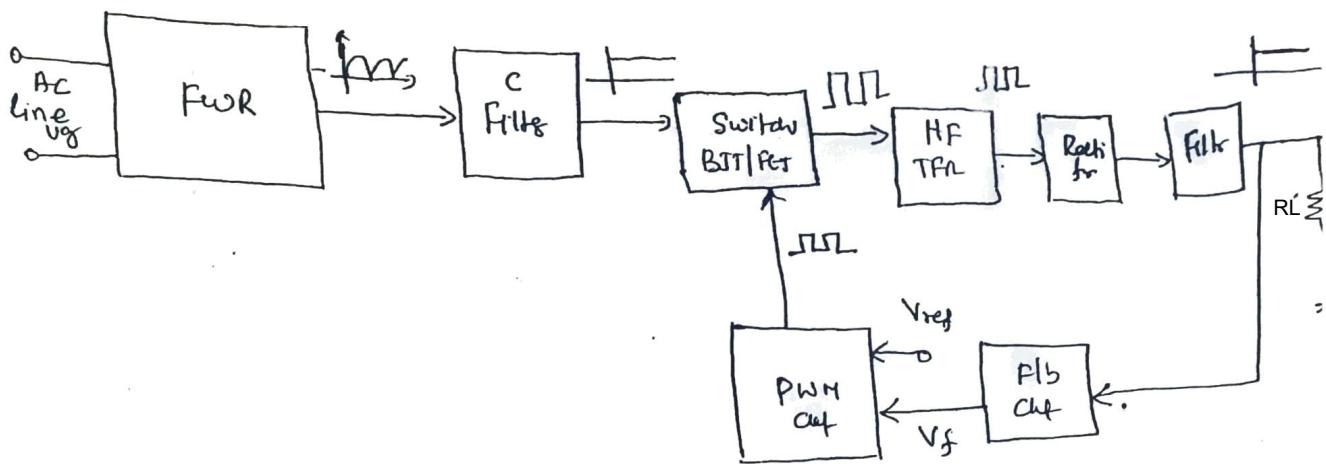
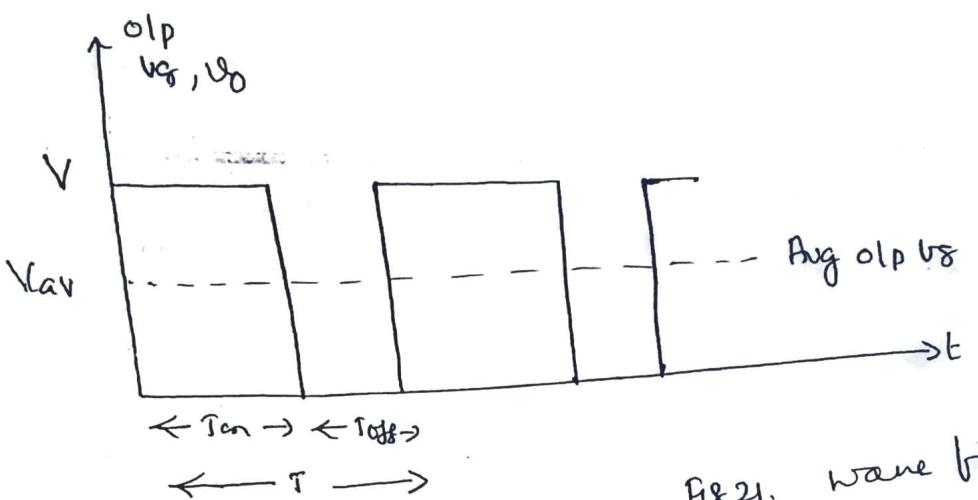


Fig 20. Block diagram of switching regulator.

- Ac line V_g is directly rectified using FWR.
- C filter is used to eliminate ripple.
- Dc V_g o/p of C filter is converted into Sq. wave using the switch controlled by PWM CLK.
- HF Step down transformer is used to reduce the amplitude of Sq. wave into convenient value.
- The transformer o/p is rectified and then filtered to obtain smooth dc.
- PWM CLK controls the duty cycle of switch by comparing V_{ref} with V_f to regulate the output voltage.



$$V_{avg} = \frac{1}{T} \int_0^T v_0 dt$$

$$= \frac{1}{T} \int_0^{T_{on}} V dt$$

$V_{avg} = \frac{T_{on}}{T} V = DV$

D is duty cycle:

$$0 \leq D \leq 1.$$

$\Rightarrow V_0$ varies from 0 to V .

Regulator Action

If $V_0 \uparrow$

- $V_f \uparrow$
- PWM Act $\downarrow D$
- $T_{on} \downarrow$
- $V_0 \downarrow$

If $V_0 \downarrow$

555 Timer

- A highly stable device used for generating accurate time delay or oscillation.

Commercial Name SE555 | NE555

8 pin circular
8 pin mini DIP

14 Pin DIP

- Available as 10^{-9} to 10^9 can provide time delay ranging from μs to hours

Features

- power supply V_g : 5 to 18V

drive load $\Rightarrow I_o(\max) : 200 \text{ mA}$

output compatible with TTL & CMOS

555 timer is versatile and easy to use in various applications

Applications

• oscillator

• pulse generator

• ramp and square wave generator

• monostable multivibrator

Burglar Alarm

• traffic light control

• V_g monitor etc.

(02)

Functional diagram of 555 timer

Three equal resistors each of value $5\text{k}\Omega$ are connected in series between pin 8 (V_{CC}) and ground.

V_g at pins of upper comparator (U_C) is $\frac{2}{3}V_{CC}$, which is the upper trip point V_{UTP} .

V_g at non inverting terminal of lower comparator (L_C) is $\frac{1}{3}V_{CC}$, which is the lower trip point V_{LTP} .

When the threshold V_g exceeds $\frac{2}{3}V_{CC}$, upper comparator o/p goes high
 $\Rightarrow S=1, Q=0, \bar{Q}=1$, output = 0
 The discharge transistor Q_1 goes to saturation.

When the trigger V_g falls below $\frac{1}{3}V_{CC}$, lower comparator o/p goes high
 $\Rightarrow S=1, Q=1, \bar{Q}=0$, output = 1
 The discharge transistor Q_1 goes to cut-off.

A capacitor of 0.01MF is recommended between pins (5) and ground to suppress noise on control V_g pin.

Pin 1 → Grounded terminal → All the voltages are measured w.r.t to the ground terminal

Pin 2 → Trigger Terminal → The trigger pin is used to feed the trigger input the 555 IC is set up as a monostable multivibrator

Pin 3 → Output terminal → Op of the timer is available at this pin.

Pin 4 → Reset → to reset or disable the timer

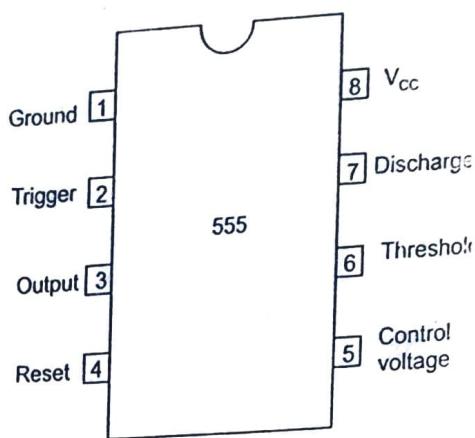
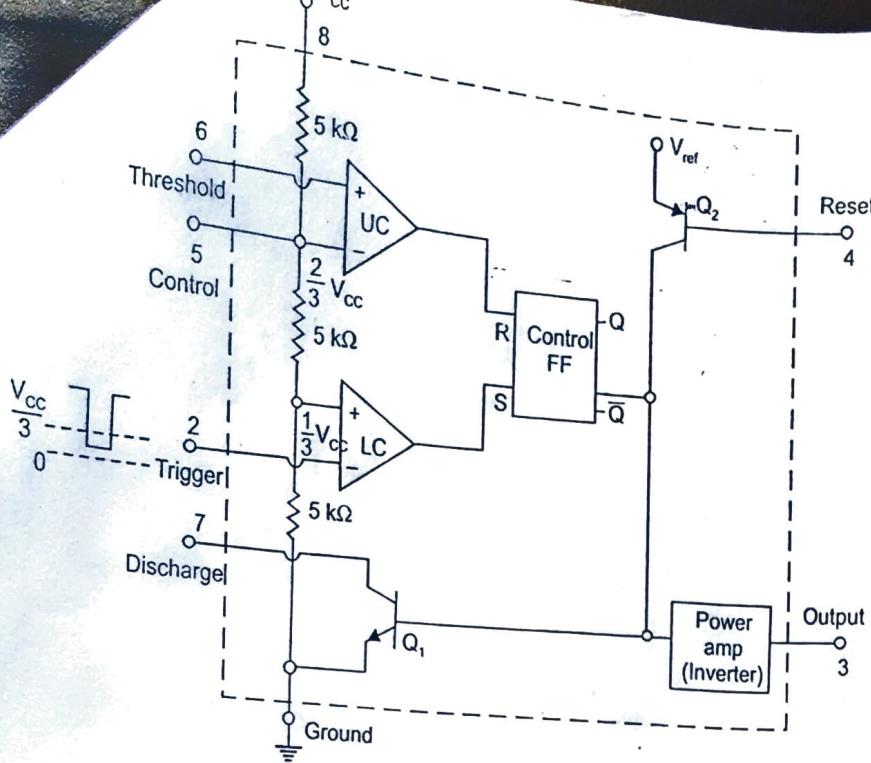
Pin 5 → Control Voltage Terminal → The threshold and trigger levels are controlled using this pin

Pin 6 → Threshold Terminal → non inverting input terminal of comparator 1 (ie Upper Comparator)

Pin 7 → Discharge terminal :- This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal & ground. It is called discharge terminal because when transistor saturates, capacitor discharges through transistor.

Pin 8 → Supply terminal → A supply voltage of +5V to +18V is applied to this terminal w.r.t ground (Pin 1)

It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5)

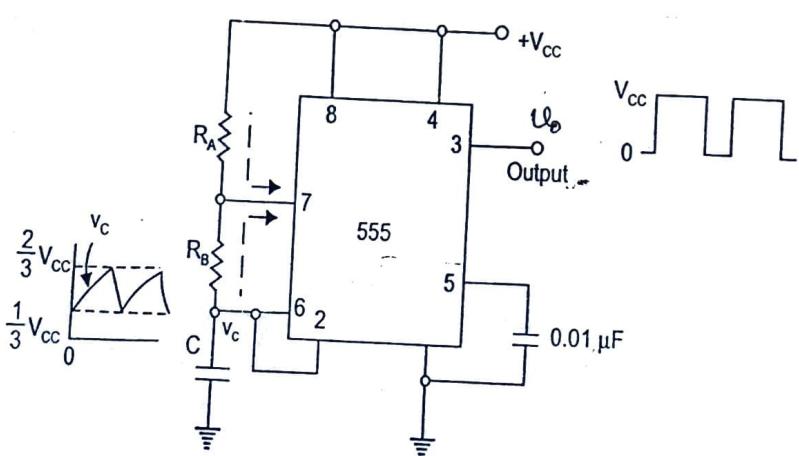


(2) Pin diagram

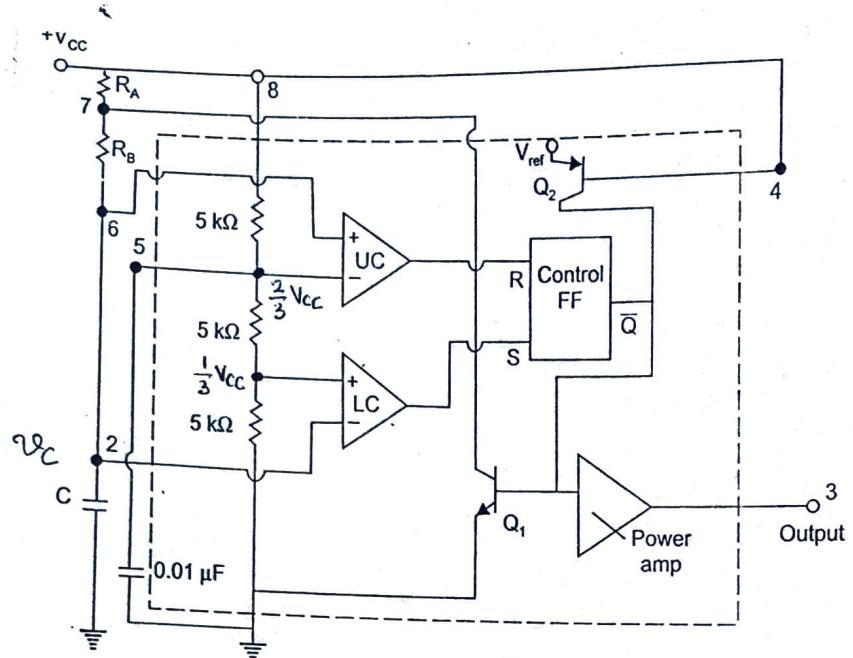
(1) Functional diagram.

Under normal use Reset pin should be connected to V_{cc} i.e. Pin 8.

555 Timer as Astable multivibrator

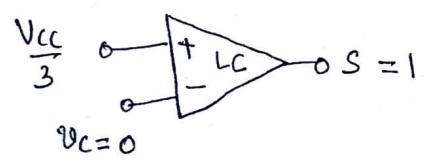
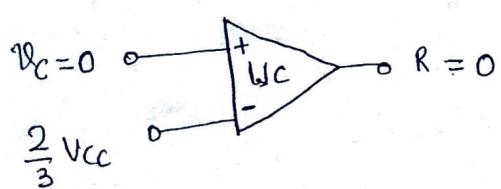


(3) Astable multivibrator



(4) Functional diagram of Astable multivibrator

- When the circuit is switched on, the flip-flop is cleared ($Q = 0$, $\bar{Q} = 1$). Initially the following conditions exist.



$(V_c = 0 \text{ since capacitor is initially uncharged})$

Since $S = 1$, $R = 0$, $Q = 1$, $\bar{Q} = 0$ and $Q_P = 1$.
The discharge transistor Q_1 is off.

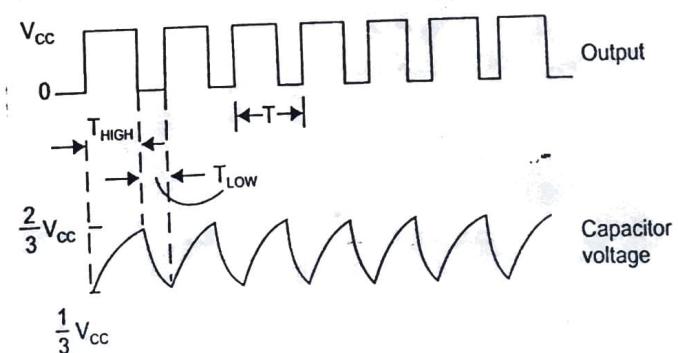
The capacitor gets charged via R_A and R_B . When the capacitor V_C exceeds $\frac{2}{3}V_{CC}$, upper comparator, Q_P goes high i.e. $Q = 0$, $\bar{Q} = 1$ and $Q_P = 0$. The discharge transistor Q_1 goes to saturation, since $\bar{Q} = 1$

Now the capacitor discharges into saturated transistor via R_B . When the capacitor V_C falls below $\frac{1}{3}V_{CC}$, the low comparator Q_P goes high. Now

$$S = 1, \quad Q = 1, \quad \bar{Q} = 0, \quad Q_P = 1$$

The discharge transistor Q_1 goes to cut-off since $\bar{Q} = 0$.

Now the capacitor once again charges via R_A & M_B and the same cycle repeats.



(5) Wave forms

$$T_{High} = T_{on}$$

$$T_{Low} = T_{off}$$

Expression for frequency of oscillations

Simil

Charging time constant = $(R_A + R_B)C$

Discharging time constant = $R_B C$

Consider the interval $0 < t \leq T_{\text{dis}}(T_m)$

Capacitor is getting charged towards V_{CC} via

$R_A + R_B$.
 $V_f \rightarrow$ final voltage to which the capacitor will charge

$V_C(t) = V_f + (V_i + V_f)e^{-t/(R_A + R_B)C}$ --- (1)
 $V_i \rightarrow$ initial capacitance voltage.

$$V_f = V_{CC}, \quad V_i = \frac{1}{3} V_{CC}.$$

$$V_C(t) = V_{CC} + \left(\frac{1}{3} V_{CC} - V_{CC}\right) e^{-t/(R_A + R_B)C}$$

at $t = T_m$, $V_C(t) = \frac{2}{3} V_{CC}$. Now

$$\frac{2}{3} V_{CC} = V_{CC} + \left(\frac{1}{3} V_{CC} - V_{CC}\right) e^{-T_m/(R_A + R_B)C}$$

$$\frac{2}{3} = 1 - \frac{2}{3} e^{-T_m/(R_A + R_B)C}$$

$$\frac{2}{3} e^{-T_m/(R_A + R_B)C} = \frac{1}{3}$$

$$e^{T_m/(R_A + R_B)C} = 2$$

$$T_m = (R_A + R_B)C \ln 2$$

$$T_m = 0.693 (R_A + R_B)C \quad (2)$$

Similarly, $T_{off} = 0.693 L_B C \dots (3)$

$$T = T_m + T_{off} = 0.693 (L_A + 2L_B) C \dots (4)$$

$$f = \frac{1}{T} = \frac{1.44}{(L_A + 2L_B) C} \dots (5)$$

$$\text{Duty cycle, } D = \frac{T_m}{T} = \frac{L_A + L_B}{L_A + 2L_B} \dots (6)$$

Verify from equation (6) that, D can only be greater than 0.5.

Note: take $D = 1/4$ write your observation from (6).

[Ex 1] Refe the circuit & Fig (3).

$$V_{CC} = 10V$$

$$R_A = R_B = 10k\Omega$$

$$C = 0.02 \mu F$$

1. Calculate T_m , T_{off} , T and f

2. Find Duty cycle

3. Sketch the waveforms of V_C and V_o .

[Ex 2] Design an astable multivibrator using 555 timer with the following specifications.

$$f = 2 kHz$$

$$D = 0.75$$

Amplitude of Sig. wave: 0 - 5V

$$V_{CC} = 10V$$

Hint:

$$f = \frac{1.64}{(LA + 2LB) C} \quad \text{--- (A)}$$

$$D = \frac{RA + LB}{LA + 2LB} \quad \text{--- (B)}$$

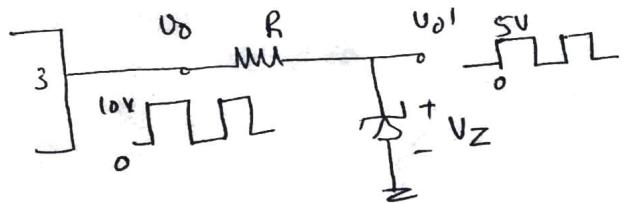
Three continuous MA, LB & C
only two cont.

choose $C = 0.1 \mu F$

Find RA & LB using (A) & (B).

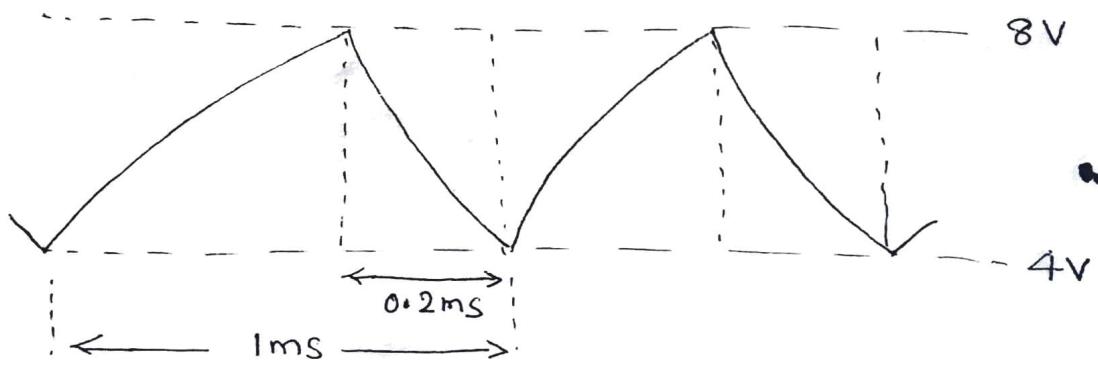
Amplitude limits

Design suitable R.



Ex 3

The V_g across capacitor in an astable multivibrator using 555 is shown below.

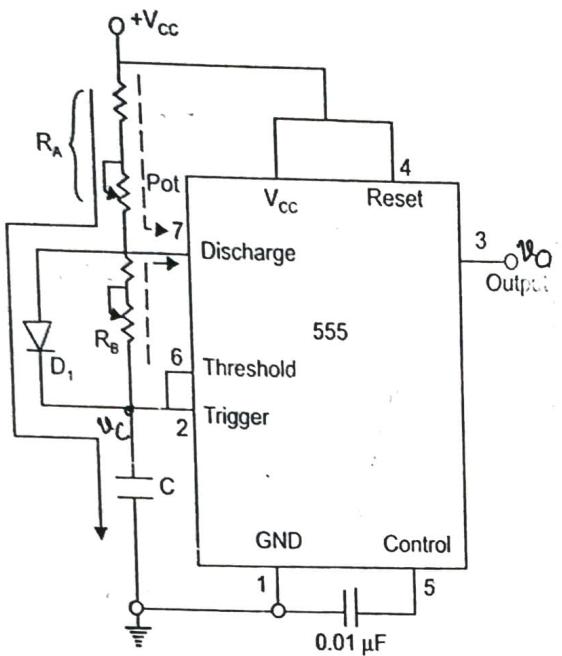


Design the Component Values for the Circuit.

Astable multivibrator with Variable

(09)

Duty Cycle.



Fig(6). Astable multivibrator with adjustable duty cycle.

Note: working is similar to that of that in Fig (3). only equations are given below.

Students are advised to write explanations,

derive the following equations and sketch down the waveforms of V_C and V_O .

Capacitor gets charged via R_A and diode.

$$T_{on} = 0.693 R_A C \quad (7)$$

Discharging of the capacitor takes place through R_B

$$T_{off} = 0.693 R_B C \quad (8)$$

$$T = 0.693 (R_A + R_B) C \quad (9)$$

$$D = T_{on}/T = \frac{R_A}{R_A + R_B} \quad (10)$$

$$f = \frac{1}{T} = \frac{1.44}{(R_A + R_B) C} - (1)$$

Observe from (10) that D can be less than and greater than 0.5. When $R_A = R_B$, $D = 0.5$

\Rightarrow The Square wave is said to be symmetrical.

Ex 4. In the circuit of Fig (6) $R_A = 6.8 \text{ k}\Omega$ $R_B = 3.3 \text{ k}\Omega$

$$C = 0.1 \text{ nF} \quad \text{Calculate}$$

T_{on} , T_{off} , T , f and D .

If $V_{CC} = 10V$ Sketch the waveforms of v_o and v_c .

Ex 5 Design a square wave generator using 555 timer to meet the following requirements.

$$T_{on} = 0.75 \text{ ms}$$

$$f = 1 \text{ kHz.}$$

Amplitude of sig. wave: 0 to 5V

$$V_{CC} = 10V.$$

Draw the circuit and sketch the waveforms of v_o and v_c .

Ex 6 Repeat Ex 5 Design a sig. wave generator using 555 timer to meet the following specifications.

$$f = 4 \text{ kHz} \quad D = 0.25 \quad \text{Amplitude of sig. wave } 10V \quad V_{CC} = 10V$$

(11)

For the circuit shown below

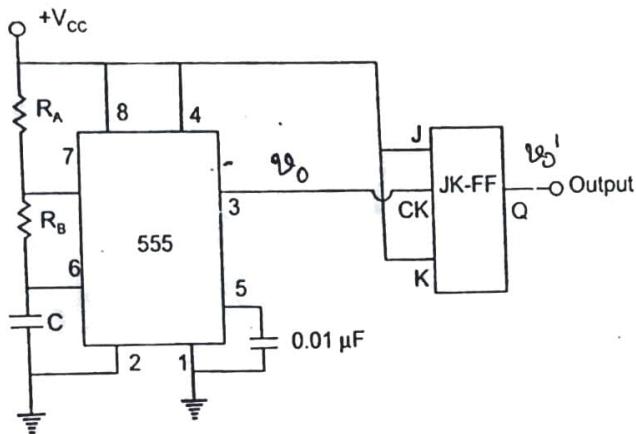
$$R_A = 8\text{ k}\Omega \quad R_B = 4\text{ k}\Omega \quad C = 0.1\text{ mF}$$

(a) Calculate T_{on} , T_{off} , f , and $D \geq v_o$.

(b) Find T_{on} , T_{off} , f and $D \geq v_o$

(c) Write your inference.

flip flop is rising edge triggered



Applications of Astable multivibrator

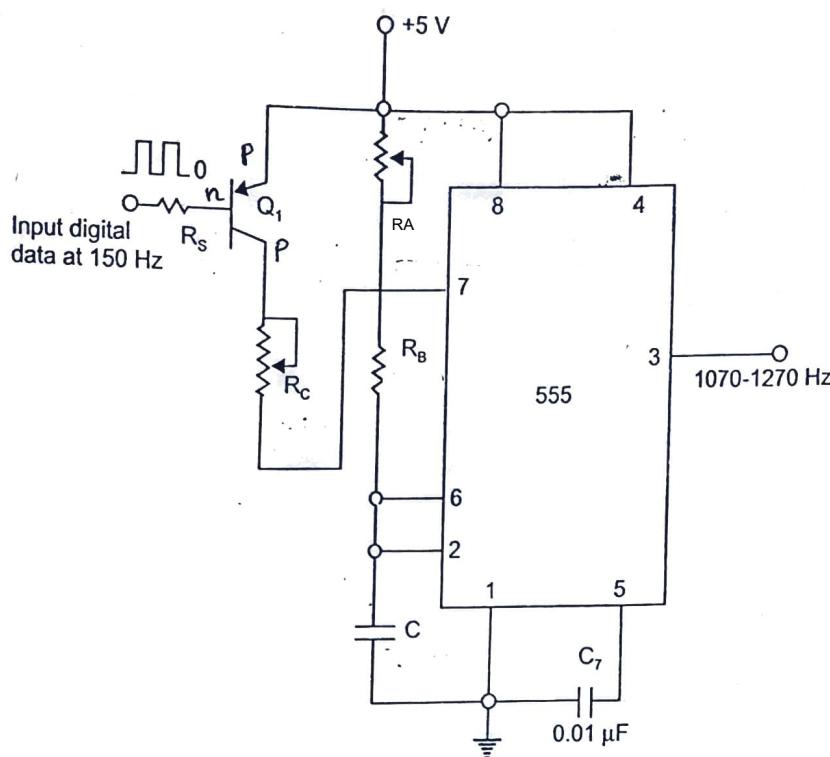
- 1) FSK Generator
- 2) Schmitt trigger
- 3) Saw tooth wave generator.
- 4) Pulse Position Modulation

FSK Generator

- In digital data communication binary code is transmitted by shifting the carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique.
- In a teletypewriter using MODEM, a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals
 - logic 1 → Mark → 1070 Hz
 - logic 0 → Space → 1270 Hz.
- The standard digital data input frequency is 150 Hz.

When the input is low, Q_1 goes on and R_A appears in parallel with R_C .

$$\therefore f = \frac{1044}{\{(R_A || R_C) + 2R_B\} C}$$



Fig(7) FSK generator.

R_C can be adjusted to set $f = 1270 \text{ Hz}$.

when the input is high, transistor Q_1 goes off.
 R_C sets dis connected from the circuit

$$f = \frac{1.44}{(R_A + 2R_B) C}$$

Values of C , R_A and R_B can be selected so

that $f = 1070 \text{ Hz}$.

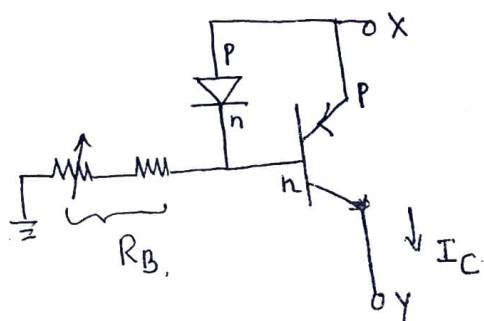
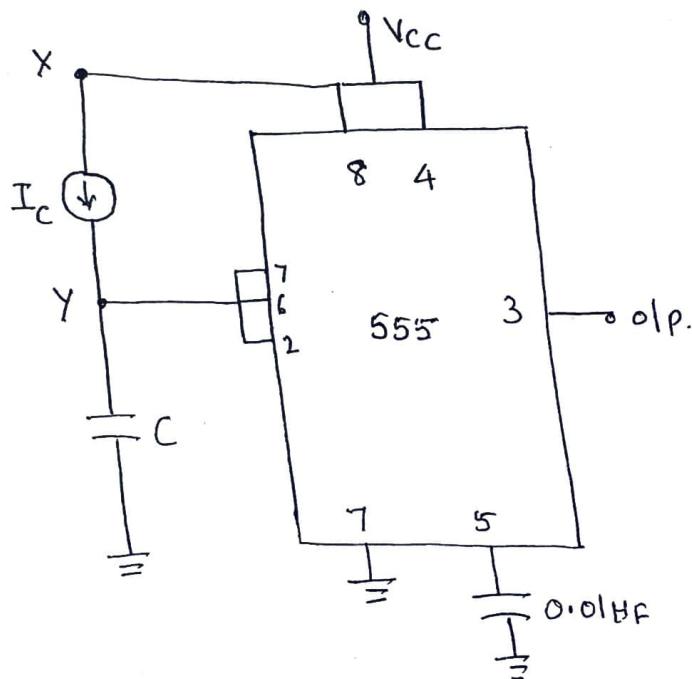
Sawtooth Generators

- When a capacitor is charged with constant current, the capacitor V_C is a ramp.

$$V_C(t) = \frac{1}{C} \int I dt$$

$$= \frac{I}{C} \cdot t \Rightarrow \text{Ramp } V_C$$

- In astable multivibrator, the capacitor is charged from a constant current instead of charging thru resistors.

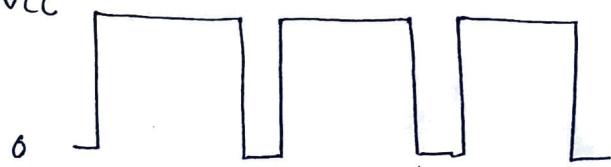


\Leftarrow Constant Current Source

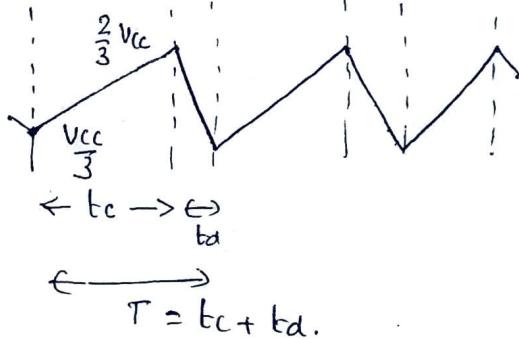
Fig (a) Sawtooth Generator

- To start with the capacitor gets charged with a constant current and the V_C across the capacitor rises linearly. and the op-amp is high.
- When the capacitor V_C exceeds $\frac{2V_{CC}}{3}$, output transistor goes to saturation.
- Now the capacitor discharges into saturated transistor. The discharge is quick since $R_{CE(sat)} \approx 0$. When the capacitor V_C falls below $\frac{V_{CC}}{3}$, output goes high, the transistor goes to cut-off.
- Once again the capacitor starts to charge through constant current source and the same cycle to operate repeat.

$V_O:$



$V_C:$



$$T = t_c + t_d$$

$$t_d \ll t_c$$

$$t_c \approx T$$

Consider the interval $0 \leq t \leq t_c$

$$\frac{1}{C} \int_0^{t_c} I_c dt = \Delta V_c = \text{change in capacitor } V_g.$$

$$\frac{I_c}{C} t_c = \frac{2}{3} V_{cc} - \frac{1}{3} V_{cc} = \frac{V_{cc}}{3}.$$

$$\therefore I_c \propto \underline{\underline{3/V_c}}$$

$$t_c = \frac{C V_{cc}}{3 I_c} \approx T$$

$$f = \frac{3 I_c}{C V_{cc}}$$

Schmitt trigger

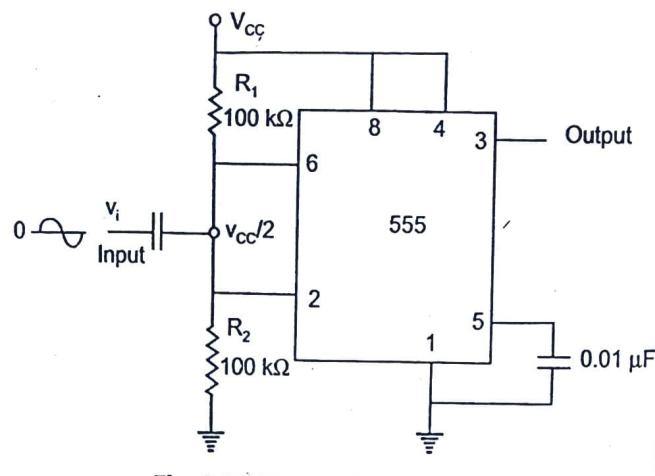
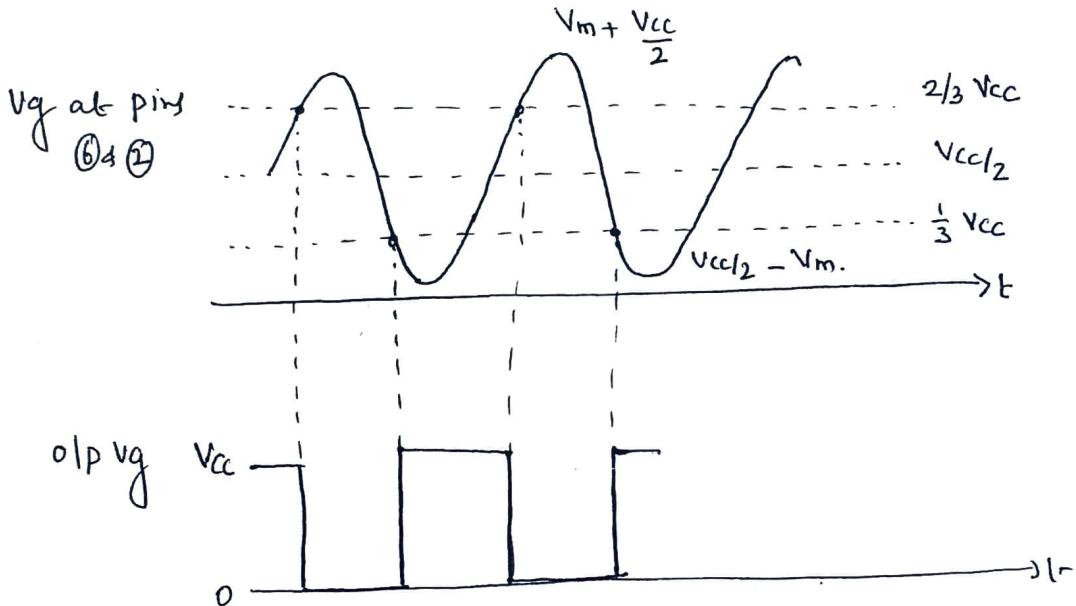


Fig (q) Schmitt trigger



- In 555 the trip point V_{gs} are $\frac{2V_{cc}}{3}$ and $\frac{V_{cc}}{3}$
and both are positive

- A $V_g \frac{V_{cc}}{2}$ derived from V_{cc} using equal potential divider is added to input which shifts the input above zero level.

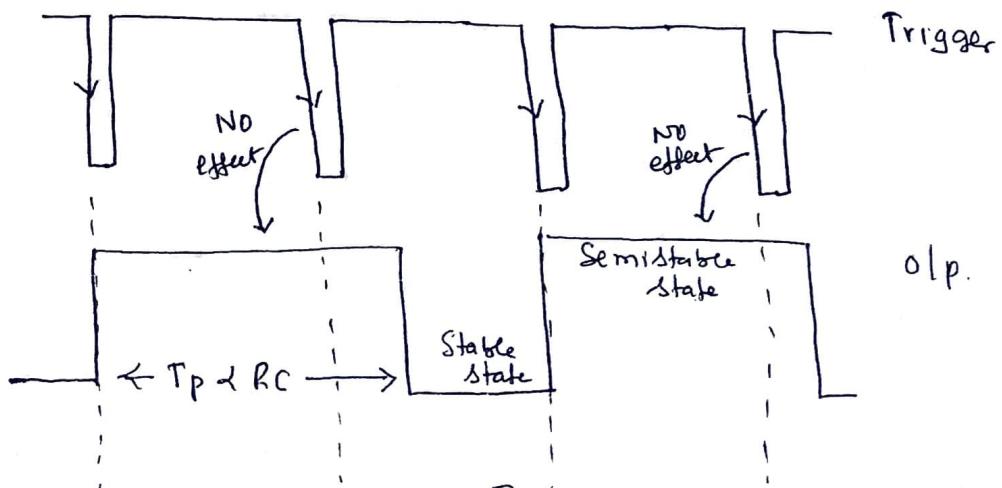
- When the resultant V_g exceeds $\frac{2}{3}V_{CC}$ o/p goes low
- When the resultant V_g falls below $\frac{1}{3}V_{CC}$ o/p goes high.
- For the circuit to work properly

$$V_m + \frac{V_{CC}}{2} > \frac{2}{3}V_{CC}$$

$$\Rightarrow V_m > \frac{V_{CC}}{6}$$

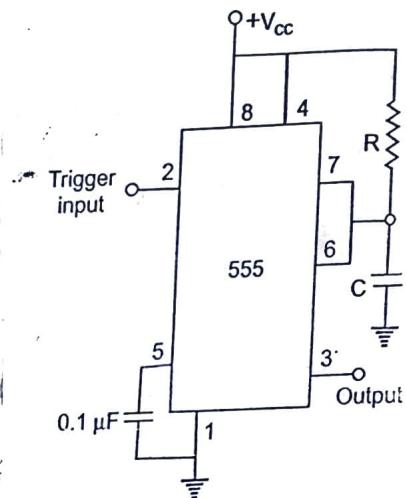
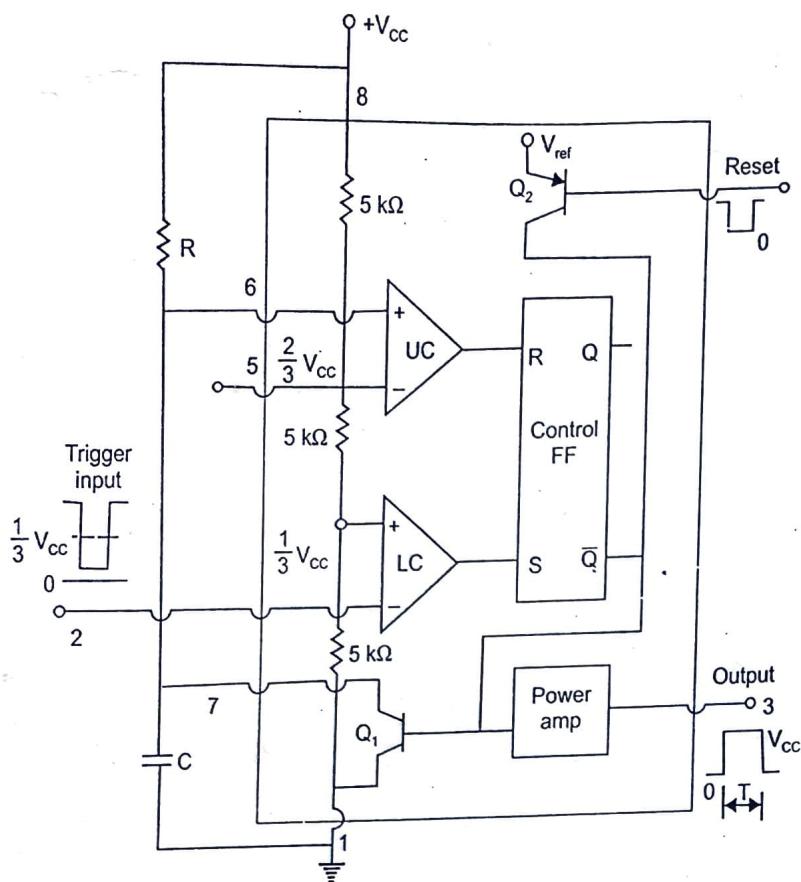
Monostable multivibrator | pulse generator | one shot | ^{Monoshot}

- In monoshot only one state is stable and other is semistable.
- when a trigger is applied it switches from stable state to semistable state and remains there for the time duration T_p , fixed by the product RC and returns back to stable state.
- Triggers applied before the completion of T_p has no effect



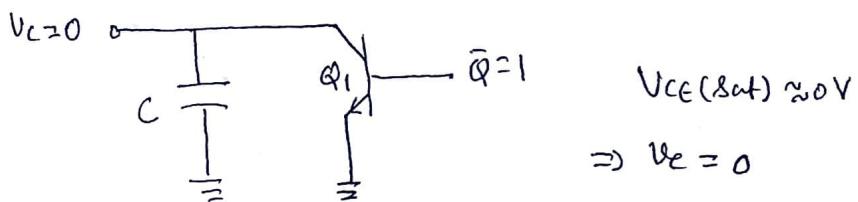
Fig(10) Monoshot waveforms.

Monostable Multivibrator using 555 Time



Fig(11) Monostable multivibrator using 555

- In the Stand by state op1 is zero. $\bar{Q} = 1$
and hence the discharge transistor is saturated.
The capacitor V_C is clamped at zero.



- When the trigger V_T falls below $\frac{V_{CC}}{3}$, the op1 of Low Compator goes high.

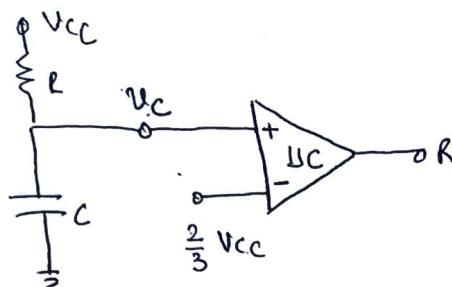
$$S=1, \quad Q=1, \quad \bar{Q}=0, \quad op1=1$$

Since $\bar{Q}=0$, the discharge transistor Q_1 goes off.

Now the capacitor gets charged towards V_{CC} through R . When the capacitor V_C exceeds $\frac{2}{3}V_{CC}$ the upper comparator output goes high.

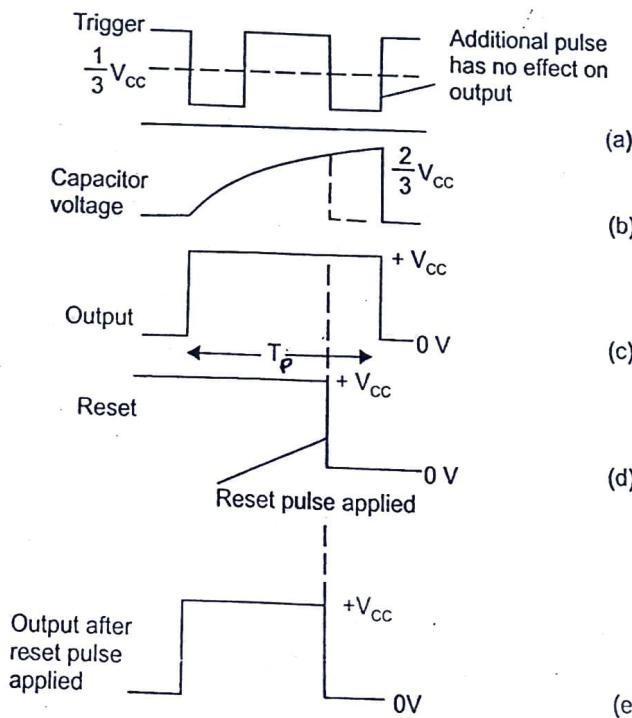
$$R=1, Q=0, \bar{Q}=1, Q_{UP}=0$$

Since $\bar{Q}=1$, discharge transistor Q_1 saturates and clamps the capacitor V_C at zero.



The op-amp remains at the stable state (zero) until next trigger is applied.

Expression for pulse width (T_p)



Fig(12) Wave forms

Expression for pulse width T_p .

$$V_c(t) = V_f + (V_i - V_f) e^{-t/RC}$$

$$V_f = V_{cc}, \quad V_i = 0$$

$$V_c(t) = V_{cc} - V_{cc} e^{-t/RC}$$

$$\text{at } t = T_p, \quad V_c(t) = \frac{2}{3} V_{cc}$$

$$\frac{2}{3} V_{cc} = V_{cc} - V_{cc} e^{-T_p/RC}$$

$$e^{-T_p/RC} = 1/3 \Rightarrow e^{T_p/RC} = 3$$

$$\Rightarrow T_p = 1.1 R C$$

Modified Circuit

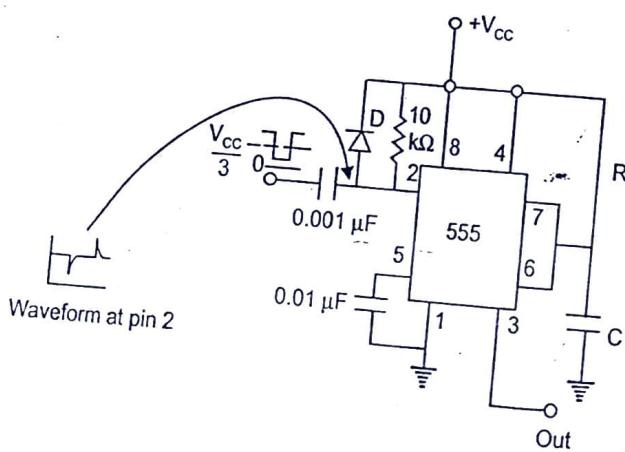
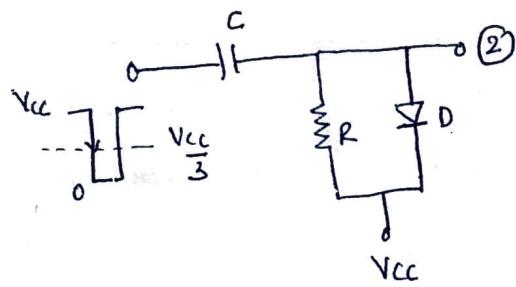


Fig (13) modified circuit



- R-C Differentiator converts biggest pulses into spike waveform



- Diode Conducts positive spikes and hence only negative spikes are applied at Pin (2)



Spikes act as effective triggers since they are sharp.

Ex 8

Design a monostable using 555 timer to produce pulse 85 width 1ms duration.

$$T_p = 1.1RC \approx 1\text{ms}$$

$$\text{Take } C = 0.1\text{HF}$$

Find R.

Ex 9

In a monostable $R = 10\text{k}\Omega$ $C = 1\text{HF}$

Calculate the Pulse width.

- Frequency Divider
- Linear Ramp generator.

Ref: Linear integrated Circuits

by

Roy Choudhury.

Phase Locked Loops (PLL)

- PLL is an important building block of linear systems.
- It was used in radar synchronization and communication applications in 1930. It was costly.
- Now PLL's are available in inexpensive monolithic IC's.
- PLL technique is ~~used~~ for electronic frequency control is used today in satellite communication systems, air ~~buses~~ ~~bus~~ borne navigation S/m/s, FM communication S/m/s, computers etc.

Basic Principles

The basic Block schematic of the PLL is shown in fig ①.

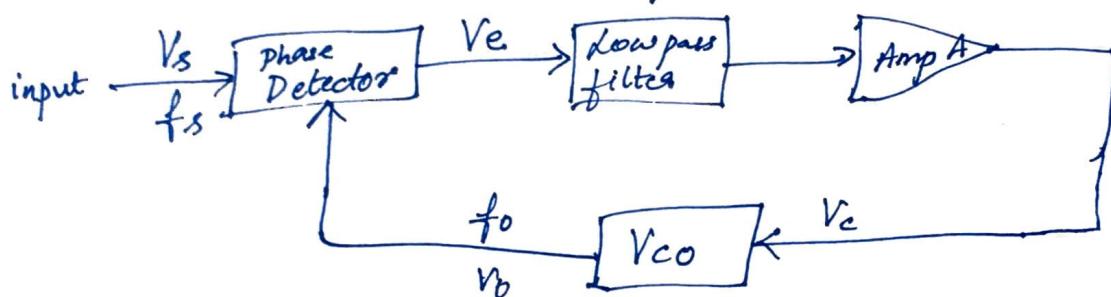


Figure 1: Block schematic of the PLL

This feedback system consists of

- Phase detector/comparator
- low Pass filter
- An error amplifier
- A Voltage Controlled Oscillator

- VCO is a free running multivibrator and (VCO) operates at a set frequency f_o called the free running frequency which is determined by external timing capacitor and external resistor.
- The frequency can be deviated by the dc control voltage, hence it is called Voltage controlled Oscillator

- If an input signal (v_s) of the frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO.
- If the two signals differ in frequency and/or phase an error voltage v_e is generated.
- Phase detector is basically a multiplier and produces the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its output
- High frequency component ($f_s + f_o$) is removed by the LPF.
- Low frequency component is amplified and then applied as control voltage v_c to VCO.
- The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o .
- The signal is in the capture range.
- The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. → Now the circuit is said to be locked.
- Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ .
- This phase difference ϕ generates corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thus maintains the lock.
- Once locked PLL tracks the frequency changes of the input signal.
PLL goes through three stages
 - Free running
 - Capture
 - locked or tracking.

10

PHASE-LOCKED LOOPS

10.1 INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

10.2 BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 10.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO).

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum ($f_s + f_o$) and difference ($f_s - f_o$) components at its output. The high frequency component ($f_s + f_o$) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_o . Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal

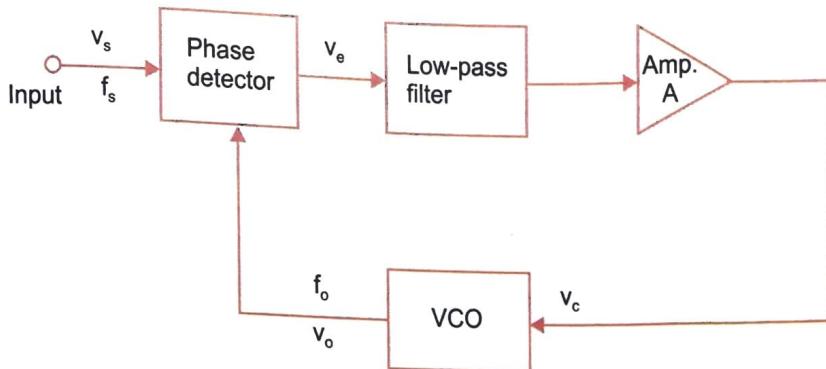


Fig. 10.1 Block schematic of the PLL

frequency. The circuit is then said to be locked. Once locked, the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ . This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 10.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_o , the VCO frequency.

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o .

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

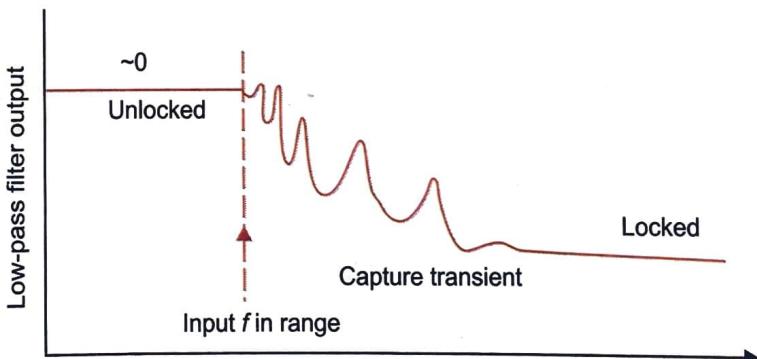


Fig. 10.2 The capture transient