

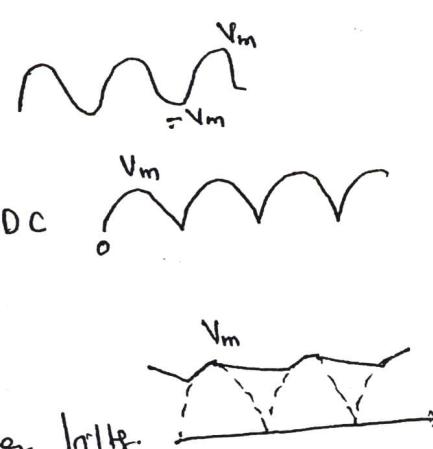
## Voltage Regulator

- A Voltage regulator is an electronic circuit that provides a stable dc voltage independent of
  - Load current
  - Temperature
  - AC line voltage variations.

## Need for Voltage regulators

All electronic equipments require a stable dc voltage for their proper operation.

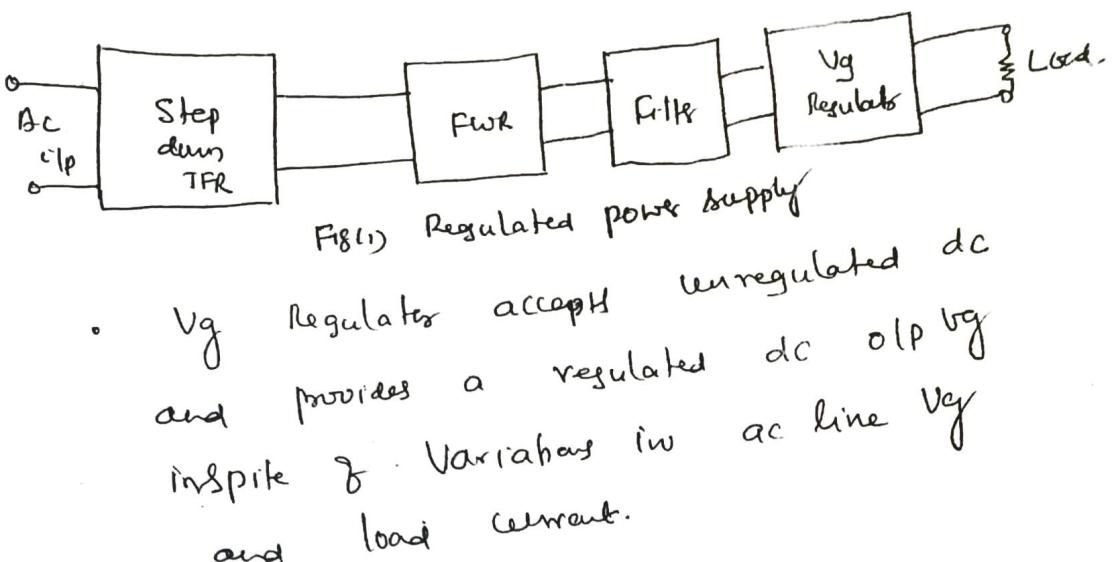
## How do we get DC Voltage

- Available source is AC
  - If it is rectified to obtain DC
  - This dc has ripple
  - Ripple is removed using filter.
- Observe that Variation in filter o/p is small  $\Rightarrow$  less ripple.
- 

The o/p of filter is unregulated dc since the dc  $V_o$  varies with load current and AC line  $V_L$ .



Block diagram of regulated power supply



- V<sub>g</sub> Regulator accepts unregulated dc and provides a regulated dc o/p V<sub>g</sub> inspite of variations in ac line V<sub>g</sub> and load current.

### Classification of Voltage Regulators

- Linear Voltage Regulator (Series Regulator)
- Switching Voltage Regulator (Switching Regulator)
- In linear Voltage Regulator the control element (BJT / FET) is operated in the active region or linear region
- In switching regulator the control element is operated as a switch (on/off) at high frequency.
- Switching Regulators are compact and efficient compared to linear Vg Regulators.

## Linear Voltage Regulator

The circuit consists of Reference voltage circuit, Error amplifier, Series pass transistor, feedback network

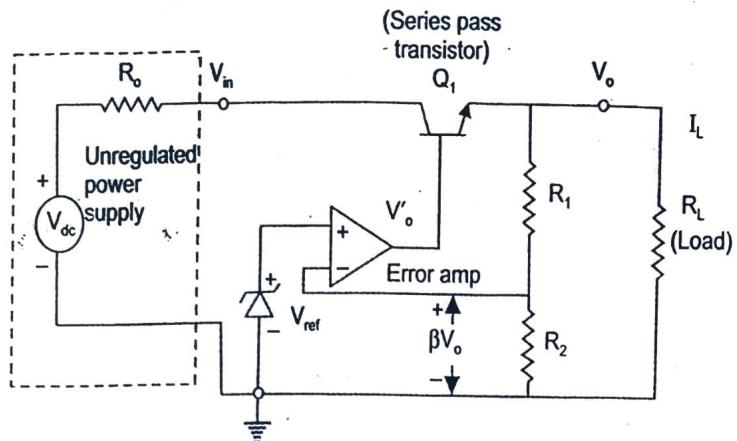


Fig.2. Linear Voltage regulator

- The Control element is  $Q_1$ , which is in series with the load

$\Rightarrow$  Series by Regulator.

The error amplifier output controls the conduction of  $Q_1$  to regulate the o/p by  $V_o$

$$\text{feed back by } V_f = V_o \left( \frac{R_2}{R_1 + R_2} \right) \\ = \beta V_o$$

Error Amplifier o/p,  $V_o' \propto (V_{ref} - V_f)$

- $Q_1$  transistor is also connected as an emitter follower and therefore provides the sufficient current gain to drive the load

## Regulating Action

### Regulation against Variation in $I_L$

If  $I_L \uparrow$

- $V_o \uparrow$
- $V_f = \beta V_o \uparrow$
- $V_o' \propto (V_{ref} - V_f) \downarrow$
- $I_{B1}, I_r \downarrow$
- $I_{C1}, I_{E1} \downarrow$
- $I_L \downarrow$
- $V_o \downarrow$   $\rightarrow$  thus the increase in  $V_o$  is nullified.

If  $I_L \downarrow$

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### Regulation against Variation in $V_{in}$

If  $V_{in} \uparrow$

- $V_{C1} \uparrow$
- $I_{C1}, I_{E1} \uparrow$
- $I_L \uparrow$
- $V_o \uparrow$
- $V_o \downarrow$

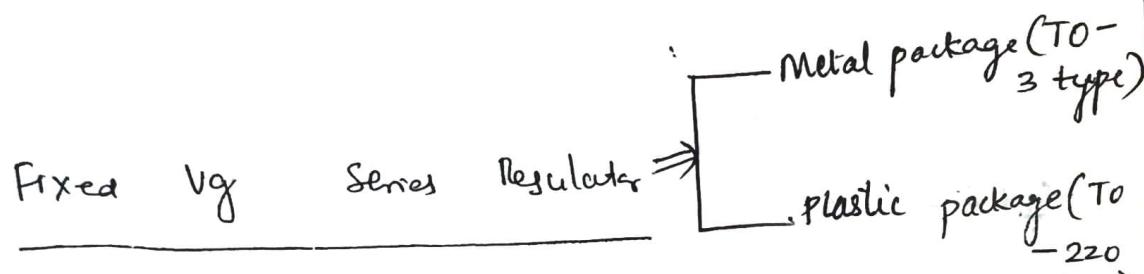
If  $V_{in} \downarrow$

## Ic Voltage Regulators

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- With advances in microelectronics it became possible to incorporate the regulator circuit on a monolithic silicon chip.
  - Examples of monolithic regulators are 78XX/79XX series.
    - This results in and 723 general purpose regulators.
- low cost
  - High reliability
  - Reduction in size
  - Excellent performance.



78XX

79XX

78  $\Rightarrow$  +ve o/p V<sub>o</sub>

79  $\Rightarrow$  -ve o/p V<sub>o</sub>  
Complements to the  
78XX series devices

XX represents  
o/p V<sub>o</sub> value.

V<sub>o</sub> options available

5, 6, 8, 12, 15, 18, 24V

Same as in 78XX

Ex: 7805, 7812, 7824

indicates a 12V  
regulator

with two extra V<sub>o</sub>'s  
-2V & -5.2V.

Ex 7905, 7902,  
7914 ...

Both are three terminal  
Regulators.

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### Three terminal positive $V_g$ regulator

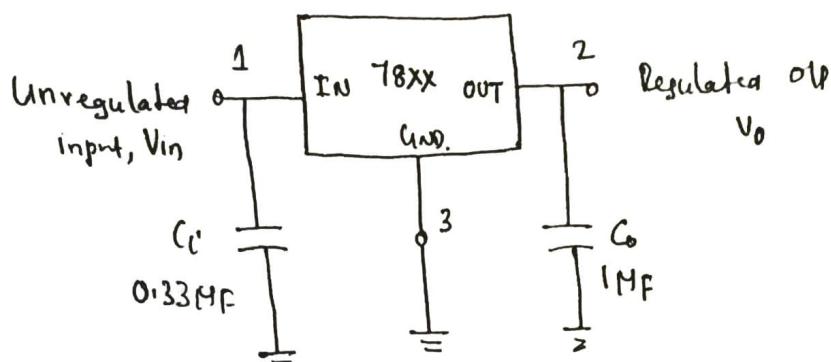


Fig 3. Three terminal regulator

- $C_1$  is connected between pin 1 & ground to cancel the inductive effects due to long distribution lead.
- $C_2$  improves transient response.

$V_{in(\text{max})} : 35V \text{ for } 5 \text{ to } 18V \text{ Regulator}$

$40V \text{ for } 24V \text{ Regulator.}$

$V_{in(\text{min})} : 2V + |V_o| \text{ Regulated}$

$\uparrow$   
drop out  $V_g$

For ex : For 7805

$$|V_o|_{\text{Reg}} = 5V$$

$$V_{in(\text{min})} = 2 + 5 = 7V, \quad V_{in(\text{max})} = 35V,$$

$$I_o(\text{max}) = 1A.$$

## Characteristics

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There are four characteristics of a three terminal IC regulators

- (1)  $V_o$  : The regulated output voltage is fixed at a value as specified by the manufacturer.
- (2)  $|V_{in}| \geq |V_o| + 2V$  : The unregulated input voltage must be atleast  $2V$  more than the regulated output voltage.  
Ex:- If  $V_o = 5V$  then  $V_{in} = V_o + 2V = 7V$   
 $\uparrow$   
drop out voltage
- (3)  $I_{o\ max}$  :- the load current may vary from 0 to rated maximum output current. (~~1A~~). The IC is usually provided with a heat sink.
- (4) Thermal shutdown :- The IC has a temperature sensor built in which turns off the IC when it becomes too hot (usually  $125^\circ C$  to  $150^\circ C$ ). The output current will drop and remains there until the IC has cooled significantly.

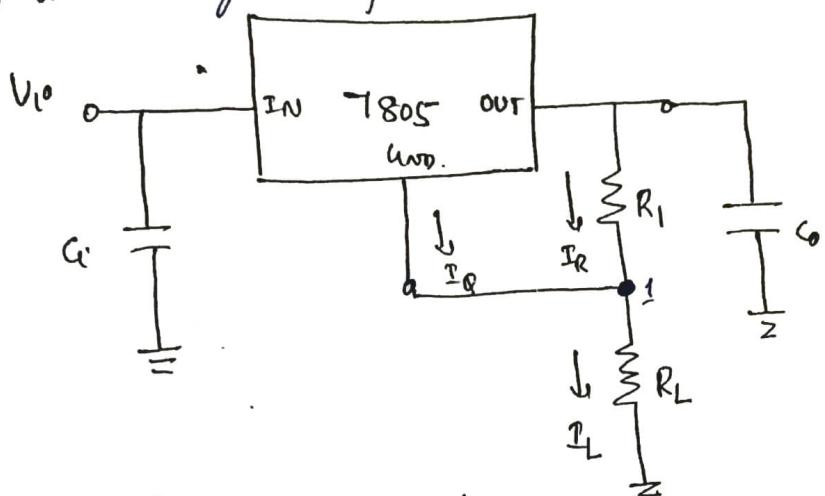
Line / Input Regulation :- It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the o/p voltage. The typical value of line regulation for 7805 is  $3mV$

Load Regulation It is defined as the change in output voltage for a change in load current and is also expressed in mV or as a percentage of  $V_o$ . The typical value of load regulation for 7805 is  $15mV$  for  $5mA < I_o < 1.5A$ .

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## Current Source using 78xx

The three terminal fixed voltage regulator can be used as a current source. Figure(4) shows the circuit when 7805 has been wired to supply a current of 1 ampere to a  $10\Omega$ , 10 watt load.



Fig(4). Current source

Given  $I_{L4} = 5V$   
Apply KCL at node ①

$$I_L = I_Q + I_R$$

$I_Q$  = Quiescent current.

$$= 4.2mA \text{ for } 7805$$

$$I_Q \ll I_L$$

$$\Rightarrow I_L \approx I_R = \frac{5V}{R_1}$$

$$\text{If } I_L = 1A, \quad R_1 = 5\Omega$$

~~But~~  $R_L = 10\Omega$

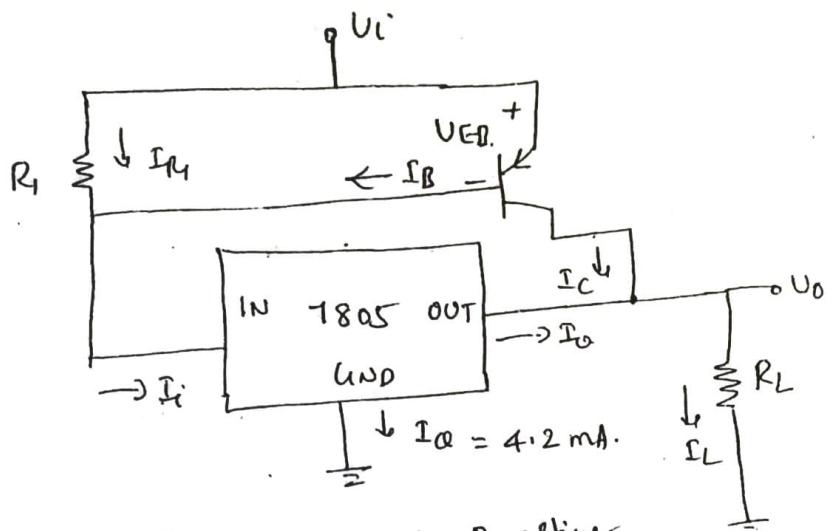
$I_L$  is independent of  $R_L$ .

How much  $V_{10}$  is needed?

Ex: Try with 7812 for a load current of 0.5A into  $10\Omega$  load.

## Cu. Boosting in 78xx and 79xx

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Fig(5) Current Boosting

\* For the regulator,  $I_i = I_o + I_q \approx I_o$ .

$$* I_{R_1} + I_B = I_i \Rightarrow I_{R_1} \approx I_i \approx I_o.$$

$$* U_{EB} = I_{R_1} R_1 = I_o R_1 \quad \text{--- (1)}$$

For the transistor to turn on

$$I_{DN} \geq 0.7 \text{ V.}$$

\* Let us limit  $I_o$  to 100 mA.

$$R_1 = \frac{0.7 \text{ V}}{0.1 \text{ A}} = 7 \Omega$$

\* For  $I_L < I_o$ ,  $\alpha$  is off

For  $I_L > I_o$ ,  $\alpha$  is on

$$I_L = I_o + I_C.$$

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If the load demands current  $> 100mA$ ,

If comes from the  $T_{Xr}$ .

Applying KCL at  $V_o$  node

$$I_L = I_C + I_0 \quad \text{--- (2)}$$

~~Also~~

$$I_C = \beta I_B$$

$$I_L = \beta I_B + I_0 \quad \text{--- (4)}$$

$$I_0 \approx I_{L0}$$

$$I_B = I_i - I_R$$

$$I_B = I_0 - \frac{V_{BE}}{R_L} \quad \text{--- (3)}$$

Sub (3) in (4)

$$I_L = \beta \left[ I_0 - \frac{V_{BE}}{R_L} \right] + I_0$$

$$I_L = (1 + \beta) I_0 - \beta \frac{V_{BE(\text{cm})}}{R_L}$$

For 7805,  $I_{out} = 1A$

$$V_{BE(\text{cm})} = 1V$$

$$\text{If } \beta = 15$$

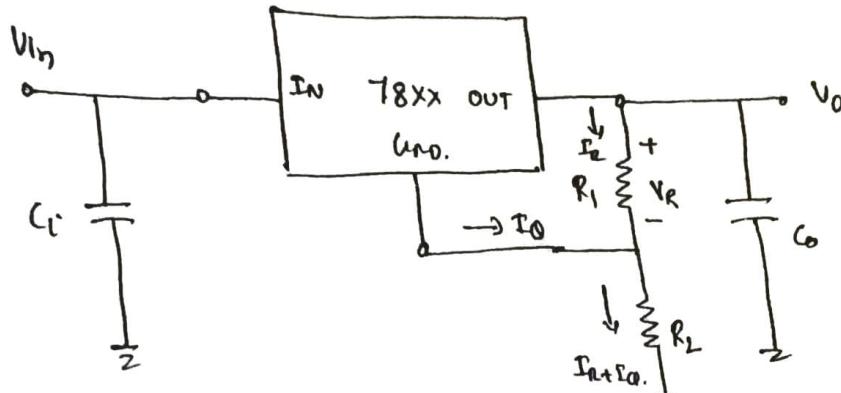
$$I_L = 13.8 A.$$

~~Output~~ ~~current~~.

Problem

- Q For the fig(3). Let  $V_{BE(\text{cm})} = 1V$ ,  $\beta = 15$ , calculate the output current coming from 7805 and  $I_C$  coming from transistor Q<sub>1</sub> for loads  $100\Omega$ ,  $5\Omega$ ,  $1\Omega$

Variable  $V_{QF}$  using 78xx



Fig(6) Variable Voltage using fixed  $V_QF$   
7805 gives 5V o/p  
7806 gives 6V o/p.

How to obtain a  $V_QF$  between 5 & 6V?

$$V_O = I_R R_1 + (I_R + I_Q) R_2$$

Neglecting  $I_Q$ .

$$V_O = I_R (R_1 + R_2)$$

$$I_R = \frac{V_R}{R_1}$$

$$\Rightarrow V_O = V_R [1 + R_2/R_1]$$

Ex: To obtain 5.4V using 7805

$$5.4 = 5 (1 + R_2/R_1) = I_R (R_1 + R_2)$$

Choose  $I_R \gg I_Q$

~~$R_2/R_1 \approx 0$~~

Let  $I_R = 25\text{mA}$

At this  $R_2$  and final  $I_2$ .

$$I_R = \frac{V_R}{R_1}$$

$$R_1 = ?$$

## Dual power Supply

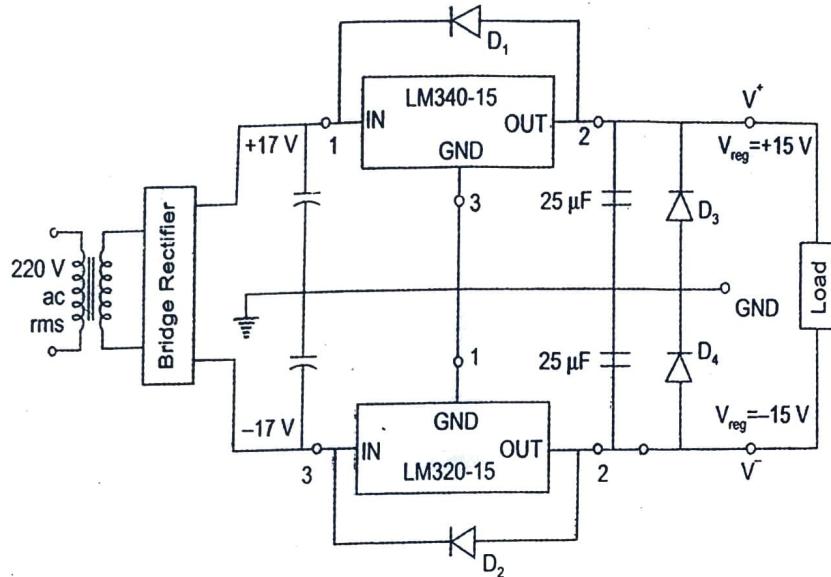


Fig (7) Dual power supply

- Many discrete and IC Circuits require dual power supply. Ex: Op-Amp.
- LM340-15 is a +15V o/p Regulator
- LM320-15 is a -15V o/p Regulator.
- We can also use 7815 and 7915 ICs.
- D<sub>1</sub> and D<sub>2</sub> protect the regulator against short circuit occurring ~~between the two~~ at its input terminals.
- D<sub>3</sub> & D<sub>4</sub> provide protection against the situation when both the regulators may not turn on simultaneously.

- If there is a load between the two outputs, the faster one will try to reverse the polarity of the other and cause it to latch up unless it is properly clamped.
- The clamping function is done by the diodes under normal operating conditions, both diodes will be reverse biased and will no longer have any effect on the circuit.
- LM325H is a dual tracking  $\pm 15V$  supply and can furnish current upto 100mA.
- An op-amp draws less than 5mA current.  
Hence LM325H can drive the circuit consisting of 20 op-amps.

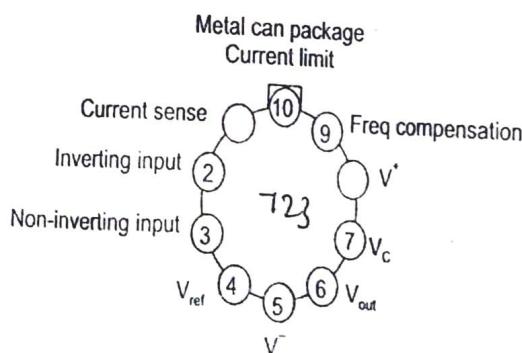
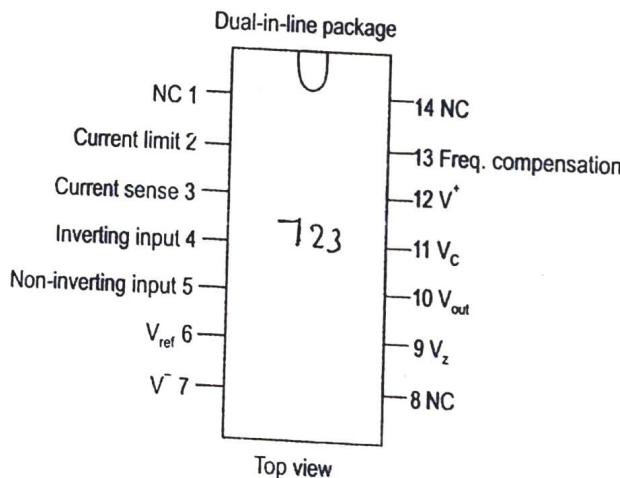
### Limitations of three terminal regulators

- No short circuit protection.
  - output  $V_{\text{G}}$  is fixed.
- These limitations ~~are~~ have been overcome in the 723 general purpose regulator.

# 723 General purpose Regulators

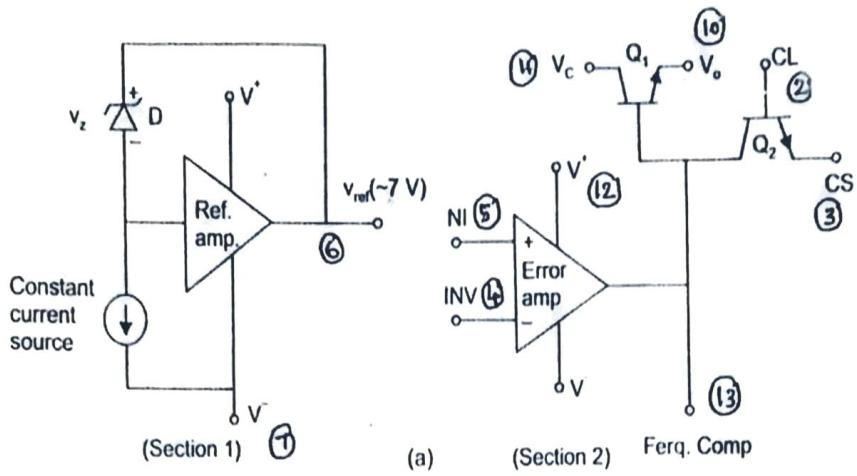
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- Output voltage can be adjusted over a wide range of both +ve or -ve regulated V<sub>o</sub>.
- V<sub>o</sub> : 2 to 7V → low voltage regulator
- V<sub>o</sub> : 7 to 37V → High voltage regulator
- I<sub>o</sub> (max) : 150 mA
- Externally boosted up to 5 Amp.
- Internal ref. V<sub>g</sub> : 7.15V
- V<sub>in</sub> (max) : 40V
- Available as 14 pin DIP & 10 pin metal can.



(e) Fig (8) 723 I.C packages

# Fenchannel Block diagram



Fig(9) Fenchannel Block diagrams 9/723

## Section (1)

- Zener Diode, Constant current source and reference amplifier produces a fixed  $V_g$  of  $7.15\text{ V}$  at pin 6

The Constant current source forces the zener diode to operate at a fixed point. So that the zener outputs a fixed  $V_g$ .

## Section (2)

- Error amplifier compares a part or full of o/p  $V_g$  at inverting input with  $V_{ref}$  applied at non inverting input
- O/p of Error amplifier controls the conduction of series pass transistor  $Q_1$

# Low voltage regulator using 723

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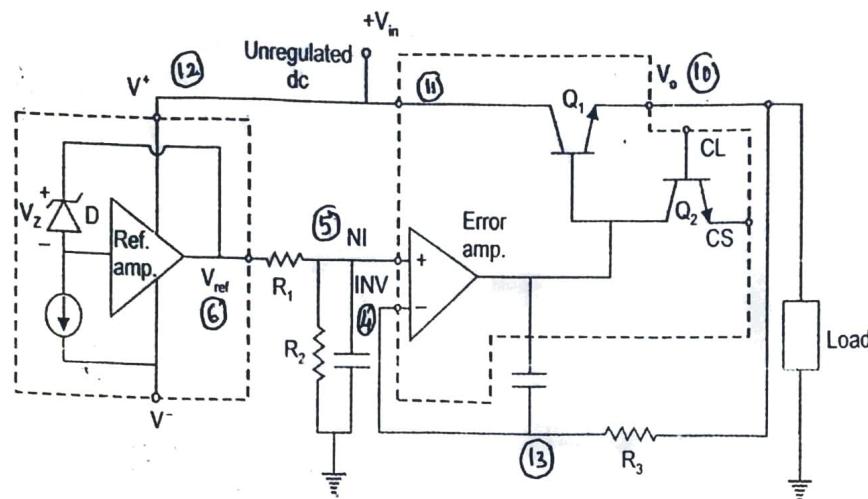


Fig (I) 723 low vg regulator. functional diagram.

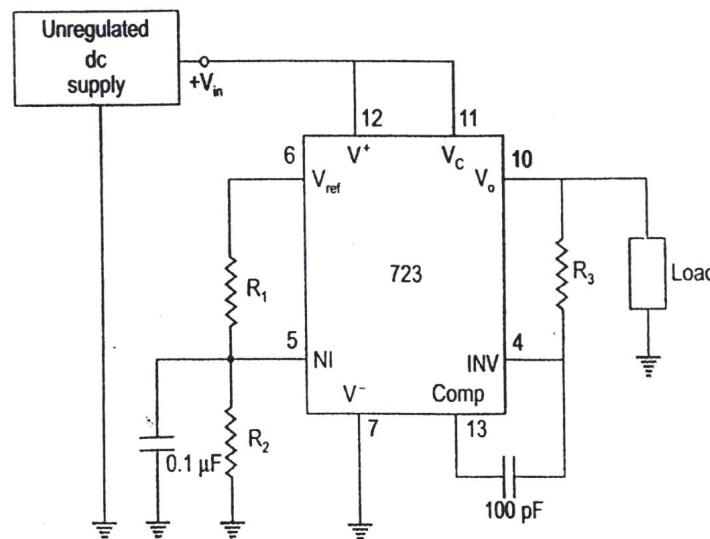
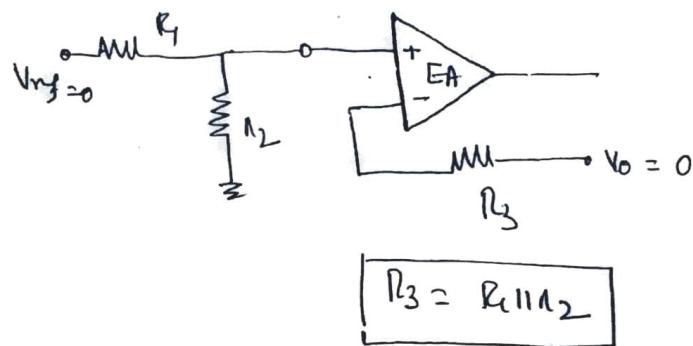


Fig (II) Ckt of low vg regulator using 723.

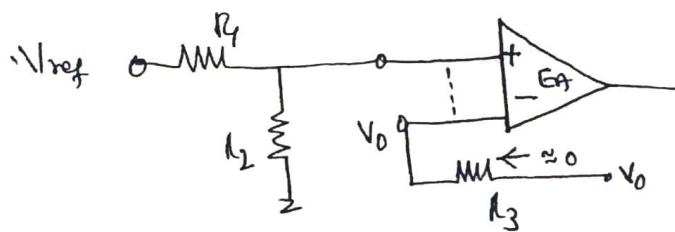
- A loop filter capacitor is recommended between pin 4 and 13 for stability purpose.
- A 0.1MF capacitor is recommended between pin 5 and ground for suppression of noise by

- V<sub>ref</sub> is divided using V<sub>g</sub> divider into R<sub>1</sub> and R<sub>2</sub> and the V<sub>g</sub> across R<sub>2</sub> is applied to N1 terminal of Error amplifier.
- Entire A<sub>op</sub> is applied to INV 111 via R<sub>3</sub>.
- R<sub>3</sub> is used to obtain minimum drift due to offset current effect.



Expression for Regulated op-amp V<sub>g</sub> V<sub>0</sub>

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Due to Virtual short at the input of EA

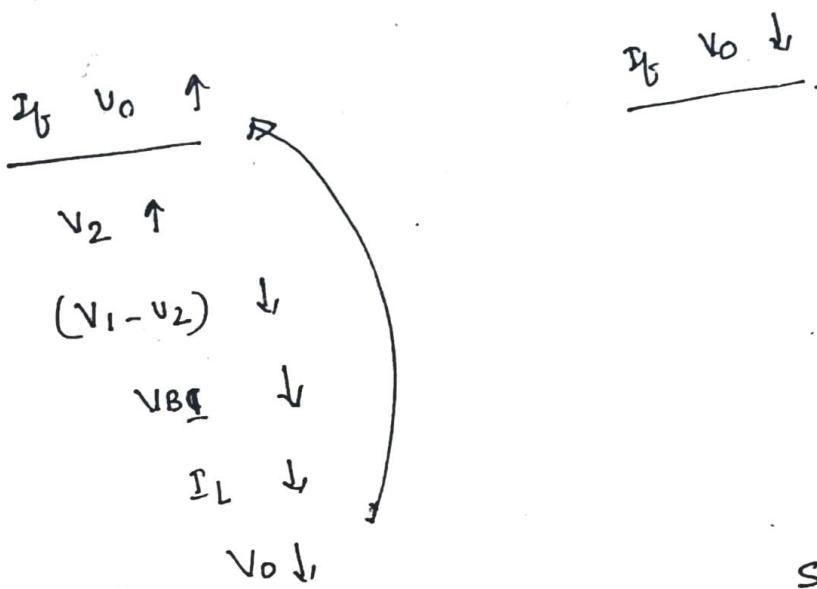
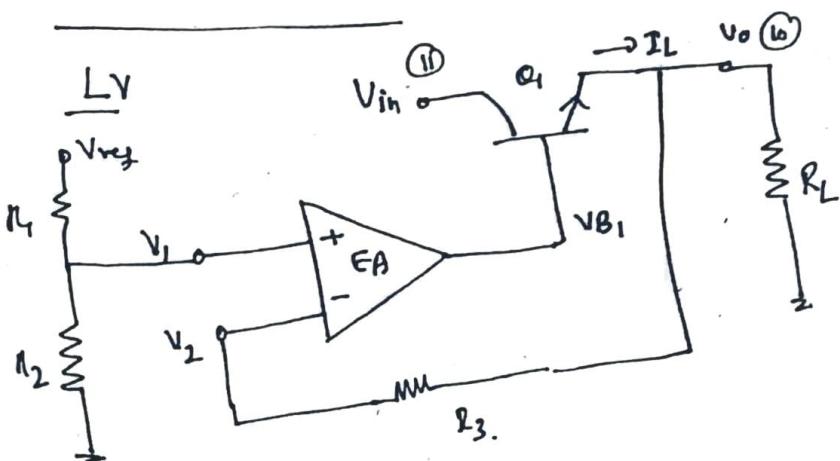
$$V_0 = V_{ref} \frac{R_2}{R_1 + R_2}$$

$$V_0 = 7.15 \left[ \frac{R_2}{R_1 + R_2} \right]$$

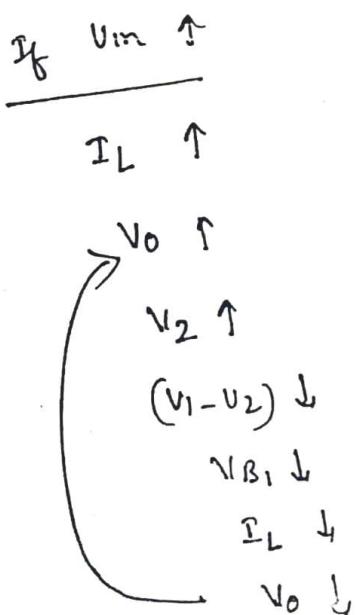
Note that  $V_0 < 7.15\text{V}$

Hence low  $\text{I}_{op}$  regulator.

## Regulating Action



Similar explain  
for HV.



# Higher Voltage Regulator

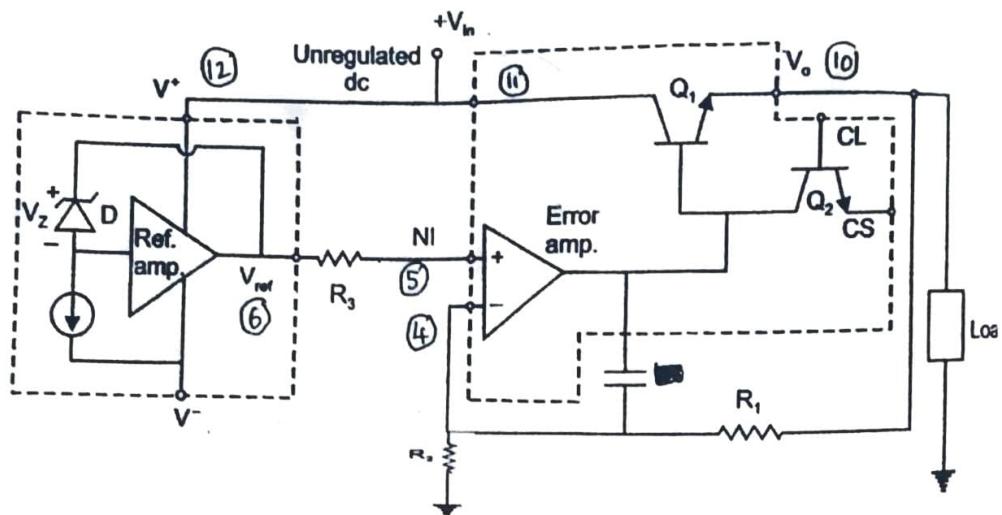
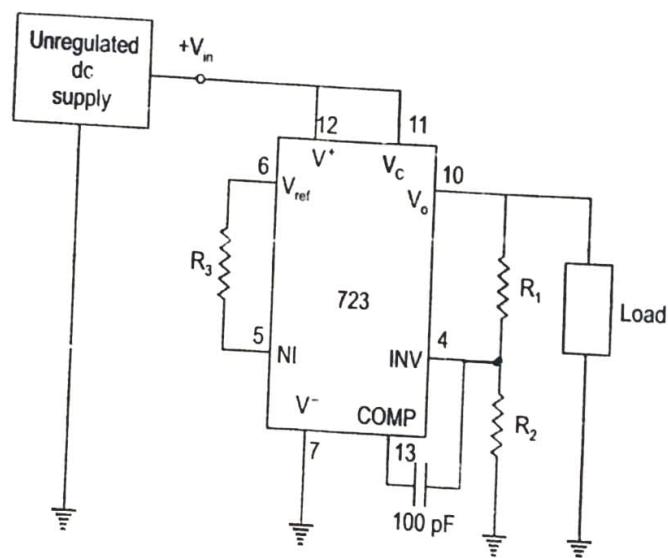


Fig (12) High voltage regulator using  
two channel diagram.



Fig(13) Circuit diagram of high voltage regulator

to 4710 723 V 100 pF

- potential divider  $R_1 - R_2$  is connected between output pin (10) and ground.  $V_g$  across  $R_2$  is applied to Inv chip.
- $R_3$  is used for minimum drift between pin 5 and 6.  $R_3 = R_1 \parallel R_2$ .
- Due to virtual short at the input of EA

$$V_{ref} = V_o \frac{R_2}{R_1 + R_2}$$

$$V_o = V_{ref} \left[ 1 + \frac{R_1}{R_2} \right]$$

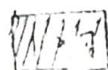
$$V_o = 7.15 \left[ 1 + 1/(12) \right]$$

Note that  $V_o > 7.15V$

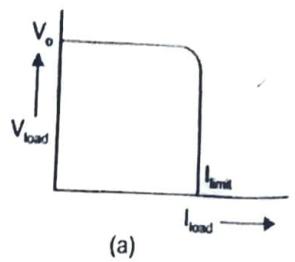
Hence high  $V_g$  regulator.

### Current limit protection

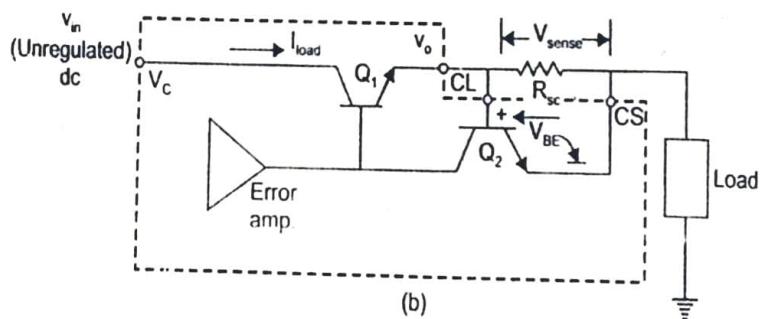
- The ICs of LV and HV regulators have no protection.
- If the load demands more current, the IC tries to provide it at a constant old  $V_g$
- As a result the IC gets hotter and ultimately burn out.



- Current limiting refers to the ability of a Cuk to prevent the load current from increasing above a preset value.
- In a current limited power supply the output voltage remains constant for a load current below  $I_{\text{limit}}$ .
- As current approaches  $I_{\text{limit}}$  the op-amp voltage drops thus reducing power dissipation



### Current limit protection circuit



Fig(14) current limit protection  
circuit

The current limit  $I_{\text{limit}}$  is set by connecting an external resistor  $R_{\text{sc}}$  between the terminals  $C_L$  and  $C_S$ .

$$V_{\text{sense}} = I_L R_{\text{sc}}$$

For  $V_{\text{sense}} < 0.5 \text{ V}$

$Q_2$  is off  $\Rightarrow$  no current limit action.

$R_{\text{sc}}$  is selected such that

$$I_{\text{limit}} \cdot R_{\text{sc}} = 0.5 \text{ V}$$

• When  $I_L > I_{limit}$

• when  $I_L > I_{limit}$

$$I_L R_{sc} > 0.5V$$

$Q_2$  turns ON

•  $V_{C_2} \downarrow \Rightarrow V_{B_1} \downarrow$

•  $I_{B_1} \downarrow, I_{E_1}, I_{C_1}, I_L \downarrow$

$$I_L R_{sc} < 0.5V$$

•  $Q_2$  goes OFF

Thus load current cannot exceed  $I_{limit}$ .

Low Voltage Regulator with Current limit Protection

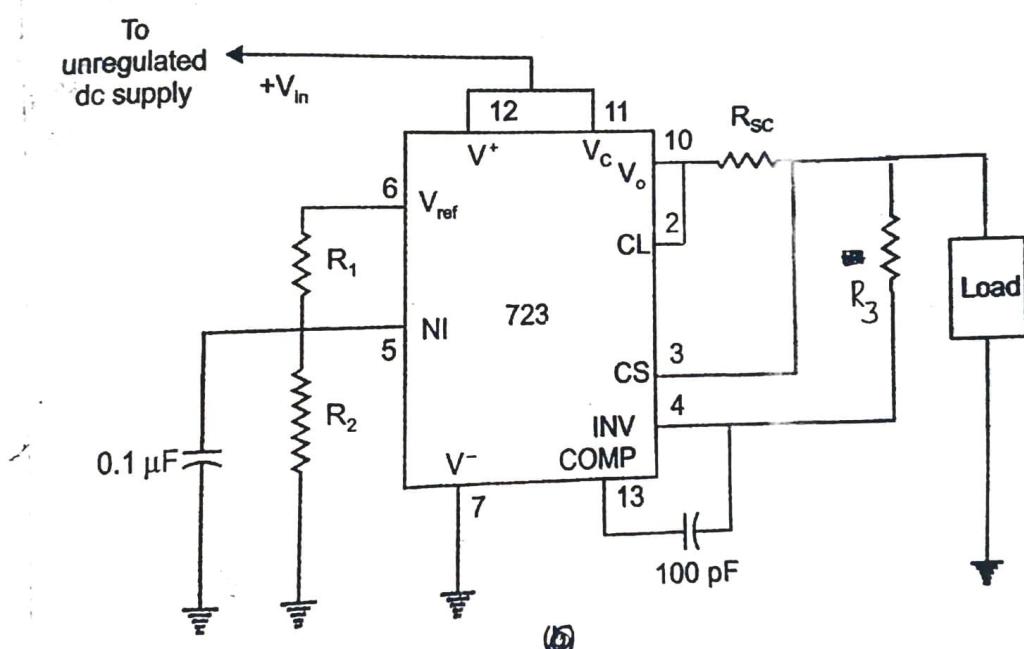


Fig 15. Circuit of low voltage regulator with current limit protection.

(25)

## Design equations for low voltage regulators

- $V_o = V_{ref} \left[ \frac{R_2}{R_1 + R_2} \right]$

- $V_{ref} = 7.15V$

- $R_3 = R_1 \parallel R_2$

$V_{in} > 7.15V$  for LV regulator

$V_{in} > V_o$  for HV regulator.

- $R_{SC} = \frac{V_{sense}}{I_{limit}} = \frac{0.5V}{I_{limit}}$

- Wattage of  $R_{SC} > (I_{limit})^2 \cdot R_{SC}$

- Loop FF Cap between 13 & 4 for stability

- 0.1 HF Cap across  $R_2$  for noise suppression.

## High Voltage Regulator with current limit protection

$$V_o = V_{ref} [1 + R_1/R_2]; \text{ other equations remain the same.}$$

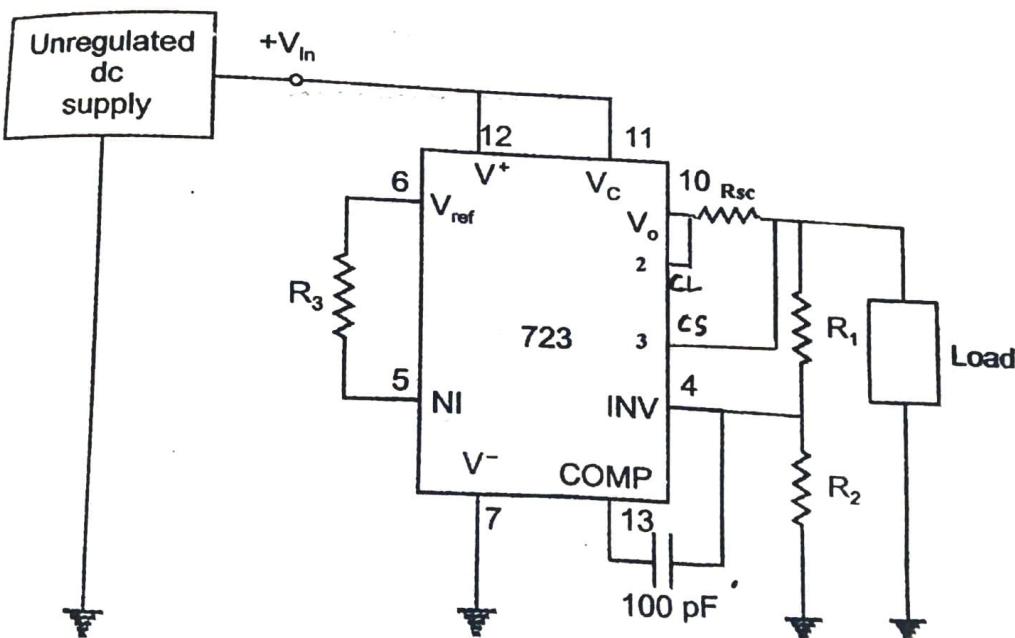


Fig 16. Circuit of high voltage regulator with current limit protection

(24)

**Ex:1** Design a VG regulator using 723 to meet the following specifications.

$$V_0 = 5V$$

$$I_L = 120mA$$

The circuit must be short cut protected.

Suggest a suitable  $V_{1^o}$ .

**Ex2** Ref the circuit of Fig 15.

$$R_1 = 10k\Omega \quad R_2 = 5k\Omega$$

a) Calculate  $V_0$

b) Find  $R_L$  for  $I_L = 130mA$

c) Calculate  $R_3$

d) Find  $R_{BC}$  and the wattage to limit the load current at  $130mA$

e) Suggest a suitable  $V_{1^o}$ .

**Ex3** Repeat Ex1 for  $V_0 = 15V$ .

**Ex4** Repeat Ex2 for the circuit of Fig 16.

(25)

Current Boosted in low voltage regulator

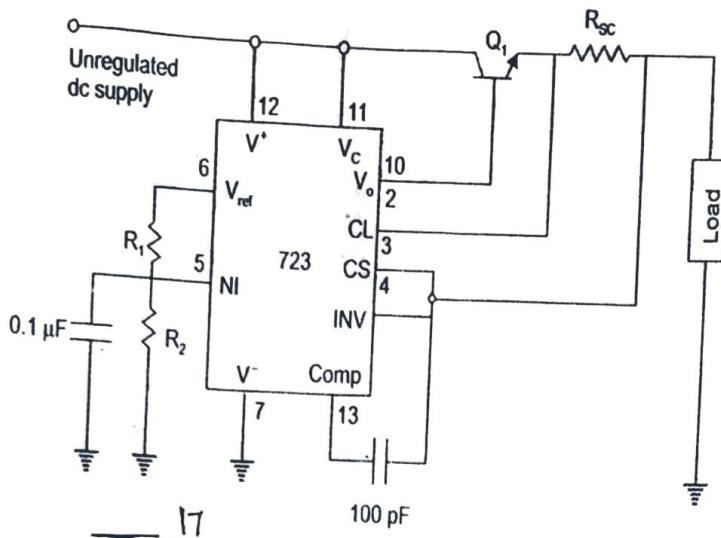


Fig. 25.1 Current boosted low voltage regulator

- Max current o/p from 723 is 140mA.
- For applications requiring load current greater than 140mA, current boosting is necessary. This is done using an external transistor  $Q_{ext}$ .
- The base current for  $Q_{ext}$  is o/p current of 723.
- $I_L = I_E(ext) = \beta \times I_o(723)$

If  $\beta = 25$  and  $I_o(723)$  is limited to 100mA then

$$I_L = 25 \times 0.1A = 2.5A$$

~~Ans~~

Ex 5

Ref. the circuit of Fig 17.

$$R_f = R_2 = 10\text{k}\Omega$$

(a) Calculate  $V_o$

(b) Find  $R_L$  and its voltage for a load current of 2A.

(c) Choose suitable  $R_{SC}$  such that  $I_0(723)$  is limited to 100 mA and  $I_L$  is limited to 2A.

(d) Suggest a suitable  $V_i$

Hint (c)

$$\beta = \frac{I_{Limit}}{I_0(723)} = \frac{2\text{A}}{0.1\text{A}} = 20$$

choose tx with  $\beta = 25$

$$R_{SC} = \frac{0.5\text{V}}{I_{Limit}} = \frac{0.5\text{V}}{2\text{A}} = 0.25\Omega$$

Voltage of  $R_{SC} > (I_{Limit})^2 \times R_{SC}$ .

Additional

- Draw the circuit of HV regulator with current boosting.

Ex 6

Repeat examples for HV regulator with current boosting.

## Current fold back.

(27)

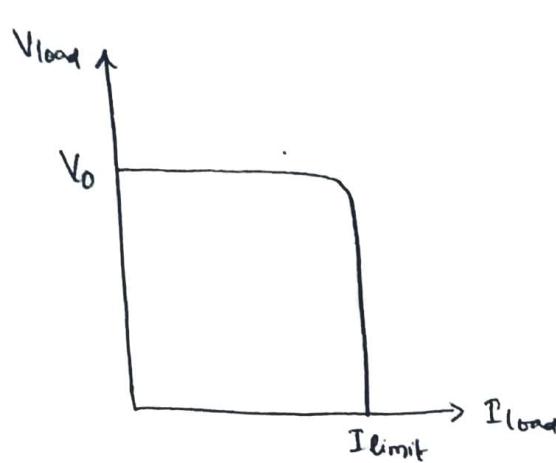
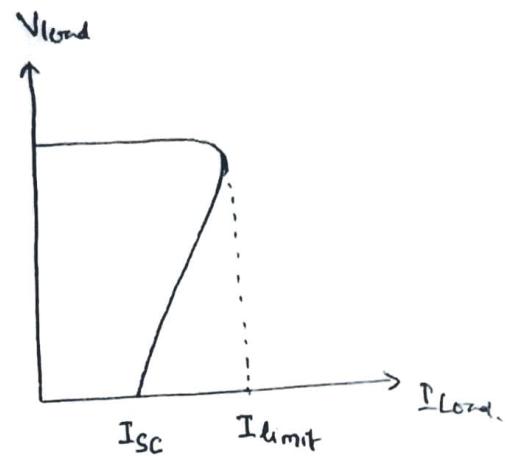


Fig 18 (a) current limiting



(b) current fold back.

- In current limiting technique, the load current is maintained at a preset value and when the over load condition occurs, the o/p v<sub>o</sub> drops to zero.
- If the regulator is short circuited, the regulator has to carry maximum current.
- To protect the regulator current fold back is used.
- In fold back current limiting both o/p v<sub>o</sub> and o/p current decreases when the load current exceeds a preset level I<sub>limit</sub>.
- When the load is short circuited  $v_o \rightarrow 0$
- $I_{load} \rightarrow I_{sc}$
- Note that  $I_{sc} < I_{limit}$ .

# Low voltage regulator using current fold back.

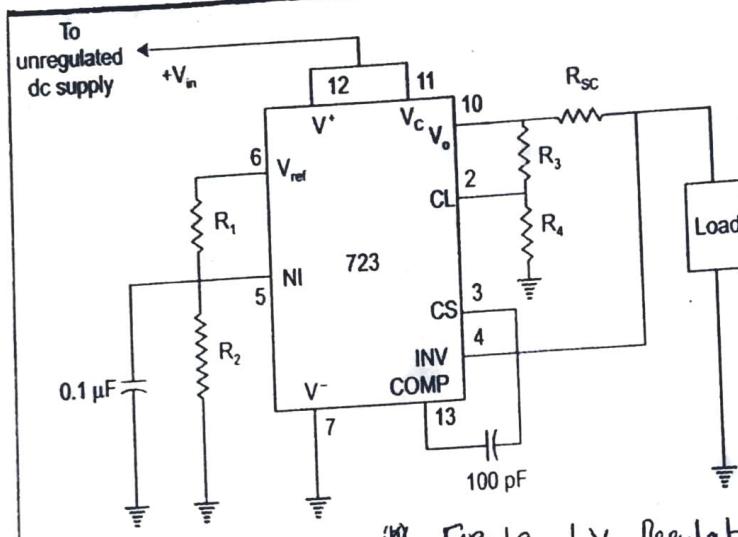


Fig 19 LV Regulates Using  
Current fold back

$$I = \frac{V_A}{R_3 + R_4} ; \quad V_{B2} = \frac{V_A R_4}{R_3 + R_4} = K V_A$$

$$K = \frac{R_4}{R_3 + R_4} ; \quad V_A = I_L R_{SC} + V_o$$

$$\therefore V_{B2} = K [ I_L R_{SC} + V_o ]$$

$$V_{BE2} = V_{B2} - V_o = K I_L R_{SC} + (K-1) V_o$$

$$I_L = \frac{V_{BE2}}{K R_{SC}} + \frac{(1-K) V_o}{K R_{SC}}$$

when Load is short circuited,  $V_o \rightarrow 0$

$$I_L = \frac{V_{BE2}}{K R_{SC}} = I_{SC}$$

$$\therefore I_L = I_{SC} + \frac{(1-K) V_o}{K R_{SC}} > I_{SC}$$

$K$  is selected such that  $I_{limit}$  is 2 to 3 times  $I_{SC}$ .

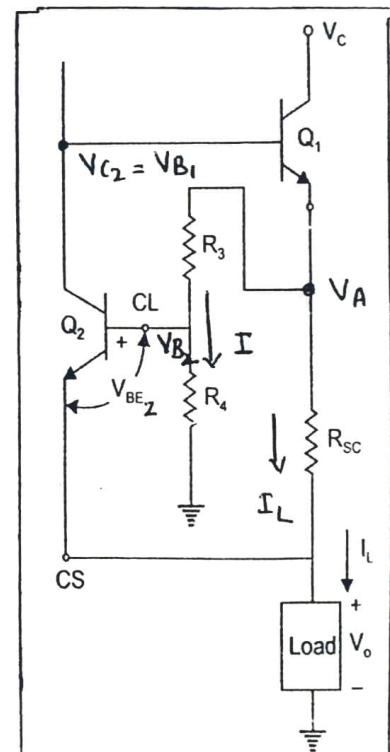


Fig (20) Current fold back circuit.

## Working of current limiting circuit

- When the load current increases to a large value
  - $V_A \uparrow \Rightarrow V_{B_2} \uparrow, V_{BE_2} \uparrow$
  - When  $V_{BE_2}$  becomes 0.5V,  $Q_2$  starts conducting.
  - $V_{C_2} \downarrow, V_{B_1} \downarrow$
  - Conduction of  $Q_1 \downarrow$
  - $I_L \downarrow, V_o \downarrow, V_B \downarrow$
  - $V_{B_2} = k [V_A] \quad V_{B_2} \downarrow$  by a small amount  
Compared to  $V_o$
  - $V_{BE_2} = V_{B_2} - V_o \uparrow$
  - Conduction of  $Q_2 \uparrow$
  - Conduction of  $Q_1 \downarrow$
  - $I_L \downarrow, V_o \downarrow$
  - This process continues until  $V_o \rightarrow 0$   
and  $V_A$  is large enough to keep  
0.5V between  $C_L$  and  $C_S$  terminals.

# Switching Regulators

## Linear Regulator vs Switching Regulator

### Linear Regulator

- Input Stepdown transformer is bulky and expensive since as because of low frequency (50Hz)

- Large values of filter capacitors are required to filter low frequency ripple.

$$r = \frac{1}{4f_3 R_L C}$$

- The pass transistors operate in its linear region to provide a controlled voltage drop across it with a steady dc current flow.

$$P_C = V_{CE} I_C$$

Continuous power loss

$$n \downarrow$$

$$\eta_{max} = 50\% \text{ Typically}$$

### Switching Regulator

- In switching regulators transformer size is less due to high frequency switching.

- Size of filter capacitors is small due to high frequency ripple.

- The pass transistors is operated as a controlled switch.  
OFF :  $I_C = 0 \Rightarrow P_C = 0$   
ON :  $V_{CE} = 0 \Rightarrow P_C = 0$  min power loss

$$n \uparrow$$

$$\eta_{max} = 90 - 95\%$$

Typically

## Block diagram of Switching Regulator

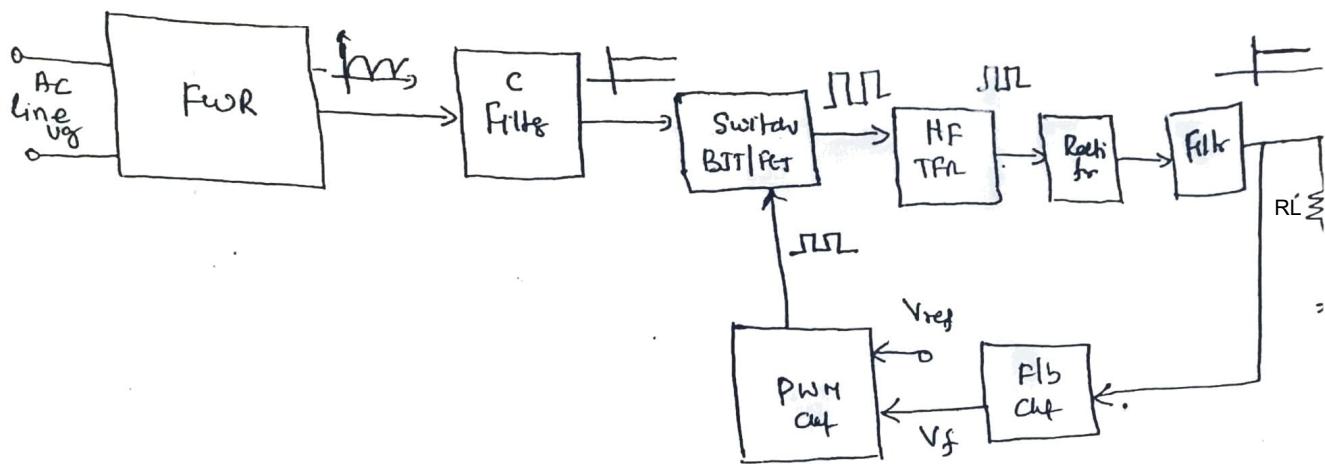
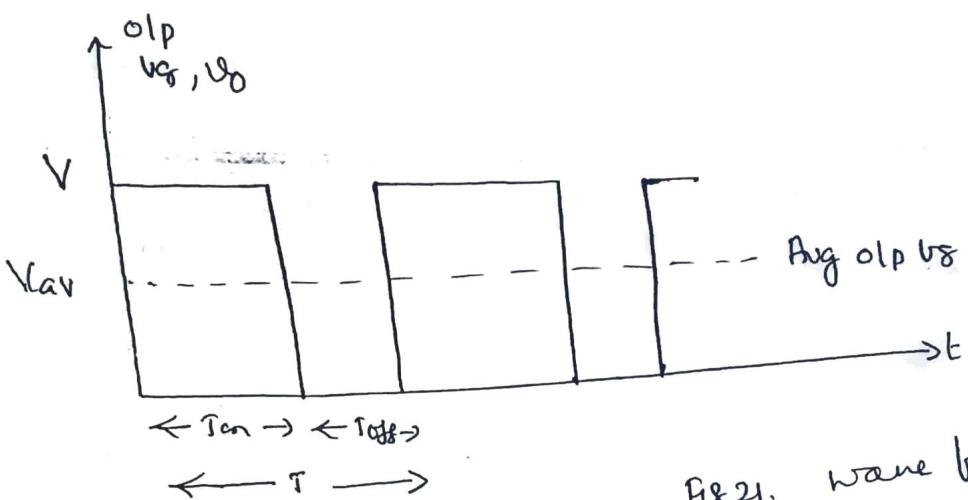


Fig 20. Block diagram of switching regulator.

- Ac line  $V_g$  is directly rectified using FWR.
- C filter is used to eliminate ripple.
- Dc  $V_g$  o/p of C filter is converted into Sq. wave using the switch controlled by PWM clkt
- HF & Step down transformer is used to reduce the amplitude of Sq. wave into convenient value.
- The transformer o/p is rectified and then filtered to obtain smooth dc.
- PWM clkt controls the duty cycle of switch by comparing  $V_{ref}$  with  $V_f$  to regulate the output voltage.



$$V_{avg} = \frac{1}{T} \int_0^T v_0 dt$$

$$= \frac{1}{T} \int_0^{T_{on}} V dt$$

$V_{avg} = \frac{T_{on}}{T} V = DV$

D is duty cycle:

$$0 \leq D \leq 1.$$

$\Rightarrow V_0$  varies from 0 to  $V$ .

Regulator Action

If  $V_0 \uparrow$

- $V_f \uparrow$
- PWM Act  $\downarrow D$
- $T_{on} \downarrow$
- $V_0 \downarrow$

If  $V_0 \downarrow$

# 555 Timer

- A highly stable device used for generating accurate time delay or oscillation.

Commercial Name SE555 | NE555

8 pin circular  
8 pin mini DIP

14 Pin DIP

- Available as  $10^{-9}$  to  $10^9$  can provide time delay ranging from  $\mu s$  to hours

## Features

- power supply  $V_g$ : 5 to 18V

drive load  $\Rightarrow I_o(\max) : 200 \text{ mA}$

output compatible with TTL & CMOS

555 timer is versatile and easy to use in various applications

## Applications

• oscillator

• pulse generator

• ramp and square wave generator

• monostable multivibrator

Burglar Alarm

• traffic light control

•  $V_g$  monitor etc.

(02)

Functional diagram of 555 timer

Three equal resistors each of value  $5\text{k}\Omega$  are connected in series between pin 8 ( $V_{CC}$ ) and ground.

$V_g$  at pins of upper comparator ( $U_C$ ) is  $\frac{2}{3}V_{CC}$ , which is the upper trip point  $V_{UTP}$ .

$V_g$  at non inverting terminal of lower comparator ( $L_C$ ) is  $\frac{1}{3}V_{CC}$ , which is the lower trip point  $V_{LTP}$ .

When the threshold  $V_g$  exceeds  $\frac{2}{3}V_{CC}$ , upper comparator o/p goes high  
 $\Rightarrow S=1, Q=0, \bar{Q}=1$ , output = 0  
 The discharge transistor  $Q_1$  goes to saturation.

When the trigger  $V_g$  falls below  $\frac{1}{3}V_{CC}$ , lower comparator o/p goes high  
 $\Rightarrow S=1, Q=1, \bar{Q}=0$ , output = 1  
 The discharge transistor  $Q_1$  goes to cut-off.

A capacitor of  $0.01\text{MF}$  is recommended between pins (5) and ground to suppress noise on control  $V_g$  pin.

Pin 1 → Grounded terminal → All the voltages are measured w.r.t to the ground terminal

Pin 2 → Trigger Terminal → The trigger pin is used to feed the trigger input the 555 IC is set up as a monostable multivibrator

Pin 3 → Output terminal → Op of the timer is available at this pin.

Pin 4 → Reset → to reset or disable the timer

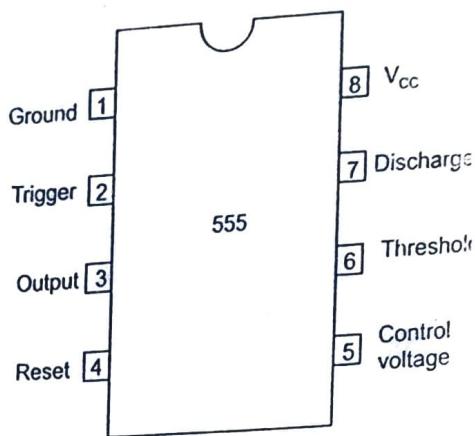
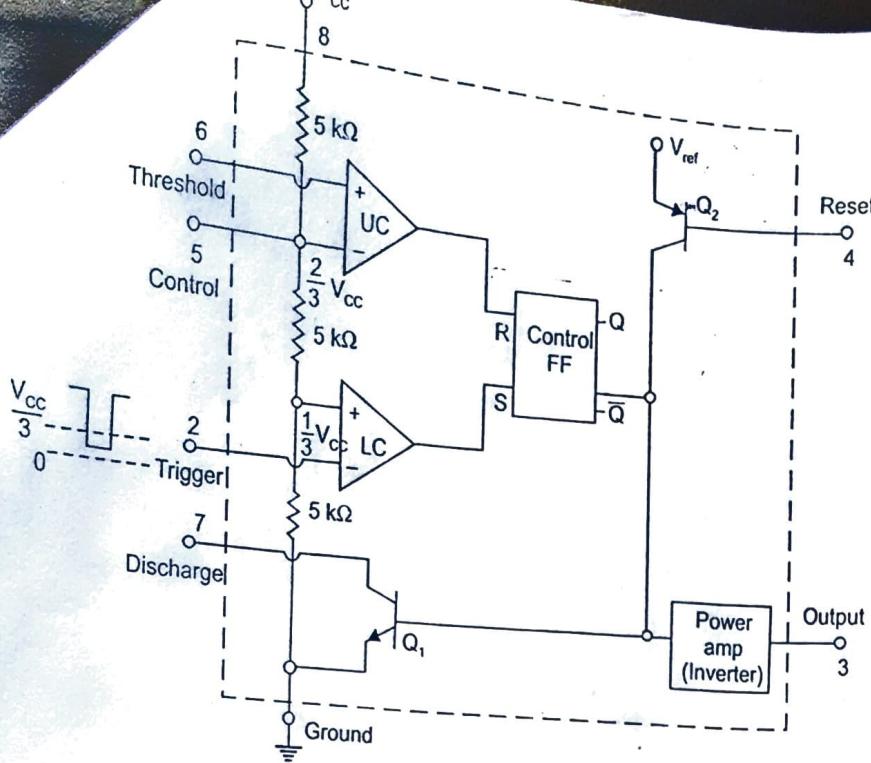
Pin 5 → Control Voltage Terminal → The threshold and trigger levels are controlled using this pin

Pin 6 → Threshold Terminal → non inverting input terminal of comparator 1 (ie Upper Comparator)

Pin 7 → Discharge terminal :- This pin is connected internally to the collector of transistor and mostly a capacitor is connected between this terminal & ground. It is called discharge terminal because when transistor saturates, capacitor discharges through transistor.

Pin 8 → Supply terminal → A supply voltage of +5V to +18V is applied to this terminal w.r.t ground (Pin 1)

It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5)

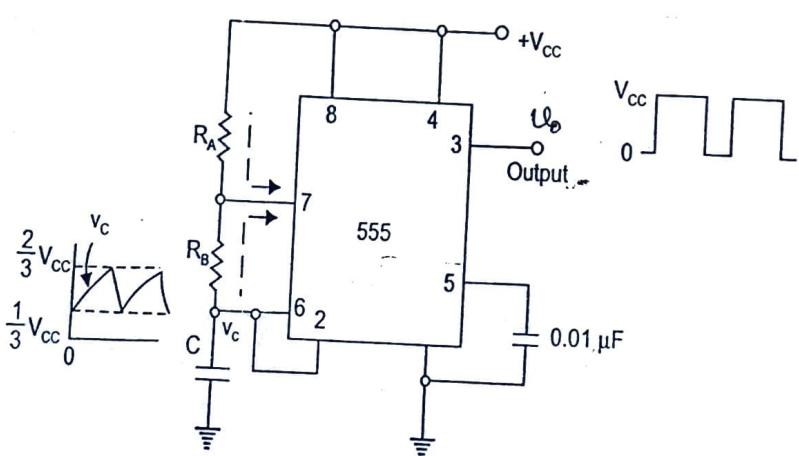


(2) Pin diagram

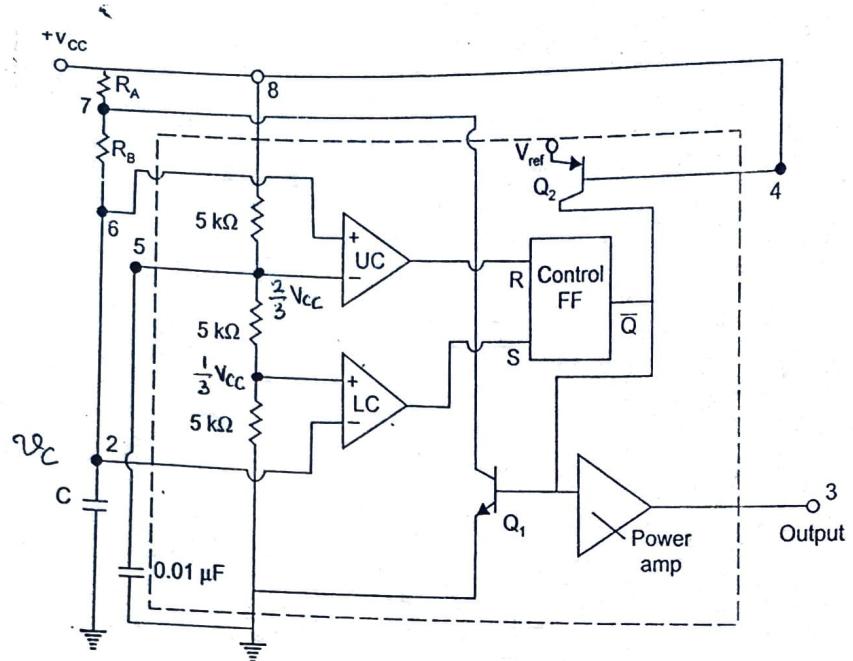
## (1) Functional diagram.

Under normal use Reset pin should be connected to  $V_{cc}$  i.e. Pin 8.

555 Timer as Astable multivibrator

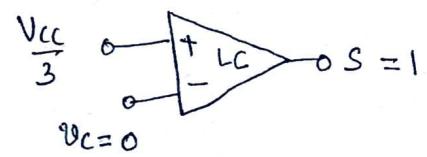
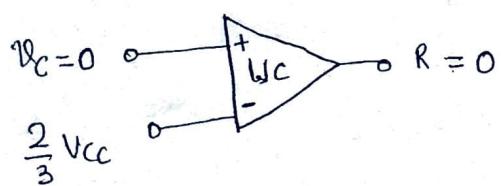


(3) Astable multivibrator



(4) Functional diagram of Astable multivibrator

- When the circuit is switched on, the flip-flop is cleared if  $Q \neq 0$ ,  $\bar{Q} \neq 1$ , which if the following conditions exist.



$(V_C = 0 \text{ since capacitor is initially uncharged})$

Since  $S = 1$ ,  $R = 0$ ,  $Q' = 1$ ,  $\bar{Q} = 0$  and  $O_P = 1$ .  
The discharge transistor  $Q_1$  is off.

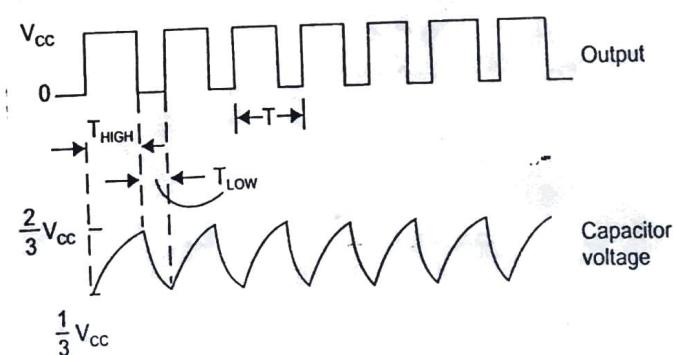
The capacitor gets charged via  $R_A$  and  $R_B$ . When the capacitor  $V_C$  exceeds  $\frac{2}{3}V_{CC}$ , upper comparator,  $Q_P$  goes high i.e.  $Q = 0$ ,  $\bar{Q} = 1$  and  $Q_P = 0$ . The discharge transistor  $Q_1$  goes to saturation, since  $\bar{Q} = 1$

Now the capacitor discharges into saturated transistor via  $R_B$ . When the capacitor  $V_C$  falls below  $\frac{1}{3}V_{CC}$ , the low comparator  $Q_P$  goes high. Now

$$S = 1, \quad Q = 1, \quad \bar{Q} = 0, \quad Q_P = 1$$

The discharge transistor  $Q_1$  goes to cut-off since  $\bar{Q} = 0$ .

Now the capacitor once again charges via  $R_A$  &  $M_B$  and the same cycle repeats.



(5) Wave forms

$$T_{High} = T_{on}$$

$$T_{Low} = T_{off}$$

# Expression for frequency of oscillations

Simil

Charging time constant =  $(R_A + R_B)C$

Discharging time constant =  $R_B C$

Consider the interval  $0 < t \leq T_{\text{dis}}(T_m)$

Capacitor is getting charged towards  $V_{CC}$  via

$R_A + R_B$ .  
 $V_f \rightarrow$  final voltage to which the capacitor will charge

$V_C(t) = V_f + (V_i + V_f)e^{-t/(R_A + R_B)C}$  --- (1)  
 $V_i \rightarrow$  initial capacitance voltage.

$$V_f = V_{CC}, \quad V_i = \frac{1}{3} V_{CC}$$

$$V_C(t) = V_{CC} + \left(\frac{1}{3} V_{CC} - V_{CC}\right) e^{-t/(R_A + R_B)C}$$

at  $t = T_m$ ,  $V_C(t) = \frac{2}{3} V_{CC}$ . Now

$$\frac{2}{3} V_{CC} = V_{CC} + \left(\frac{1}{3} V_{CC} - V_{CC}\right) e^{-T_m/(R_A + R_B)C}$$

$$\frac{2}{3} = 1 - \frac{2}{3} e^{-T_m/(R_A + R_B)C}$$

$$\frac{2}{3} e^{-T_m/(R_A + R_B)C} = \frac{1}{3}$$

$$e^{T_m/(R_A + R_B)C} = 2$$

$$T_m = (R_A + R_B)C \ln 2$$

$$T_m = 0.693 (R_A + R_B)C \quad (2)$$

Similarly,  $T_{off} = 0.693 L_B C \dots (3)$

$$T = T_m + T_{off} = 0.693 (L_A + 2L_B) C \dots (4)$$

$$f = \frac{1}{T} = \frac{1.44}{(L_A + 2L_B) C} \dots (5)$$

$$\text{Duty cycle, } D = \frac{T_m}{T} = \frac{L_A + L_B}{L_A + 2L_B} \dots (6)$$

Verify from equation (6) that,  $D$  can only be greater than 0.5.

Note: take  $D = 1/4$  write your observation from (6).

**[Ex 1]** Refe the circuit & Fig (3).

$$V_{CC} = 10V$$

$$R_A = R_B = 10k\Omega$$

$$C = 0.02 \mu F$$

1. Calculate  $T_m$ ,  $T_{off}$ ,  $T$  and  $f$

2. Find Duty cycle

3. Sketch the waveforms of  $V_C$  and  $V_o$ .

**[Ex 2]** Design an astable multivibrator using 555 timer with the following specifications.

$$f = 2 kHz$$

$$D = 0.75$$

Amplitude of Sig. wave: 0 - 5V

$$V_{CC} = 10V$$

Hint:

$$f = \frac{1.64}{(LA + 2LB) C} - \quad (A)$$

$$D = \frac{RA + LB}{LA + 2LB} - \quad (B)$$

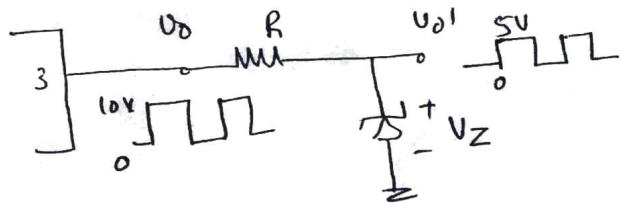
Three continuous MA, LB & C  
only two cont.

choose  $C = 0.1 \mu F$

Find  $RA$  &  $LB$  using (A) & (B).

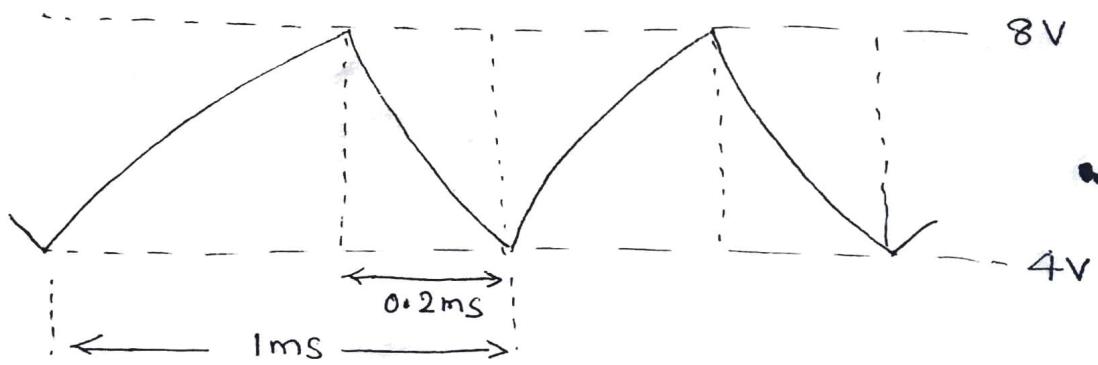
Amplitude limits

Design suitable R.



Ex 3

The  $V_g$  across capacitor in an astable multivibrator using 555 is shown below.

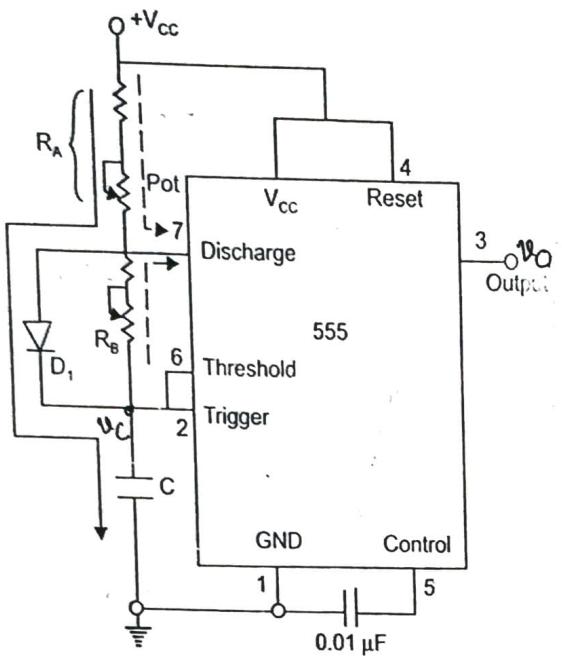


Design the Component Values for the Circuit.

# Astable multivibrator with Variable

(09)

## Duty Cycle.



Fig(6). Astable multivibrator with adjustable duty cycle.

Note: working is similar to that of that in Fig (3). only equations are given below.

Students are advised to write explanations,

derive the following equations and sketch down the waveforms of  $V_C$  and  $V_O$ .

Capacitor gets charged via  $R_A$  and diode.

$$T_{on} = 0.693 R_A C \quad (7)$$

Discharging of the capacitor takes place through  $R_B$

$$T_{off} = 0.693 R_B C \quad (8)$$

$$T = 0.693 (R_A + R_B) C \quad (9)$$

$$D = T_{on}/T = \frac{R_A}{R_A + R_B} \quad (10)$$

$$f = \frac{1}{T} = \frac{1.44}{(R_A + R_B) C} - (1)$$

Observe from (1) that  $D$  can be less than and greater than 0.5. When  $R_A = R_B$ ,  $D = 0.5$

$\Rightarrow$  The Square wave is said to be symmetrical.

**Ex 4.** In the circuit of Fig (6)  $R_A = 6.8 \text{ k}\Omega$   $R_B = 3.3 \text{ k}\Omega$

$$C = 0.1 \text{ nF} \quad \text{Calculate}$$

$T_{on}$ ,  $T_{off}$ ,  $T$ ,  $f$  and  $D$ .

If  $V_{CC} = 10V$  Sketch the waveforms of  $v_o$  and  $v_c$ .

**Ex 5** Design a square wave generator using 555 timer to meet the following requirements.

$$T_{on} = 0.75 \text{ ms}$$

$$f = 1 \text{ kHz.}$$

Amplitude of sig. wave: 0 to 5V

$$V_{CC} = 10V.$$

Draw the circuit and sketch the waveforms of  $v_o$  and  $v_c$ .

**Ex 6** Repeat Ex 5 Design a sig. wave generator using 555 timer to meet the following specifications.

$$f = 4 \text{ kHz} \quad D = 0.25 \quad \text{Amplitude of sig. wave } 10V \quad V_{CC} = 10V$$

(11)

For the circuit shown below

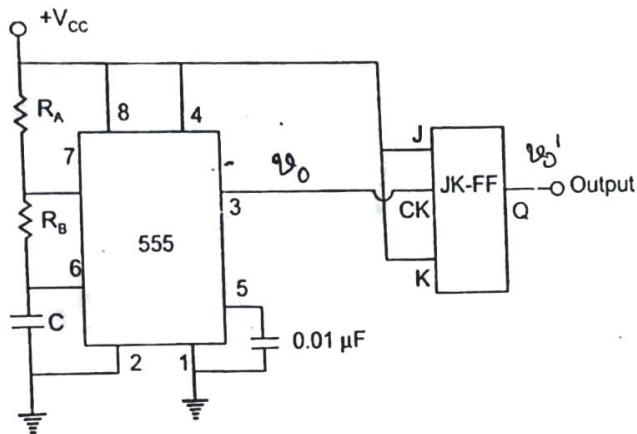
$$R_A = 8\text{ k}\Omega \quad R_B = 4\text{ k}\Omega \quad C = 0.1\text{ mF}$$

(a) Calculate  $T_{on}$ ,  $T_{off}$ ,  $f$ , and  $D \geq v_o$ .

(b) Find  $T_{on}$ ,  $T_{off}$ ,  $f$  and  $D \geq v_o$

(c) Write your inference.

flip flop is rising edge triggered



## Applications of Astable multivibrator

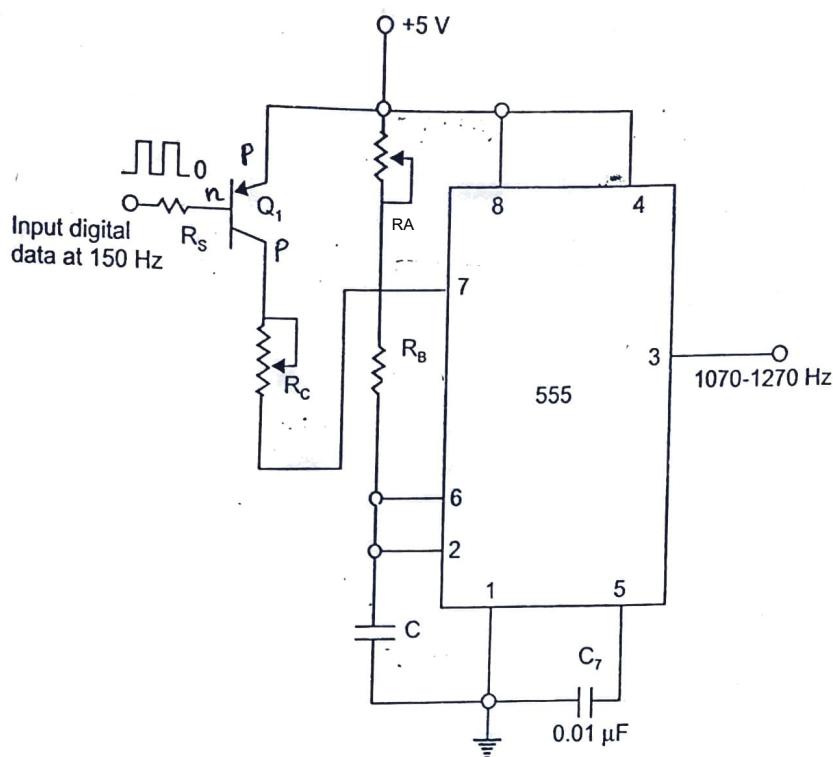
- 1) FSK Generator
- 2) Schmitt trigger
- 3) Saw tooth wave generator.
- 4) Pulse Position Modulation

### FSK Generator

- In digital data communication binary code is transmitted by shifting the carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique.
- In a teletypewriter using MODEM, a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals
  - logic 1 → Mark → 1070 Hz
  - logic 0 → Space → 1270 Hz.
- The standard digital data input frequency is 150 Hz.

When the input is low,  $Q_1$  goes on and  $R_A$  appears in parallel with  $R_C$ .

$$\therefore f = \frac{1044}{\{(R_A || R_C) + 2R_B\} C}$$



Fig(7) FSK generator.

$R_c$  can be adjusted to set  $f = 1270 \text{ Hz}$ .

when the input is high, transistor  $Q_1$  goes off.  
 $R_c$  sets dis connected from the circuit

$$f = \frac{1.44}{(R_A + 2R_B) C}$$

Values of  $C$ ,  $R_A$  and  $R_B$  can be selected so

that  $f = 1070 \text{ Hz}$ .

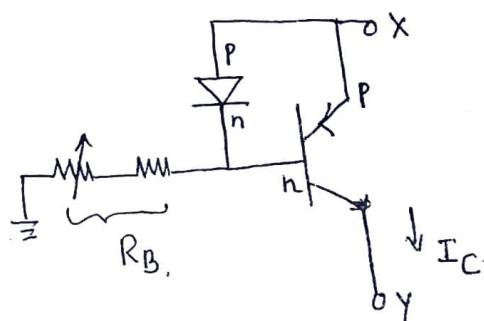
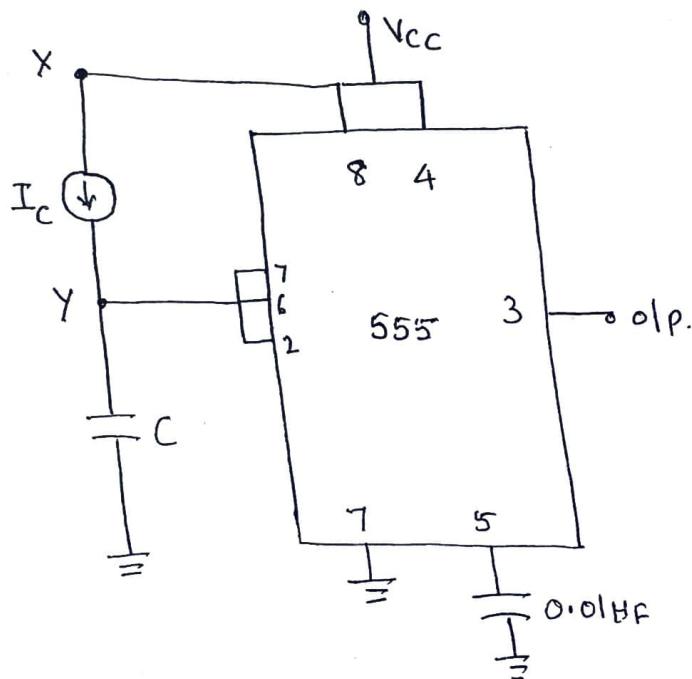
## Sawtooth Generators

- When a capacitor is charged with constant current, the capacitor  $V_C$  is a ramp.

$$V_C(t) = \frac{1}{C} \int I dt$$

$$= \frac{I}{C} \cdot t \Rightarrow \text{Ramp } V_C$$

- In astable multivibrator, the capacitor is charged from a constant current instead of charging thru resistors.

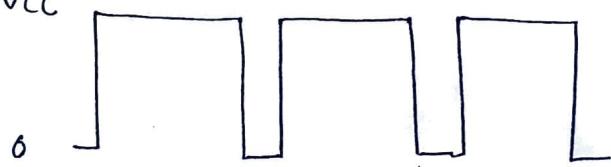


$\Leftarrow$  Constant Current Source

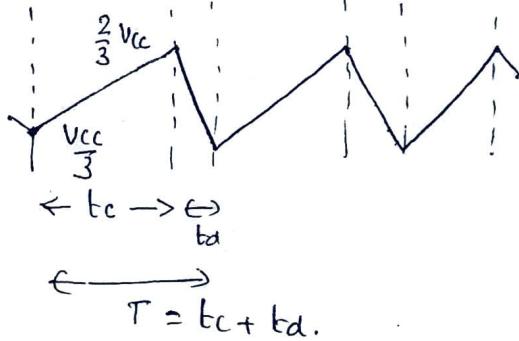
Fig (a) Sawtooth Generator

- To start with the capacitor gets charged with a constant current and the  $V_C$  across the capacitor rises linearly. and the op-amp is high.
- When the capacitor  $V_C$  exceeds  $\frac{2V_{CC}}{3}$ , output transistor goes to saturation.
- Now the capacitor discharges into saturated transistor. The discharge is quick since  $R_{CE(sat)} \approx 0$ . When the capacitor  $V_C$  falls below  $\frac{V_{CC}}{3}$ , output goes high, the transistor goes to cut-off.
- Once again the capacitor starts to charge through constant current source and the same cycle to operate repeat.

$V_O:$



$V_C:$



$$T = t_c + t_d$$

$$t_d \ll t_c$$

$$t_c \approx T$$

Consider the interval  $0 \leq t \leq t_c$

$$\frac{1}{C} \int_0^{t_c} I_c dt = \Delta V_c = \text{change in capacitor } V_g.$$

$$\frac{I_c}{C} t_c = \frac{2}{3} V_{cc} - \frac{1}{3} V_{cc} = \frac{V_{cc}}{3}.$$

$$\therefore I_c \propto \underline{\underline{3/V_c}}$$

$$t_c = \frac{C V_{cc}}{3 I_c} \approx T$$

$$f = \frac{3 I_c}{C V_{cc}}$$

## Schmitt trigger

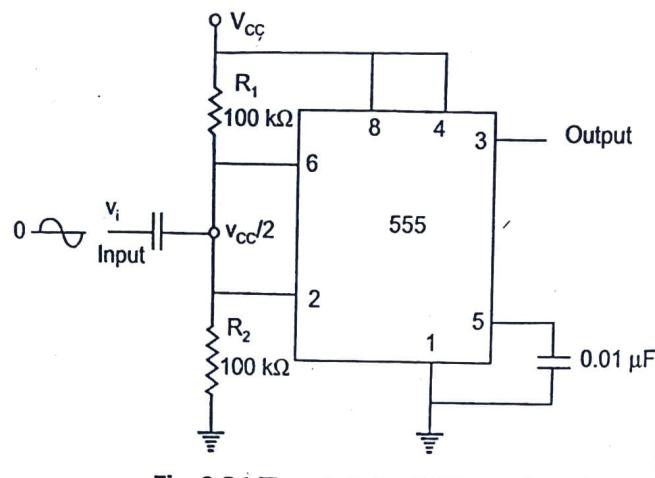
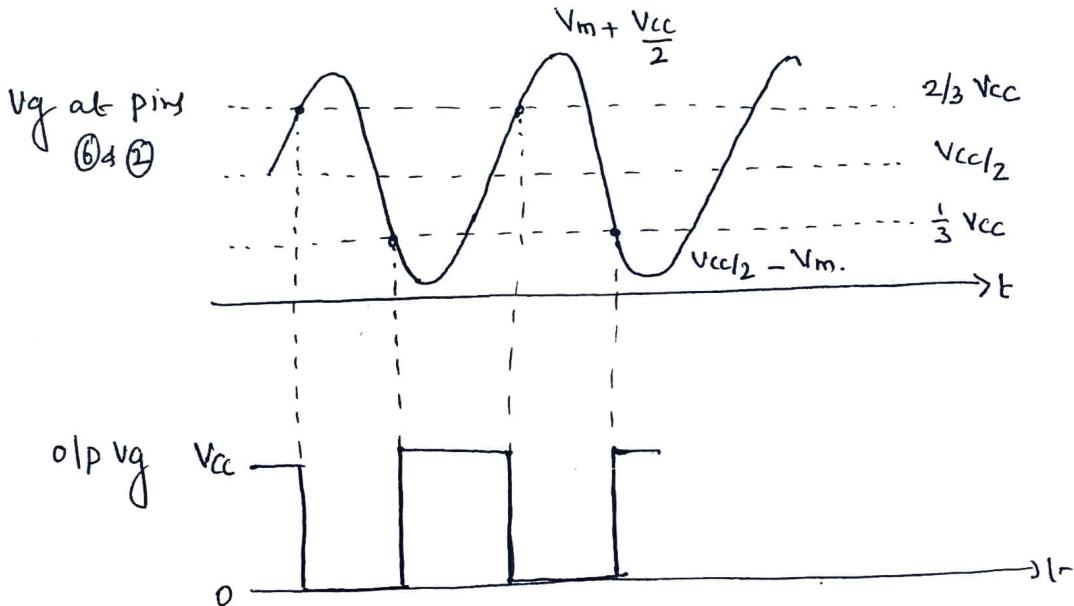


Fig (q) Schmitt trigger



- In 555 the trip point  $V_{gs}$  are  $\frac{2V_{cc}}{3}$  and  $\frac{V_{cc}}{3}$   
and both are positive

- A  $V_g \frac{V_{cc}}{2}$  derived from  $V_{cc}$  using equal potential divider is added to input which shifts the input above zero level.

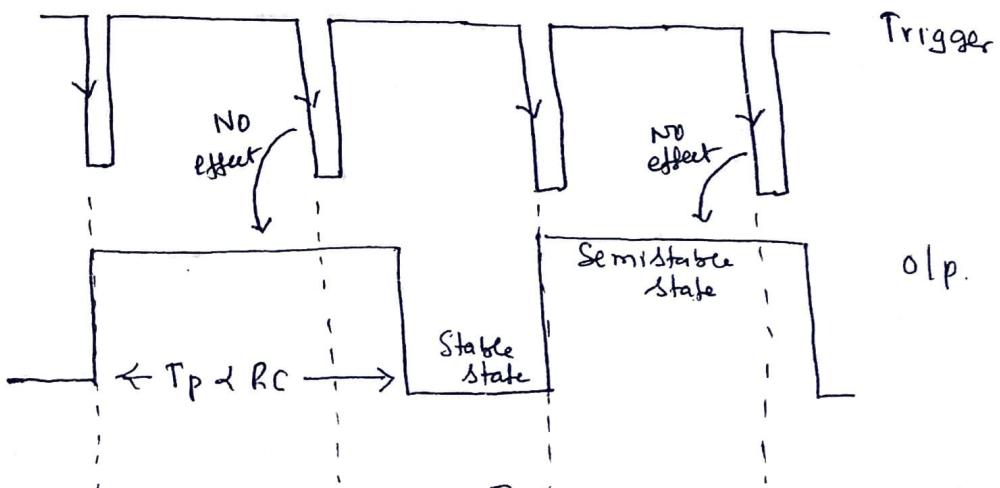
- When the resultant  $V_g$  exceeds  $\frac{2}{3}V_{CC}$  o/p goes low
- When the resultant  $V_g$  falls below  $\frac{1}{3}V_{CC}$  o/p goes high.
- For the circuit to work properly

$$V_m + \frac{V_{CC}}{2} > \frac{2}{3}V_{CC}$$

$$\Rightarrow V_m > \frac{V_{CC}}{6}$$

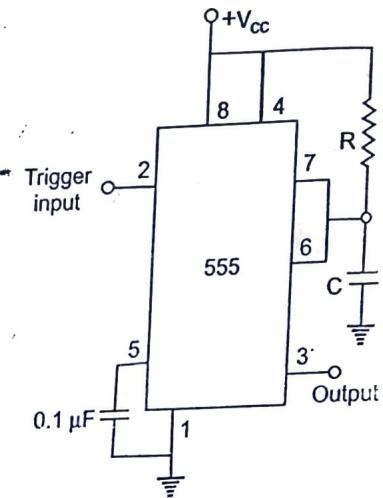
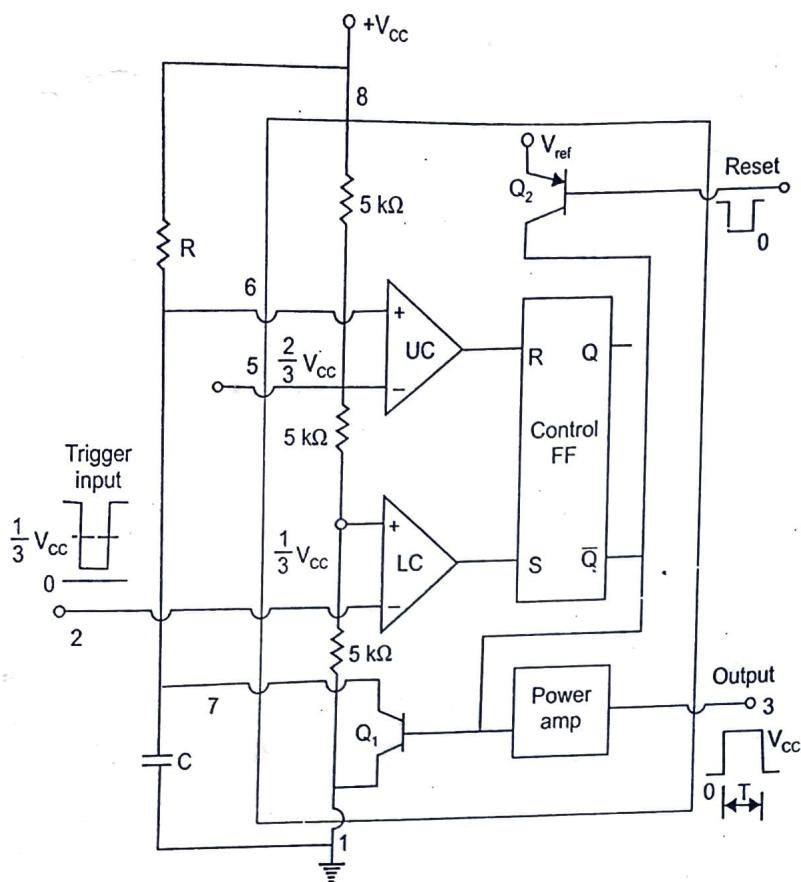
Monostable multivibrator | pulse generator | one shot | <sup>Monoshot</sup>

- In monoshot only one state is stable and other is semistable.
- when a trigger is applied it switches from stable state to semistable state and remains there for the time duration  $T_p$ , fixed by the product  $RC$  and returns back to stable state.
- Triggers applied before the completion of  $T_p$  has no effect



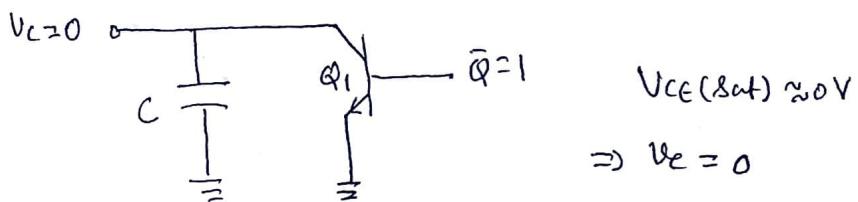
Fig(10) Monoshot waveforms.

# MonoStable Multivibrator using 555 Time



Fig(11) MonoStable multivibrator using 555

- In the Stand by state op1 is zero.  $\bar{Q} = 1$   
and hence the discharge transistor is saturated.  
The capacitor  $V_C$  is clamped at zero.



- When the trigger  $V_T$  falls below  $\frac{V_{CC}}{3}$ , the op1 of Low Compator goes high.

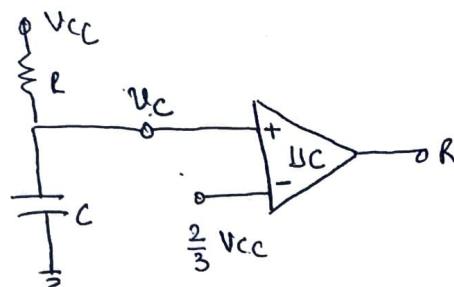
$$S=1, \quad Q=1, \quad \bar{Q}=0, \quad op1=1$$

Since  $\bar{Q}=0$ , the discharge transistor  $Q_1$  goes off.

Now the capacitor gets charged towards  $V_{CC}$  through  $R$ . When the capacitor  $V_C$  exceeds  $\frac{2}{3}V_{CC}$  the upper comparator output goes high.

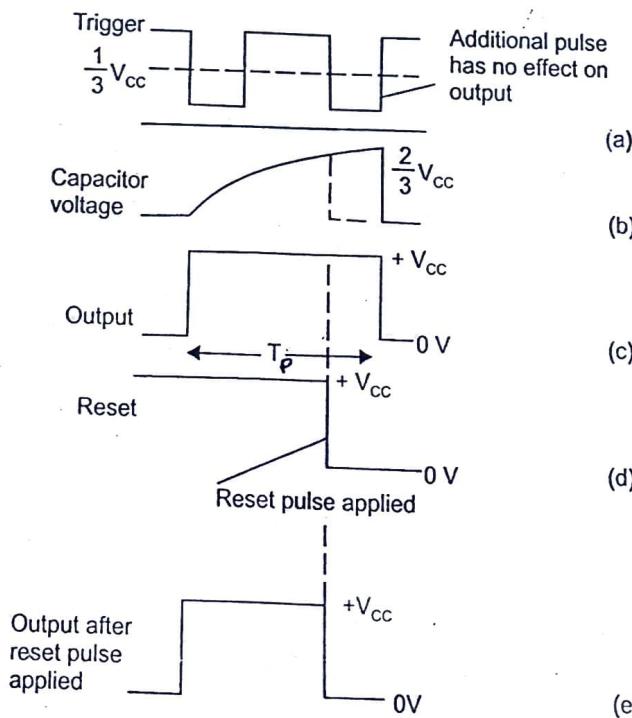
$$R=1, Q=0, \bar{Q}=1, o_{LP}=0$$

Since  $\bar{Q}=1$ , discharge transistor  $Q_1$  saturates and clamps the capacitor  $V_C$  at zero.



The op-amp remains at the stable state (zero) until next trigger is applied.

### Expression for pulse width ( $T_p$ )



Fig(12) Wave forms

Expression for pulse width  $T_p$ .

$$V_c(t) = V_f + (V_i - V_f) e^{-t/RC}$$

$$V_f = V_{cc}, \quad V_i = 0$$

$$V_c(t) = V_{cc} - V_{cc} e^{-t/RC}$$

$$\text{at } t = T_p, \quad V_c(t) = \frac{2}{3} V_{cc}$$

$$\frac{2}{3} V_{cc} = V_{cc} - V_{cc} e^{-T_p/RC}$$

$$e^{-T_p/RC} = 1/3 \Rightarrow e^{T_p/RC} = 3$$

$$\Rightarrow T_p = 1.1 R C$$

Modified Circuit

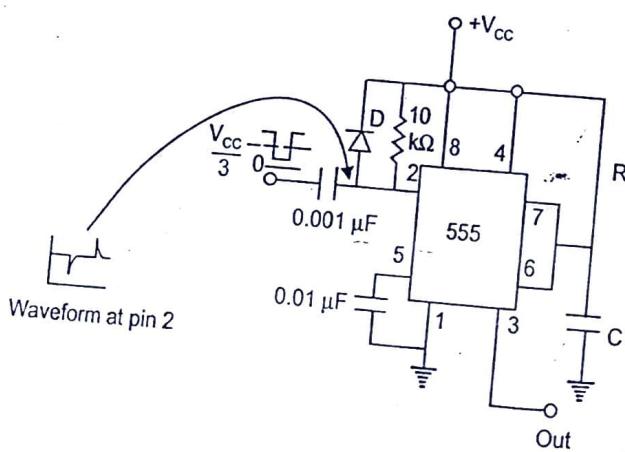
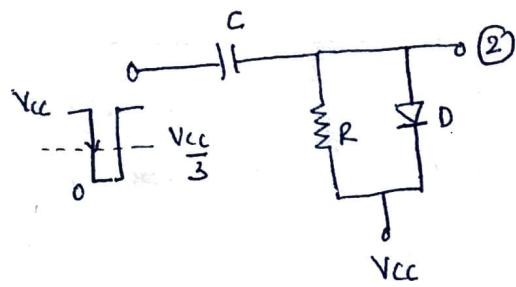


Fig (13) modified circuit



- R-C Differentiator converts biggest pulses into spike waveform



- Diode conducts positive spikes and hence only negative spikes are applied at Pin (2)



Spikes act as effective triggers since they are sharp.

**Ex 8**

Design a monostable using 555 timer to produce pulse 85 width 1ms duration.

$$T_p = 1.1RC \approx 1\text{ms}$$

$$\text{Take } C = 0.1\text{HF}$$

Find R.

**Ex 9**

In a monostable  $R = 10\text{k}\Omega$   $C = 1\text{HF}$

Calculate the Pulse width.

- Frequency Divider
- Linear Ramp generator.

Ref: Linear integrated Circuits

by

Roy Choudhury.

## Phase Locked Loops (PLL)

- PLL is an important building block of linear systems.
- It was used in radar synchronization and communication applications in 1930. It was costly.
- Now PLL's are available in inexpensive monolithic IC's.
- PLL technique is ~~used~~ for electronic frequency control is used today in satellite communication systems, air ~~buses~~ ~~bus~~ borne navigation S/m/s, FM communication S/m/s, computers etc.

### Basic Principles

The basic Block schematic of the PLL is shown in fig ①.

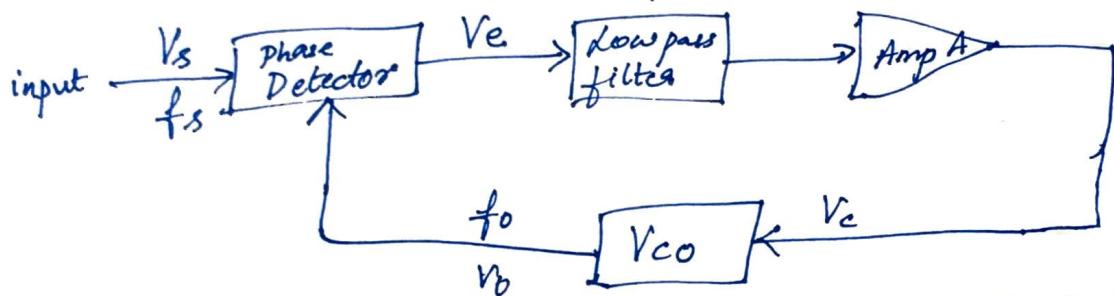


Figure 1: Block schematic of the PLL

This feedback system consists of

- Phase detector/comparator
- low Pass filter
- An error amplifier
- A Voltage Controlled Oscillator

- VCO is a free running multivibrator and (VCO) operates at a set frequency  $f_o$  called the free running frequency which is determined by external timing capacitor and external resistor.
- The frequency can be deviated by the dc control voltage, hence it is called Voltage controlled Oscillator

- If an input signal ( $v_s$ ) of the frequency  $f_s$  is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output  $v_o$  of the VCO.
- If the two signals differ in frequency and/or phase an error voltage  $v_e$  is generated.
- Phase detector is basically a multiplier and produces the sum ( $f_s + f_o$ ) and difference ( $f_s - f_o$ ) components at its output
- High frequency component ( $f_s + f_o$ ) is removed by the LPF.
- Low frequency component is amplified and then applied as control voltage  $v_c$  to VCO.
- The signal  $v_c$  shifts the VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$ .
- The signal is in the capture range.
- The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. → Now the circuit is said to be locked.
- Once locked, the output frequency  $f_o$  of VCO is identical to  $f_s$  except for a finite phase difference  $\phi$ .
- This phase difference  $\phi$  generates corrective control voltage  $v_c$  to shift the VCO frequency from  $f_o$  to  $f_s$  and thus maintains the lock.
- Once locked PLL tracks the frequency changes of the input signal.  
PLL goes through three stages
  - Free running
  - Capture
  - locked or tracking.

# 10

## PHASE-LOCKED LOOPS

### 10.1 INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

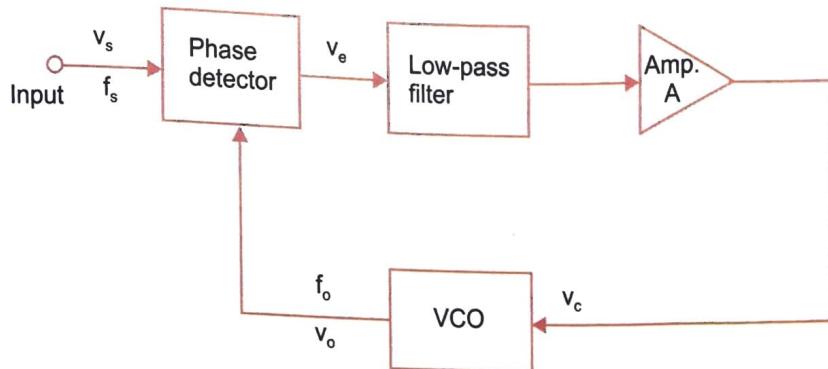
### 10.2 BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 10.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO).

The VCO is a free running multivibrator and operates at a set frequency  $f_o$  called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage  $v_c$  to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal  $v_s$  of frequency  $f_s$  is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output  $v_o$  of the VCO. If the two signals differ in frequency and/or phase, an error voltage  $v_e$  is generated. The phase detector is basically a multiplier and produces the sum ( $f_s + f_o$ ) and difference ( $f_s - f_o$ ) components at its output. The high frequency component ( $f_s + f_o$ ) is removed by the low pass filter and the difference frequency component is amplified and then applied as control voltage  $v_c$  to VCO. The signal  $v_c$  shifts the VCO frequency in a direction to reduce the frequency difference between  $f_s$  and  $f_o$ . Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal



**Fig. 10.1** Block schematic of the PLL

frequency. The circuit is then said to be locked. Once locked, the output frequency  $f_o$  of VCO is identical to  $f_s$  except for a finite phase difference  $\phi$ . This phase difference  $\phi$  generates a corrective control voltage  $v_c$  to shift the VCO frequency from  $f_o$  to  $f_s$  and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 10.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

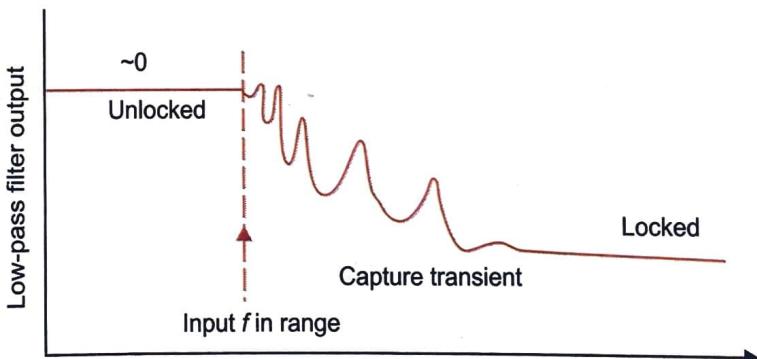
The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

**Lock-in Range:** Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of  $f_o$ , the VCO frequency.

**Capture Range:** The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of  $f_o$ .

**Pull-in time:** The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.



**Fig. 10.2** The capture transient