8086 Basic System Concepts

8086 can be used either in a minimum mode system or a maximum mode system. The fig. 10 and fig. 11 shows minimum and maximum modes with groups of ICs to generate address bus, data bus and control bus signals. Using these buses, the CPU can be connected to ROM, RAM, PORTS and other devices to form a complete system.

BASIC 8086 Minimum mode System

8282 I/O ports are used to latch the addresses from the 8086 Microprocessor Data/Address bus. By using three 8282, A0-A15, $\overline{BHE}$, A16-A19 lines are latched during T1 state. $\overline{OE}$ (Output Enable) input of the 8288 I/O ports are grounded; the bus will therefore, never be floated. ALE signal from 8286 is used to strobe the addresses into the 8282 I/O latches.

Since the Data Bus is bi-directional, 8286 bi-directional bus transceivers are used, in order to create a separate Data Bus from the 8086 Address/data Bus. The DT/$\overline{R}$ and $\overline{DEN}$ outputs from 8086 are used for 8286 "T" signal and $\overline{OE}$ inputs respectively.

Maximum Mode Configuration

When MN/$\overline{MX}$ pin is strapped to GND, the 8086 treats pin 24 through 31 to be in maximum mode. An 8288 bus controller interprets status information coded into S0, S1 and S2 to generate bus timing and control signals compatible. DEN, DT/$\overline{R}$ and ALE control outputs, are now generated by the 8288 bus controller. The DEN from 8288 is inverted and given to 8286 transceiver to enable the output. The output enable of 8282 latch is grounded. As in minimum mode the address-data lines are latched through 8282 latch. The ALE signal from the 8288 bus controller latches the address during the T_1 state of the microprocessor. The DEN signal is used to enable the transceiver either to transmit or receive data from I/O devices and memory. The DT/$\overline{R}$ signal is used to transmit or receive the data as the need may be.

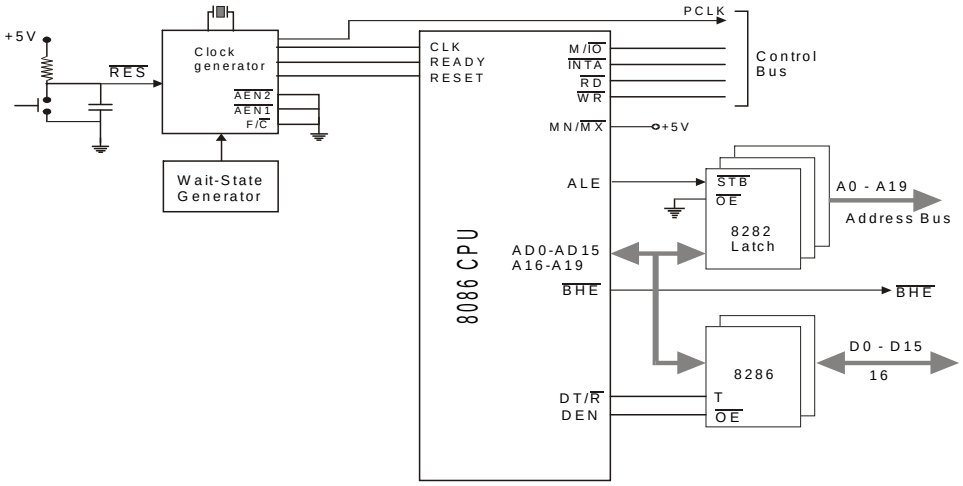

Fig. 10 - 8086 Minimum Mode System

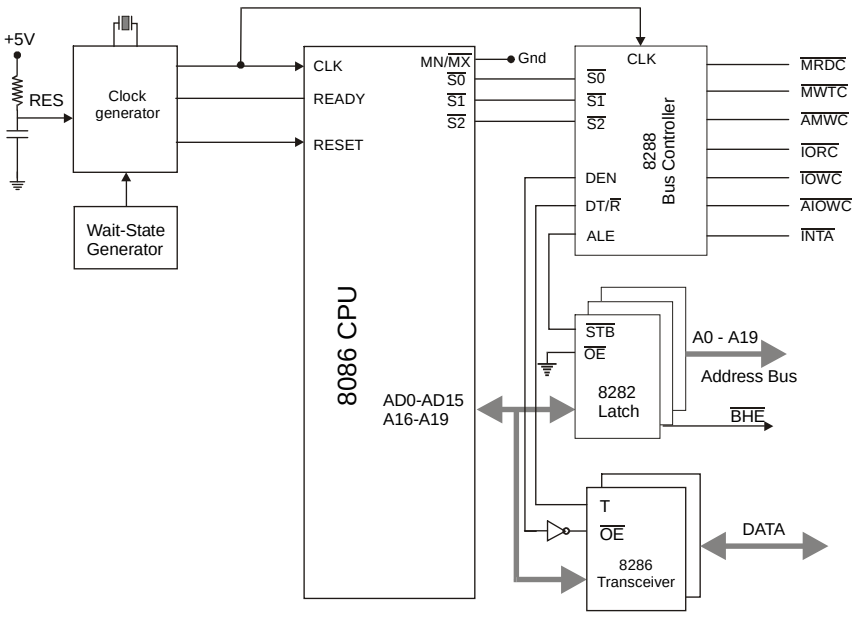

Fig. 11 - 8086 Maximum Mode Configuration

Bus Read Machine Cycle

Fig- 12 shows the timing diagram of 8086 read machine cycle with WAIT state. The clock (CLK) signal is obtained from the clock-generator 8284. Each cycle of the clock is referred to as a state. Minimum number of states to access a data is four. They are T1, T2, T3, and T4 states.

During T1 state of a read machine cycle an 8086 first asserts the $M/\overline{IO}$ signal. It will assert this signal high if it is going to read from memory during memory read cycle and it will assert $M/\overline{IO}$ low if it is going to do a read from an Input port during its read cycle. The timing diagram in fig. 12 shows two lines for the $M/\overline{IO}$ signal, because the signal may be going LOW or going HIGH for a read cycle. The point where the two lines cross indicate the time at which the signal becomes valid for this machine cycle.

After asserting $M/\overline{IO}$, the 8086 sends out a high on the address latch enable signal, ALE. The microprocessor sends out on AD0-AD15, A16 through A19 and $\overline{BHE}$ lines, the address of the memory location that it wants to read. Since the latches are enabled by ALE being high, this address information passes through the latches to their outputs. The 8086 then makes the ALE output low. This disables the latches (8282) and holds the address information latched on the latch outputs. The address information latched on the latch outputs can now be used to select the desired memory or port location.

In the timing diagram, the first point at which the two ($AD_0 - AD_{15}$) cross represents the time at which the 8086 has put a valid address on these lines. Two lines DO NOT indicate that all 16 lines are going high or going low at this point. The crossed lines indicate the time at which a valid address is on the bus.

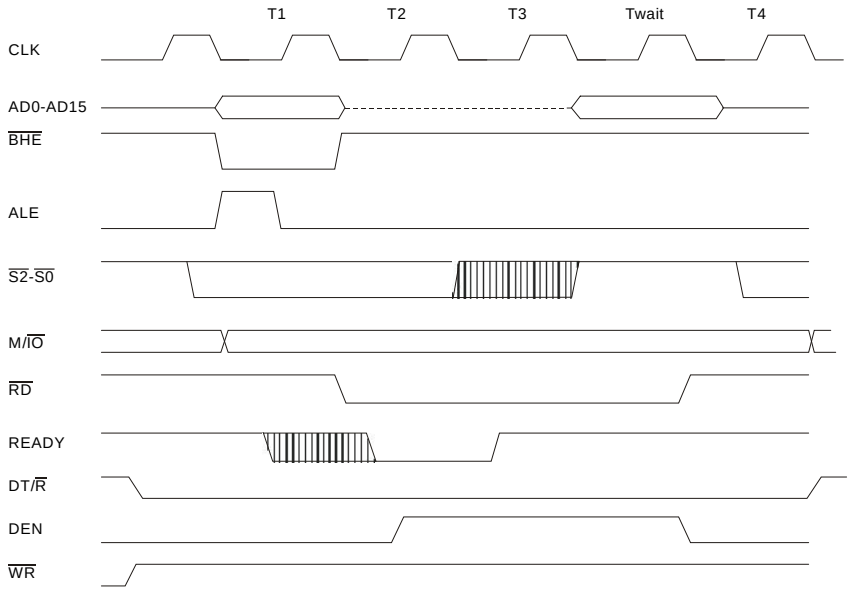

Fig. 12 - Read Timing Diagram

Since the address information is now held on the latch, the 8086 does not need to send it out any more. As shown in fig. 12 the 8086 floats the AD0 - AD15 lines so that they can be used to input data from memory or from a port. At about the same time the 8086 also remove the $\overline{BHE}$ and A16-A19 information from the upper lines and sends out some status information on these lines.

The 8086 is now ready to read data from the addressed memory locations or port. During T2-state the 8086 asserts its $\overline{RD}$ signal low. This signal is used to enable the addressed memory device or port device.

At the end of T3 state the microprocessor makes the $\overline{RD}$ signal high and reads the data available on the data bus, provided the READY input signal is high. It is the duty of the external circuit to see that valid data is made available on the data bus.

If the READY input pin is not high at the sampled time in a machine cycle, the 8086 will insert one or more WAIT states between T3 and T4 states in that machine cycle. An external hardware device is set up to pulse READY low before the rising edge of the clock in T2 state. After the 8086 finishes T3 of the machine cycle, it enters a WAIT state.

If the READY input is still low at the end of a WAIT state, then the 8086 will insert another WAIT state. The 8086 will continue inserting WAIT states until the READY input is sampled high again. If the READY input is sampled high again during T3 or during the WAIT state, the microprocessor comes out of the WAIT state and will initiate T4 of the machine cycle.

The $\overline{DEN}$ signal is used to enable bi-directional buffers on the data bus. The data enable signal, $\overline{DEN}$, from the 8086 will enable the data buffer when it is asserted LOW. The data transmit / receive signal DT/$\overline{R}$ from the 8086 is used to specify the direction in which the buffers are enabled. When DT/$\overline{R}$ is asserted high, the buffers will, if enabled by $\overline{DEN}$, transmit data from the 8086 to Memory or I/O ports. When DT/$\overline{R}$ is asserted

low, the buffers, if enabled by $\overline{DEN}$, will allow data to be received from Memory or I/O ports of the 8086. DT/$\overline{R}$ is asserted during T1 of the machine cycle. The $\overline{DEN}$ is asserted after the 8086 finishes using the data bus to send the lower 16 address bits.

BUS Write Machine Cycle

The 8086 write operation is very similar to the read cycle. During T1 of a write machine cycle the 8086 asserts M/$\overline{IO}$ low if the write is going to a port and it asserts M/$\overline{IO}$ high if the write is going to memory. At about the same time the 8086 raises ALE high to enable the address latches. The 8086 then assert $\overline{BHE}$ and on the lines AD0 - AD19, it output the address that it will be writing to. When writing to a port, line A16 - A19 will always be low, because the 8086 only sends out 16-bits port addresses. The 8086 brings ALE low again to latch the address on the outputs of the latches. In addition to holding the address, the latches also function as buffers for the address lines. After the address information is latched, the 8086 remove the address information from AD0 - AD15 and outputs the desired data on these lines.

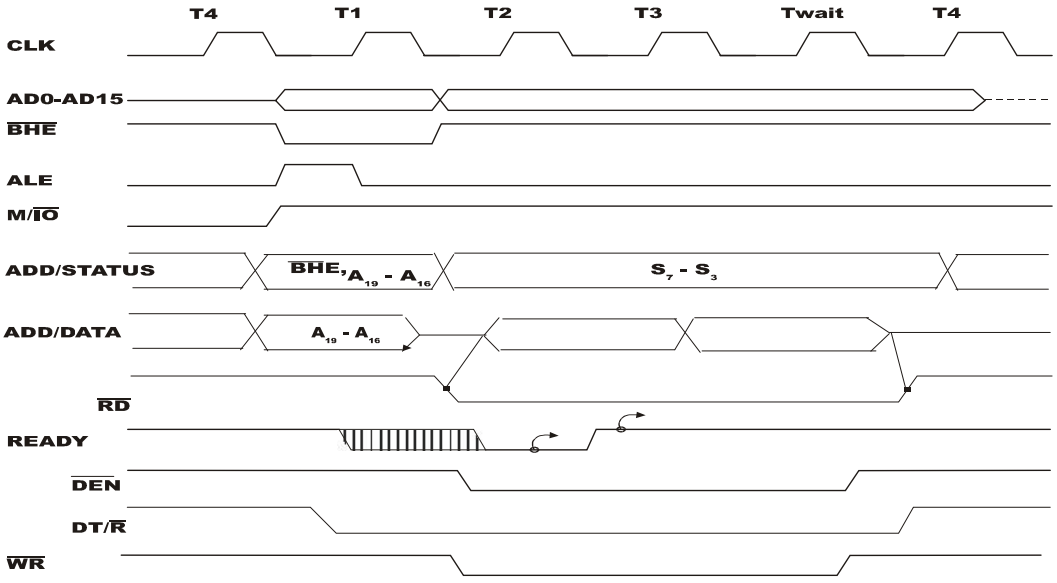

Fig. 13 - Write Timing Diagram

If the READY input is sampled LOW by the 8086 before or during T2 of the machine cycle, the 8086 will insert a WAIT state after T3. If the READY input is sampled high before the end of the WAIT state, the 8086 will go on with state T4 as soon as it completes the WAIT state. The 8086 will continue to insect wait states for as long as the READY is sampled low just before the end of each WAIT state.

Pin Configuration

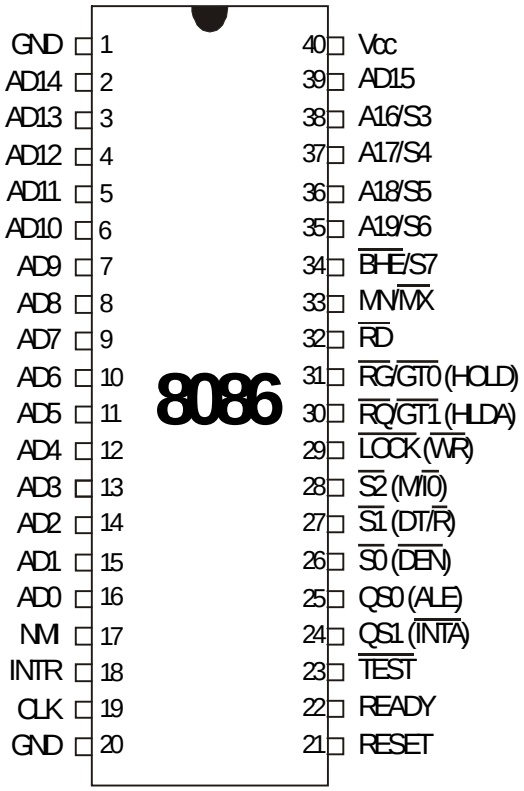

Fig. 1 - Pin Configuration

The following pin function descriptions are for the microprocessor 8086 in either minimum or maximum mode. The 8086 pins signals are TTL compatible.

AD0 - AD15 (I/O): Address Data Bus

These lines constitute the time multiplexed memory/IO address during the first clock cycle (T1) and data during T2, T3 and T4 clock cycles. A0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D0-D7. A0 bit is Low during T1 state when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. 8-bit oriented devices tied to the lower half would normally use A0 to condition chip select functions. These lines are active high and float to tri-state during interrupt acknowledge and local bus "Hold acknowledge". Fig. 2 shows the timing of $AD_0 - AD_{15}$ lines to access data and address.

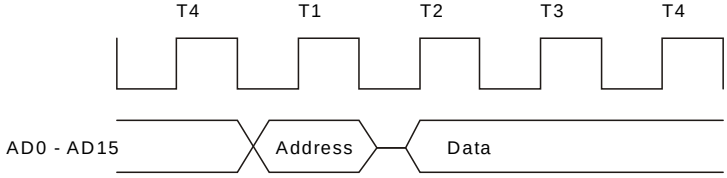

Fig. .2

A19/S6, A18/S5, A17/S4, A16/S3 (0): Address/Status

During T1 state these lines are the four most significant address lines for memory operations. During I/O operations these lines are low. During memory and I/O operations, status information is available on these lines during T2, T3, and T4 states.

S5: The status of the interrupt enable flag bit is updated at the beginning of each cycle. The status of the flag is indicated through this bus.

S6: When Low, it indicates that 8086 is in control of the bus. During a "Hold acknowledge" clock period, the 8086 tri-states the S6 pin and thus allows another bus master to take control of the status bus.

S3 & S4: Lines are decoded as follows:

A17/S4	A16/S3	Function
0	0	Extra segment access
0	1	Stack segment access
1	0	Code segment access
1	1	Data segment access

Table 1

After the first clock cycle of an instruction execution, the A17/S4 and A16/S3 pins specify which segment register generates the segment portion of the 8086 address. Thus by decoding these lines and using the decoder outputs as chip selects for memory chips, up to 4 Megabytes (one Mega per segment) of memory can be accesses. This feature also provides a degree of protection by preventing write operations to one segment from erroneously overlapping into another segment and destroying information in that segment.

$\overline{\text{BHE}}$**/S7 (O): Bus High Enable/Status**

During T1 state the $\overline{\text{BHE}}$ should be used to enable data onto the most significant half of the data bus, pins D15 - D8. Eight-bit oriented devices tied to the upper half of the bus would normally use $\overline{\text{BHE}}$ to control chip select functions. $\overline{\text{BHE}}$ is Low during T1 state of read, write and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus.

The S7 status information is available during T2, T3 and T4 states. The signal is active Low and floats to 3-state during "hold" state. This pin is Low during T1 state for the first interrupt acknowledge cycle.

$\overline{\text{RD}}$ **(O): READ**

The Read strobe indicates that the processor is performing a memory or I/O read cycle. This signal is active low during T2 and T3 states and the Tw states of any read cycle. This signal floats to tri-state in "hold acknowledge cycle".

$\overline{\text{TEST}}$ **(I)**

$\overline{\text{TEST}}$ pin is examined by the "WAIT" instruction. If the $\overline{\text{TEST}}$ pin is Low, execution continues. Otherwise the processor waits in an "idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK.

INTR (I): Interrupt Request

It is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge

operation. A subroutine is vectored to via an interrupt vector look up table located in system memory. It can be internally masked by software resetting the interrupt enable bit INTR is internally synchronized. This signal is active HIGH.

NMI (I): Non-Muskable Interrupt

An edge triggered input, causes a type-2 interrupt. A subroutine is vectored to via the interrupt vector look up table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH on this pin initiates the interrupt at the end of the current instruction. This input is internally synchronized.

Reset (I)

Reset causes the processor to immediately terminate its present activity. To be recognised, the signal must be active high for at least four clock cycles, except after power-on which requires a 50 Micro Sec. pulse. It causes the 8086 to initialize registers DS, SS, ES, IP and flags to all zeros. It also initializes CS to FFFF H. Upon removal of the RESET signal from the RESET pin, the 8086 will fetch its next instruction from the 20 bit physical address FFFF0H. The reset signal to 8086 can be generated by the 8284. (Clock generation chip). To guarantee reset from power-up, the reset input must remain below 1.5 volts for 50 Micro sec. after Vcc has reached the minimum supply voltage of 4.5V. The RES input of the 8284 can be driven by a simple RC circuit as shown in fig.3.

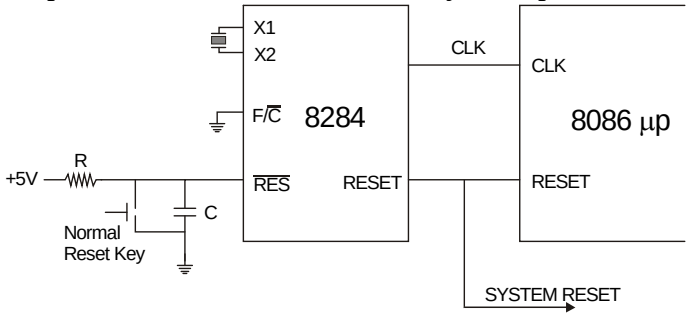

Fig. .3

The value of R and C can be selected as follows:

$Vc(t) = V(1 - e^{-t/RC})$ t = 50 Micro sec.

V = 4.5 volts, Vc = 1.05V and RC = 188 Micro sec.

C = 0.1 Micro F; R = 1.88 K ohms.

CPU component	Contents
Flags	Cleared
Instruction Pointer	0000H
CS register	FFFFH
DS register	0000H
SS register	0000H
ES register	0000H
Queue	Empty

Table – .2 System Registers after Reset

8086/88 RESET line provide an orderly way to start an executing system. When the processor detects the positive-going edge of a pulse on RESET, it terminates all activities until the signal goes low, at which time it initializes the system as shown in table .2.

Ready (I)

Ready is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. The READY signal from memory or I/O is synchronized by the 8284 clock generator to form READY. This signal is active HIGH. The 8086 READY input is not synchronized. Correct operation is not guaranteed if the setup and hold times are not met.

CLK (I): Clock

Clock provides the basic timing for the processor and bus controller. It is asymmetric with 33% duty cycle to provide optimized internal timing. Minimum frequency of 2 MHz is required, since the design of 8086 processors incorporates dynamic cells. The maximum clock frequencies of the 8086-4, 8086 and 8086-2 are

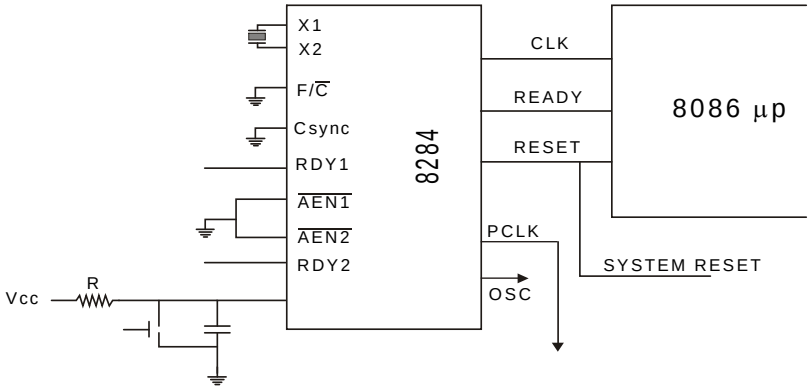

Fig..4

4MHz, 5MHz and 8MHz respectively. Since the 8086 does not have on-chip clock generation circuitry, and 8284 clock generator chip must be connected to the 8086 clock pin. The crystal connected to 8284 must have a frequency 3 times the 8086 internal frequency. The 8284 clock generation chip is used to generate READY, RESET and CLK. It is as shown in fig..4

MN/$\overline{MX}$ (I): Maximum / Minimum

This pin indicates what mode the processor is to operate in. In minimum mode, the 8086 itself generates all bus control signals. In maximum mode the three status signals are to be decoded to generate all the bus control signals.

Minimum Mode Pins

The following 8 pins function descriptions are for the 8086 in minimum mode; MN/$\overline{MX}$ = 1. The corresponding 8 pins function descriptions for maximum mode is explained later.

M/$\overline{IO}$ (O): Status line

This pin is used to distinguish a memory access or an I/O accesses. When this pin is Low, it accesses I/O and when high it access memory. M / $\overline{IO}$ becomes valid in the T4 state preceding a bus cycle and remains valid until the final T4 of the cycle. M/$\overline{IO}$ floats to 3 - state OFF during local bus "hold acknowledge".

$\overline{WR}$ **(O): Write**

Indicates that the processor is performing a write memory or write IO cycle, depending on the state of the M / $\overline{IO}$ signal. $\overline{WR}$ is active for T2, T3 and Tw of any write cycle. It is active LOW, and floats to 3-state OFF during local bus "hold acknowledge ".

$\overline{INTA}$ **(O): Interrupt Acknowledge**

It is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T2, T3, and T4 of each interrupt acknowledge cycle.

ALE (O): Address Latch Enable

ALE is provided by the processor to latch the address into the 8282/8283 address latch. It is an active high pulse during T1 of any bus cycle. ALE signal is never floated.

DT/$\overline{R}$ (O): DATA Transmit/Receive

In minimum mode, 8286/8287 transceiver is used for the data bus. DT/$\overline{R}$ is used to control the direction of data flow through the transceiver. This signal floats to tri-state off during local bus "hold acknowledge".

$\overline{DEN}$ **(O): Data Enable**

It is provided as an output enable for the 8286/8287 in a minimum system which uses the transceiver. $\overline{DEN}$ is active LOW during each memory and IO access. It will be low beginning with T2 until the middle of T4, while for a write cycle, it is active from the beginning of T2 until the middle of T4. It floats to tri-state off during local bus "hold acknowledge".

HOLD & HLDA (I/O): Hold and Hold Acknowledge

Hold indicates that another master is requesting a local bus "HOLD". To be acknowledged, HOLD must be active HIGH. The processor receiving the "HOLD " request will issue HLDA (HIGH) as an acknowledgement in the middle of the T1-clock cycle. Simultaneous with the issue of HLDA, the processor will float the local bus and control lines. After "HOLD" is detected as being Low, the processor will lower the HLDA and when the processor needs to run another cycle, it will again drive the local bus and control lines.

Maximum Mode

The following pins function descriptions are for the 8086/8088 systems in maximum mode (*i.e.*. MN/$\overline{MX}$ = 0). Only the pins which are unique to maximum mode are described below.

.

S2, S1, S0 (O): Status Pins

These pins are active during T4, T1 and T2 states and is returned to passive state (1,1,1 during T3 or Tw (when ready is inactive). These are used by the 8288 bus controller to generate all memory and I/O operation) access control signals. Any change by S2, S1, S0

during T4 is used to indicate the beginning of a bus cycle. These status lines are encoded as shown in table 3.

S2	S1	S0	Characteristics
0	0	0	Interrupt acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive State

Table 3

QS0, QS1 (O): Queue – Status

Queue Status is valid during the clock cycle after which the queue operation is performed. QS0, QS1 provide status to allow external tracking of the internal 8086 instruction queue. The condition of queue status is shown in table 4.

Queue status allows external devices like In-circuit Emulators or special instruction set extension co-processors to track the CPU instruction execution. Since instructions are executed from the 8086 internal queue, the queue status is presented each CPU clock cycle and is not related to the bus cycle activity. This mechanism allows

(1) A processor to detect execution of a ESCAPE instruction which directs the co-processor to perform a specific task and

(2) An in-circuit Emulator to trap execution of a specific memory location.

QS1	QS1	Characteristics
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

Table 4

$\overline{\text{LOCK}}$ **(O)**

It indicates to another system bus master, not to gain control of the system bus while $\overline{\text{LOCK}}$ is active Low. The $\overline{\text{LOCK}}$ signal is activated by the "LOCK" prefix instruction and remains active until the completion of the instruction. This signal is active Low and floats to tri-state OFF during 'hold acknowledge".

Example: LOCK XCHG reg., Memory ; Register is any register and memory GT_0
;is the address of the semaphore.

$\overline{\text{RQ}}/\overline{\text{GT}_0}$ and $\overline{\text{RQ}}/\overline{\text{GT}_1}$ **(I/O): Request/Grant**

These pins are used by other processors in a multi processor organization. Local bus masters of other processors force the processor to release the local bus at the end of the processors current bus cycle. Each pin is bi-directional and has an internal pull up resistors. Hence they may be left un-connected.