FPGAspeaks

Level-1

Chittidi Dhanusha Lakshmi Durga

October 2023

1 Introduction

This level-1 of FPGAspeaks describes about the fundamental logic gates AND,OR,NAND,NOR,NOT,XOR,XNOR and their implementation in verilog.

2 Tools/Requirements

Xilinx Vivado 2016

3 Basic Logic gates

i. **AND Gate:** Output becomes high when both inputs are high.

ii. **OR Gate:** Output becomes low when both inputs are low.

iii. **NAND Gate:** Output becomes low when both inputs are high.It can be designed by negation of AND gate

iv. **NOR Gate:** Output becomes high when both inputs are low.It can be designed by applying negation to OR gate

v. **NOT Gate:** Output becomes compliment of the input.

vi. **XOR Gate:** Output becomes high when odd number of inputs are high.

vii. **XNOR Gate:**Output becomes high when even number of inputs are high..It can be designed by applying negation to XOR gate.

4 What have I done in this level?

Basic logic gates are implemented using Xilinx Vivado for digital circuit design. In Vivado, we can create designs that utilize these fundamental logic gates to perform various logical operations in digital systems.

5 Links

Link to my GitHub