Digital Design and Computer Organisation Laboratory

3rd Semester, Academic Year 2025

Date:

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Week Number: 2

1. Circuit- 1

Design.v

```
module simple_circuit  (A, B, C, D, E);
output D, E;  input A, B, C;  wire w1;
and G1 (w1,A,B); // Optional  gate instance name
not G2 (E,C);
or G3 ( D, w1 ,E);
endmodule

~
~
```

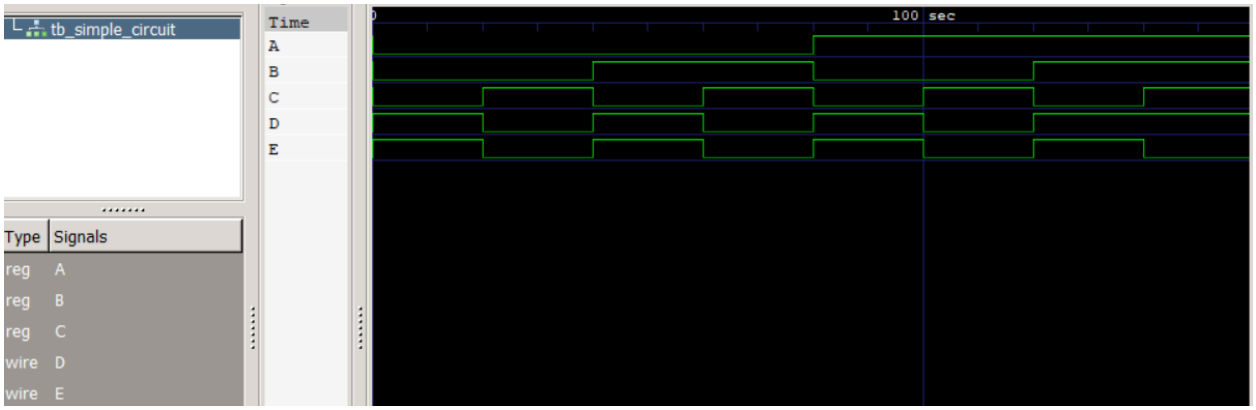
Testbench.v

```
module tb_simple_circuit;
  wire D, E;
  reg A, B, C;

  simple_circuit M1(A, B, C, D, E);

  initial begin
    A = 1'b0; B = 1'b0; C = 1'b0; #20;
    A = 1'b0; B = 1'b0; C = 1'b1; #20;
    A = 1'b0; B = 1'b1; C = 1'b0; #20;
    A = 1'b0; B = 1'b1; C = 1'b1; #20;
    A = 1'b1; B = 1'b0; C = 1'b0; #20;
    A = 1'b1; B = 1'b0; C = 1'b1; #20;
    A = 1'b1; B = 1'b1; C = 1'b0; #20;
    A = 1'b1; B = 1'b1; C = 1'b1; #20;
  end

  initial begin
    $monitor($time, " A=%b, B=%b, C=%b, D=%b, E=%b", A, B, C, D, E);
  end

  initial begin
    $dumpfile("tb_simple_circuit.vcd");
    $dumpvars(1, tb_simple_circuit);
  end
endmodule

~
~
```

Vvp output:

```
PS C:\Users\anu29\Course_materials\sem3\DDCO_lab\week2\circuit1> vvp test
VCD info: dumpfile tb_simple_circuit.vcd opened for output.
                   0 A=0, B=0, C=0, D=1, E=1
                  20 A=0, B=0, C=1, D=0, E=0
                  40 A=0, B=1, C=0, D=1, E=1
                  60 A=0, B=1, C=1, D=0, E=0
                  80 A=1, B=0, C=0, D=1, E=1
                 100 A=1, B=0, C=1, D=0, E=0
                 120 A=1, B=1, C=0, D=1, E=1
                 140 A=1, B=1, C=1, D=1, E=0
```

Gtkwave:



2. Circuit- 2

Design.v

```
module simple_circuit  (A, B, C, D);
output D;
input A, B, C;
wire w1;
and G1 (w1,C,B); // Optional  gate instance name
or G3 ( D, w1 ,A);
endmodule

~
```

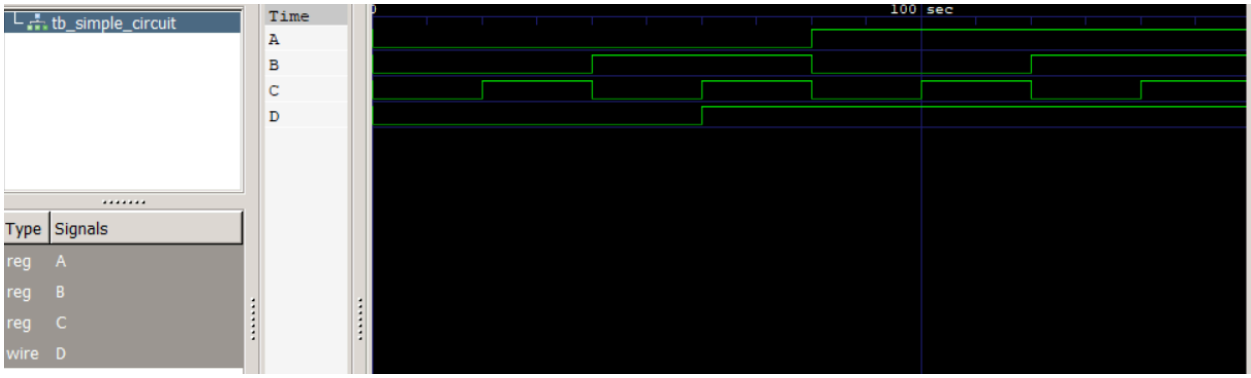
Testbench.v

```
module tb_simple_circuit;
  wire D;
  reg A, B, C;

  simple_circuit M1(A, B, C, D);

  initial begin
    A = 1'b0; B = 1'b0; C = 1'b0; #20;
    A = 1'b0; B = 1'b0; C = 1'b1; #20;
    A = 1'b0; B = 1'b1; C = 1'b0; #20;
    A = 1'b0; B = 1'b1; C = 1'b1; #20;
    A = 1'b1; B = 1'b0; C = 1'b0; #20;
    A = 1'b1; B = 1'b0; C = 1'b1; #20;
    A = 1'b1; B = 1'b1; C = 1'b0; #20;
    A = 1'b1; B = 1'b1; C = 1'b1; #20;
  end

  initial begin
    $monitor($time, " A=%b, B=%b, C=%b, D=%b", A, B, C, D);
  end

  initial begin
    $dumpfile("tb_simple_circuit.vcd");
    $dumpvars(1, tb_simple_circuit);
  end
endmodule
```

Vvp o/p:

```
PS C:\Users\anu29\Course_materials\sem3\DDCO_lab\week2\circuit2> vvp test
VCD info: dumpfile tb_simple_circuit.vcd opened for output.
                   0 A=0, B=0, C=0, D=0
                  20 A=0, B=0, C=1, D=0
                  40 A=0, B=1, C=0, D=0
                  60 A=0, B=1, C=1, D=1
                  80 A=1, B=0, C=0, D=1
                 100 A=1, B=0, C=1, D=1
                 120 A=1, B=1, C=0, D=1
                 140 A=1, B=1, C=1, D=1
```

Gtkwave:



Circuit 3:

Design.v

```
module simple_circuit  (A, B, C, D);
output D;  input A, B, C;
wire w1,w2,w3;
and G1 (w1,C,B);
or G2 (w2,A,w1);
and G3 (w3,A,B);
or G4 (D,w3,w2);
endmodule
```

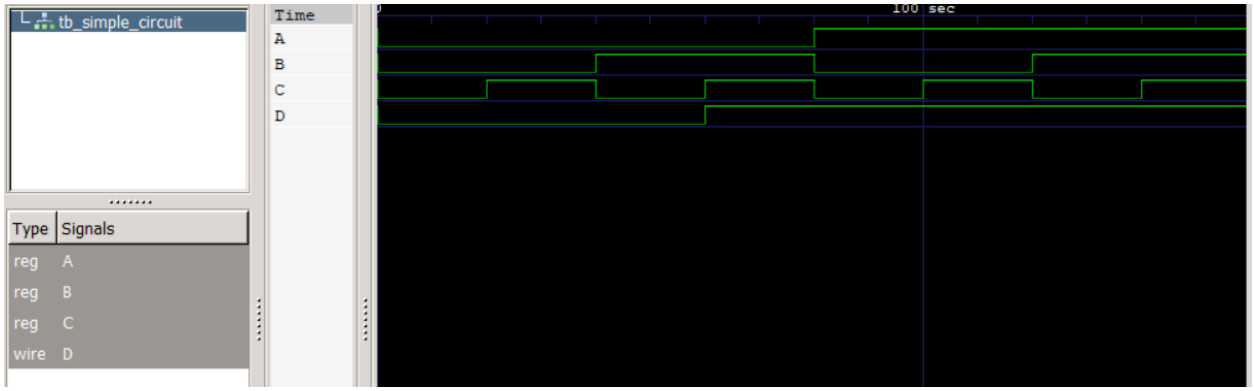
Testbench.v

```
module tb_simple_circuit;
  wire D;
  reg A, B, C;


  simple_circuit M1(A, B, C, D);

  initial begin
    A = 1'b0; B = 1'b0; C = 1'b0; #20;
    A = 1'b0; B = 1'b0; C = 1'b1; #20;
    A = 1'b0; B = 1'b1; C = 1'b0; #20;
    A = 1'b0; B = 1'b1; C = 1'b1; #20;
    A = 1'b1; B = 1'b0; C = 1'b0; #20;
    A = 1'b1; B = 1'b0; C = 1'b1; #20;
    A = 1'b1; B = 1'b1; C = 1'b0; #20;
    A = 1'b1; B = 1'b1; C = 1'b1; #20;
  end

  initial begin
    $monitor($time, " A=%b, B=%b, C=%b, D=%b ", A, B, C, D);
  end

  initial begin
    $dumpfile("tb_simple_circuit.vcd");
    $dumpvars(1, tb_simple_circuit);
  end
endmodule
```

Vvp o/p:

```
PS C:\Users\anu29\Course_materials\sem3\DDCO_lab\week2\circuit3> vvp test
VCD info: dumpfile tb_simple_circuit.vcd opened for output.
                   0 A=0, B=0, C=0, D=0
                  20 A=0, B=0, C=1, D=0
                  40 A=0, B=1, C=0, D=0
                  60 A=0, B=1, C=1, D=1
                  80 A=1, B=0, C=0, D=1
                 100 A=1, B=0, C=1, D=1
                 120 A=1, B=1, C=0, D=1
                 140 A=1, B=1, C=1, D=1
```

Gtkwave:



Circuit 4:

design.v

```
design.v
6   module simple_circuit  (A, B, O, F);
5   output F;
4   input A, B, O;
3   wire w1;
2   and G1 (w1,A,B);
1   or G2 (F,w1,O);
7   endmodule
1
```

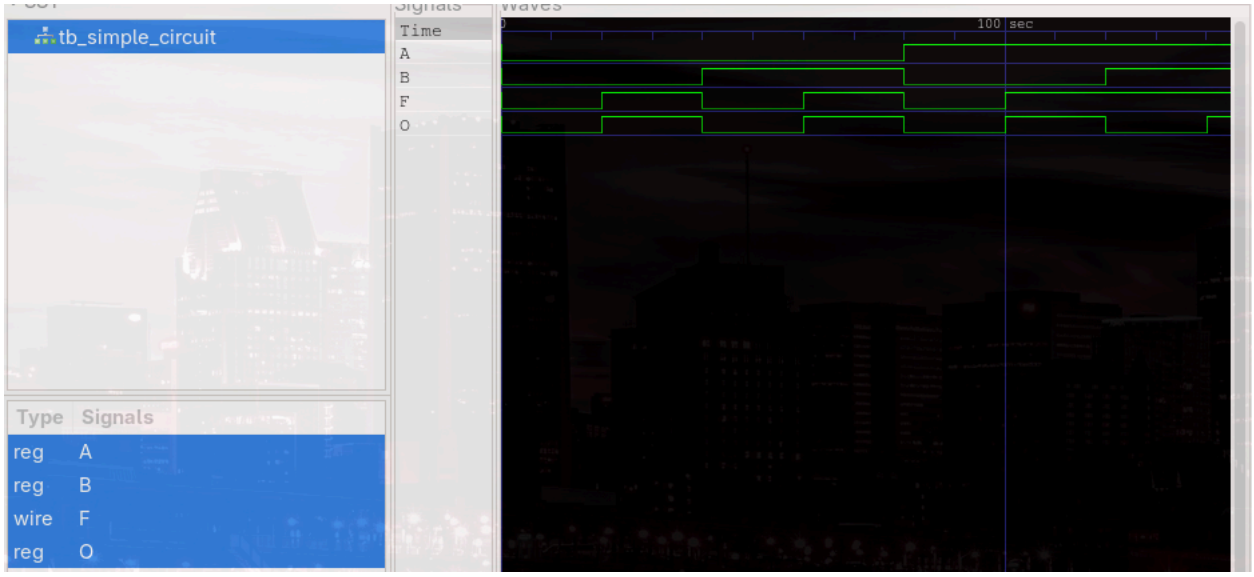
Testbench.v

```
module tb_simple_circuit;
  wire F;
  reg A, B, O;

  simple_circuit M1(A, B, O, F);

  initial begin
    A = 1'b0; B = 1'b0; O = 1'b0; #20;
    A = 1'b0; B = 1'b0; O = 1'b1; #20;
    A = 1'b0; B = 1'b1; O = 1'b0; #20;
    A = 1'b0; B = 1'b1; O = 1'b1; #20;
    A = 1'b1; B = 1'b0; O = 1'b0; #20;
    A = 1'b1; B = 1'b0; O = 1'b1; #20;
    A = 1'b1; B = 1'b1; O = 1'b0; #20;
    A = 1'b1; B = 1'b1; O = 1'b1; #20;
  end

  initial begin
    $monitor($time, " A=%b, B=%b, O=%b, F=%b ", A, B, O, F);
  end

  initial begin
    $dumpfile("tb_simple_circuit.vcd");
    $dumpvars(1, tb_simple_circuit);
  end
endmodule
```

Vvp o/p

```
dharani@archlinux /m/s/U/a/C/s/D/w/circuit4 ✓>
vvp test
VCD info: dumpfile tb_simple_circuit.vcd opened for output.
                   0 A=0, B=0, O=0, F=0
                  20 A=0, B=0, O=1, F=1
                  40 A=0, B=1, O=0, F=0
                  60 A=0, B=1, O=1, F=1
                  80 A=1, B=0, O=0, F=0
                 100 A=1, B=0, O=1, F=1
                 120 A=1, B=1, O=0, F=1
                 140 A=1, B=1, O=1, F=1
```

Gtkwave:


tb_simple_circuit
Type Signals
reg A
reg B
wire F
reg O
Time
A
B
F
O
100 sec