PES UNIVERSITY, Bangalore

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Department of Computer Science & Engineering

UE24CS251A: DIGITAL DESIGN AND COMPUTER ORGANIZATION

Unit 3

1. Which is NOT a characteristic of secondary memory?
   a) Non-volatile storage
   b) Cheaper per bit than primary memory
   c) Directly accessible by the CPU
   d) Provides large storage capacity

Ans: c) Directly accessible by the CPU

2. Which of the following best describes the function of the Control Unit (CU)?
   a) Performs logical comparisons of data.
   b) Generates timing and control signals to coordinate computer operations.
   c) Stores frequently accessed data and instructions.
   d) Acts as a permanent repository for system programs.

Answer: b) Generates timing and control signals to coordinate computer operations

3. Which of the following statements is correct regarding **primary vs secondary memory**?
   a) Primary memory is slower but larger than secondary memory.
   b) Secondary memory is volatile, whereas primary memory is non-volatile.
   c) Primary memory is directly accessible by the CPU, while secondary memory is not.
   d) Both memories are equally fast but differ in size.

Answer: c) Primary memory is directly accessible by the CPU, while secondary memory is not

4. The Program Counter (PC) of a processor contains 0x200. The instruction at 0x200 is a branch instruction to address 0x400. Assuming the branch is taken, what will be the content of the PC after the instruction is executed?

a) 0x200
b) 0x201
c) 0x400
d) 0x401

Answer: c) 0x400
Explanation: PC holds the address of the next instruction. For a branch instruction, if the branch is taken, the PC is loaded with the branch target (0x400).

5. Which of the following registers acts as a buffer between CPU and main memory?

a) Program Counter (PC)

b) Memory Address Register (MAR)

c) Memory Data Register (MDR)

d) Instruction Register (IR)

Answer: c) Memory Data Register (MDR)

Explanation: MDR holds the actual data being transferred to/from memory, acting as a buffer.

6. An **interrupt** in a computer system is best described as:

a) A request from an I/O device for immediate processor service
b) A program error caused by division by zero
c) A trap used to handle illegal instructions
d) A buffer overflow condition

Answer: a) A request from an I/O device for immediate processor service
Explanation: Interrupts are signals raised by I/O devices to get urgent CPU service.

7. Which of the following is a major drawback of the **single-bus structure** in computer organization?

a) High cost of connecting devices
b) Only one transfer at a time is possible
c) Difficult to attach peripheral devices
d) Requires multiple buffer registers

Answer: b) Only one transfer at a time is possible
Explanation: A single bus allows only two devices to communicate at a time, creating bottlenecks.

8. In sign-and-magnitude representation using 4 bits, the result of $(+5) + (-5)$is:

a) 0000 (unique zero)
b) 1000 (alternate zero)
c) Either 0000 or 1000 (two representations of zero)
d) 1111

Answer: c) Either 0000 or 1000 (two representations of zero)

9. Which of the following statements about overflow in signed integer arithmetic is correct?

a) Overflow can occur when adding two numbers of opposite signs.
b) Overflow occurs when carry-out from MSB is 1.
c) Overflow occurs when adding two numbers of same sign and the result has opposite sign.
d) Overflow occurs when sign extension is applied.

Answer: c) Overflow occurs when adding two numbers of same sign and the result has opposite sign.

10. If numbers $X = 0111$and $Y = 1101$are added in 2's complement 4-bit representation, what is the result?

a) 0100 with overflow
b) 0010 with no overflow

c) 1110 with overflow
d) 1000 with no overflow

Answer: a) 0100 with overflow

11. system has 1K words of 16-bit memory. How many address lines are required to address the memory?

a) 8
b) 10
c) 16
d) 32

Answer: b) 10
(Reason: 210=10242^{10} = 1024210=1024 → 1K words, independent of word size.)

12. Consider a computer with 32-bit word length using **Big-Endian** format. If a 32-bit integer is stored at address 1000, which byte holds the Most Significant Byte (MSB)?

a) Address 1000
b) Address 1001
c) Address 1002
d) Address 1003

Answer: a) Address 1000
(Big-endian → MSB stored at lowest memory address.)

13. A memory unit has 16 address lines. If the memory is byte-addressable, what is the maximum memory capacity?

a) 64 KB
b) 128 KB
c) 256 KB
d) 512 KB

Answer: c) 256 KB
(Reason: 216=65,5362^{16} = 65,536216=65,536 addresses → 64K bytes = 64 KB.)

14. A computer uses 32-bit word length. In a byte-addressable memory, what are the addresses of the first four words?

a) 0, 1, 2, 3

b) 0, 4, 8, 12

c) 0, 2, 4, 6

d) 0, 8, 16, 24

Answer: b) 0, 4, 8, 12(Reason: Each word = 4 bytes; hence addresses increase by 4 for successive words.)

15. A processor executes instructions in **straight-line sequencing** unless:

a) A Load instruction is encountered
b) A Store instruction is encountered
c) A Branch instruction is encountered
d) A Condition Code is set

Answer: c) A Branch instruction is encountered
Explanation: Branch instructions alter the normal program counter (PC) sequence

16. Which condition flag is set to 1 if an arithmetic operation results in a value too large for the number of bits available?

a) Zero (Z)
b) Carry (C)
c) Overflow (V)
d) Sign (N)

Answer: c) Overflow (V)
Explanation: Overflow flag is set when the signed result exceeds representable range

17. Which one of the following instruction formats uses the **accumulator (AC)** implicitly as one operand?

a) Zero-address instruction
b) One-address instruction
c) Two-address instruction
d) Three-address instruction

Answer: b) One-address instruction
Explanation: In one-address instructions, one operand is explicitly given, while the accumulator (AC) is the implicit second operand

18. Consider the sequence of instructions:

Load P

Add Q

Store S

This corresponds to which instruction format?

a) Three-address
b) Two-address
c) One-address
d) Zero-address

Answer: c) One-address
Explanation: Only one explicit operand is specified in each instruction; the other operand is the accumulator

19. In **Register Addressing Mode**, which of the following is correct?
a) Operand is always stored in memory
b) Operand is always a constant
c) Operand is stored in CPU register specified in instruction
d) Operand is fetched using Program Counter (PC)

Answer: c) Operand is stored in CPU register specified in instruction

20.Which addressing mode is commonly used to implement **looping with counters**?
a) Immediate
b) Indexed
c) Register Indirect
d) Relative

Answer: b) Indexed

21. Which of the following addressing modes **does NOT require memory access** for operand fetch?
a) Register Addressing
b) Indirect Addressing
c) Direct Addressing
d) Indexed Addressing

Answer: a) Register Addressing

22.Which of the following addressing modes requires **two memory references** (excluding instruction fetch) to access an operand?
a) Immediate
b) Register Direct
c) Indirect
d) Indexed

Answer: c) Indirect

23. In Program Controlled I/O, which synchronization flag is set to 1 when a key is pressed on the keyboard?

a) SOUT
b) DATAIN
c) SIN
d) DATAOUT

Answer: c) SIN

24. The END directive in an Assembly program is used to:

a) Terminate program execution
b) Mark end of source program text
c) Generate an unconditional jump
d) Indicate the return address

Answer: b) Mark end of source program text

25. Which one of the following is an **assembler directive** and not a machine instruction?

a) MOVE
b) ADD
c) ORIGIN
d) LOAD

Answer: c) ORIGIN

26. A two-pass assembler is required mainly because:

a) It must scan the program twice to detect all errors
b) Forward references to labels cannot be resolved in a single pass
c) Directives must be placed before instructions
d) Loader requires two passes for relocation

Answer: b) Forward references to labels cannot be resolved in a single pass

27. In a computer system, if the **I/O devices and memory share the same address space**, the system is said to use:
a) Memory-mapped I/O
b) Isolated I/O
c) Program-controlled I/O
d) Direct I/O

Answer: a) Memory-mapped I/O

28.The CPU waits for a device to complete its operation by repeatedly checking its status register. This is called:

Interrupt-driven I/O

b) Direct Memory Access (DMA)

c) Polling

d) Channel I/O

Answer: c) Polling

29. The daisy chain priority scheme for handling multiple interrupts has the disadvantage that:

a) It requires more hardware lines

b) The device closest to the CPU has the lowest priority

c) The device farthest from the CPU has the lowest priority

d) All devices must generate interrupts simultaneously

Answer: c) The device farthest from the CPU has the lowest priority

30.The delay between the generation of an interrupt request and the execution of the corresponding ISR is known as

a) Cycle time

b) Instruction delay

c) Interrupt latency

d) Response time

Answer: c) Interrupt latency

31. In a DMA transfer, the role of the CPU is to:
a) Transfer data between I/O and memory directly
b) Provide the starting address and control to the DMA controller, then get interrupted after transfer
c) Continuously poll the device for data readiness
d) Perform all I/O operations itself

Answer: (b)
Explanation: CPU initializes DMA by giving starting address, word count, and direction. After completion, the DMA controller interrupts the CPU.

32.In a system using **cycle stealing DMA**, which statement is correct?
a) CPU is completely halted during DMA transfer.
b) CPU and DMA share bus cycles — DMA steals one memory cycle at a time.
c) CPU executes only I/O instructions during DMA transfer.
d) DMA controller uses dual-port RAM.

Answer: (b)
Explanation: In cycle stealing, DMA "steals" one memory cycle from the CPU, allowing CPU execution in the remaining cycles.

33.In a **daisy chain** priority scheme used for bus arbitration, which statement is true?
a) Highest priority device is closest to the processor.
b) Lowest priority device is closest to the processor.
c) All devices have equal priority.
d) Bus grant signal propagates from lowest to highest priority device.

Answer: (a)
Explanation: Bus grant passes sequentially through devices; the nearest device has highest priority.

34. In **distributed arbitration**,
a) A single bus arbiter assigns bus mastership.
b) Each device compares its ID on arbitration lines and highest ID wins.
c) Lowest ID device wins control.
d) Arbitration depends on interrupt priority levels.

Answer: (b)
Explanation: All devices participate by putting their 4-bit IDs on shared arbitration lines. Highest ID wins the bus.

35. In a **PCI transaction**, data transfer takes place when:
a) Both IRDY# and TRDY# signals are low.
b) Either IRDY# or TRDY# is high.
c) FRAME# and DEVSEL# are high.
d) DEVSEL# is low and TRDY# is high.

Answer: (a)
Explanation: Data is transferred only when both Initiator Ready (IRDY#) and Target Ready (TRDY#) are asserted low — ensuring handshake completion

36. Which of the following represents the correct sequence of phases during a PCI bus read operation?
a) Data → Address → Handshake → Completion
b) Address → Data → Handshake → Completion
c) Handshake → Address → Data → Completion
d) Address → Handshake → Data → Completion

Answer: (b)
Explanation: Address phase comes first, followed by one or more data phases controlled by IRDY#/TRDY#, then handshake and bus release (FRAME# deasserted)

37. In USB communication:
a) Devices can communicate directly with each other.
b) Communication is always initiated by the host.
c) Hubs can transfer data without host intervention.
d) Devices use interrupt lines to alert the host.

Answer: (b)
Explanation: USB uses a **host-controlled polling** mechanism — all transactions are host-initiated

38.SCSI supports high-speed transfers by:
a) Using interrupts for each byte.
b) Direct memory access (DMA) block transfers.
c) Polling I/O ports continuously.
d) Bit-serial CPU register copy.

Answer: (b)
Explanation: SCSI bus uses DMA for direct block transfers between I/O and memory

without CPU intervention

39. A 1K × 1 memory chip requires how many address lines?
a) 8
b) 10
c) 12
d) 16

Answer: (b)
Explanation:
Number of address lines = $\log_2(1024) = 10$.
Each address accesses one bit (1K × 1 = 1024 × 1-bit array)

40. In **SDRAM**, the term **"burst mode"** refers to:
a) Writing multiple rows simultaneously.
b) Reading or writing a sequence of data words in consecutive clock cycles after a single address.
c) Refreshing multiple rows in one clock cycle.
d) Transferring data on both clock edges.

Answer: (b)
Explanation: SDRAM burst mode allows sequential access to a series of columns within a row in consecutive cycles, improving data throughput

41. Which combination of memory technologies provides the best compromise between **speed, cost, and capacity** in a typical computer?
a) SRAM + DRAM + Magnetic Disk
b) SRAM + Flash + Optical Disk
c) DRAM + PROM + Cache
d) Flash + EEPROM + Tape

Answer: (a)
Explanation:

- **SRAM** → Cache (fast)
- **DRAM** → Main memory (moderate speed, cost)
- **Magnetic Disk** → Secondary storage (large capacity, cheap)
  This combination forms the standard memory hierarchy