DIGITAL DESIGN AND COMPUTER ORGANIZATION

Other counters

Team DDCO
Department of Computer Science and Engineering

Other Counters(T1 section 6.5)

Counters can be designed to generate any desired sequence of states. A divide-by- N counter (also known as a modulo- N counter) is a counter that goes through a repeated sequence of N states.

A circuit with n flip-flops has 2^n binary states. There are occasions when a sequential circuit uses fewer than this maximum possible number of states. **States that are not used in specifying the sequential circuit are not listed in the state table. In simplifying the input equations, the unused states may be treated as don't-care conditions or may be assigned specific next states.**

it is necessary to ensure that the circuit eventually goes into one of the valid states so that it can resume normal operation. Otherwise, if the sequential circuit circulates among unused states, there will be no way to bring it back to its intended sequence of state transitions

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Counter with Unused States

A circuit with n flip-flops has 2n binary states. There are occasions when a sequential circuit uses fewer than this maximum possible number of states. States that are not used In sequential circuit.

The count has a repeated sequence of six states, with flip-flops B and C repeating the binary count 00, 01, 10, and flip-flop A alternating between 0 and 1 every three counts.

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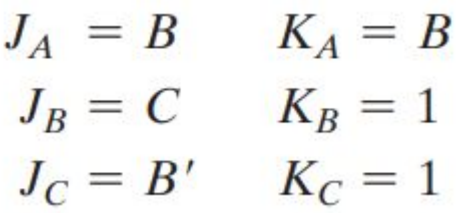
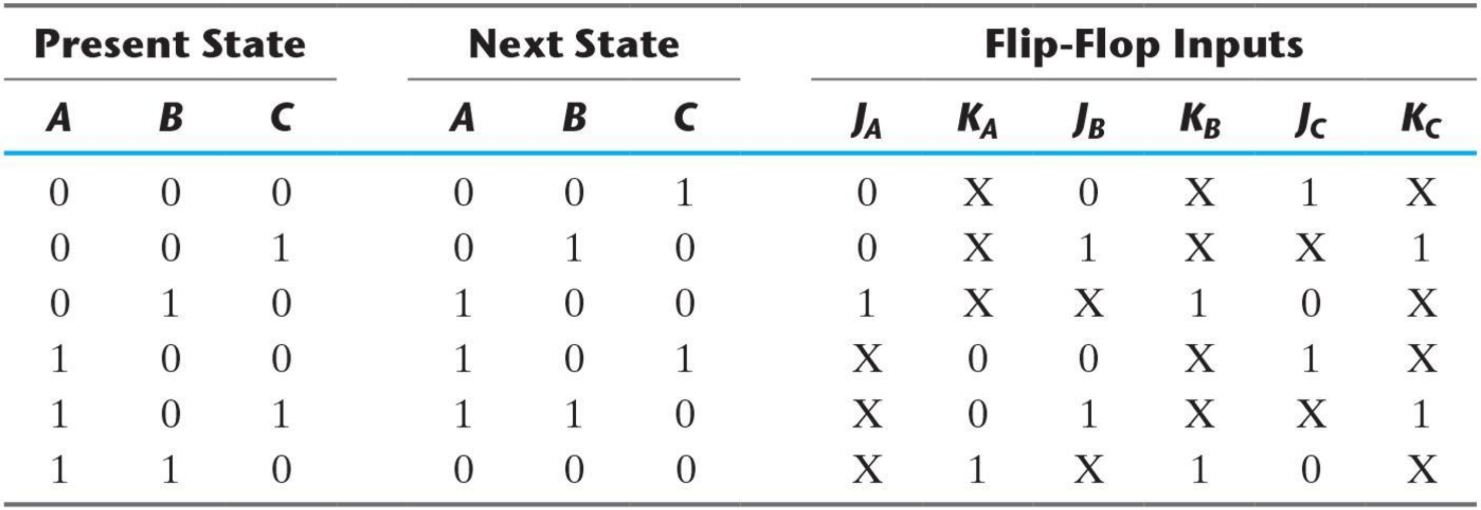
Other Counters with Unused States

Table 6.7
State Table for Counter.



$$J_A = B \qquad K_A = B$$
$$J_B = C \qquad K_B = 1$$
$$J_C = B' \qquad K_C = 1$$



Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

Unused states= 011 and 111

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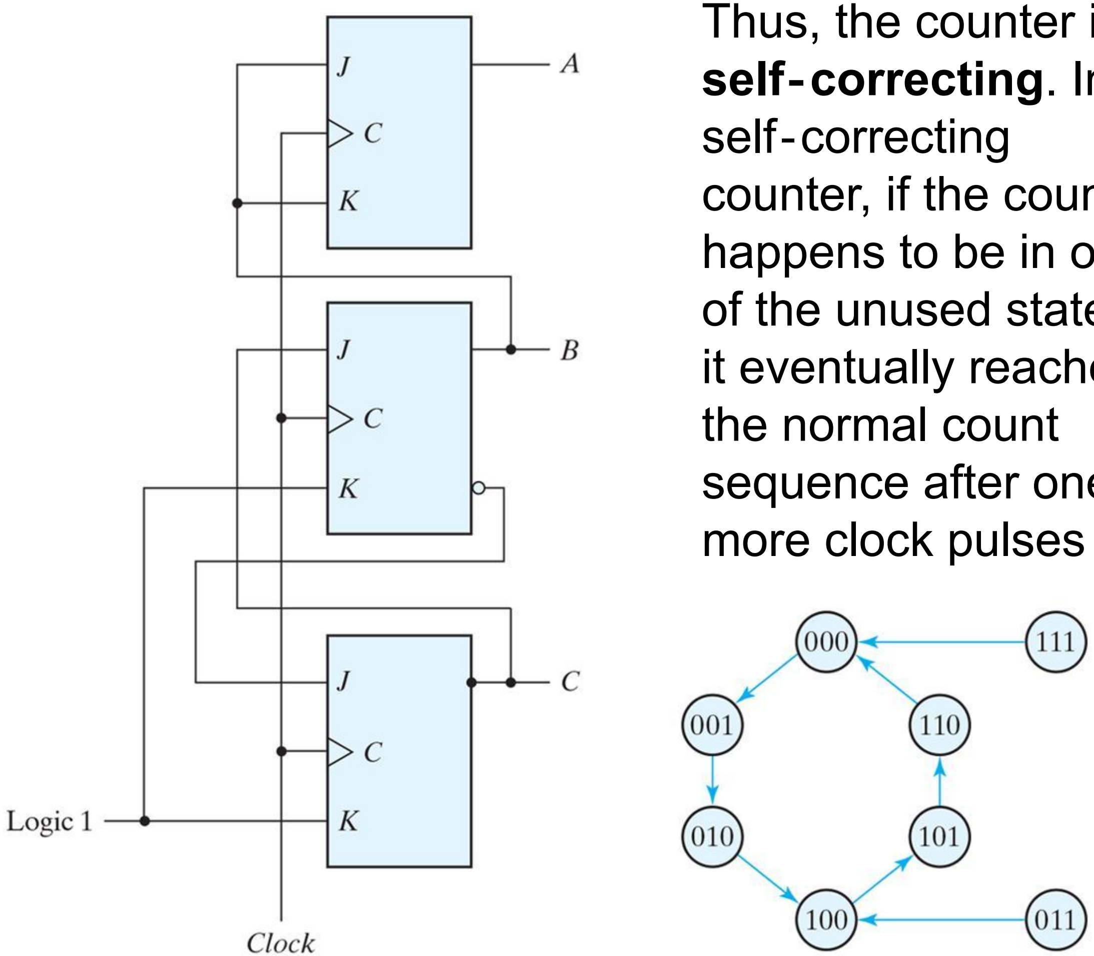
Other Counters with Unused States

Thus, the counter is **self-correcting**. In a self-correcting counter, if the counter happens to be in one of the unused states, it eventually reaches the normal count sequence after one or more clock pulses

Figure 6.16 Counter with unused states.



(a) Logic circuit diagram

(b) State transition diagram

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Ring Counters

A Ring Counter is a circular shift register with only one flip-flop being set at any particular time; all others are cleared. The single bit is shifted from one flip-flop to the next to produce the sequence of timing signals

The initial value of the register is 1000 and requires Preset/Clear flip-flops.

Each flip-flop is in the 1 state once every four clock cycles and produces one of the four timing signals

Each output becomes a 1 after the negative-edge transition of a clock pulse and remains 1 during the next clock cycle.

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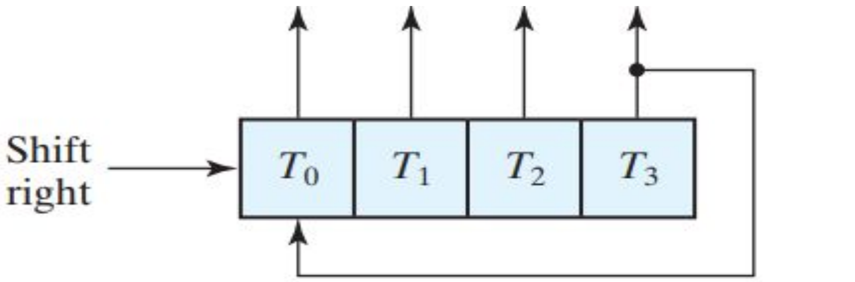
Ring Counters

- Single bit shifted right with every clock pulse and circulates back from T3 to T0. Each flip-flop is in the 1 state once every four clock cycles



(a) Ring-counter (initial value = 1000)

- It is negative edge triggered flipflop state changes on negative edge
- Initial value is always 1000

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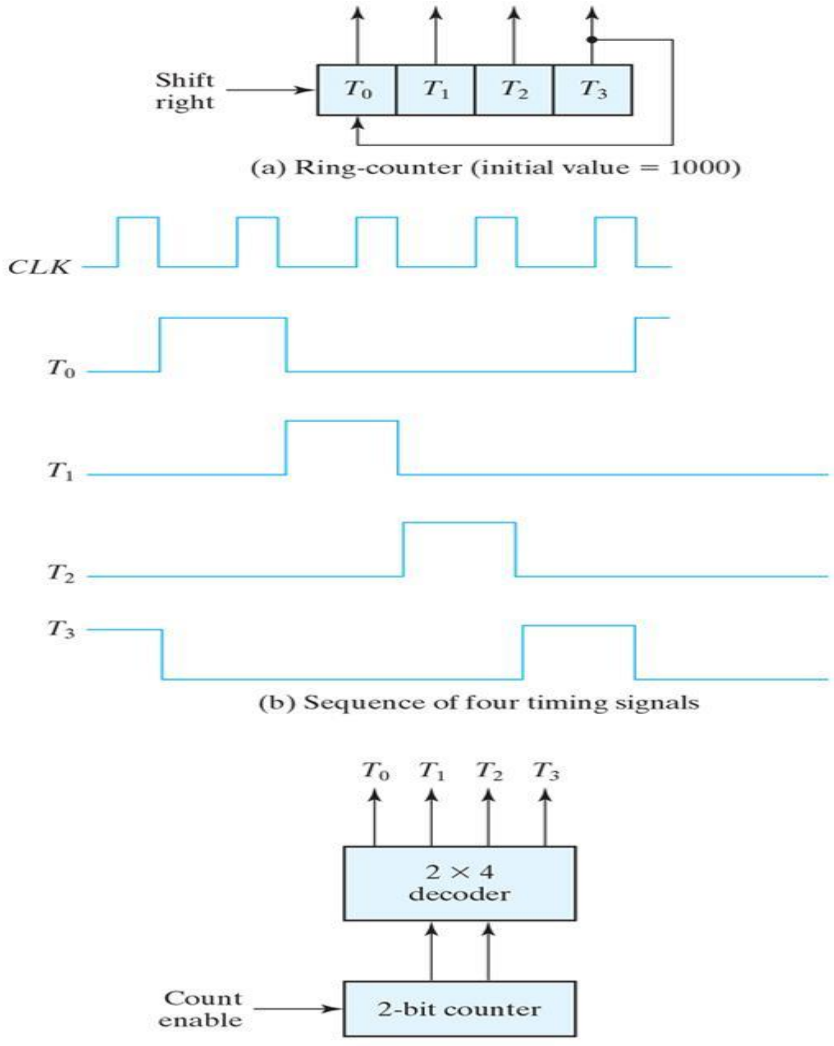
Ring Counters

Figure 6.17
Generation of timing signals.



(a) Ring-counter (initial value = 1000)

(b) Sequence of four timing signals

(c) Counter and decoder

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Ring Counters

To generate 2^n timing signals, we need either a shift register with 2^n flip-flops or an n -bit binary counter together with an n -to-2 ^{n} -line decoder.

For example, **16 timing signals can be generated with a 16-bit shift register connected as a ring counter or with a 4-bit binary counter and a 4-to-16-line decoder**. In the first case, we need 16 flip-flops. In the second, we need 4 flip-flops and 16 four-input AND gates for the decoder. It is also possible to generate the timing signals with a combination of a shift register and a decoder. That way, the number of flip-flops is less than that in a ring counter, and the decoder requires only two-input gates. This combination is called a Johnson counter .

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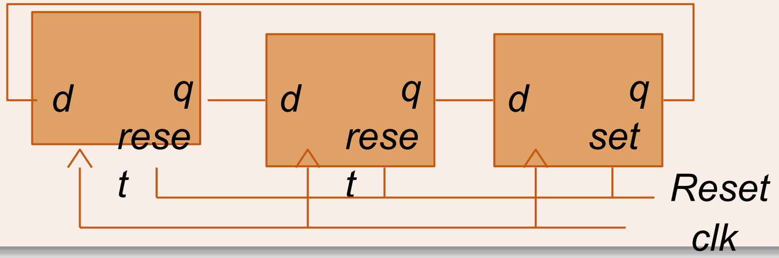
Ring Counters –Summary

- Counters constructed by connecting together flip-flops in closed loop, typically with a single 1 bit circulating among them, are called **ring counters**
- Modulus of an *n*-bit ring counter is *n*

3-bit Ring Counter



- Also called “one-hot” counters (as in one-hot encoding)

  Number of states= number of flipflop, mod-8 ring counter requires eight flip-flops and a mod-16 ring counter would require sixteen flip-flops.(number of states=number of flipflops) but Other flipflop number of states is =2^n

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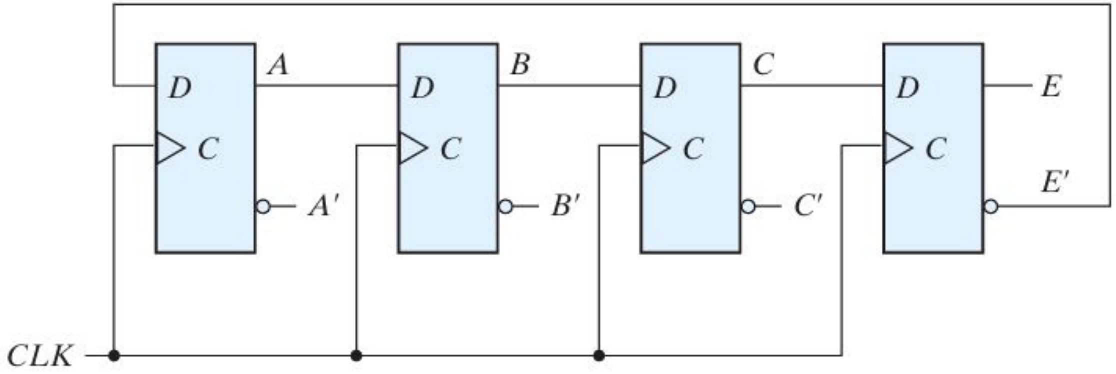
Johnson Counter

- A k -bit ring counter circulates a single bit among the flip-flops to provide k distinguish able states. The number of states can be doubled if the shift register is connected as a **switch-tail ring counter**.

- A switch-tail ring counter is a circular shift register with the complemented output of the last flip-flop connected to the input of the first flip-flop.



(a) Four-stage switch-tail ring counter

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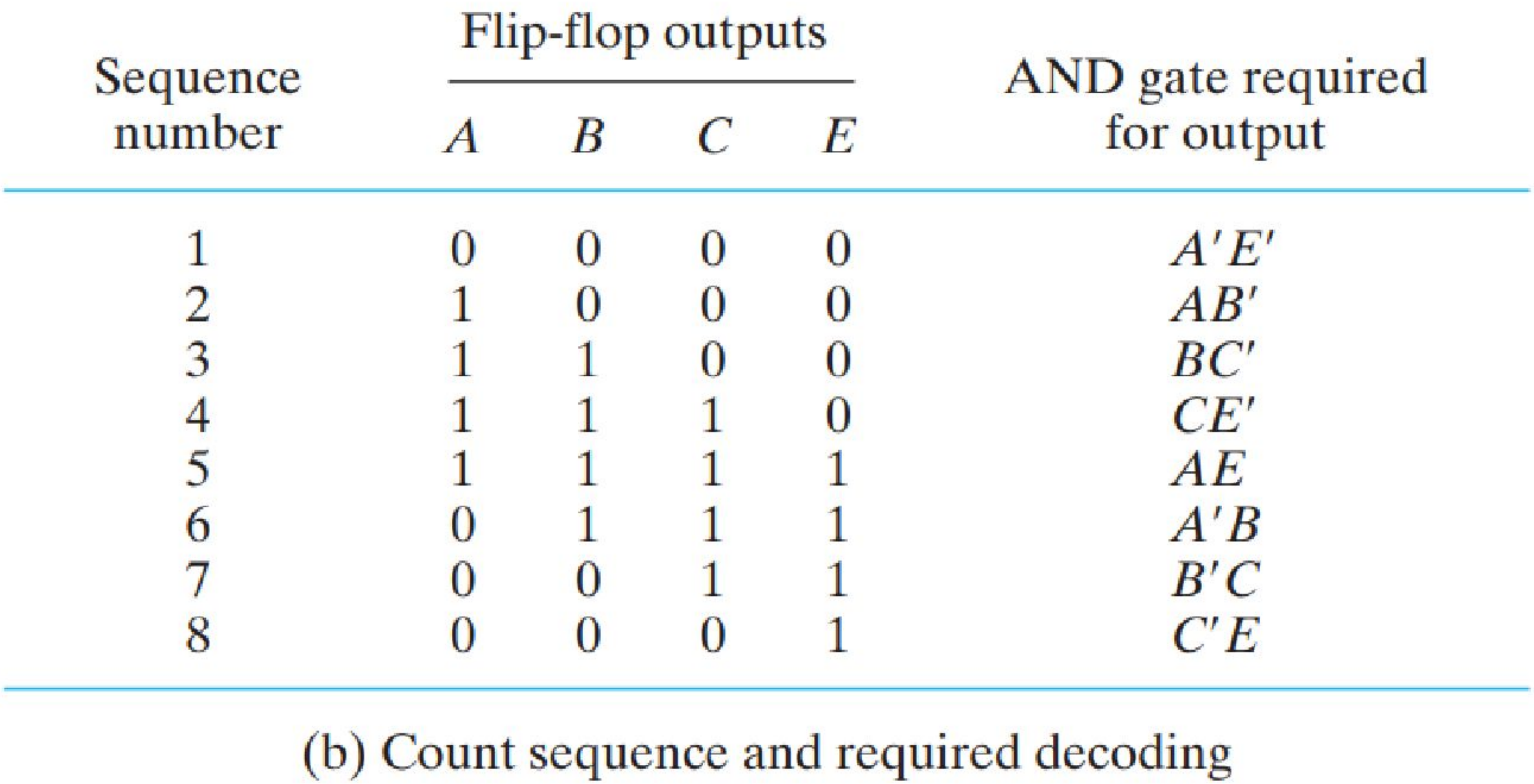
Johnson counter



Sequence number	Flip-flop outputs				AND gate required for output
	A	B	C	E	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

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Johnson counter

The circular connection is made from the complemented output of the rightmost flip-flop to the input of the leftmost flip-flop.
The register shifts its contents once to the right with every clock pulse, and at the same time, the complemented value of the E flip-flop is transferred into the A flip-flop.

In general, a k -bit switch-tail ring counter will go through a sequence of **2 k states**. Starting from all 0’s, each shift operation inserts 1’s from the left until the register is filled with all 1’s. In the next sequences, 0’s are inserted from the left until the register is again filled with all 0’s.

A Johnson counter is a k -bit switch-tail ring counter with 2 k decoding gates to pro vide outputs for 2 k timing signals.

The eight AND gates listed in the table, when connected to the circuit, will complete the construction of the Johnson counter.

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Johnson Counter

- One disadvantage of the circuit in Fig. 6.18 (a) is that if it finds itself in an unused state, it will persist in moving from one invalid state to another and never find its way to a valid state. The difficulty can be corrected by modifying the circuit to avoid this undesirable condition
- One correcting procedure is to disconnect the output from flip-flop B that goes to the D input of flip-flop C and instead enable the input of flip-flop C by the function
- $D_C = (A + C)B$ where D_C is the flip-flop input equation for the D input of flip-flop C. Johnson counters can be constructed for any number of timing sequences. The number of flip-flops needed is one-half the number of timing signals.
- The number of decoding gates is equal to the number of timing signals, and only two-input gates are needed.

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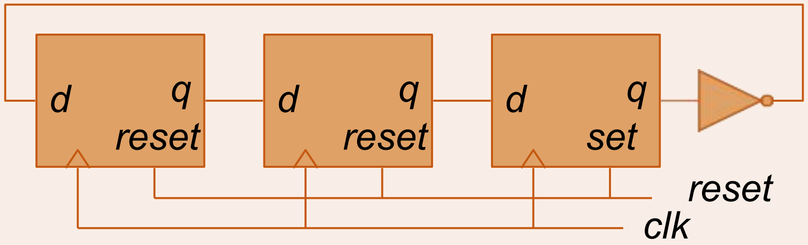
Johnson counter using D flipflop(negative edge triggered)-summary

3-bit Johnson (Twisted Ring) Counter (switch tail counter)



- What is the modulus of an *n*-bit Johnson counter?
  The MOD of the Johnson counter is 2n if n flip-flops are used. The main advantage of the Johnson counter is that it only needs half the number of flip-flops compared to the standard ring counter for the same MOD. (4ff=8 states(2n))

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Ring Counter applications

- **Application: Instruction Pipeline Controller in Microprocessors**
- In certain simple microcontrollers and DSP cores, a ring counter is used as the control unit for the pipeline stages (Fetch → Decode → Execute → Memory → Write-back).
- Why? A ring counter naturally cycles one “hot” bit through its outputs, so each stage gets activated in perfect round-robin order.
- This avoids the need for complex decoders and guarantees non-overlapping control signals, which is critical for synchronous CPU timing.
- *Practical use:* Intel’s early pipeline controllers and some ARM/DSP cores have used ring counters in control sequencing because they are simple, reliable, and glitch-free.

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Johnson Counter applications

Johnson Counter in LED Chaser / Marquee Display

- A Johnson counter (e.g., CD4017 IC) generates 10 sequential outputs (Q0–Q9).
- Each clock pulse activates one output at a time
- Connect 10 LEDs to Q0–Q9.On each clock tick:
- Q0 HIGH → LED1
- ONNext tick → Q1 HIGH → LED2 ON… continues until Q9, then loops back to Q0.
- LEDs light up one after another in a running sequence → “chaser” or “marquee” effect.

Applications:

- Advertising signboards

Why Johnson Counter?

- Only 5 flip-flops → 10 outputs
- No extra decoder needed

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MCQ

- A **4-bit synchronous counter with unused states** is designed to count only 6 states. If the counter accidentally enters an unused state, it eventually returns to the valid sequence. Such a counter is called:

(A) Non-deterministic counter
(B) Self-correcting counter
(C) Johnson counter
(D) Binary coded decimal counter

A 4-bit **switch-tail ring counter** (Johnson counter) starts from all 0's. Which of the following will be the **fifth state**?

(A) 1110
(B) 1111
(C) 0111
(D) 1000

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MCQ

- A **4-bit synchronous counter with unused states** is designed to count only 6 states. If the counter accidentally enters an unused state, it eventually returns to the valid sequence. Such a counter is called:

(A) Non-deterministic counter
(B) Self-correcting counter
(C) Johnson counter
(D) Binary coded decimal counter

Answer: (B) Self-correcting counter
Explanation: Self-correcting counters ensure that invalid states eventually lead back into the normal cycle.

- A 4-bit **switch-tail ring counter** (Johnson counter) starts from all 0's. Which of the following will be the **fifth state**?

(A) 1110
(B) 1111
(C) 0111
(D) 1000

Answer: (B) 1111
Explanation: Sequence: 0000 → 1000 → 1100 → 1110 → 1111 → … The 5th state = **1111**.

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MCQ

- A 3-bit synchronous counter is implemented using T-flip-flops and its present state is 101. What will be the next state?

A) 110
B) 011
C) 010
D) 001

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MCQ

- A 3-bit synchronous counter is implemented using T-flip-flops and its present state is 101. What will be the next state?

- A) 110
  B) 011
  C) 010
  D) 001

- **Answer:** (A) 110
  Explanation: In a synchronous up counter using T-FFs, each output toggles if its T input is 1. For a typical design, all T inputs = 1, so the next state from 101 (5) is 110 (6).

T0 = 1 (LSB toggles on every clock).

T1 = Q0 (next bit toggles when Q0 = 1).

T2 = Q0·Q1 (next bit toggles when Q0 and Q1 = 1).

In general, Tk=Q0⋅Q1⋅…⋅Qk−1T_k = Q_0 · Q_1 · … · Q_{k-1}

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