DIGITAL DESIGN AND COMPUTER ORGANIZATION

Multiplexers

Team DDCO

Department of Computer Science and Engineering

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Multiplexers

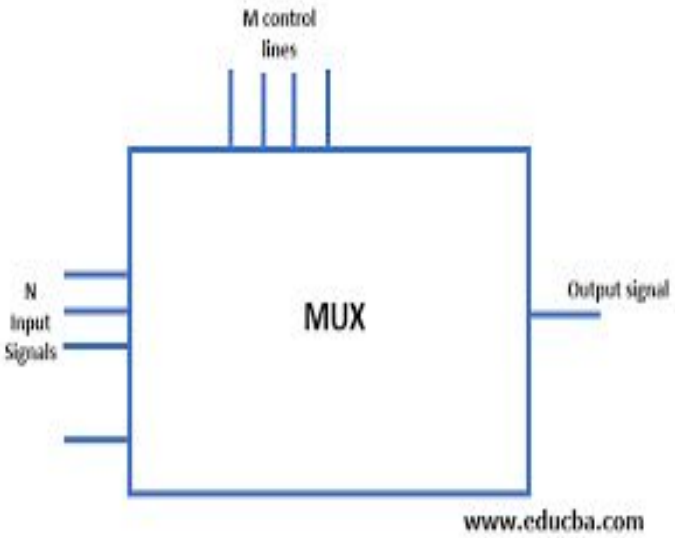
Department of Computer Science and Engineering

Combinational logic
Multiplexers

A multiplexer (also called a mux) *multiplexes* many inputs onto a single output
Data selector

Many to one

N:1 MUX
2^N inputs n select lines , one output



M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 4.11

Combinational logic

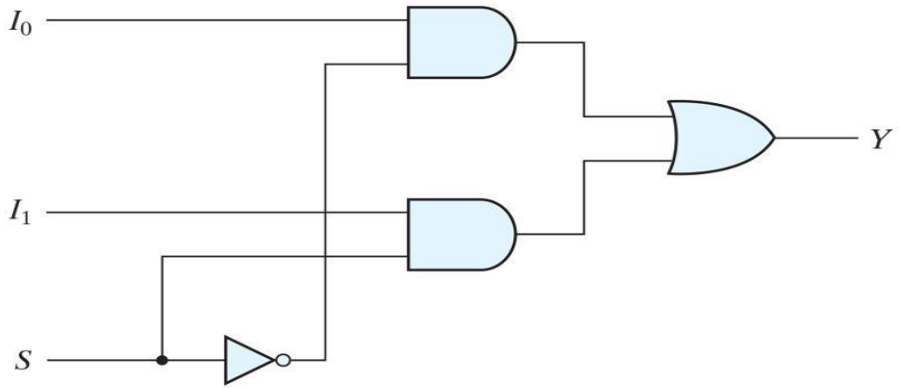
Multiplexers

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs it to a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selection lines whose bit combinations determine which input is selected.

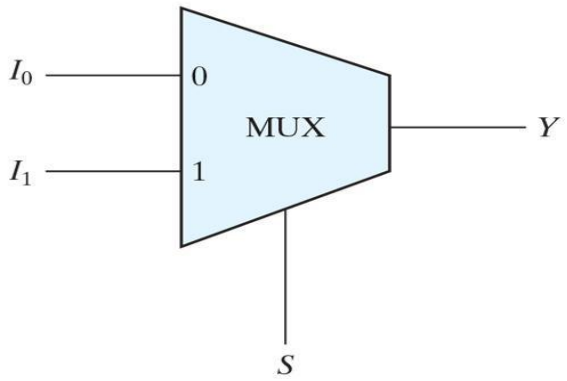
M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 4.11

Combinational logic
Multiplexers

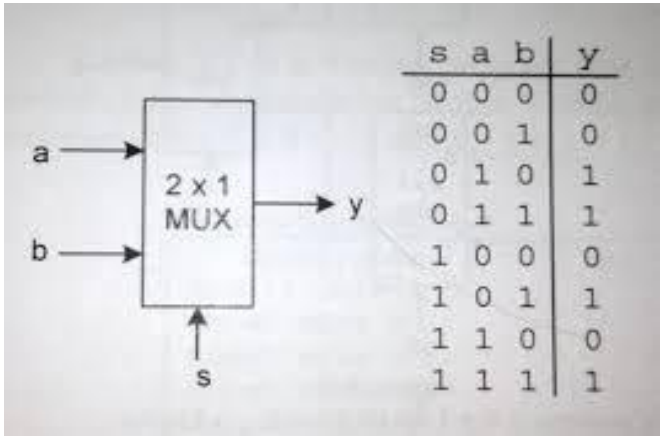
Two to One Line Multiplexer



(a) Logic diagram

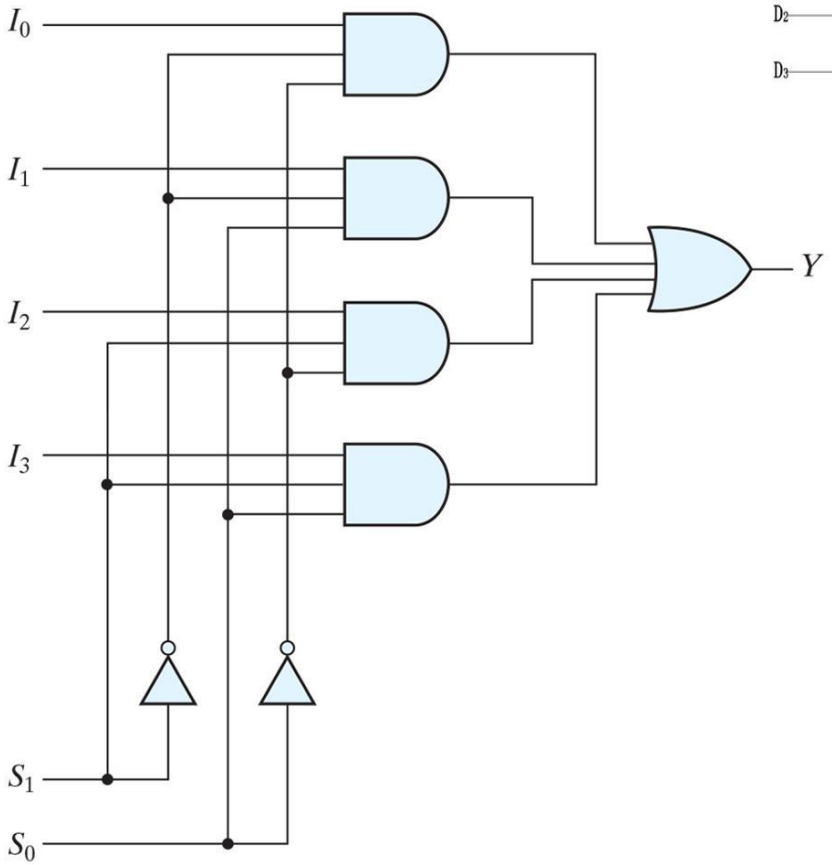


(b) Block diagram

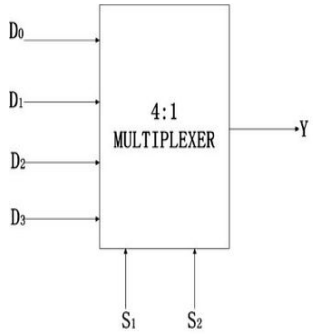


Combinational logic
Multiplexers

Four to One Line Multiplexer



(a) Logic diagram



(a)

INPUT		OUTPUT
S_2	S_1	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

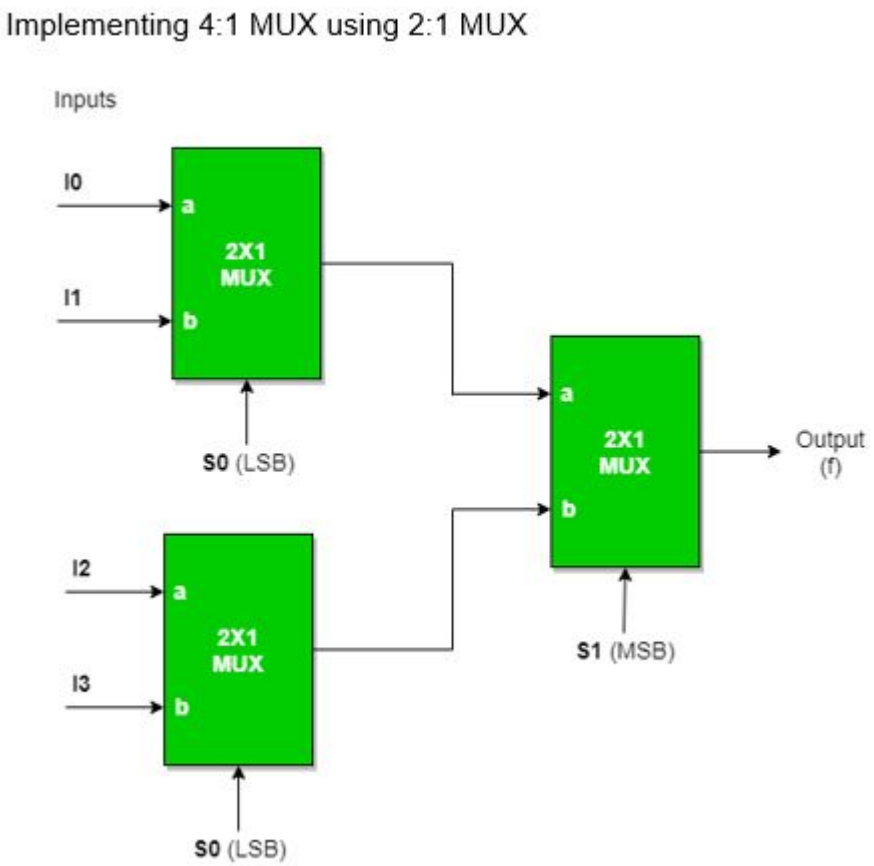
(b)

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

Combinational logic
Multiplexers

Implementing 4:1 MUX using 2:1 MUX



Truth Table

S1	S0	f
0	0	I0
0	1	I1
1	0	I2
1	1	I3

Combinational logic

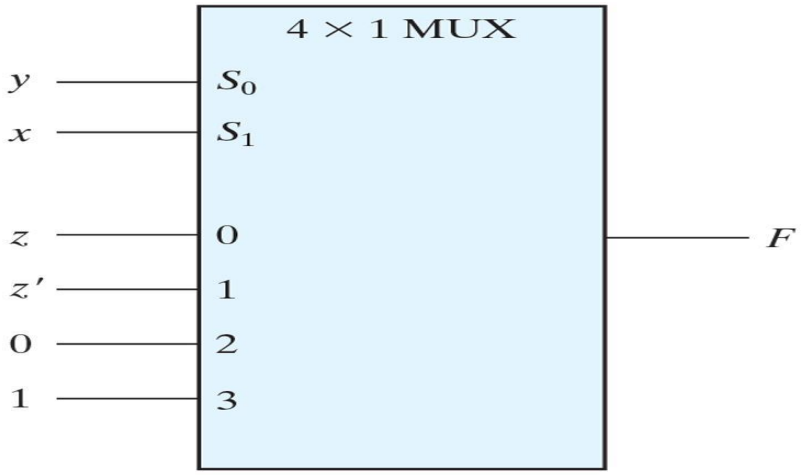
Multiplexers-Boolean Function Implementation

Implementing a Boolean Function with a Multiplexer

$F(x, y, z) = (1, 2, 6, 7)$

x	y	z	F	
0	0	0	0	$F = z$
0	0	1	1	
0	1	0	1	$F = z'$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	1	$F = 1$
1	1	1	1	

(a) Truth table



(b) Multiplexer implementation

Connect input variables to select inputs of multiplexer *(n-1 for n variables)*

Set data inputs to multiplexer equal to values of function for corresponding assignment of select variables

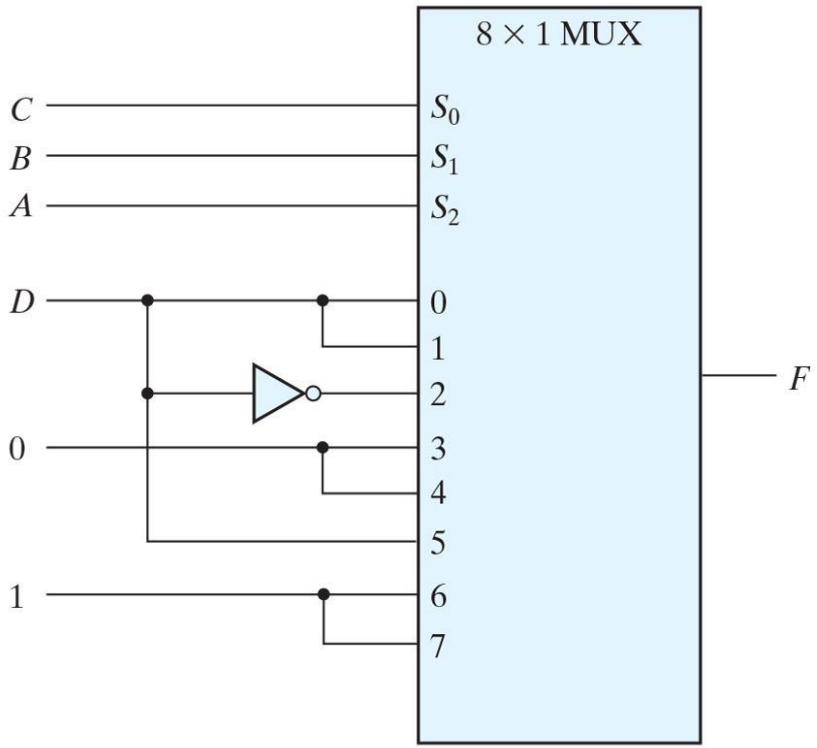
Using a variable at data inputs reduces size of the multiplexer

Combinational logic
Multiplexers

Implementing a four input Function with a 8X1 Multiplexer

$F(A, B, C, D) = (1, 3, 4, 11, 12, 13, 14, 15)$

A	B	C	D	F	
0	0	0	0	0	$F = D$
0	0	0	1	1	
0	0	1	0	0	$F = D$
0	0	1	1	1	
0	1	0	0	1	$F = D'$
0	1	0	1	0	
0	1	1	0	0	$F = 0$
0	1	1	1	0	
1	0	0	0	0	$F = 0$
1	0	0	1	0	
1	0	1	0	0	$F = D$
1	0	1	1	1	
1	1	0	0	1	$F = 1$
1	1	0	1	1	
1	1	1	0	1	$F = 1$
1	1	1	1	1	



Combinational logic

Multiplexers- Three State Gates

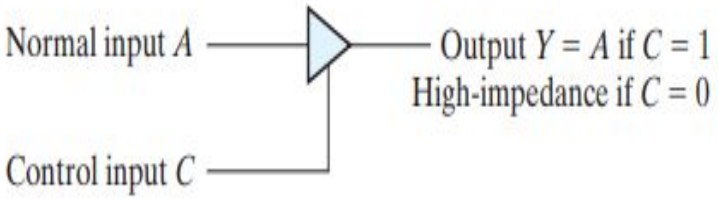
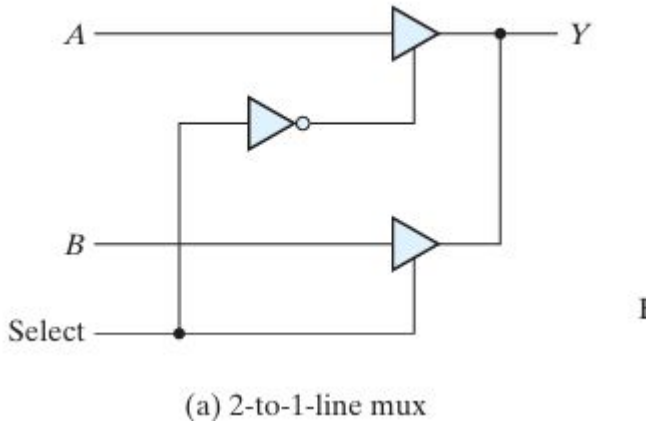


FIGURE 4.29
Graphic symbol for a three-state buffer

Two of the states are signals equivalent to logic 1 and logic 0 as in a conventional gate. The third state is a high-impedance state in which (1) the logic behaves like an **open circuit**, which means that the output appears to be disconnected, (2) the circuit has **no logic significance**, and (3) the circuit connected to the **output** of the **three-state gate is not affected by the inputs to the gate.**

Combinational logic

Multiplexers- Three State Gates



(a) 2-to-1-line mux

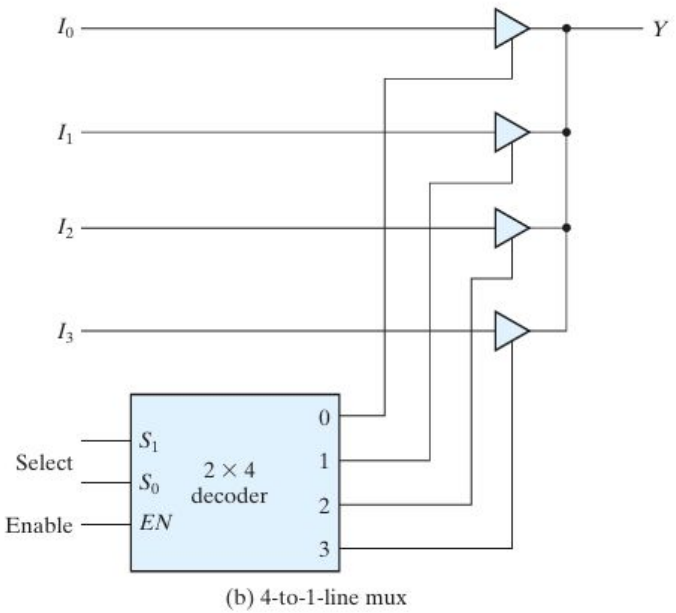
FIGURE 4.30
Multiplexers with three-state gates

When the select input is 0, the upper buffer is enabled by its control input and the lower buffer is disabled. Output Y is then equal to input A . When the select input is 1, the lower buffer is enabled and Y is equal to B

The construction of multiplexers with three-state buffers is demonstrated in Fig. 4.30 . Figure 4.30(a) shows the construction of a two-to-one-line multiplexer with 2 three-state buffers and an inverter. The two outputs are connected together to form a single output line.

Combinational logic

Multiplexers- Three State Gates



(b) 4-to-1-line mux

No more than one buffer may be in the active state at any given time.

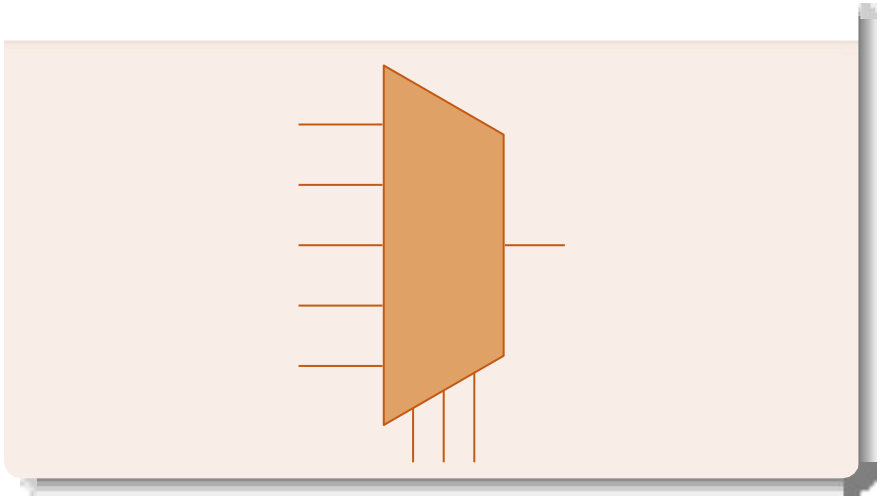
One way to ensure that no more than one control input is active at any given time is to use a decoder, as shown in the diagram

When the **enable** input of the decoder is **0**, all of its four outputs are 0 and **the bus line is in a high-impedance state because all four buffers are disabled.** When the **enable input is active, one of the three state buffers will be active, depending on the binary value in the select inputs of the decoder.**

Combinational logic

Multiplexers- Think about it

5:1 Mux



A combinational logic circuit having n data inputs, $\lceil \log_2 n \rceil$ control inputs and one output, that connects the data input indicated by the control inputs to the output

- What is the Boolean formula for a 3:1 mux? Construct a 3:1 mux using 2:1 muxes AND, OR and NOT gates

Combinational logic

Multiplexers- Think about it

Using 2 X 1 MUX design y=AB

Using 4 X 1 MUX design y=AB`+ B`C`+A`BC

Combinational logic

Multiplexers-

A 4-to-1 multiplexer is used to implement the Boolean function

$F(A,B,C)=\sum m(1,3,5,7)$

Which variables should be connected to the select lines of the MUX?

A) A and B

B) B and C

C) A and C

D) Any two variables

How many select lines are required for a **5:1 multiplexer**?

A) 2

B) 3

C) 4

D) 5

Combinational logic

Multiplexers-

A 4-to-1 multiplexer is used to implement the Boolean function
$F(A,B,C)=\sum m(1,3,5,7)$
Which variables should be connected to the select lines of the MUX?
A) A and B
B) B and C
C) A and C
D) Any two variables

Answer: D

. How many select lines are required for a **5:1 multiplexer**?
A) 2
B) 3
C) 4
D) 5
Answer: B) 3

Combinational logic

Multiplexers-

The Boolean function $F(x,y,z)=\sum m(1,2,6,7)$ is implemented using an 8:1 multiplexer. What should be the values of data inputs D_0 to D_7?

A) D = {1,1,1,0,0,0,1,1}

B) D = {0,1,0,1,0,1,0,1}

C) D = {1,0,0,1,1,1,0,0}

D) D = {0,1,1,0,0,0,1,1}

Combinational logic

Multiplexers-

The Boolean function $F(x,y,z)=\sum m(1,2,6,7)$ is implemented using an 8:1 multiplexer. What should be the values of data inputs D_0 to D_7?

A) D = {1,1,1,0,0,0,1,1}
B) D = {0,1,0,1,0,1,0,1}
C) D = {1,0,0,1,1,1,0,0}
D) D = {0,1,1,0,0,0,1,1}

Answer: D) D = {0,1,1,0,0,0,1,1}

Explanation:

The minterms correspond to the positions where F = 1.

So, $D_1 = D_2 = D_6 = D_7 = 1$, rest are 0.

THANK YOU

Team DDCO

Department of Computer Science