DIGITAL DESIGN AND COMPUTER ORGANIZATION

Ripple counters

Team DDCO

Department of Computer Science and Engineering

Ripple Counters(T1- section 6.3)

In digital logic and computing, a counter is a device which stores (and sometimes displays) the **number of times a particular event or process** has occurred, often in relationship to a clock

A register that goes through a **prescribed sequence of states upon the application of input pulses is called a counter.** The input pulses may be clock pulses, or they may originate from some external source and may occur at a fixed interval of time or at random.

The sequence of states may follow the binary number sequence or any other sequence of states. A counter that follows the binary number sequence is called a **binary counter** . **An n -bit binary counter consists of n flip-flops and can count in binary from 0 through 2^n - 1.**
EX: 3 bit counter- consists of 3 flipflops, counts from 0-7 (000-111)

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 6.3.

Ripple Counters

Counters are available in two categories: **ripple counters and synchronous counters.**

In a ripple counter, a flip-flop output transition serves as a source for triggering other flip-flops. In other words, the C input of some or all flip-flops are triggered, not by the common clock pulses, but rather by the transition that occurs in other flip-flop outputs.

In a synchronous counter, the C inputs of all flip-flops receive the common clock

Counters (Ripple, synchronous)- **upcounter, down counter, updown counter**

Ripple Counters

Asynchronous / Ripple Counter	Synchronous Counter
Output of one flip-flop drives the clock of the next flip-flop.	No connection between output of one flip-flop and clock of next flip-flop.
Flip-flops are not clocked simultaneously.	Flip-flops are clocked simultaneously.
Circuit is simple even for more number of states.	Circuit becomes complicated as number of states increases.
Speed is slow since clock is propagated through multiple stages.	Speed is high as clock is given to all flip-flops at the same time.

Binary Ripple Counters

Binary Ripple Counter:

A binary ripple counter consists of a series connection of complementing flip-flops, with the output of each flip-flop connected to the C input of the next higher order flip-flop.

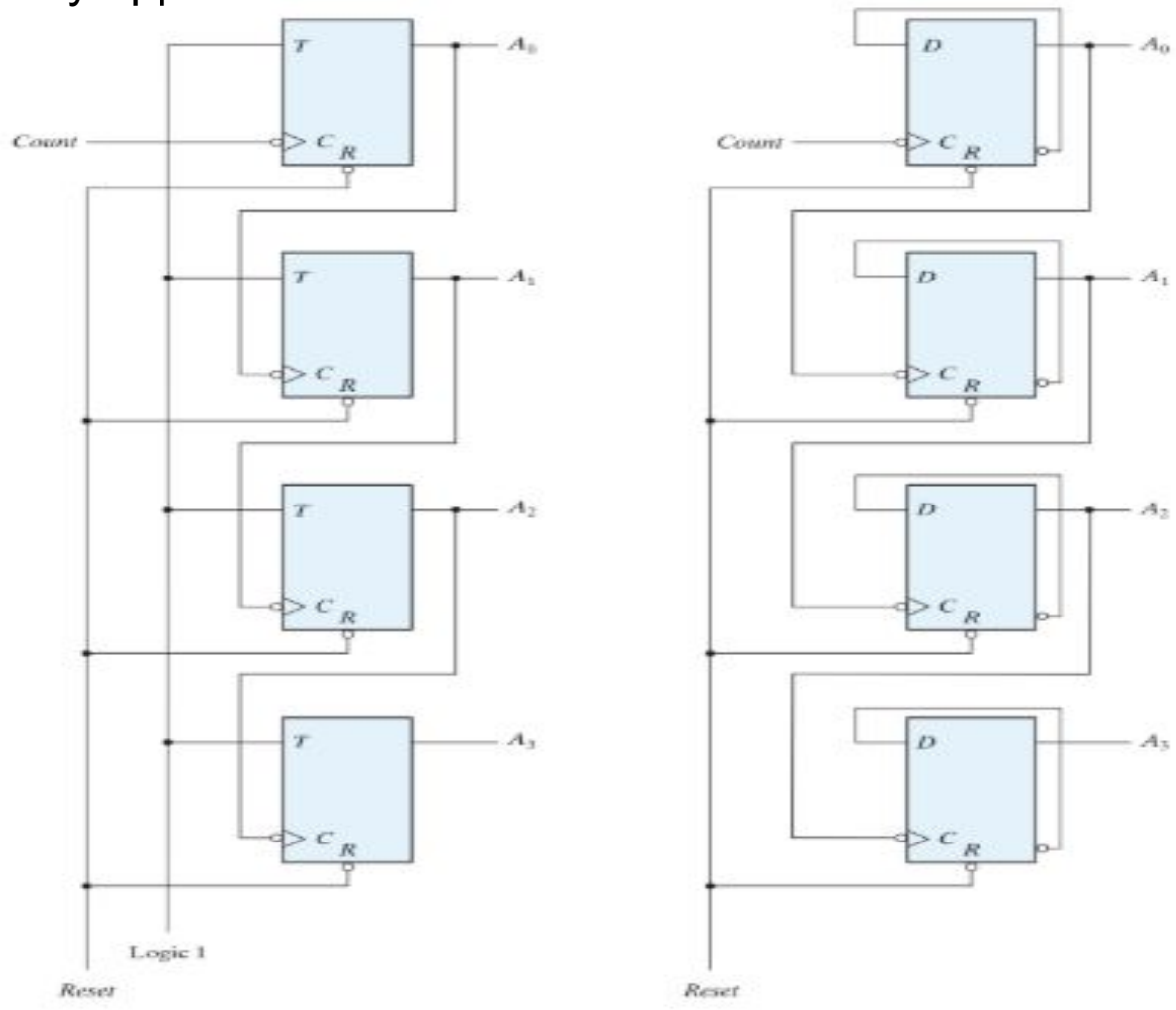
Can be obtained by:
JK connected to same input and converting it into toggle (T flipflop)
D flipflop- D input is always the complement of the present state, and the next clock pulse will cause the flip-flop to complement.

The bubble in front of the dynamic indicator symbol next to C indicates that the flip-flops respond to the negative-edge transition of the input. (transition from 1 to 0)

Binary Ripple Counters-

Figure 6.8

Four-bit binary ripple counter.



(a) With T flip-flops (b) With D flip-flops

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 6.3.

Binary Ripple Counters

Binary Ripple counter:
The flip-flop holding the least significant bit receives the incoming count pulses.

The T inputs of all the flip-flops in

(a) are connected to a permanent logic 1, making each flip- flop complement if the signal in its C input goes through a negative transition. The bubble in front of the dynamic indicator symbol next to C indicates that the flip-flops respond to the negative-edge transition of the input. The negative transition occurs when the output of the previous flip-flop to which C is connected goes from 1 to 0.

Binary Ripple Counters

Binary Ripple Counter:

Table 6.4
Binary Count Sequence

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 6.3.

Binary Ripple Counters

Four-bit Binary Ripple Counter.

Binary Ripple counter : four-bit binary ripple counter

4 flipflop
2^4=16 states
0-15 sequence(0000-1111)

The count starts with binary 0 and increments by 1 with each count pulse input. After the count of 15, the counter goes back to 0 to repeat the count

Working-
The least significant bit, A0, is complemented with each count pulse input.
Every time that A0 goes from 1 to 0, it complements A1
Every time that A1 goes from 1 to 0, it complements A2.
Every time that A2 goes from 1 to 0, it complements A3

Binary Ripple Counters

- A binary counter with a reverse count is called a **binary countdown counter** . In a countdown counter, the binary count is decremented by 1 with every input count pulse.

- The count of a four-bit countdown counter starts from binary 15 and continues to binary counts 14, 13, 12, . . . , 0 and then back to 15

- A list of the count sequence of a binary countdown counter shows that the least significant bit is complemented with every count pulse. Any other bit in the sequence is complemented if its previous least significant bit goes from **0 to 1.**

- **all flip-flops trigger on the positive edge of the clock**
- If negative-edge-triggered flip-flops are used, then the C input of each flip-flop must be connected to the complemented output of the previous flip-flop. Then, when the true output goes from 0 to 1, the complement will go from 1 to 0 and complement the next flip-flop as required.

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 6.3.

BCD Ripple Counters

A decimal counter follows a sequence of 10 states and returns to 0 after the count of 9.

Such a counter must have at least four flip-flops to represent each decimal digit, since a decimal digit is represented by a binary code with at least four bits

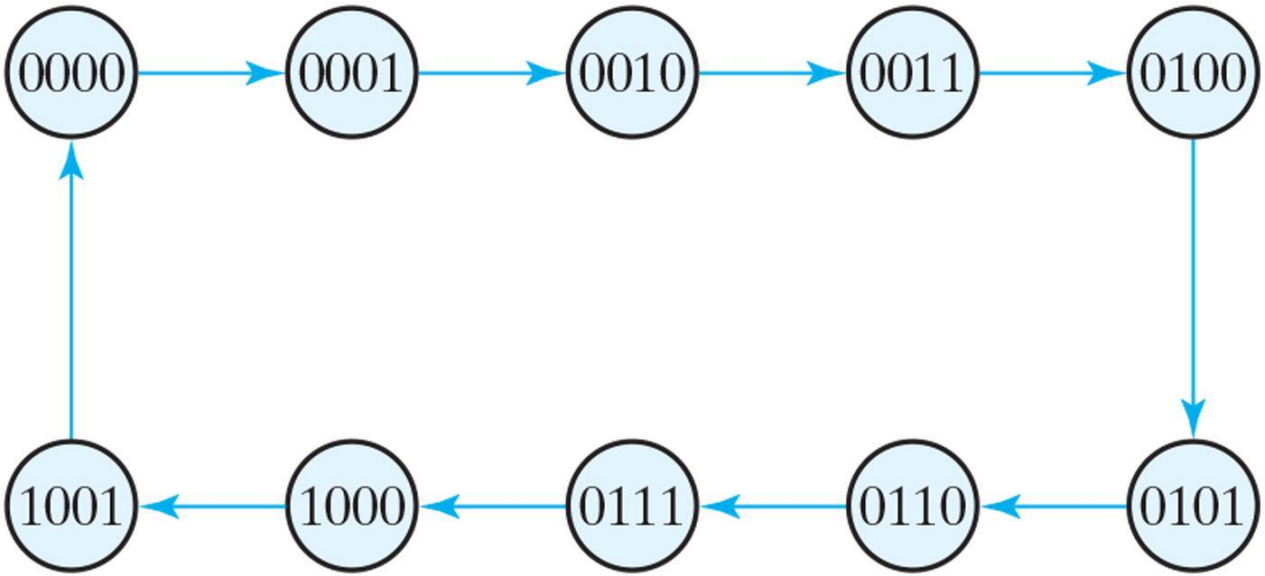
Also called Mod 10 counter.

$2^n=10$

N=4

BCD Ripple Counters

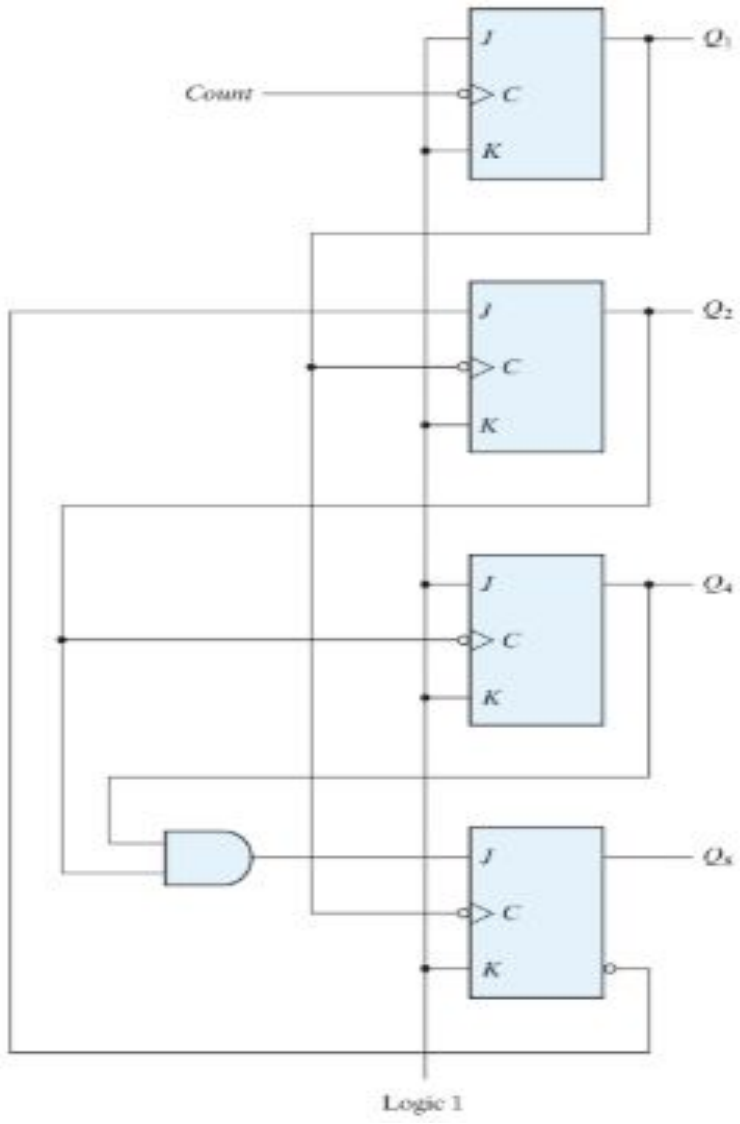
Figure 6.9
State diagram of a decimal BCD counter.



M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 6.3.

BCD Ripple Counters

Figure 6.10
BCD ripple counter.



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BCD Ripple Counters

- A ripple counter is an asynchronous sequential circuit. Signals that affect the flip-flop transition depend on the way they change from 1 to 0
- when the C input goes from 1 to 0, the flip-flop is set if J = 1, is cleared if K = 1, is complemented if J = K = 1, and is left unchanged if J = K = 0.

- Q1 changes state after each clock pulse. Q2 complements every time Q1 goes from 1 to 0, as long as Q8 = 0. When Q8 becomes 1, Q2 remains at 0. Q4 complements every time Q2 goes from 1 to 0. Q8 remains at 0 as long as Q2 or Q4 is 0. When both Q2 and Q4 become 1, Q8 complements when Q1 goes from 1 to 0. Q8 is cleared on the next transition of Q1.

BCD Ripple Counters

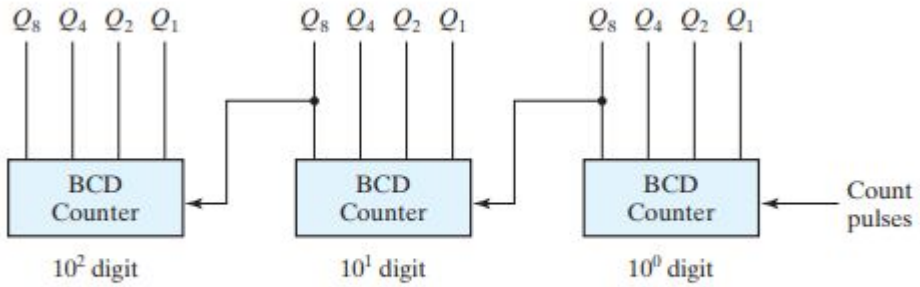

FIGURE 6.11
Block diagram of a three-decade decimal BCD counter

The BCD counter of Fig. 6.10 is a decade counter, since it counts from 0 to 9. To count in decimal from 0 to 99, we need a two-decade counter. To count from 0 to 999, we need a three-decade counter. Multiple decade counters can be constructed by connecting BCD counters in cascade, one for each decade. A three-decade counter is shown in Fig. 6.11 . The inputs to the second and third decades come from Q8 of the previous decade. When Q8 in one decade goes from 1 to 0, it triggers the count for the next higher order decade while its own decade goes from 9 to 0.

Applications

In automated industries like **bottling plants, packaging units, and textile mills**, machines need to **count repetitive events** — e.g., bottles filled, packets sealed, or cloth rolls measured. A **counter** circuit is ideal because it can automatically keep track of such pulses and trigger control actions.

Ripple Counter Stage : The sensor pulses are fed into a binary ripple counter.
Example: a 4-bit ripple counter can count from 0000 (0) to 1111 (15).
Each flip-flop toggles on the falling edge of the previous flip-flop's output → "ripple effect."

Count Expansion (Cascading)
If we need to count higher numbers (e.g., 1000 bottles), multiple counters are cascaded (seconds → minutes analogy in clocks).
For example, 3 cascaded BCD ripple counters give **000–999** counts.

Step-by-Step Ripple Counter Operation
Bottle 1 passes → Counter = 0001
Bottle 2 passes → Counter = 0010…

Bottle 15 passes → Counter = 1111 (overflow → resets back to 0)

Cascading ensures higher count capacity (e.g., up to 9999).

MCQ

In a 4-bit down ripple counter, the initial state is 1111. After 5 clock pulses, the state will be:
A) 1010
B) 1011
C) 1101
D) 1001

The modulus of a BCD counter is:
A) 8
B) 10
C) 12
D) 16

MCQ

In a 4-bit down ripple counter, the initial state is 1111. After 5 clock pulses, the state will be:
A) 1010
B) 1011
C) 1101
D) 1001

Answer: B) 1011
Explanation: Sequence goes 1111 (15) → 1110 (14) → 1101 (13) → 1100 (12) → 1011 (11).

The modulus of a BCD counter is:
A) 8
B) 10
C) 12
D) 16

Answer: B) 10
Explanation: BCD counter counts 10 states (0–9). After 1001, it resets to 0000.

MCQ

If a BCD counter is implemented with 4 flip-flops, how many states are unused?
A) 2
B) 4
C) 6
D) 10

In a 2-digit decimal counter, how many flip-flops are required?
A) 4
B) 6
C) 7
D) 8

MCQ

If a BCD counter is implemented with 4 flip-flops, how many states are unused?
A) 2
B) 4
C) 6
D) 10

Answer: C) 6
Explanation: 4 flip-flops = 16 possible states (0000–1111). Only 10 (0000–1001) are used. Remaining 6 (1010–1111) are **unused**.

In a 2-digit decimal counter, how many flip-flops are required?
A) 4
B) 6
C) 7
D) 8

Answer: D) 8
Explanation: One BCD counter needs 4 flip-flops. For 2-digit (00–99), need 2 counters → total 8 flip-flops.

THANK YOU

Team DDCO

Department of Computer Science and Engineering