DIGITAL DESIGN AND COMPUTER ORGANIZATION

Decoders

Team DDCO

Department of Computer Science and Engineering

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Decoders

Department of Computer Science and Engineering

Combinational logic

Decoders

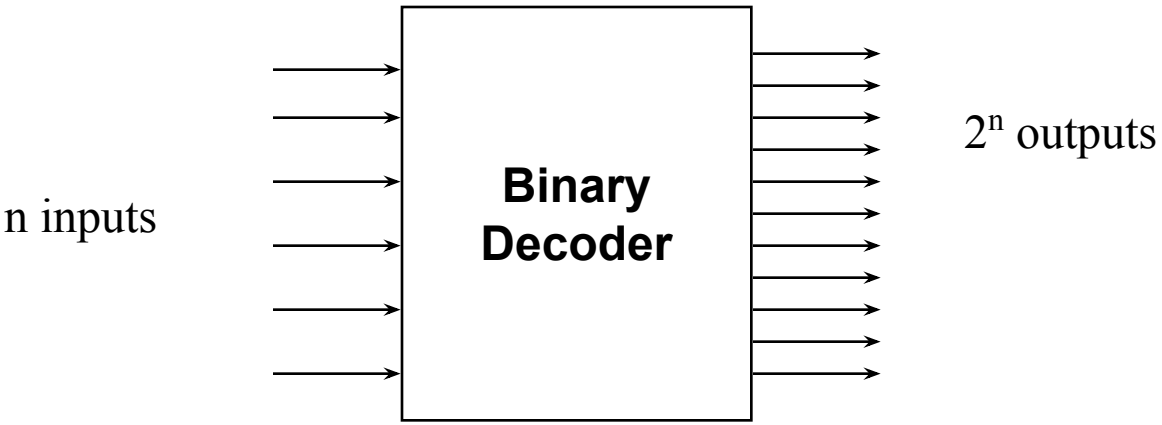
- Discrete quantities of information are represented in digital systems by binary codes.
- A binary code of n bits is capable of representing up to 2^n distinct elements of coded information
- A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. If the n -bit coded information has unused combinations, the decoder may have fewer than 2^n outputs.
- The decoders presented here are called n -to- m -line decoders, where m … 2^n
- The name decoder is also used in conjunction with other code converters, such as a BCD-to-seven-segment decoder.

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 4.9

Combinational logic
Decoders

Decoders

Black box with n input lines and 2^n output lines



Only one output is a 1 for any given input

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 4.9

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Decoders

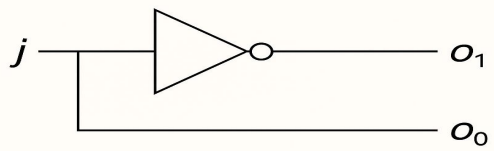
1: 2 Decoder:

A **1-to-2 decoder** is a simple combinational logic circuit that takes **1 input** and produces **2 outputs**. It is used to activate exactly **one of the two outputs** based on the binary value of the input.

Truth table :

Input (J)	Output(O_1)	Output(O_0)
0	1	0
1	0	1

1:2 decoder logic circuit:



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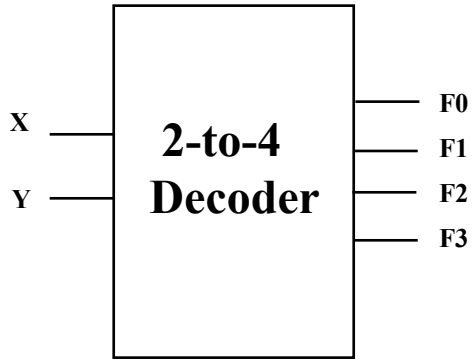
Combinational logic
Decoders

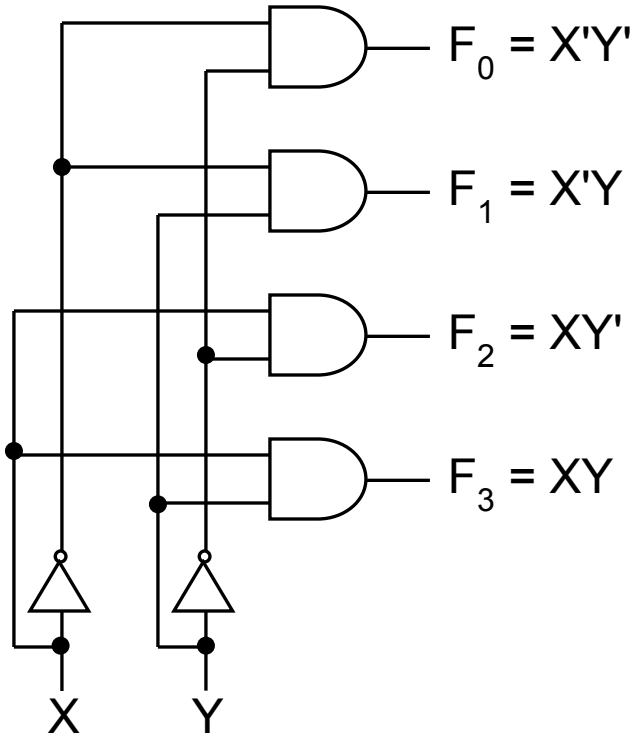


From truth table, circuit for 2x4 decoder is:

Note: Each output is a 2-variable minterm (X'Y', X'Y, XY' or XY)

Truth Table:

X	Y	F_0	F_1	F_2	F_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



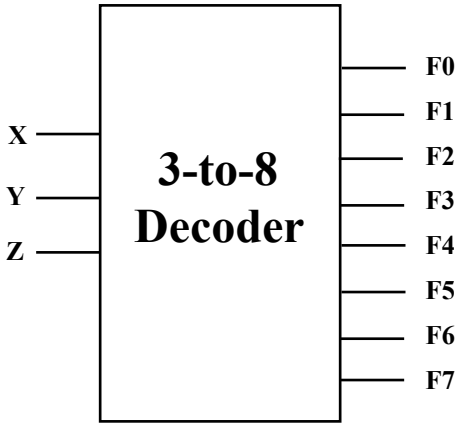
Combinational logic

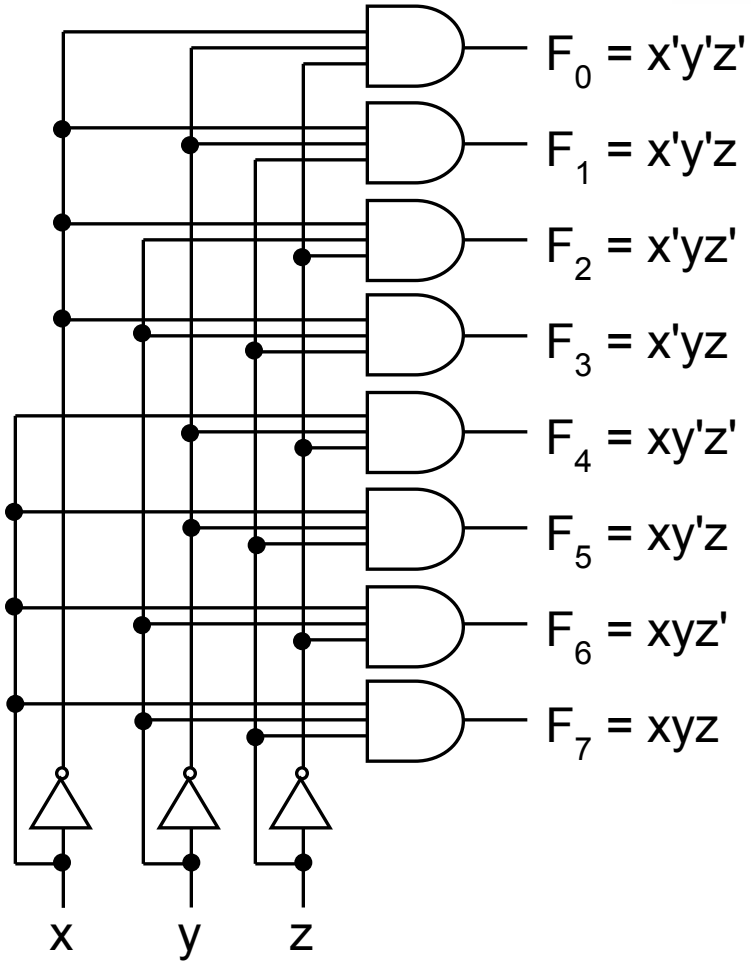
Decoders (similar to code converter – binary to octal)

3-to-8 Binary Decoder

Truth Table:

x	y	z	F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1





Combinational logic

Decoders with enable input

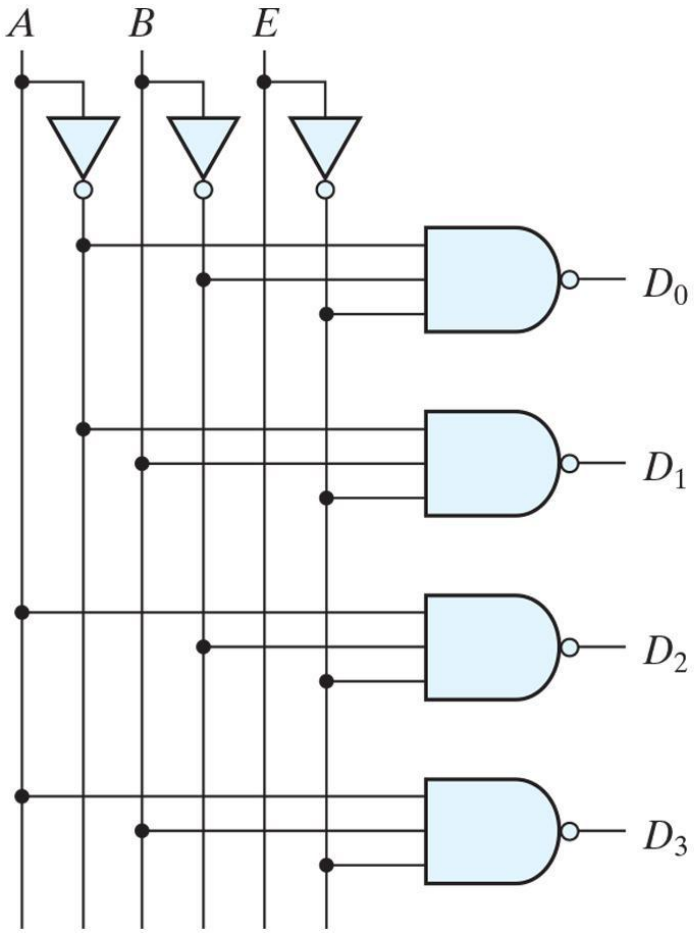
Enable input- allows the decoders outputs to be turned “ON” or “OFF” as required. Output is only generated when the Enable input has value 1; otherwise, all outputs are 0.

Some decoders are constructed with NAND gates. Since a NAND gate produces the AND operation with an inverted output, it becomes more economical to generate the decoder minterms in their complemented form

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 4.9

Combinational logic
Decoders with NAND gates

Two to four line Decoder with Enable Input



Start with a 2-bit decoder
Add an enable signal (E)

Note: use of NANDs
only one 0 active! **(active low)**
if E = 0

AB=10 then output is D2

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Combinational logic

Decoders with enable input

A decoder with enable input can function as a demultiplexer— a circuit that receives information from a single line and directs it to one of 2^n possible output lines. The selection of a specific output is controlled by the bit combination of n selection lines.

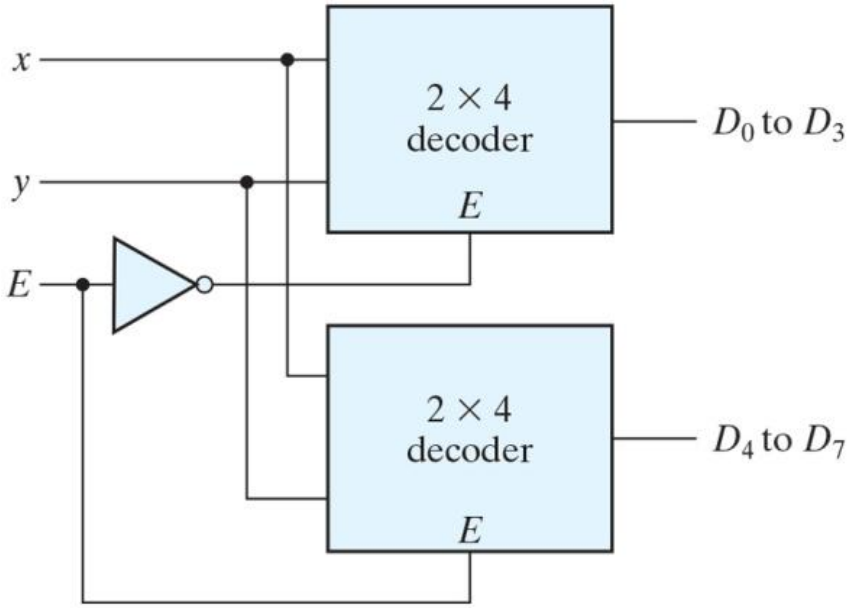
Because decoder and demultiplexer operations are obtained from the same circuit, a decoder with an enable input is referred to as a decoder – demultiplexer

Decoders with enable inputs can be connected together to form a larger decoder

M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 4.9

Combinational logic
Decoders

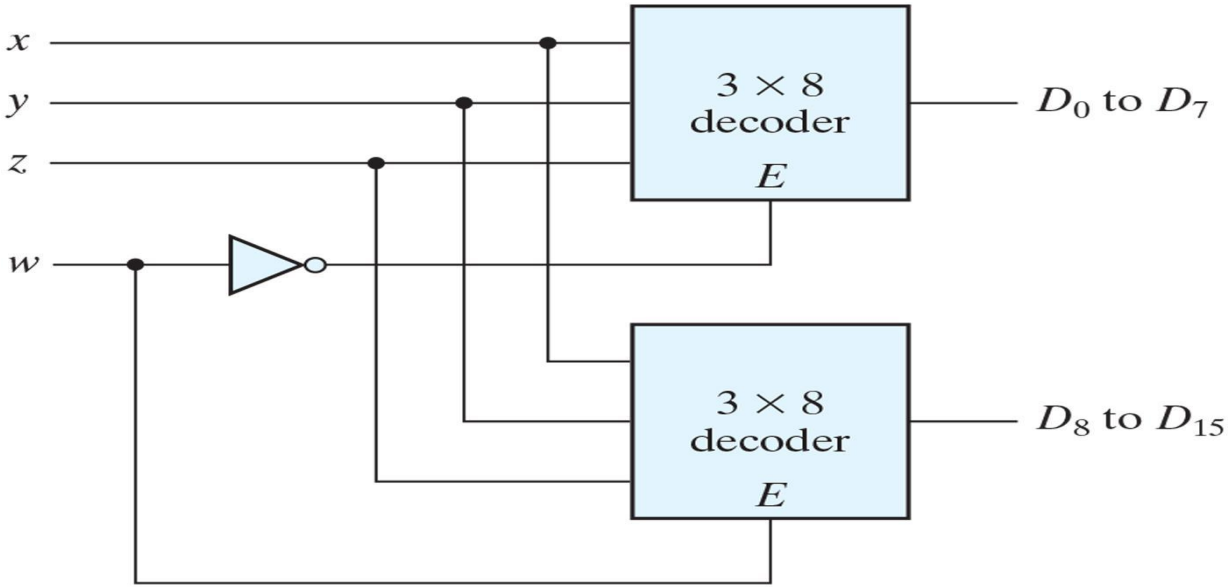
3 x 8 decoder constructed with two 2 x 4 decoders.



E	x	y	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Combinational logic
Decoders

4 x 16 decoder constructed with two 3 x 8 decoders.



Enable can also be active high
In this example, only one decoder can be active at a time.
x, y, z effectively select output line for w

Combinational logic
Decoders

Implementing Functions Using Decoders

Any n-variable logic function can be implemented using a single n-to-2^n decoder to generate the minterms

- **OR gate forms the sum.**
- **The output lines of the decoder corresponding to the minterms of the function are used as inputs to the or gate.**

Any combinational circuit with *n* inputs and *m* outputs can be implemented with an n-to-2^n decoder with *m* OR gates.

Suitable when a circuit has many outputs, and each output function is expressed with few minterms.

Combinational logic

Decoders-Combinational Logic implementation

A decoder provides the 2^n minterms of n input variables
Each asserted output of the decoder is associated with a unique pattern of input bits.

Since any Boolean function can be expressed in sum-of-minterms form, a decoder that generates the minterms of the function, together with an external OR gate that forms their logical sum, provides a hardware implementation of the function.

In this way, any combinational circuit with n inputs and m outputs can be implemented with an n -to-2^n -line decoder and m OR gates.

Questions:
1.Build XNOR Gate with 2 inputs using Decoders.
2.Implement full adder using decoders

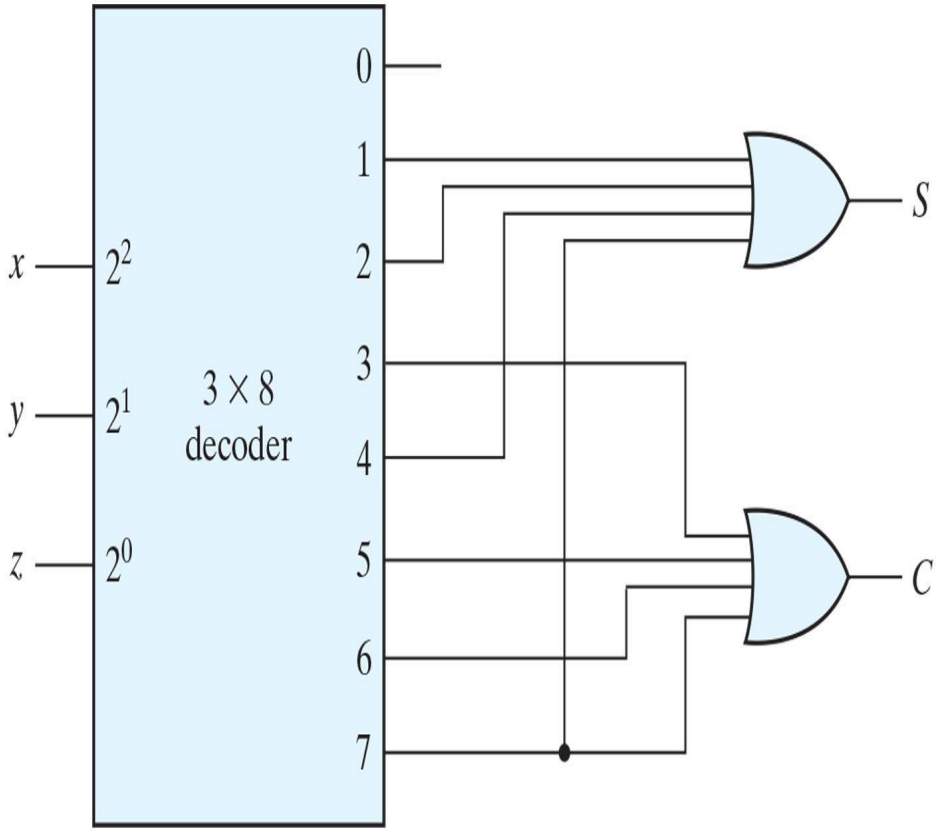
Combinational logic

Decoders-Combinational Logic implementation

A decoder provides the 2^n minterms of n input variables

Implementation of a full adder with a decoder.

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Full adder

$S(x, y, z) = \sum (1,2,4,7)$

$C(x, y, z) = \sum (3,5,6,7)$

Combinational logic

Decoders

A function with a long list of minterms requires an OR gate with a large number of inputs.

A function having a list of k minterms can be expressed in its complemented form F` with 2^n- k minterms.

If the number of minterms in the function is greater than $2^n/2$, then F` can be expressed with fewer minterms.

(Example: For 3 variables (n=3), total = 8 minterms.

If F = 6 minterms, better to write

F=(Σ6$minterms$)=(Σ o$fall$8–6)=$complementof$2$minterms$

F=(Σ6minterms)=(Σofall8–6)=complementof2minterms.

In such a case, it is advantageous to use a NOR gate to sum the minterms of F.

Combinational logic

Decoders-Application

To manage traffic at a **4-way intersection** (North, South, East, West) **efficiently using fewer control lines**, by using a **2-to-4 line decoder**.

Why Use a Decoder?

In a 4-way intersection:

You need to **control each direction's traffic light individually**.

Without a decoder, you'd need **4 separate control signals**, one for each direction.

A **2-to-4 decoder** allows you to **use only 2 input lines** to control 4 outputs, reducing hardware complexity

Combinational logic
Decoders-Application

Understanding the 2-to-4 Decoder
Inputs: 2 bits (say A and B)

Outputs: 4 lines: Y0, Y1, Y2, Y3

Operation:When inputs = 00, output Y0 is active (others inactive)
When inputs = 01, output Y1 is active
When inputs = 10, output Y2 is active
When inputs = 11, output Y3 is active

Decoder Output	Controls Traffic Light at
Y0	**North** direction
Y1	**South** direction
Y2	**East** direction
Y3	**West** direction

Combinational logic

Decoders-Think about it

1. Build XNOR gate using Decoder
2. A function with more than $2^n/2$ minterms is better implemented using:

(A) A single AND gate
(B) Complemented function and a NOR gate
(C) Only XOR gates
(D) Full adders

3. In a 2-to-4 decoder with an active-low enable input, what happens when the enable input is 1?

(A) All outputs are enabled
(B) Decoder functions normally
(C) All outputs are 0
(D) All outputs are 1

Combinational logic
Decoders-Think about it

1. Build XNOR gate using Decoder

2.A function with more than $2^n/2$ minterms is better implemented using:
(A) A single AND gate
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(C) Only XOR gates
(D) Full adders
Answer: (B)

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Answer: (D)

THANK YOU

Team DDCO

Department of Computer Science