DIGITAL DESIGN AND COMPUTER ORGANIZATION

Encoders

Team DDCO
Department of Computer Science and Engineering

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Combinational logic
Encoders

Encoders

An encoder is a digital circuit that performs the inverse operation of a decoder. An encoder has 2^n (or fewer) input lines and n output lines. The output lines, as an aggregate, generate the binary code corresponding to the input value.

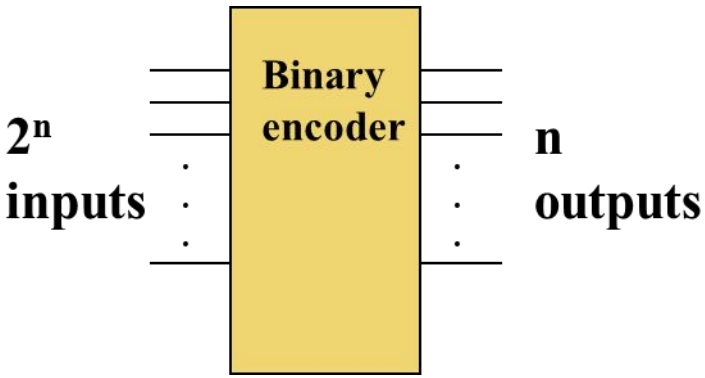
If the a decoder's output code has fewer bits than the input code, the device is usually called an encoder.

e.g. 2^n-to-n

The simplest encoder is a 2^n-to-n binary encoder

One of 2^n inputs = 1

Output is an n-bit binary number



M. Morris Mano, Michael D. Ciletti, *Digital Design: With an Introduction to the Verilog HDL*, 5th ed., Prentice Hall, 2012, Section 4.10

Combinational logic
Encoders

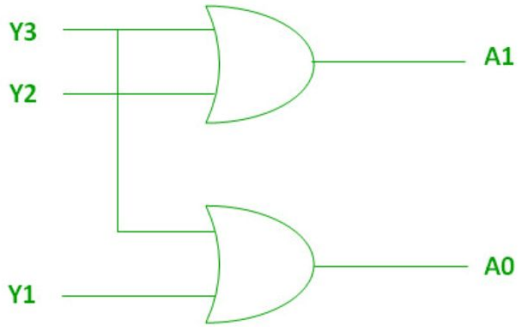
4:2 Encoder

$$A1 = Y3 + Y2$$

$$A0 = Y3 + Y1$$

The Truth table of 4 to 2 encoders is as follows.

INPUTS				OUTPUTS	
Y3	Y2	Y1	Y0	A1	A0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



Implementation using OR Gate

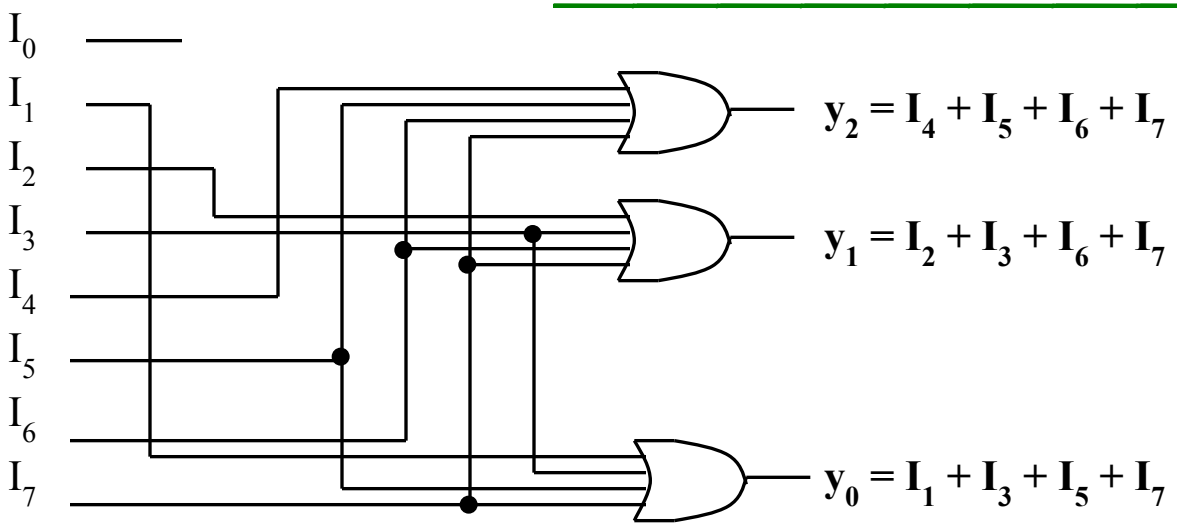
Combinational logic

Encoders (octal to binary)

8-to-3 Binary Encoder

At any one time, only one input line has a value of 1.

Inputs								Outputs		
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	y_2	y_1	y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1



Combinational logic
Encoders (octal to binary)

Truth Table for Octal-to-Binary Encoder

Truth Table of an Octal-to-Binary Encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$z = D_1 + D_3 + D_5 + D_7$$
$$y = D_2 + D_3 + D_6 + D_7$$
$$x = D_4 + D_5 + D_6 + D_7$$

Combinational logic

Priority Encoder

A priority encoder is an encoder circuit that includes the priority function. The operation of the priority encoder is such that if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

Combinational logic
Priority Encoder

Truth Table of a Priority Encoder

Inputs				Outputs		
D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

Combinational logic

Priority Encoder

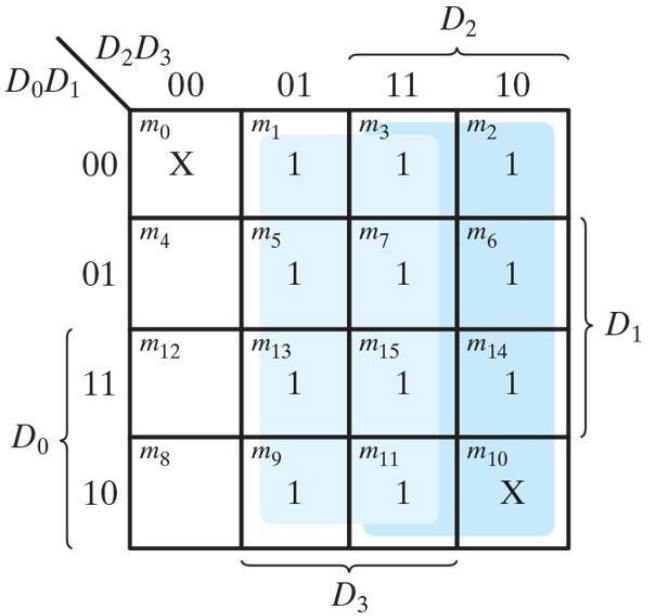
In addition to the two outputs x and y , the circuit has a third output designated by V ; this is a valid bit indicator that is set to 1 when one or more inputs are equal to 1. If all inputs are 0, there is no valid input and V is equal to 0. The other two outputs are not inspected when V equals 0 and are specified as don't-care conditions.

higher the subscript number, the higher the priority of the input. Input D3 has the highest priority, so, regardless of the values of the other inputs, when this input is 1, the output for xy is 11 (binary 3). D2 has the next priority level. The output is 10 if D2=1, provided that D3=0, regardless of the values of the other two lower priority inputs. The output for D1 is generated only if higher priority inputs are 0, and so on down the priority levels.

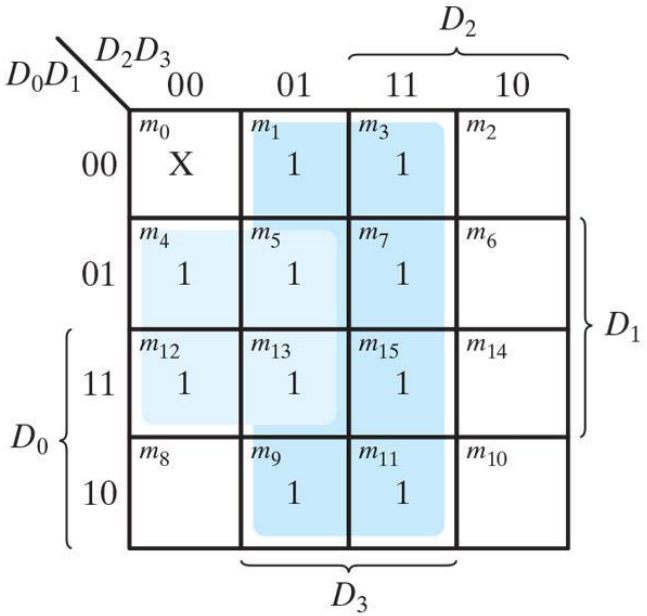
Combinational logic
Priority Encoders

Maps for a Priority Encoder

$$x = D_2 + D_3$$
$$y = D_3 + D_1 D_2'$$
$$V = D_0 + D_1 + D_2 + D_3$$



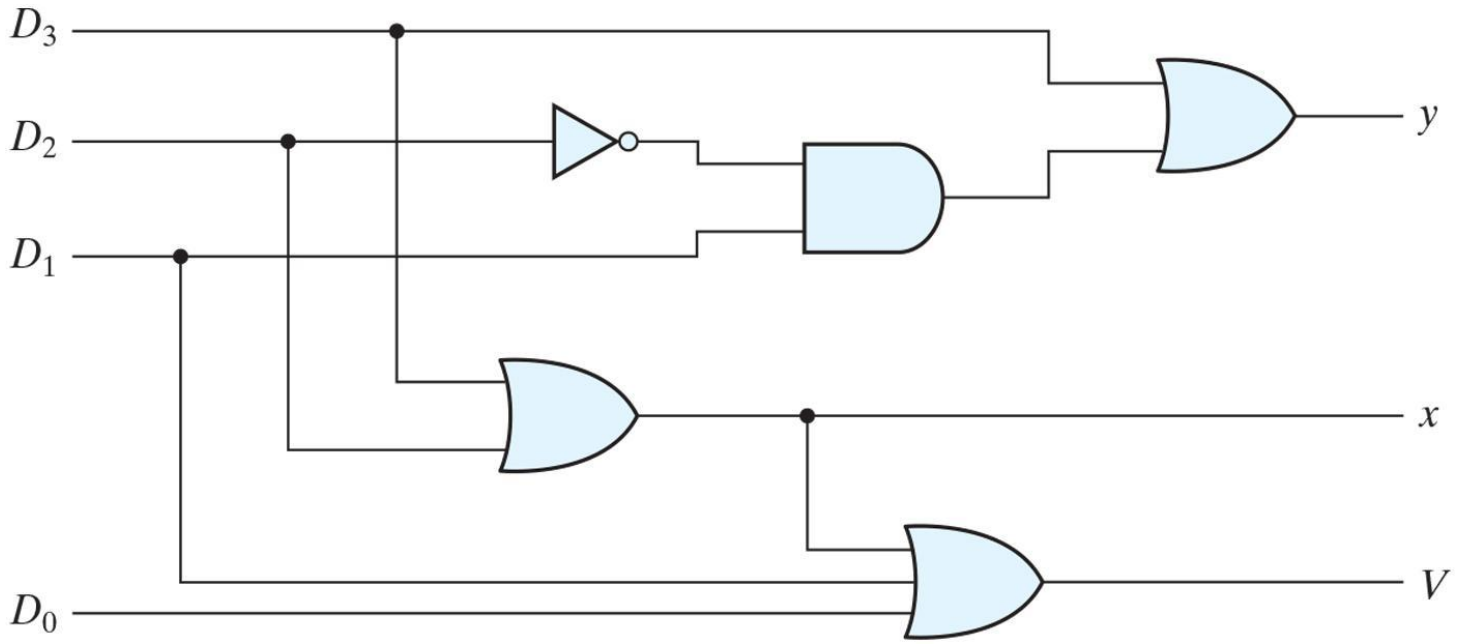
$x = D_2 + D_3$



$y = D_3 + D_1 D'_2$

Combinational logic
Priority Encoders

Four input Priority Encoder



Combinational logic
Priority Encoders

•8-to-3 Priority Encoder

- What if more than one input line has a value of 1?
- Ignore "lower priority" inputs.
- Idle indicates that no input is a 1.
- Note that polarity of Idle is opposite from Table 4-8 in Mano

Inputs								Outputs			
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	y_2	y_1	y_0	
0	0	0	0	0	0	0	0	x	x	x	Idle
1	0	0	0	0	0	0	0	0	0	0	0
X	1	0	0	0	0	0	0	0	0	1	0
X	X	1	0	0	0	0	0	0	1	0	0
X	X	X	1	0	0	0	0	0	1	1	0
X	X	X	X	1	0	0	0	1	0	0	0
X	X	X	X	X	1	0	0	1	0	1	0
X	X	X	X	X	X	1	0	1	1	0	0
X	X	X	X	X	X	X	1	1	1	1	0

Combinational logic

Encoders

Priority Encoder (8 to 3 encoder)

Assign priorities to the inputs

When more than one input are asserted, the output generates the code of the input with the highest priority

Priority Encoder :

H7=I7 (Highest Priority)

H6=I6.I7'

H5=I5.I6'.I7'

H4=I4.I5'.I6'.I7'

H3=I3.I4'.I5'.I6'.I7'

H2=I2.I3'.I4'.I5'.I6'.I7'

H1=I1. I2'.I3'.I4'.I5'.I6'.I7'

H0=I0.I1'. I2'.I3'.I4'.I5'.I6'.I7'

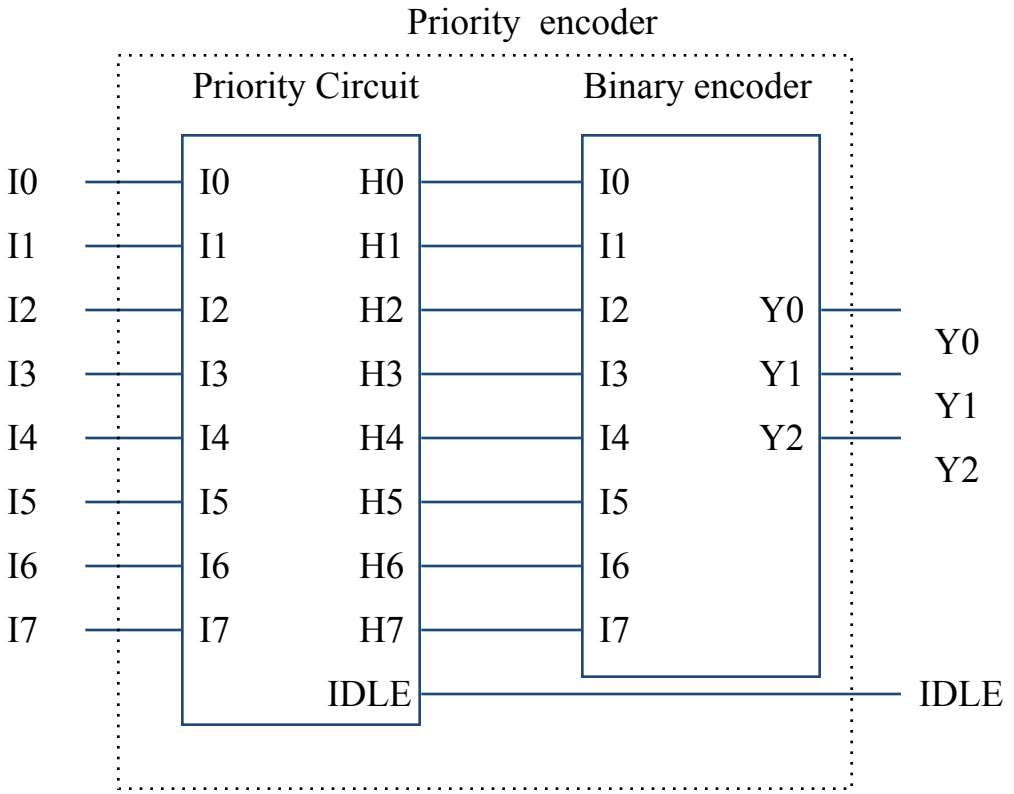
IDLE= I0'.I1'. I2'.I3'.I4'.I5'.I6'.I7'

Encoder

Y0 = I1 + I3 + I5 + I7

Y1 = I2 + I3 + I6 + I7

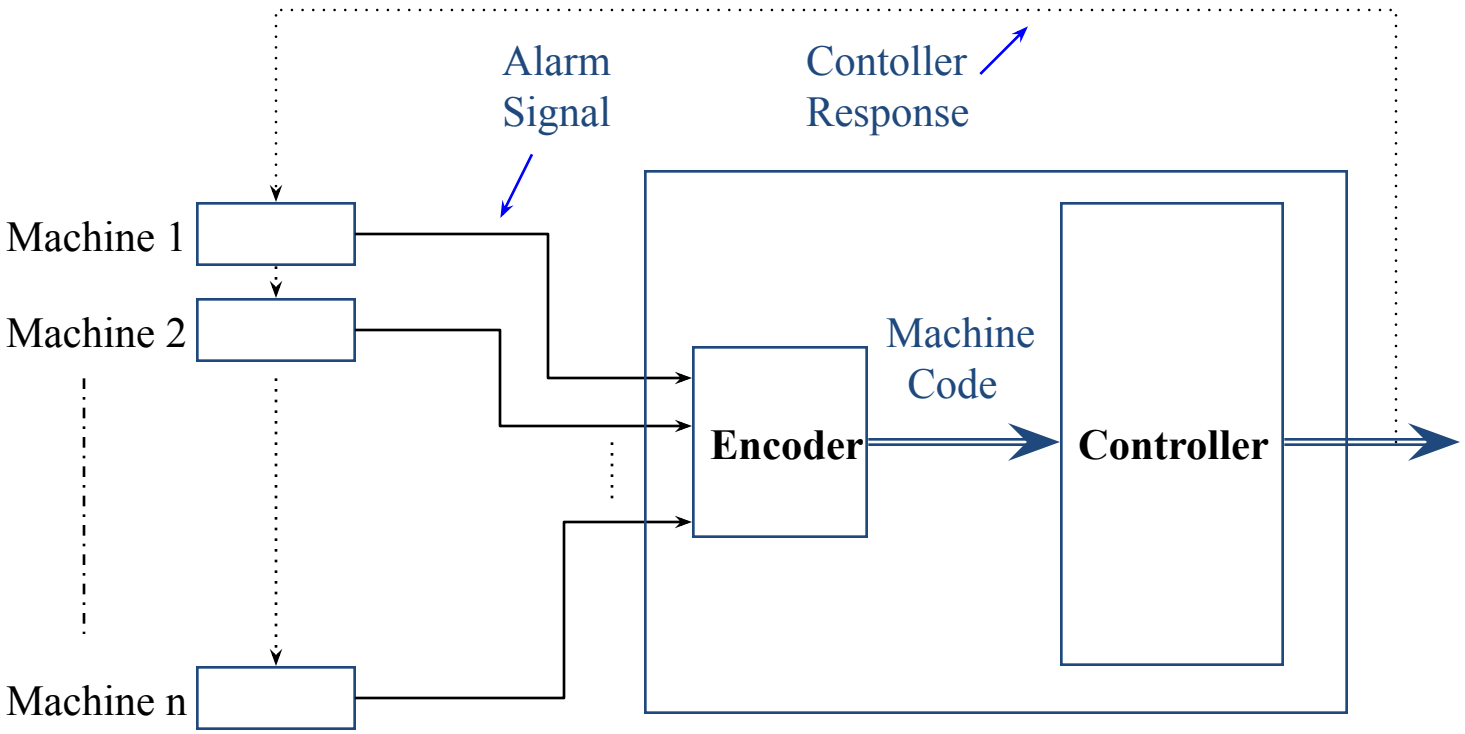
Y2 = I4 + I5 + I6 + I7



Combinational logic
Encoders

Encoder Application (Monitoring Unit)

Encoder identifies the requester and encodes the value
Controller accepts digital inputs.



Combinational logic
Encoders

Machines (Machine 1, Machine 2, ... Machine n):

- These are the different machines connected to the encoder. Each machine sends data or a request to the encoder.

Encoder:

- **The encoder's primary role is to identify which machine is sending the request** and then encode the value or information from that machine into a machine code.
- It also generates an alarm signal when needed, possibly indicating an issue or a specific condition that requires attention.

controller:

- The controller receives the encoded machine code from the encoder.
- Based on the received machine code, the **controller performs specific actions or responses, such as sending signals back to the machines.**

Alarm Signal:

- **The alarm signal seems to be an alert generated by the encoder if a certain condition is met**. This could indicate a **malfunction**, a process completion, or any other situation that needs immediate attention.

Controller Response:

- After processing the machine code, **the controller might send a response back to the machine or trigger other actions as needed.**

Combinational logic
Encoders

Applications:

Encoders- Application: In digital systems like computers, a keyboard encoder converts the pressing of keys into binary codes that the computer's processor can understand and act upon.

Priority encoders are commonly used in interrupt systems in microprocessors, where multiple interrupt signals may be received at the same time, and the processor needs to know which one to service first based on priority.

Decoders- In memory systems, a decoder takes the binary address provided by the CPU and activates the corresponding memory cell, allowing data to be read from or written to that specific location. For example, a 3-to-8 decoder can select one of eight memory locations based on a 3-bit address input.

Combinational logic

Encoders- think about it

Which of the following best describes the functionality of a **priority encoder**?

A. It encodes the input having the lowest subscript among all active inputs.

B. It encodes only the first input line, irrespective of other inputs.

C. It encodes the input having the highest subscript (priority) among active inputs.

D. It generates output only when a single input is active.

In a **4-to-2 priority encoder**, the output is “11” when:

A. Only D0 is 1

B. D1 and D2 are 1

C. D3 is 1

D. D3 is 0 and others are 1

Combinational logic

Encoders- think about it

Which of the following best describes the functionality of a **priority encoder**?

A. It encodes the input having the lowest subscript among all active inputs.

B. It encodes only the first input line, irrespective of other inputs.

C. It encodes the input having the highest subscript (priority) among active inputs.

D. It generates output only when a single input is active.

Answer: C

Explanation: In a priority encoder, if multiple inputs are active, the one with the **highest priority (usually highest subscript)** is considered.

In a **4-to-2 priority encoder**, the output is "11" when:

A. Only D0 is 1

B. D1 and D2 are 1

C. D3 is 1

D. D3 is 0 and others are 1

Answer: C

Explanation: D3 has highest priority.

THANK YOU

Team DDCO

Department of Computer Science