Digital Design and Computer Organisation Laboratory

3rd Semester, Academic Year 2025

Date:07-08-2025

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Week Number: 1

TITLE: Basic Logic Gates.

1. OR gate:

Verilog Code:

```
module or_test;
        reg a, b;  wire y;
        or_gate meow(y,a,b);
        initial
        begin
                #0 a=0;b=0;
                #5 a=0;b=1;
                #10 a=1;b=0;
                #15 a=1;b=1;
        end

        initial
        begin
                $monitor($time, "a=%b, b=%b, y=%b", a ,b
,y);
        end

        initial
        begin
                $dumpfile ("or_test.vcd");
                $dumpvars (0, or_test);
        end

endmodule
~
~
test_bench.v                          25,0-1          All
```

```
/*or gate*/
module or_gate(y,a,b);
input a,b;
output y;
assign y= a | b;
endmodule
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design.v
```
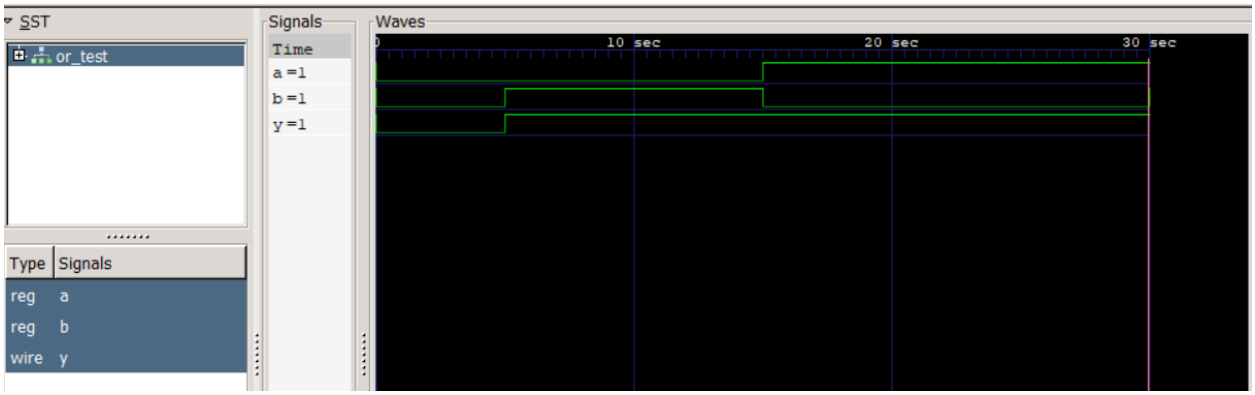

Vvp o/p:

```
PS C:\Users\anu29\DDCO_lab\week1\OR> vvp test1
VCD info: dumpfile or_test.vcd opened for output.
                    0a=0, b=0, y=0
                    5a=0, b=1, y=1
                   15a=1, b=0, y=1
                   30a=1, b=1, y=1
```

Gtkwave:



2. XOR

Verilog code

```
module xor_test;
        reg a, b;  wire y;
        xor_gate meow(y,a,b);
        initial
        begin
                #0 a=0;b=0;
                #5 a=0;b=1;
                #10 a=1;b=0;
                #15 a=1;b=1;
        end

        initial
        begin
                $monitor($time, "a=%b, b=%b, y=%b", a ,b
,y);
        end

        initial
        begin
                $dumpfile ("xor_test.vcd");
                $dumpvars (0, xor_test);
        end

endmodule


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test_bench.v                          1,1           All
```

```
/*XOR Gate*/

module xor_gate(y,a,b);
input a,b;
output y;
assign y= a ^ b;
endmodule

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design.v
```
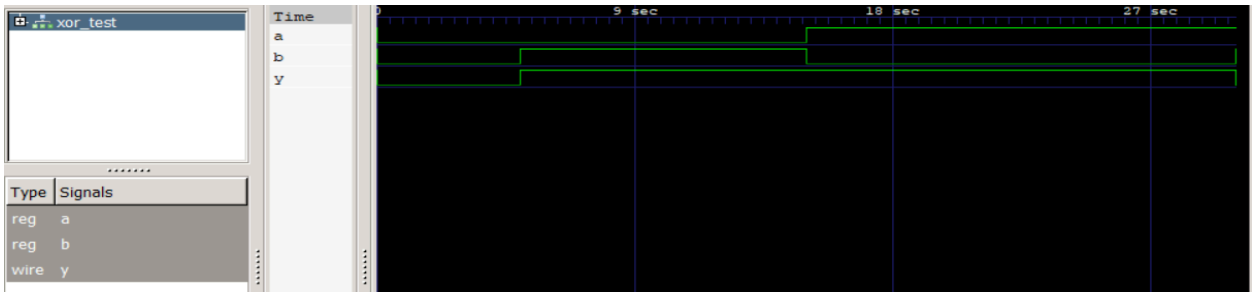

Vvp o/p

```
PS C:\Users\anu29\DDCO_lab\week1\XOR> vvp test1
VCD info: dumpfile xor_test.vcd opened for output.
                    0a=0, b=0, y=0
                    5a=0, b=1, y=1
                   15a=1, b=0, y=1
                   30a=1, b=1, y=0
```

Gtkwave:



3. NOR

Verilog code:

```
module nor_test;
        reg a, b;  wire y;
        nor_gate meow(y,a,b);
        initial
        begin
                #0 a=0;b=0;
                #5 a=0;b=1;
                #10 a=1;b=0;
                #15 a=1;b=1;
        end

        initial
        begin
                $monitor($time, "a=%b, b=%b, y=%b", a ,b
,y);
        end

        initial
        begin
                $dumpfile ("nor_test.vcd");
                $dumpvars (0, nor_test);
        end

endmodule


~
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test_bench.v                                1,1           All
```

```
/*NOR Gate */

module nor_gate(y,a,b);
input a,b;
output y;
assign y= !(a | b);
endmodule
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design.v
```
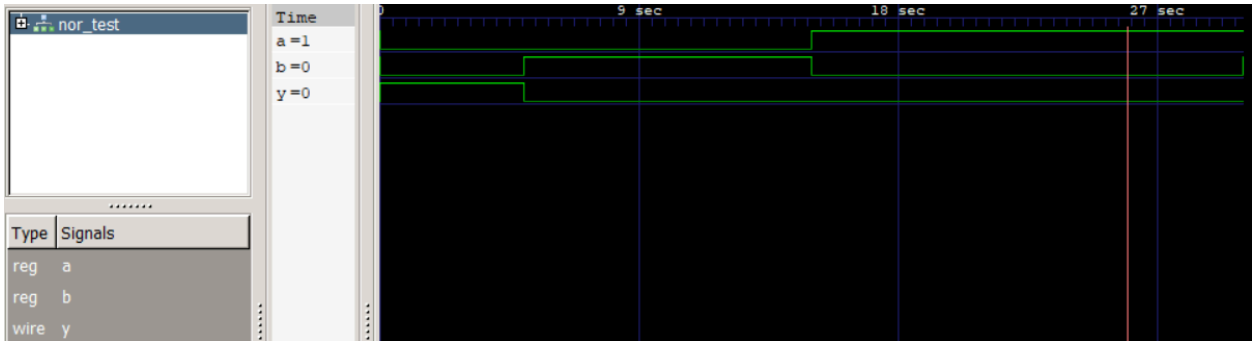

Vvp o/p:

```
PS C:\Users\anu29\DDCO_lab\week1\NOR> vvp test1
VCD info: dumpfile nor_test.vcd opened for output.
                    0a=0, b=0, y=1
                    5a=0, b=1, y=0
                   15a=1, b=0, y=0
                   30a=1, b=1, y=0
```

Gtk wave:



4. NOT

Verilog code:

```
module not_test;
        reg a;  wire y;
        not_gate meow(y,a);
        initial
        begin
                #0 a=0;
                #10 a=1;
        end

        initial
        begin
                $monitor($time, "a=%b, y=%b", a,y);
        end

        initial
        begin
                $dumpfile ("not_test.vcd");
                $dumpvars (0, not_test);
        end

endmodule
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~
test_bench.v                                1,1           All
```

```
/*Not Gate*/
module not_gate(y,a);
input a;
output y;
assign y = !a;
endmodule


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design.v
```
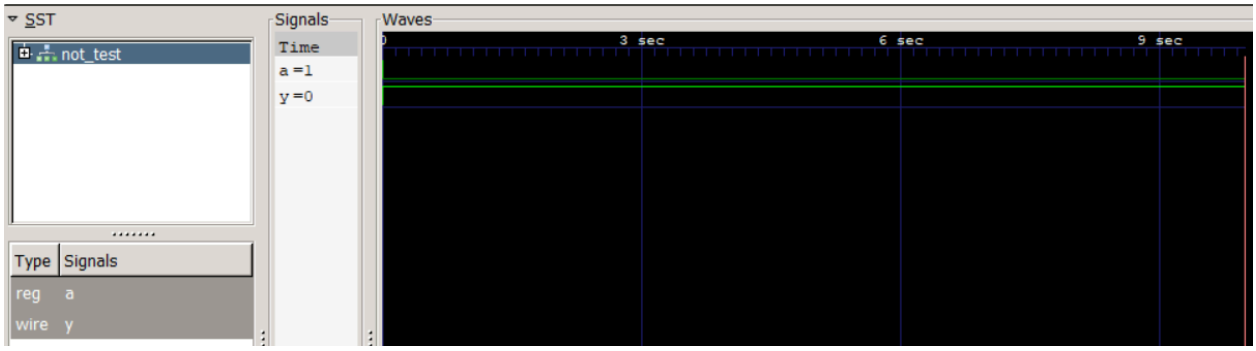

Vvp o/p:

```
PS C:\Users\anu29\DDCO_lab\week1\NOT> vvp test1
VCD info: dumpfile not_test.vcd opened for output.
                    0a=0, y=1
                   10a=1, y=0
```

Gtk wave:



5. NAND

Iverilog code:

```
module nand_test;
        reg a, b;  wire y;
        nand_gate meow(y,a,b);
        initial
        begin
                #0 a=0;b=0;
                #5 a=0;b=1;
                #10 a=1;b=0;
                #15 a=1;b=1;
        end

        initial
        begin
                $monitor($time, "a=%b, b=%b, y=%b", a ,b
,y);
        end

        initial
        begin
                $dumpfile ("nand_test.vcd");
                $dumpvars (0, nand_test);
        end

endmodule
~
test_bench.v                          1,1           All
```

```
/*NAND_gate*/
module nand_gate(y,a,b);
input a,b;
output y;
assign y= !(a & b);
endmodule
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design.v
```

Vvp o/p:

```
VCD info: dumpfile nand_test.vcd opened for output.
                   0a=0, b=0, y=1
                   5a=0, b=1, y=1
                  15a=1, b=0, y=1
                  30a=1, b=1, y=0
```

Gtkwave: