**Digital Design and Computer Organisation Laboratory**

**3rd Semester, Academic Year 2025**

Date:07-08-2025

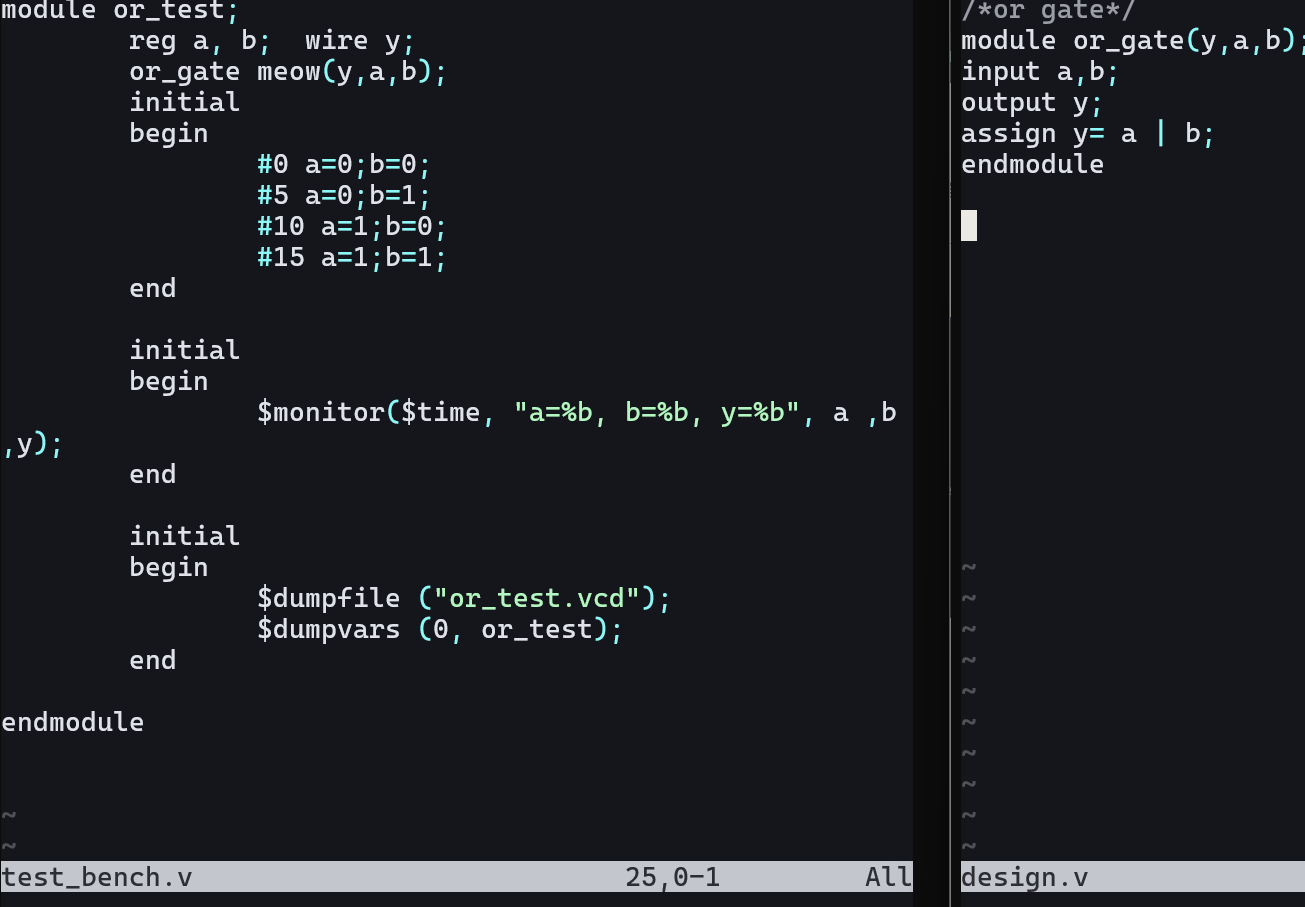
| Name: Dharani S | SRN: PES2UG24CS157 | Section  : c |
| --- | --- | --- |

Week Number: 1

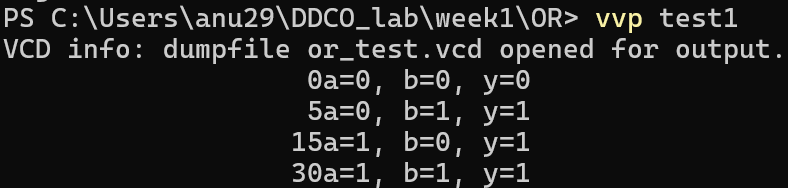
TITLE: Basic Logic Gates.

1. OR gate:

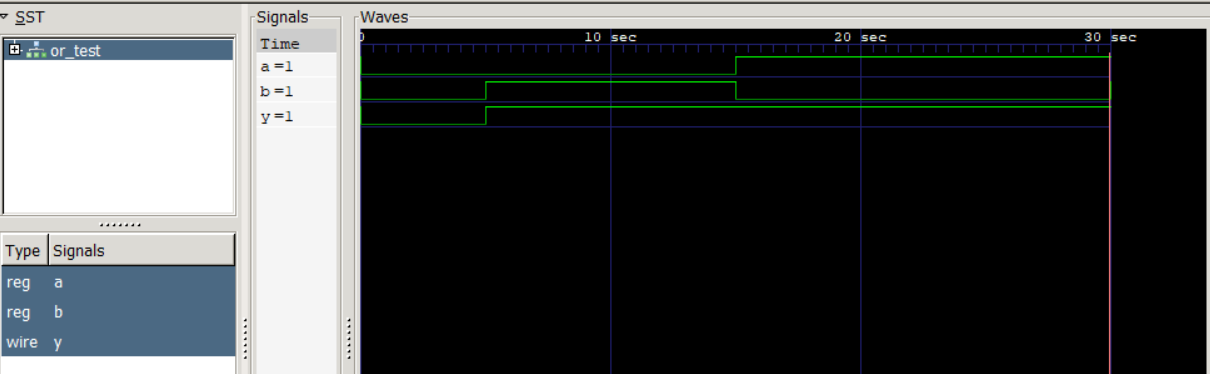
Verilog Code:



Vvp o/p:

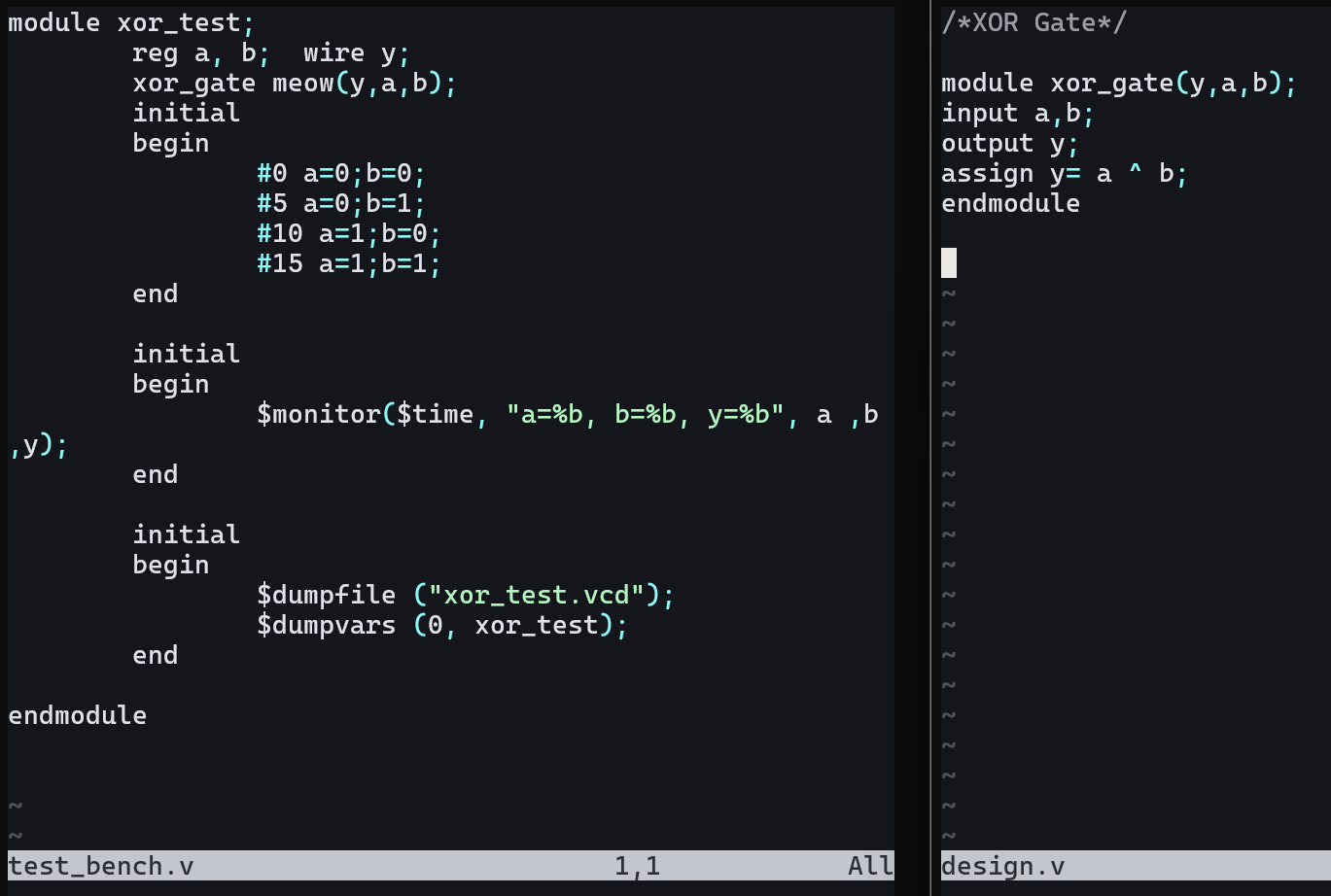


Gtkwave:

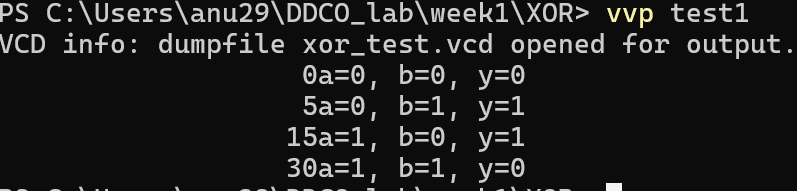


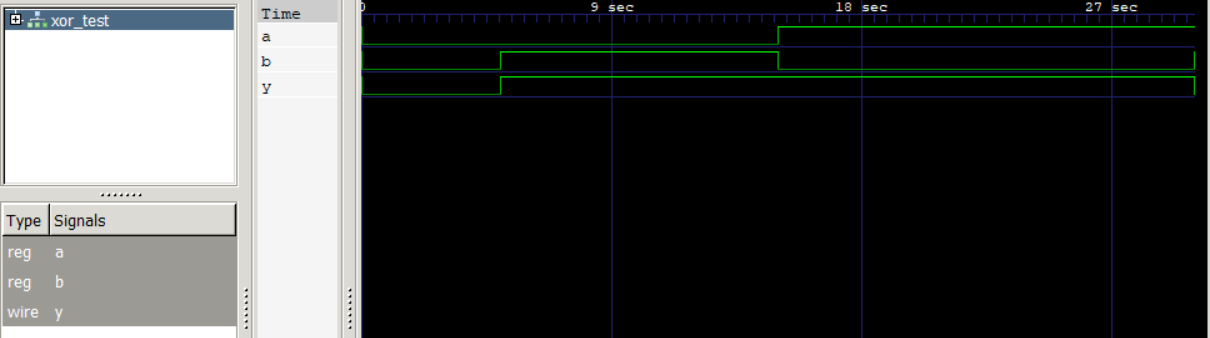
1. XOR

Verilog code



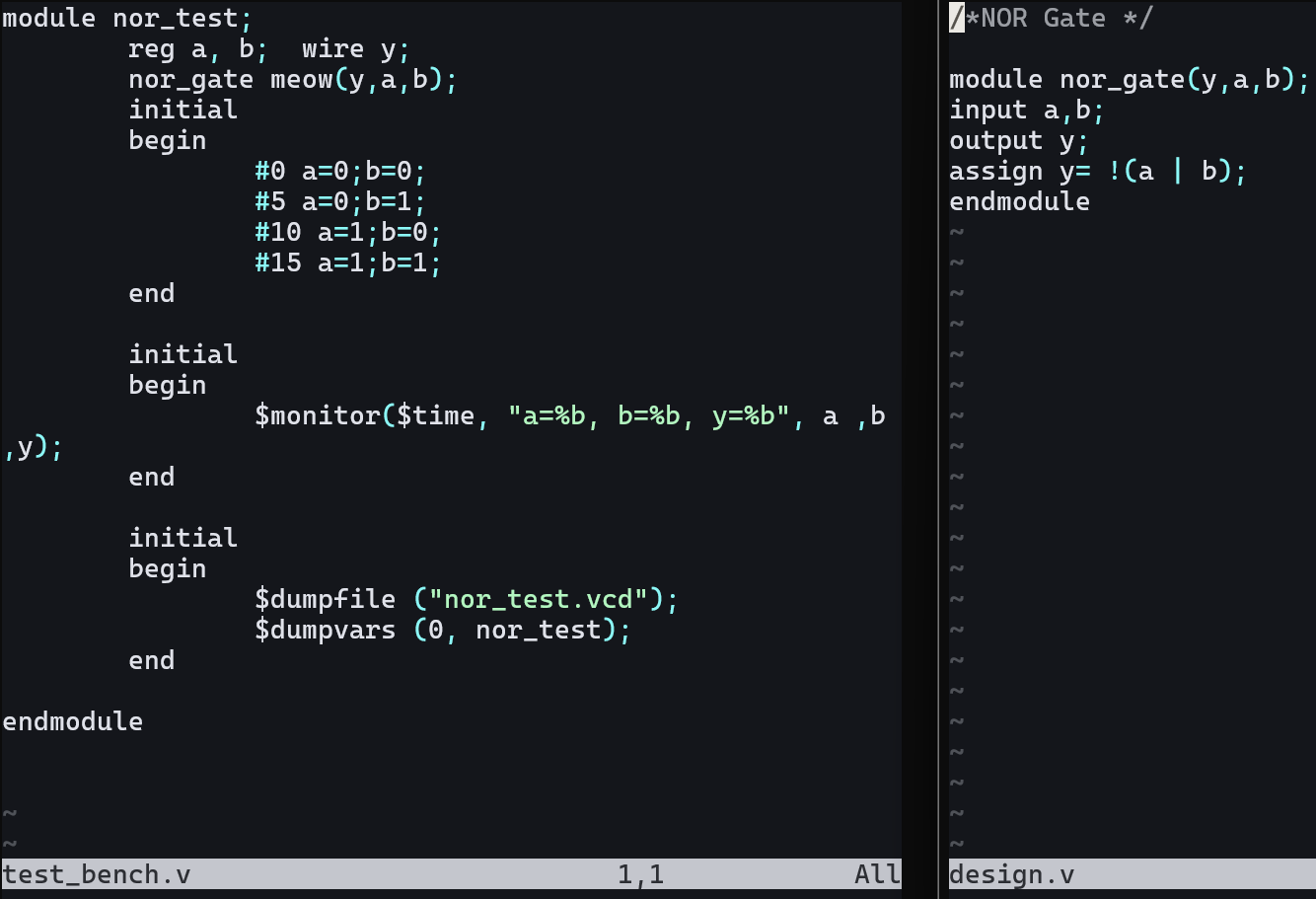
Vvp o/p



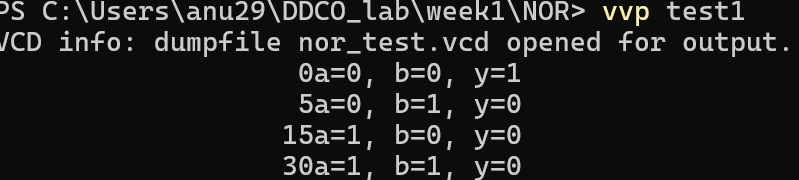
Gtkwave:

1. NOR

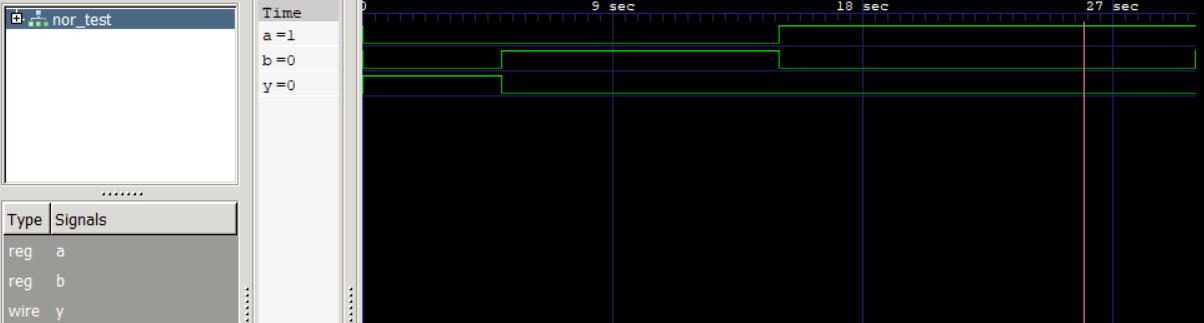
Verilog code:



Vvp o/p:

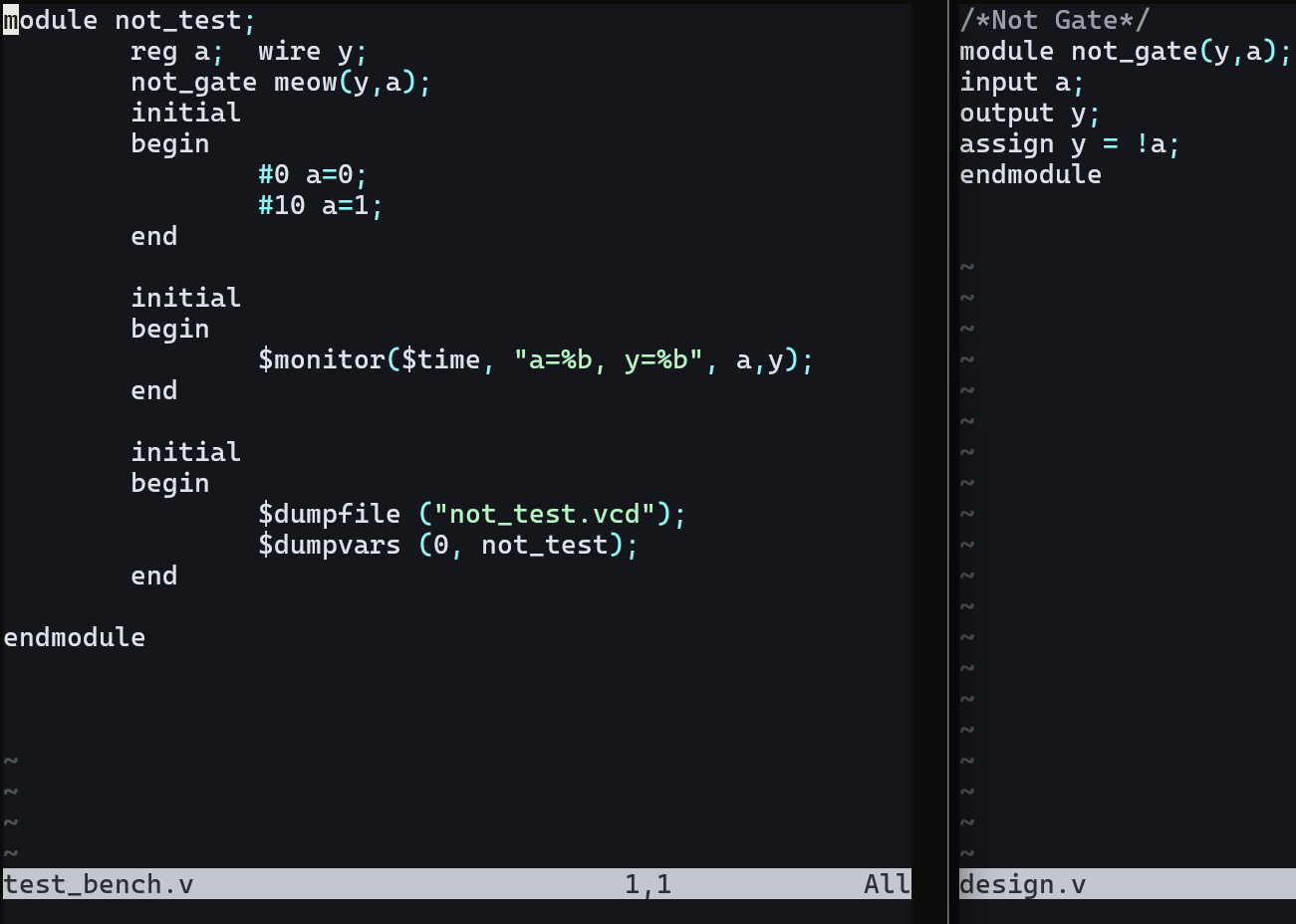


Gtk wave:

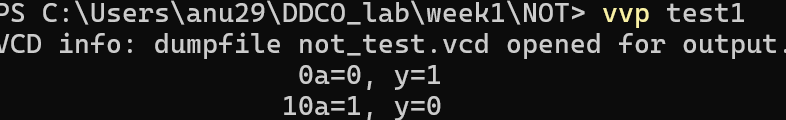


1. NOT

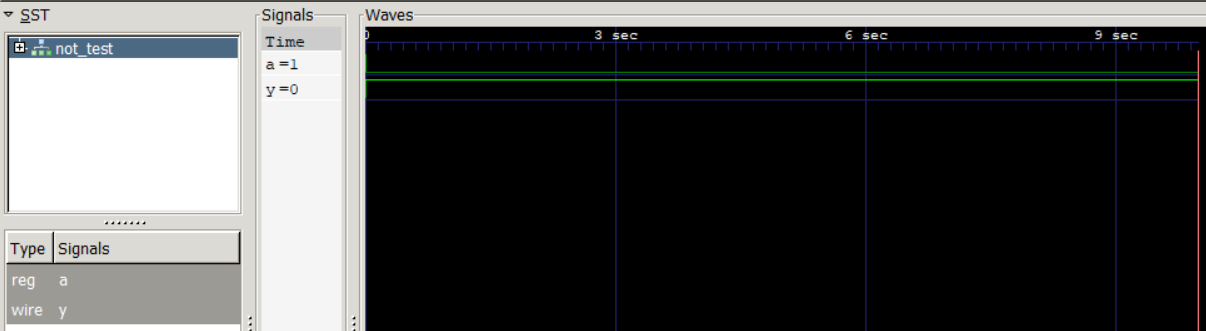
Verilog code:



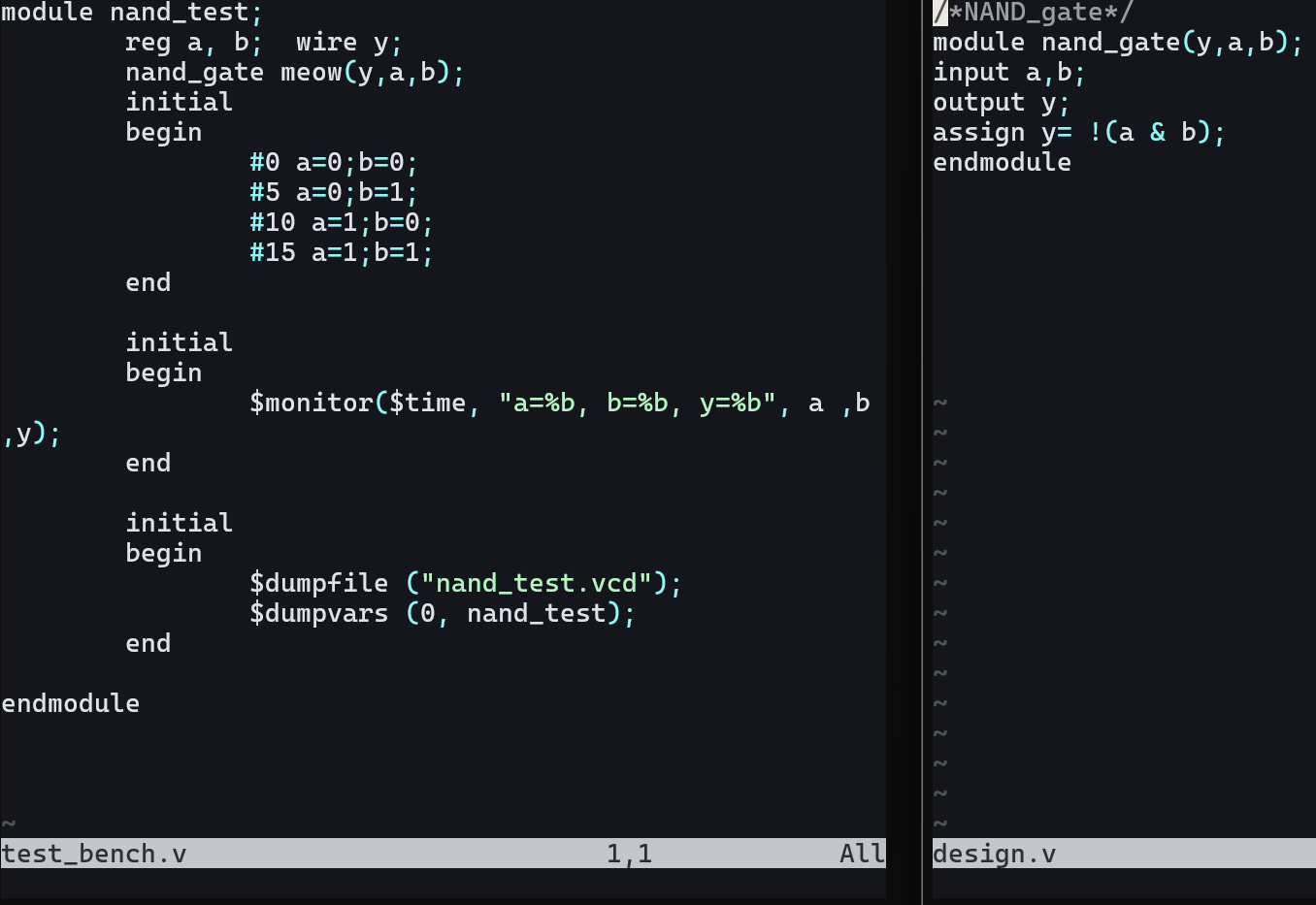
Vvp o/p:



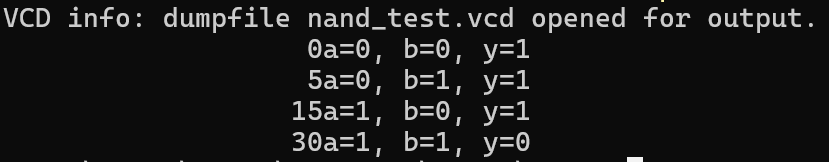
Gtk wave:



1. NAND

Iverilog code:

Vvp o/p:



Gtkwave:

