Indian Institute Of Information Technology,

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4:2 Compressor CMOS Design

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- **Abstract-**

  The 4:2 compressor is a combinational circuit that takes four input bits and produces two output bits. It is commonly used in arithmetic circuits such as adders and multipliers to reduce the number of inputs and simplify the circuit design. In this project, we have designed a 4:2 compressor circuit using CMOS technology.

1. Introduction - The 4:2 compressor circuit is a combinational circuit that takes in four input bits and produces two output bits. It is used in arithmetic circuits such as adders and multipliers to reduce the number of inputs required and simplify the overall circuit design. The 4:2 compressor works by comparing the values of the input bits in pairs, and generating the output bits based on the comparison result. For example, if the first two input bits are greater than the second two input bits, the output bits would be '10', otherwise, they would be '01'.

The significance of the project lies in the importance of optimizing circuit designs for improved performance in modern computing systems. As digital devices become more ubiquitous and powerful, there is a need to design circuits that are not only more efficient and faster but also smaller and more compact. The 4:2 compressor CMOS circuit is a crucial building block in such circuit designs, and developing an efficient and effective implementation can lead to significant improvements in the performance and power consumption of the system as a whole.

CMOS (Complementary Metal-Oxide-Semiconductor) is a type of semiconductor technology used in digital circuit design. It is known for its low power consumption, fast switching speed, and ease of miniaturization. In CMOS technology, a complementary pair of MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) transistors is used to implement logic gates, resulting in efficient and low-power circuit designs.

The scope of the project is to design a 4:2 compressor circuit using CMOS technology, with the objective of achieving a compact and efficient implementation. The project involves selecting appropriate CMOS components, designing the circuit layout, and testing the circuit's performance using simulation tools.

2. Circuit Diagram -

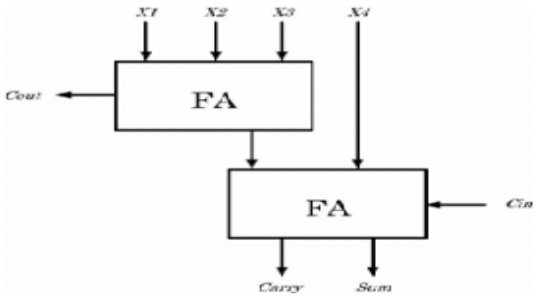


Fig1. (a) Conventional method of 4:2 compressor

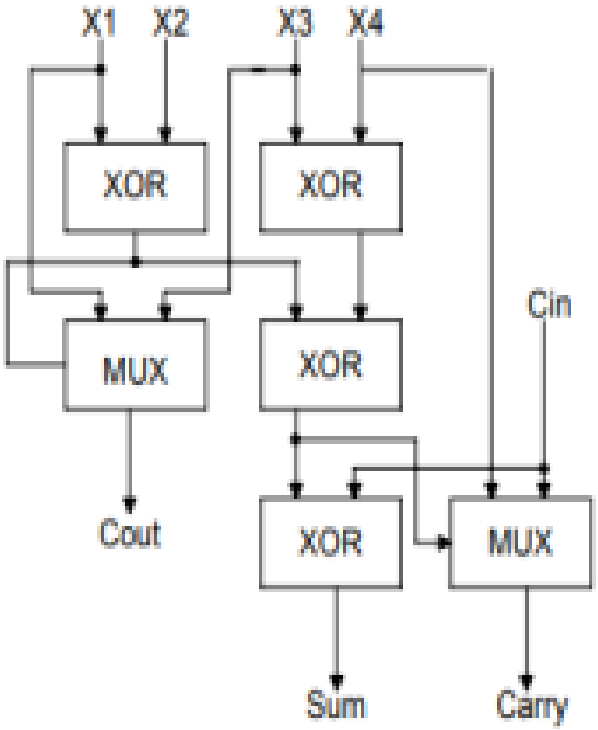
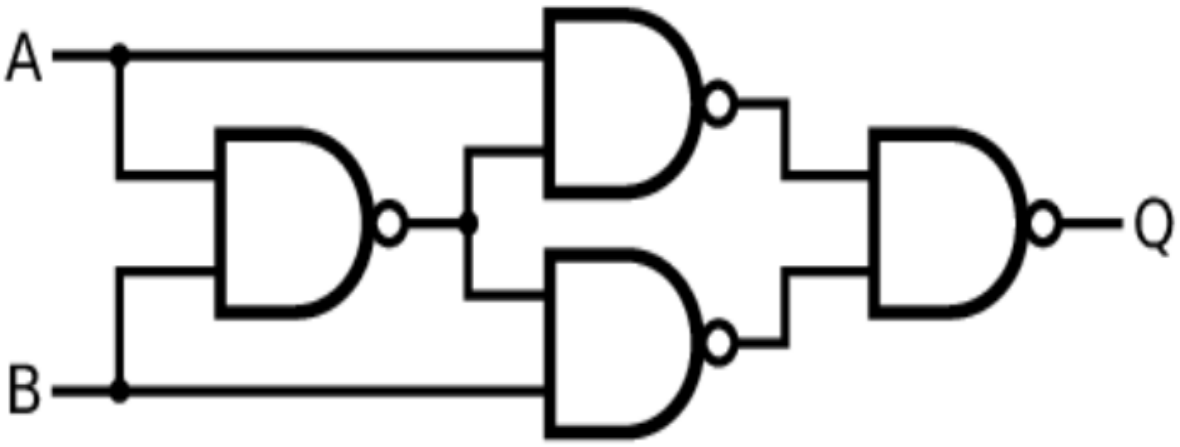


Fig1. (b) 4:2 compressor internal structure of two full adders

Here we are performing this using xor and mux so implement this we need circuit of these

Circuit of XOR—



Circuit for MUX(2:1)—

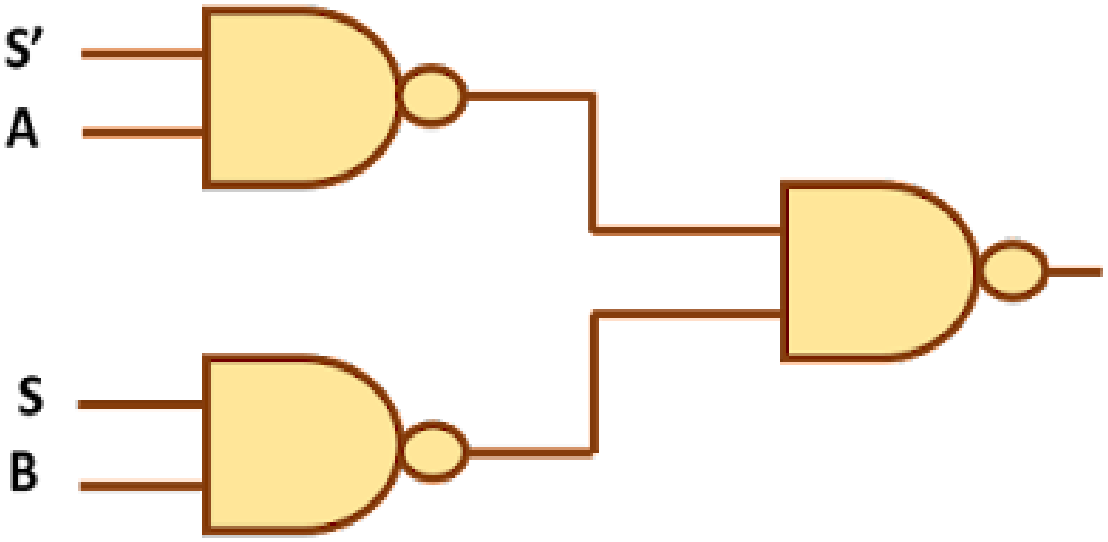
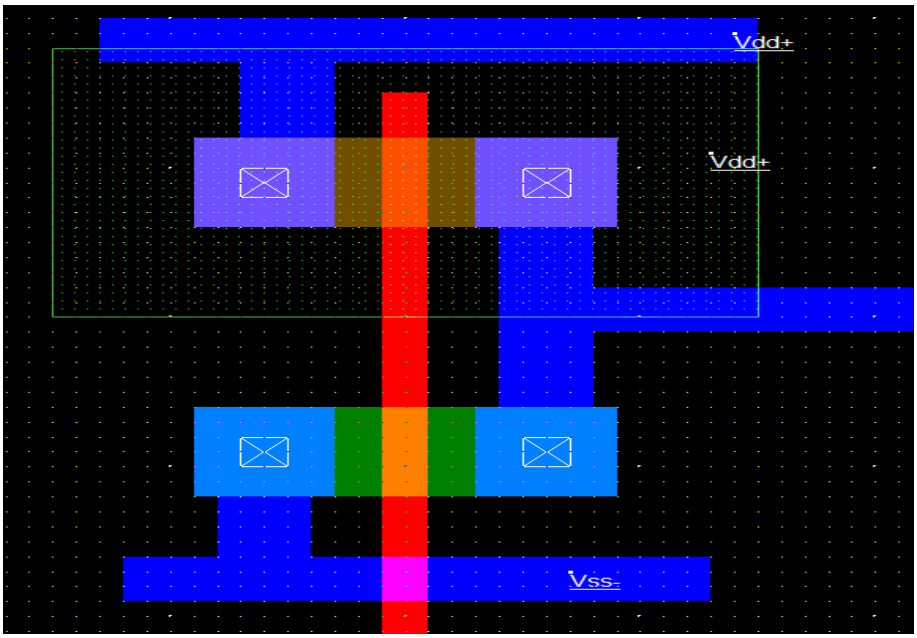


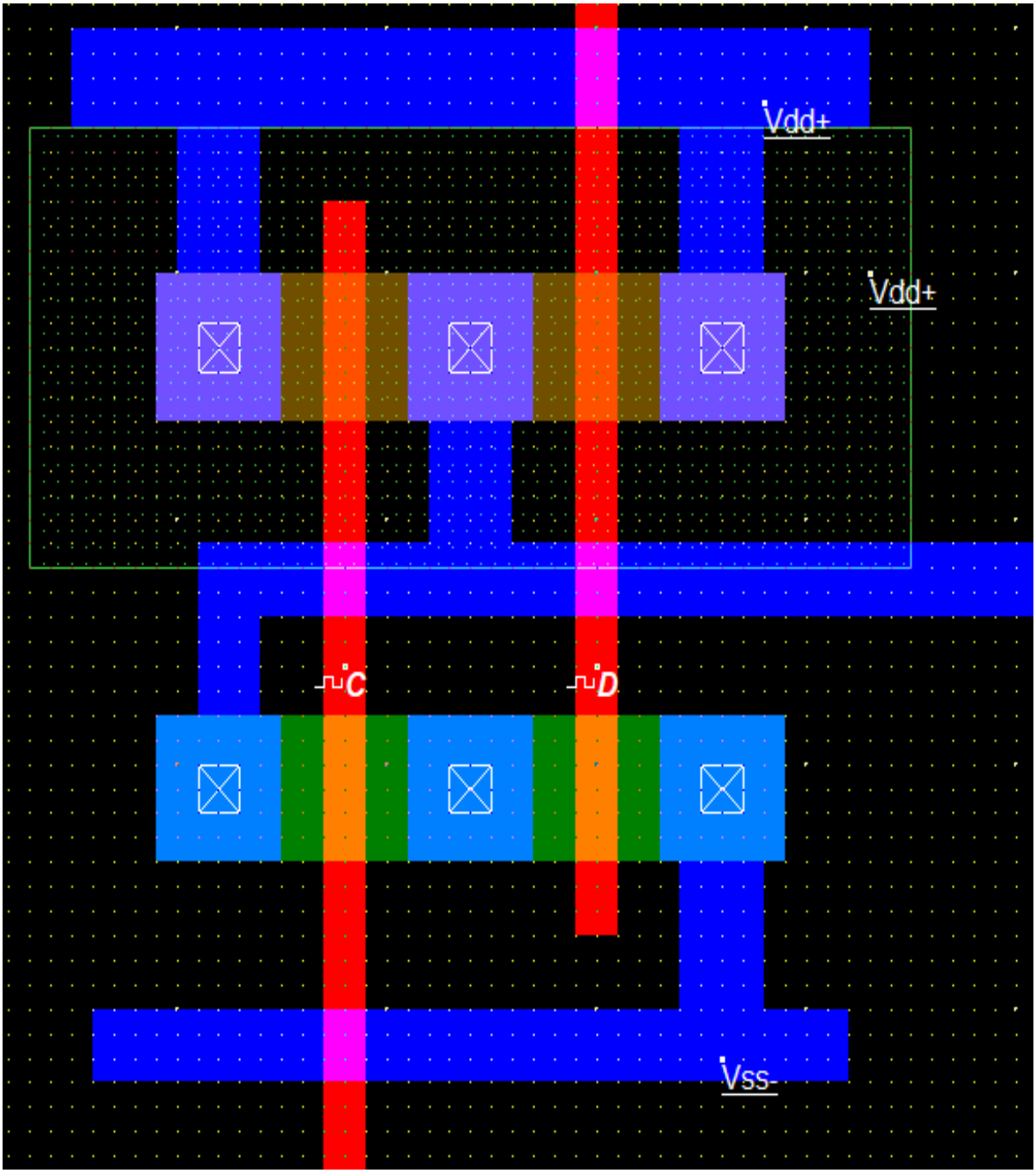
Figure 1: 2:1 Mux using NAND gates

3. Circuit layout -

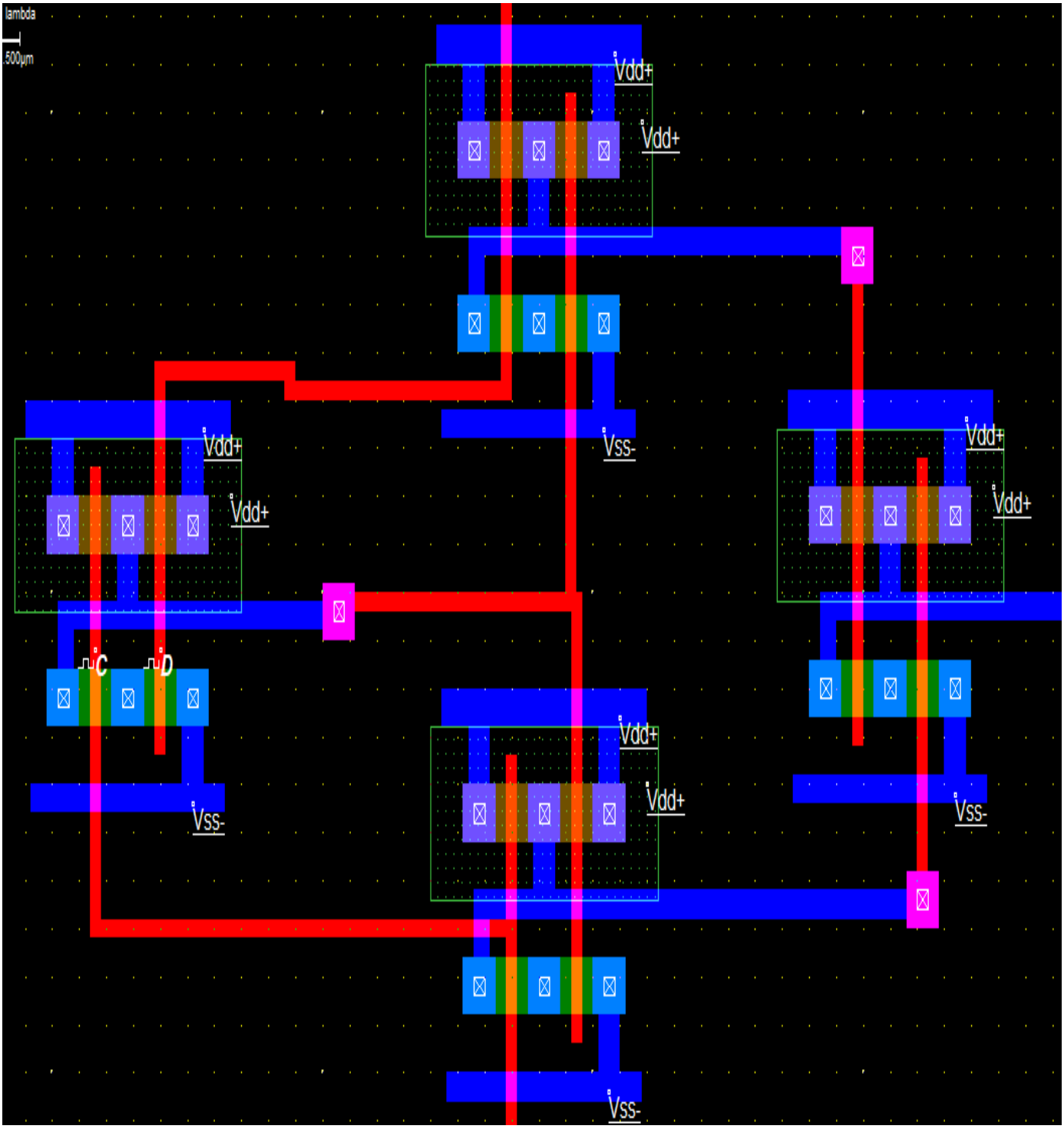
To design this whole circuit we also need invertor layout—



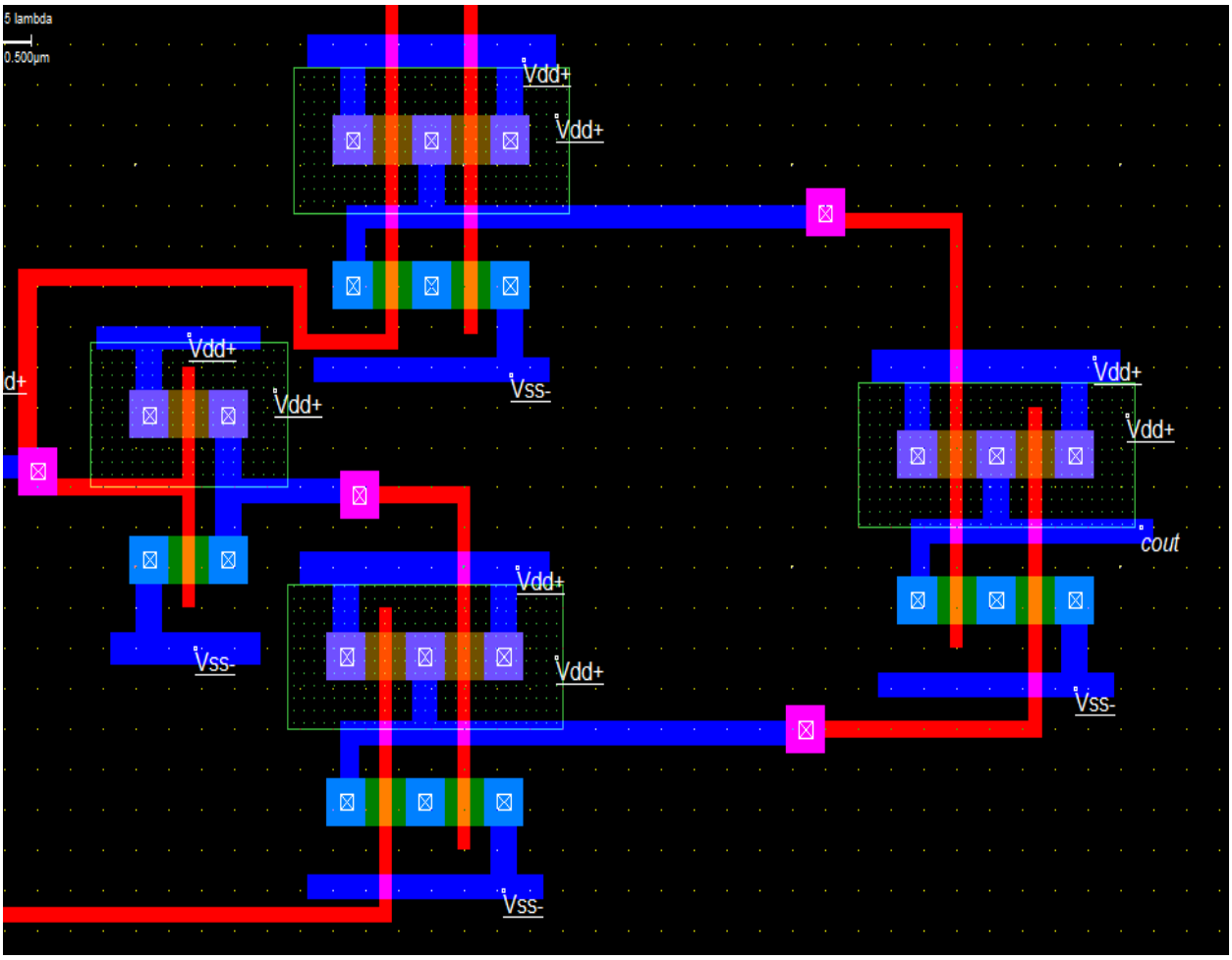
And we also need nand gate layout---



Now we are computing Xor gate using nand gate layout

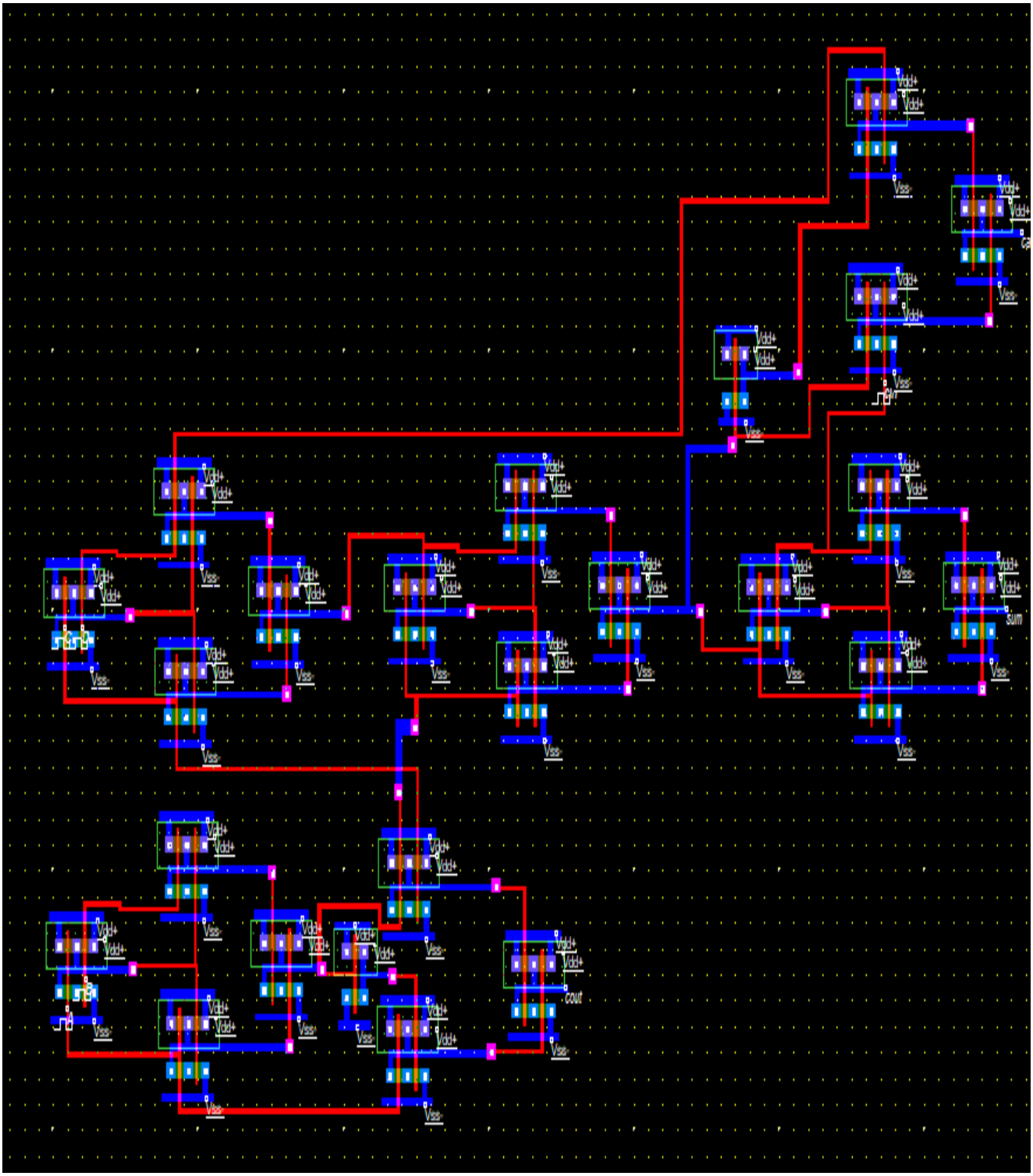


2:1 mux using nand gate layout----

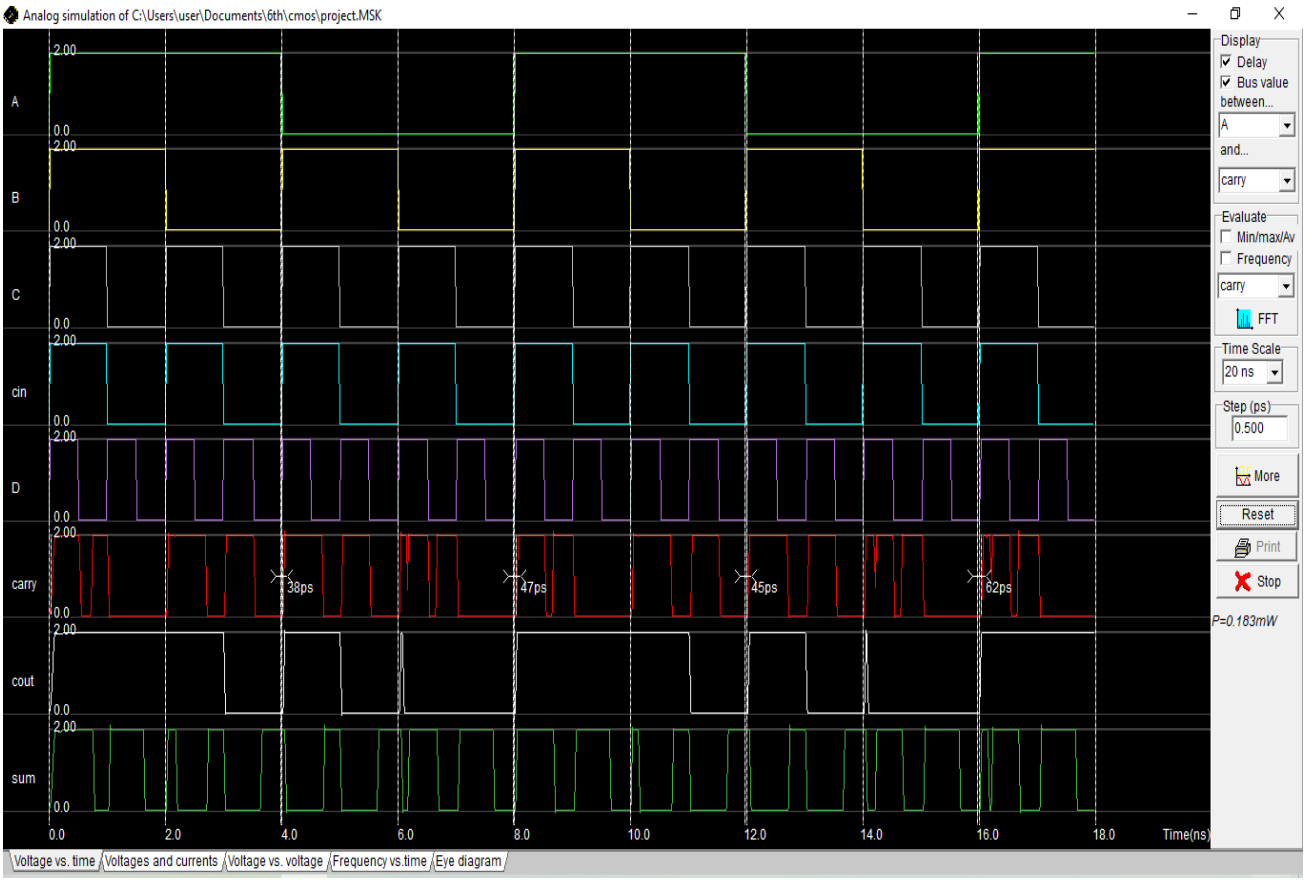


Now using all gate we are designing whole 4:2 compressor layout it consists 4 xor gate and 2:1 mux(2) . for connect them we are using circuit given in circuit diagram section . In this we are giving 4 input to circuit, A,B,C,D and Cin .

All inputs are in form of clock so we want to do analysis of our output.



4.outputs—



5. Simulation Program –

Netlist for the simulation was made using various subcircuits in a ladder like nested structure as each subcircuit was used in another subcircuit for implementation. Starting from subcircuit of inverter, then NAND. Using subcircuit of Inverter, subcircuit of XOR was made, then using it and NAND, subcircuit of MUX was made, and then finally using 4 XOR and 2 MUX final desired circuit was made

Netlist(ngspice)-

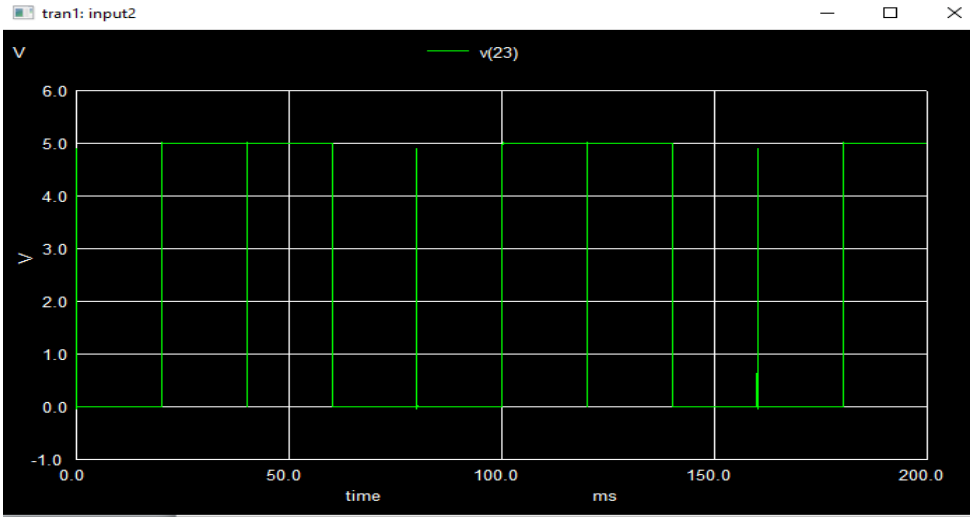
```
***project_cmos created by dharmendra singh roj


.subckt invertor_ckt 1 3 2


.model nmod nmos level=54 version=4.7

.model pmod pmos level=54 version=4.7
```

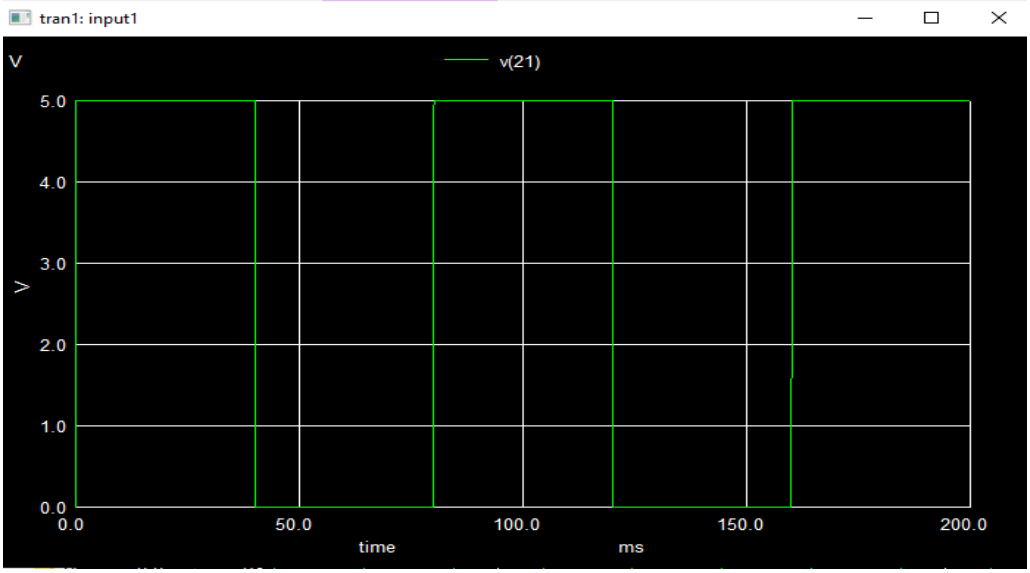
```
M1 2 1 0 0 nmod w=100u l=10u

M2 2 1 3 3 pmod w=100u l=10u

.ends



.subckt NAND_CKT 1 2 3 4


.model nmod nmos level=54 version=4.7

.model pmod pmos level=54 version=4.7


M1 5 1 0 0 nmod w=100u l=10u

M2 4 2 5 5 nmod w=100u l=10u

M3 4 2 3 3 pmod w=100u l=10u

M4 4 1 3 3 pmod w=100u l=10u

.ends


.subckt XOR_CKT 11 12 3 16


Xfirst_nand 11 12 3 13 NAND_CKT


Xsecond_nand 12 13 3 14 NAND_CKT


Xthird_nand 11 13 3 15 NAND_CKT
```

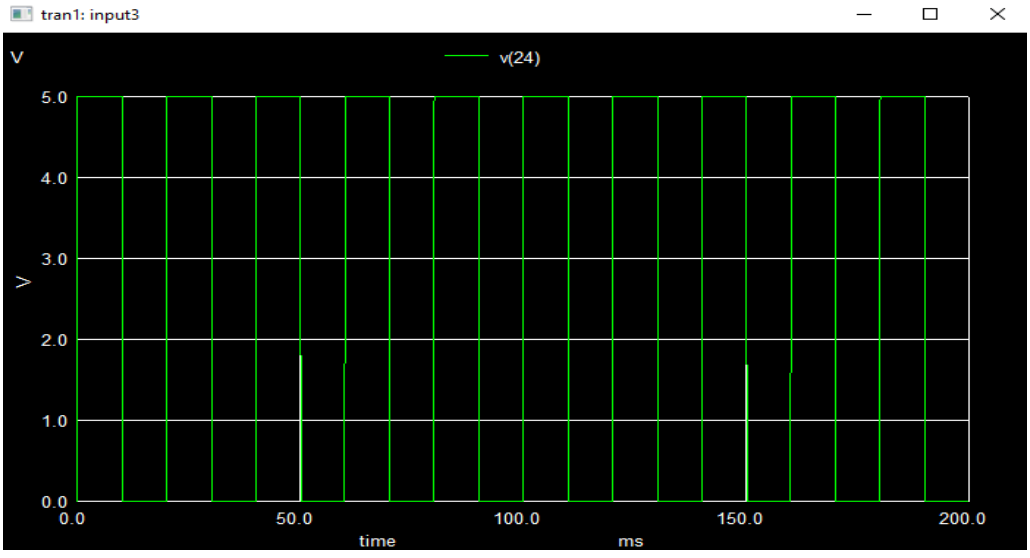
```
Xfourth_nand 14 15 3 16 NAND_CKT


.ends


.subckt MUX_CKT 11 12 13 3 17


Xfirst_nand 11 13 3 15 NAND_CKT


Xinvert 11 3 14 invertor_ckt


Xsecond_nand 12 14 3 16 NAND_CKT


Xthird_nand 15 16 3 17 NAND_CKT

.ends




Va 21 0 pulse(0 5 0 0 0 40m 80m)

Vb 22 0 pulse(0 5 0 0 0 20m 40m)

Vc 24 0 pulse(0 5 0 0 0 10m 20m)

Vd 25 0 pulse(0 5 0 0 0 5m 10m)

Ve 29 0 pulse(0 5 0 0 0 10m 20m)


Vdd 3 0 dc 5v
```

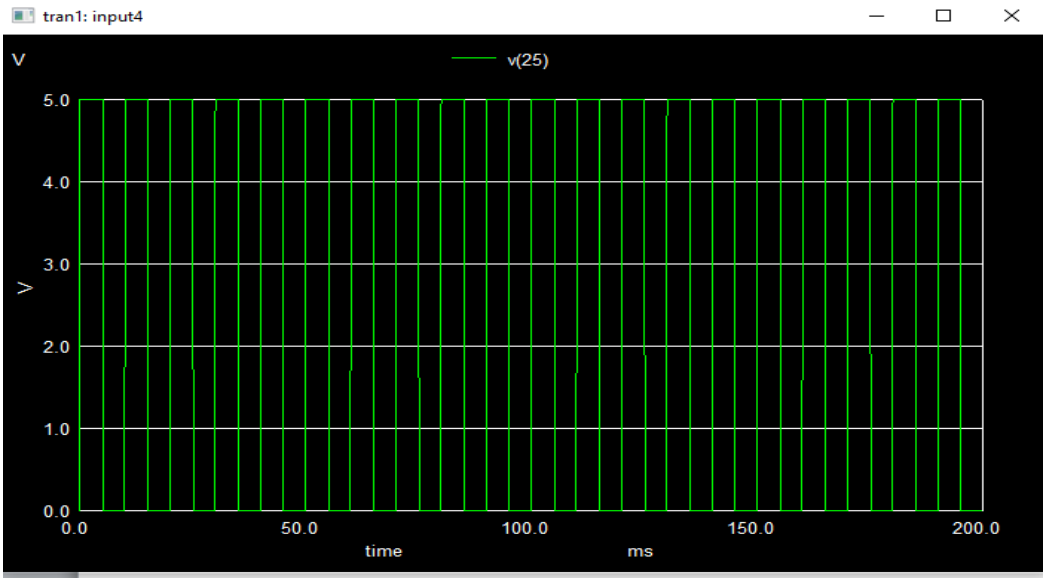
```
Xxor_1 21 22 3 23 XOR_CKT

Xxor_2 24 25 3 27 XOR_CKT

Xmux_1 21 24 23 3 26 MUX_CKT

Xxor_3 23 27 3 28 XOR_CKT

Xmux_2 25 29 28 3 31 MUX_CKT

Xxor_4 28 29 3 30 XOR_CKT


.tran 0.1m 200m

.control

run


plot V(21) xlabel 'time' ylabel 'V' title 'input1'

plot V(23) xlabel 'time' ylabel 'V' title 'input2'

plot V(24) xlabel 'time' ylabel 'V' title 'input3'

plot V(25) xlabel 'time' ylabel 'V' title 'input4'

plot V(29) xlabel 'time' ylabel 'V' title 'Cin'

plot V(31) xlabel 'time' ylabel 'V' title 'CARRY'

plot V(30) xlabel 'time' ylabel 'V' title 'SUM'

plot V(26) xlabel 'time' ylabel 'V' title 'COUT'


.endc

.end
```

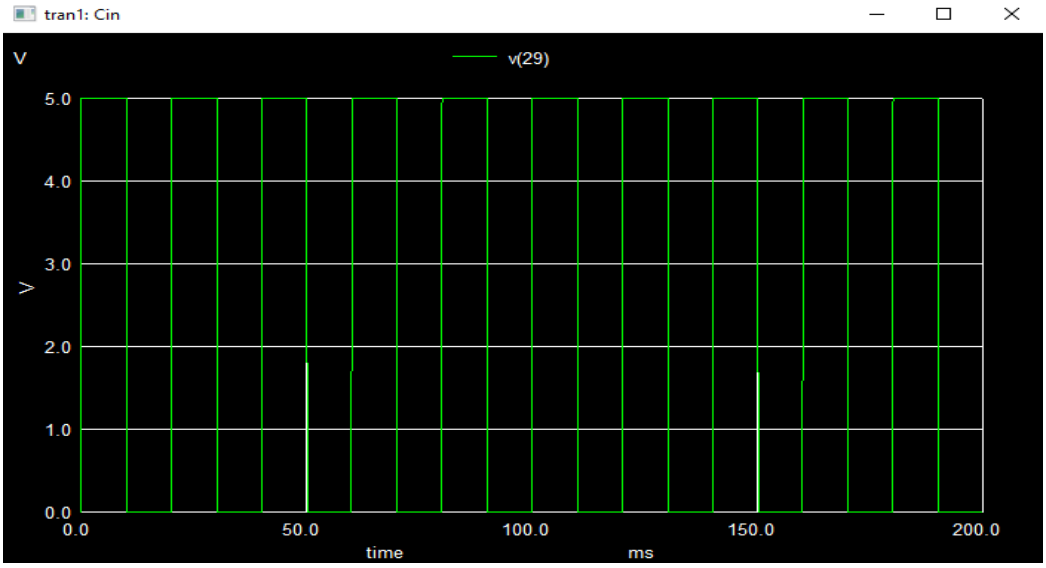
Inputs and outputs of netlist(ngspice)

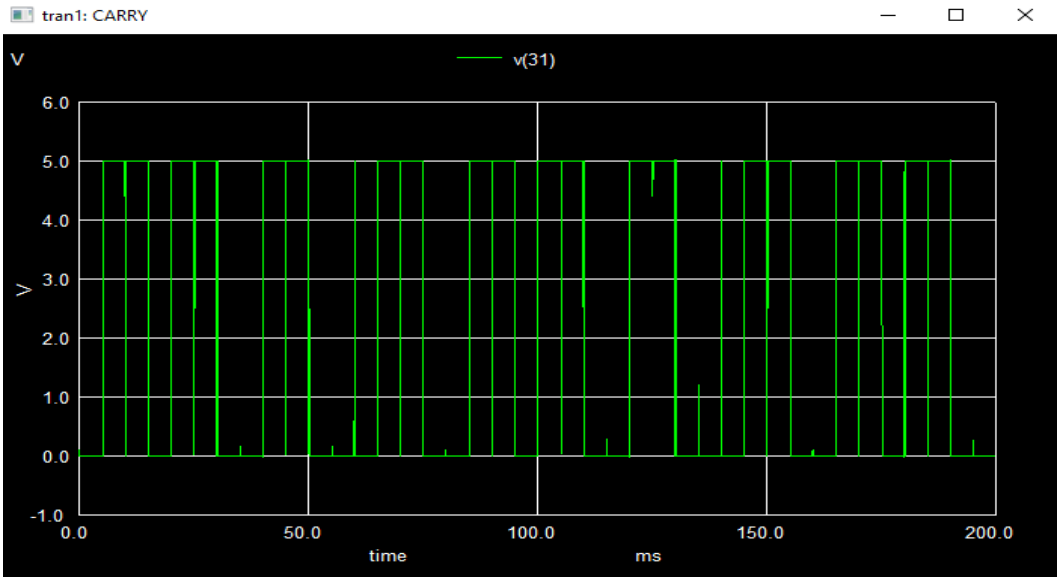


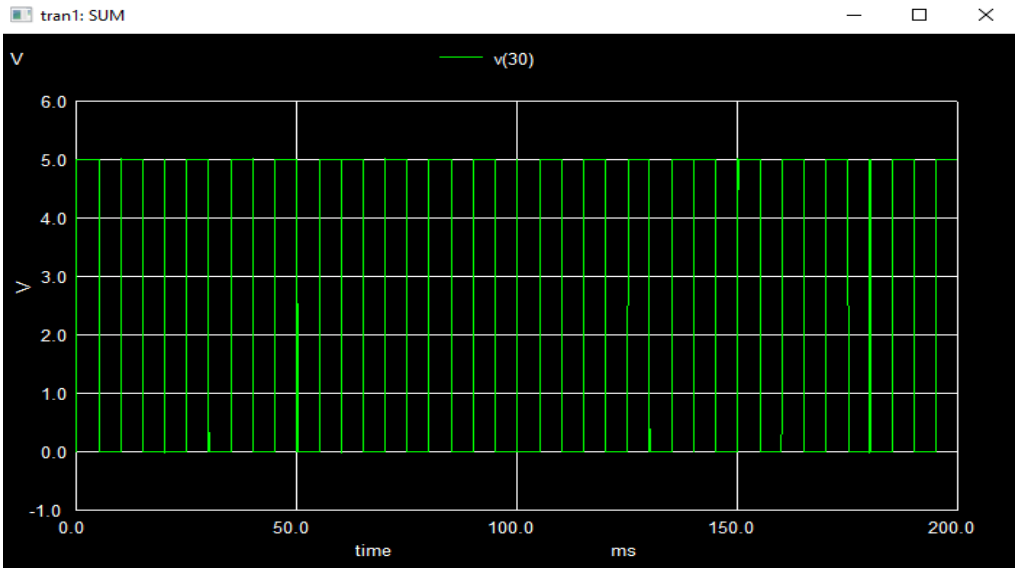


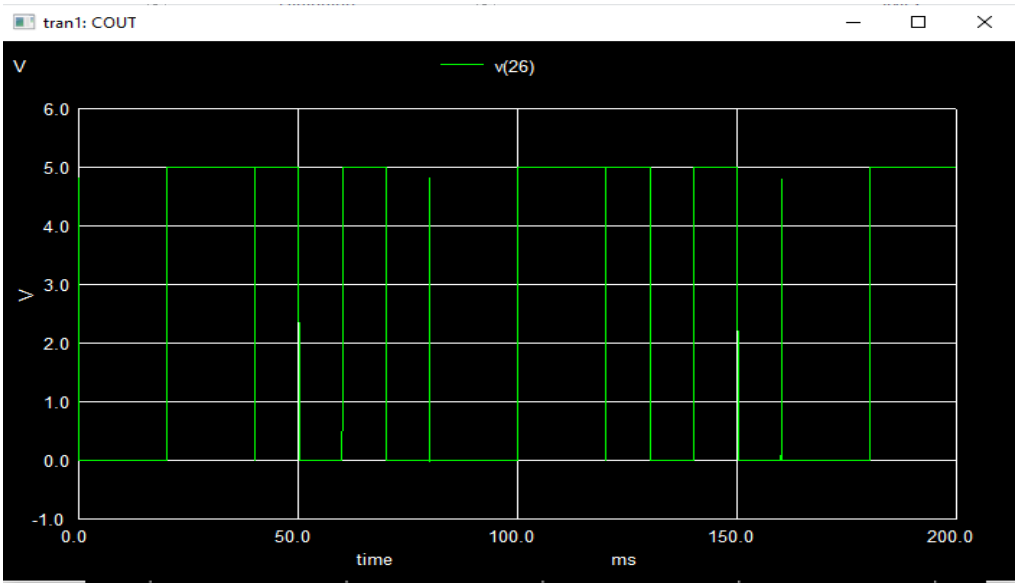



tran1: input4
V
v(25)
5.0
4.0
3.0
2.0
1.0
0.0
V
0.0
50.0
100.0
150.0
200.0
time
ms


tran1: Cin
V
v(29)
5.0
4.0
3.0
2.0
1.0
0.0
V
0.0
50.0
100.0
150.0
200.0
time
ms


tran1: CARRY
V
v(31)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
-1.0
V
0.0
50.0
100.0
150.0
200.0
time
ms





6. Optimized circuit –

A new layout comprises of transmission logic (four Multiplexers), six transistor (6T) XNOR inverter and two 8T (eight transistors)XOR-XNORunits. For getting good result in speed, full potential swing we have to use XNOR gate operation in this layout and also it consumes less power.

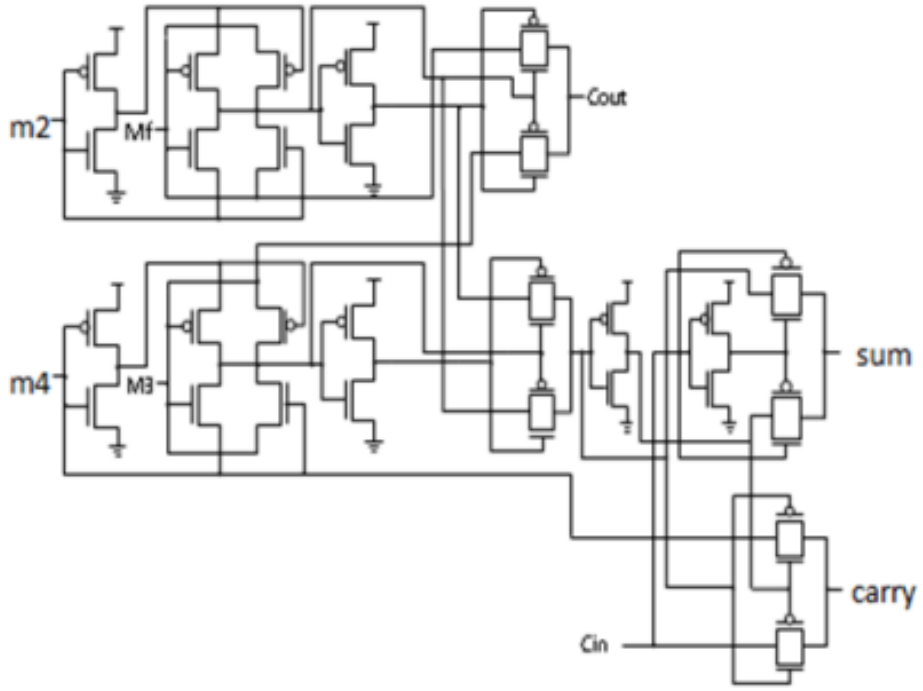
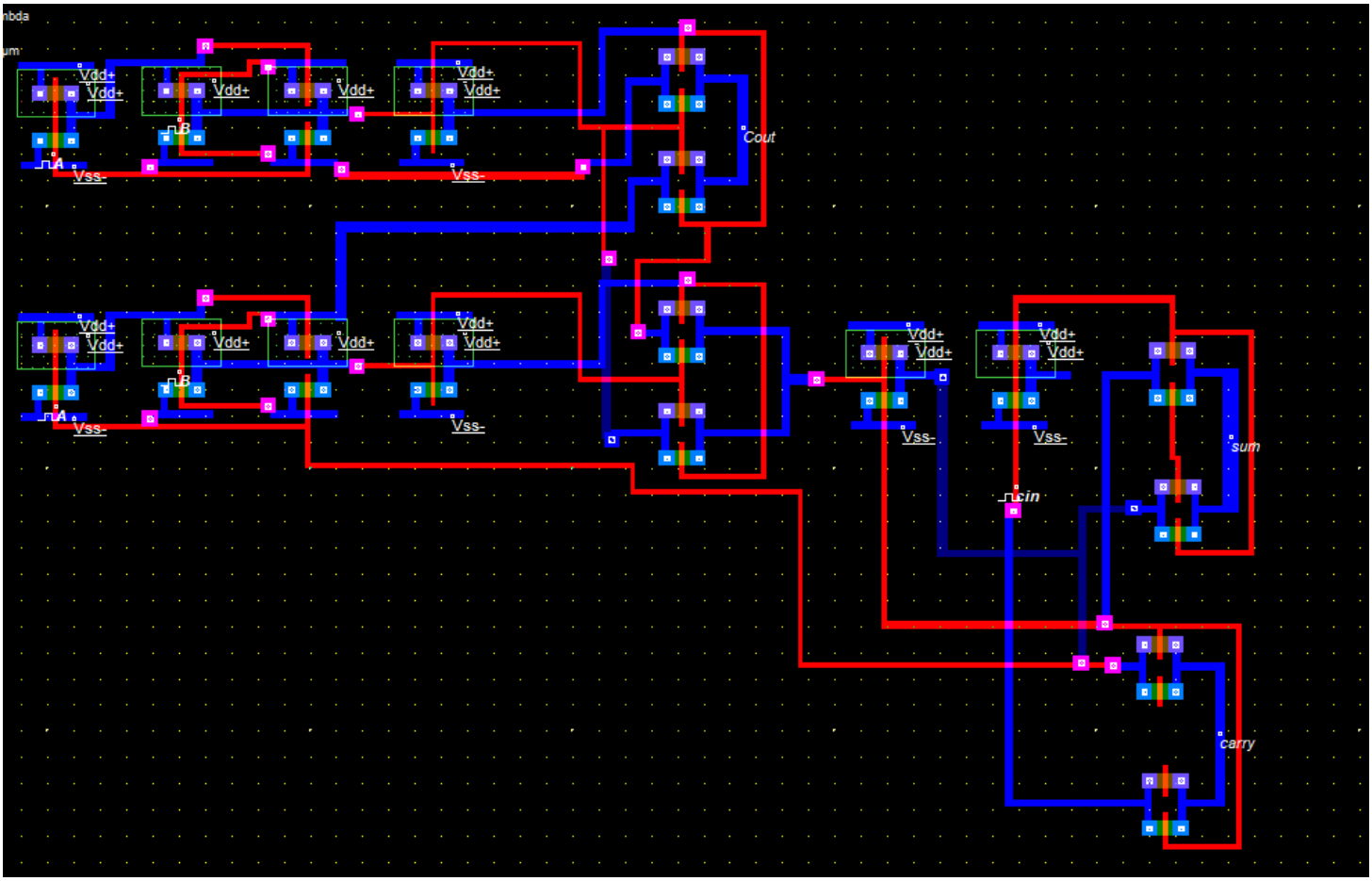
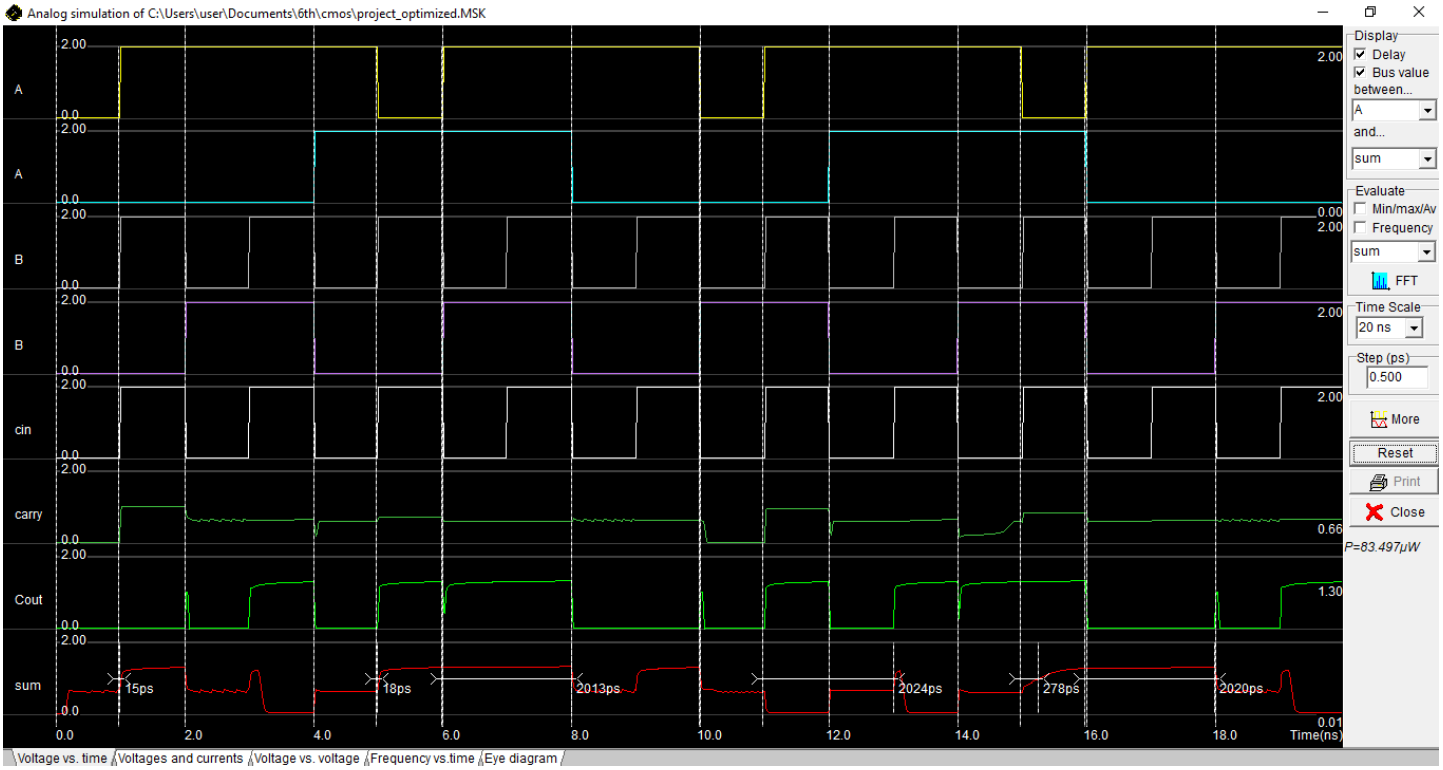


Fig4.Proposed Compressor diagram



Output-----



7. Conclusion –

The proposed layout consequently attains the reduced power consumption and less delay using 36 transistors. For achieving the good energy-efficient compressor reduced transistor area is proposed. Comparing with previous designs the proposed module achieved less no. of transistors, cut down area and high energy efficiency. As result for above modules with givenvoltageof3.3V, anaveragepowercut down by theproposedcompressoris23.26µWandthesuperlative delay is 400.2ns.

Different styles of 4:2 Compressors	POWER (Micro Watts)	DELAY (Nano sec)
Conventional method Compressor	74.96	400.5
Proposed Compressor	23.26	400.2

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