Design and Verification of 12-bit SAR ADC with Non-Binary Multiple-LSB-Redundant and Non-Integer-and-Split-Capacitor DAC

Dharma Anargya Jowandy – Personal Project Proposal
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Project Background

This personal project was initiated as a result of participating in the Chipathon 2025 contest. The proposal for the analog track focuses on an 8-bit SAR ADC design. As a second-year undergraduate Electrical Engineering student from ITB, Indonesia, with no prior IC design experience, I was unable to continue because the demanding pace of the competition design stage was too fast. Nevertheless, I am eager to complete the design as a personal project on my own timeline. In carrying it out, I’m fortunate to be supervised by a senior who is now pursuing a master’s degree at KAIST and has experience in the mixed-signal field

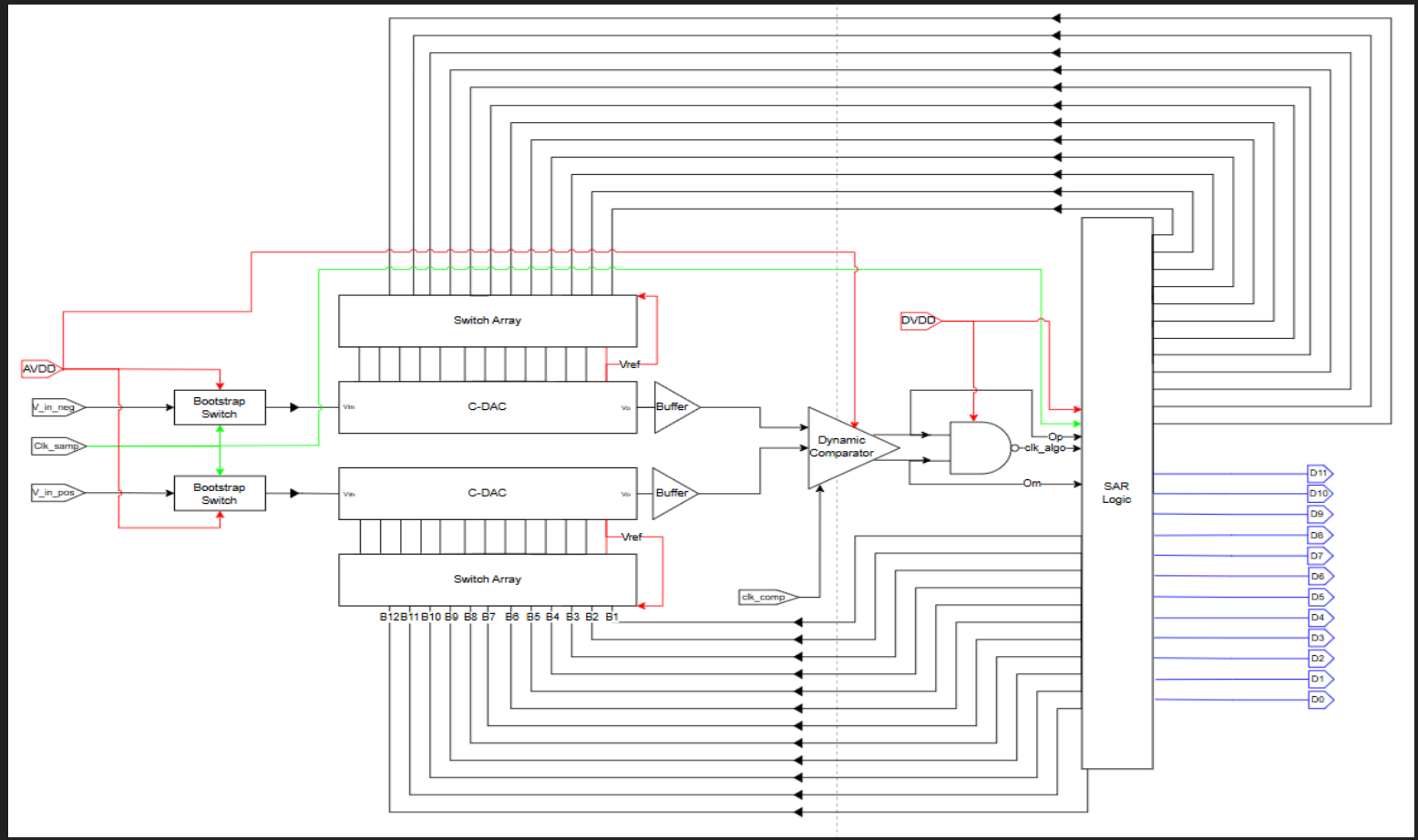
Objectives

Proposed Design Specifications

Parameter	Value
Resolution (bit)	12
Technology (nm)	180
Supply Voltage (V)	5
Sampling Rate (MS/s)	1
DNL (LSB)	0,54
INL (LSB)	0,89
ENOB (Bit) @Nyquist	11,25
Power Cons. (µW)	44,78
Area (mm^2)	0,367
Unit Cap. (fF)	20
Total Cap. (pF)	10,24
FoM (fJ/conv.-step)	18,39
FoM (dB)	169,99

- The main goal of this project is to design a 12-bit SAR ADC architecture, covering the ideal circuit simulation, transistor-level circuit implementation & simulation, and layout design.
- Design performance itself is taken from the work of Kuo et al. (2017) as a reference.
- The focused design stage will be implemented using an open-source toolchain, such as gf180mcuD PDK, Ngspice, Magic, and Klayout.

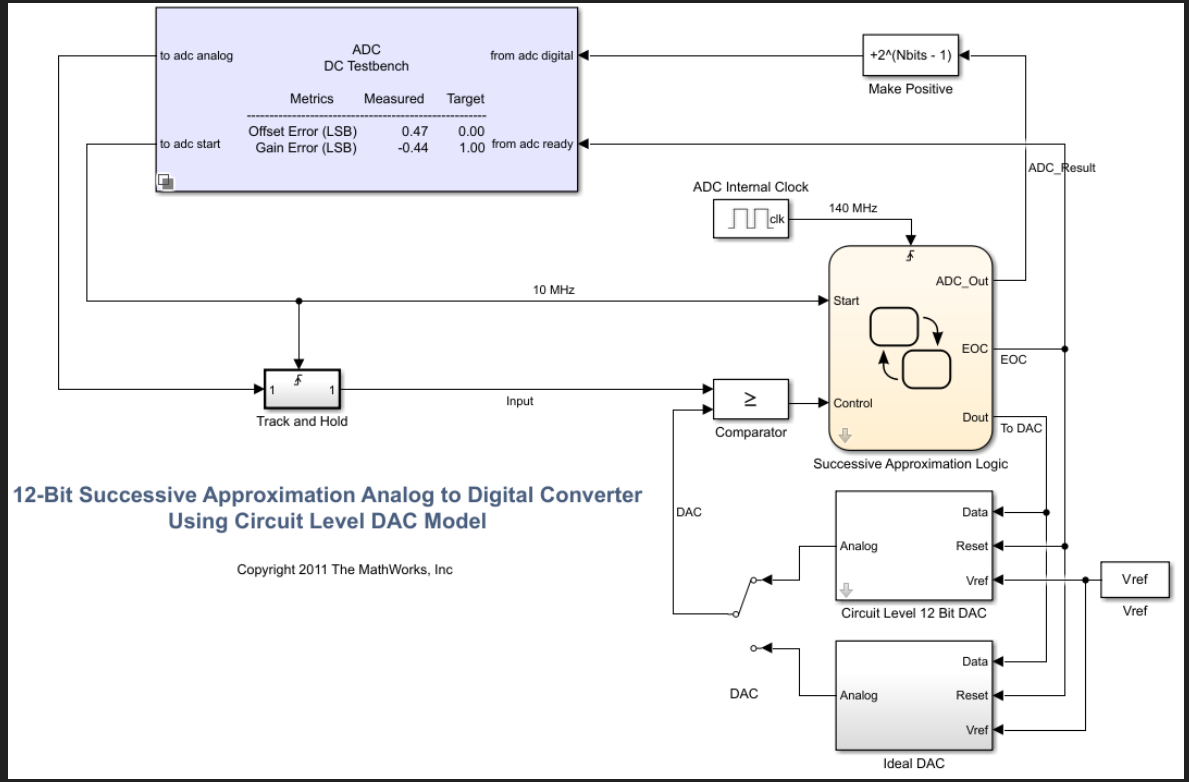
Block Diagram (Top Level)



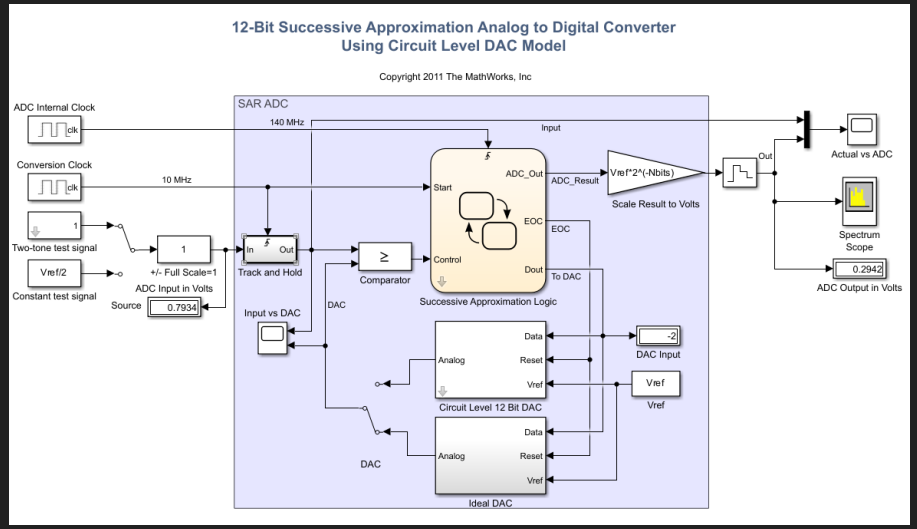
Electrical Spesifications

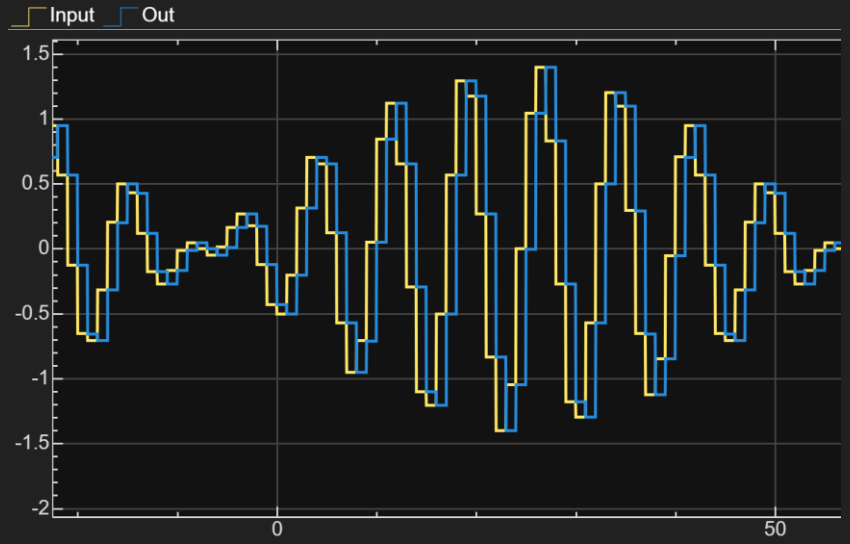
Parameter	Value	Description
AVDD (V)	5	Positive power supply (analog circuit)
AVSS (V)	GND	Ground reference (analog circuit)
DVDD (V)	5	Positive power supply (digital circuit)
DVSS (V)	GND	Ground reference (digital circuit)
VIN (V)	1.2 - 4	Differential analog input range.
VREFP (V)	2,8	Positive reference voltage
VREFN (V)	-2,8	Negative reference voltage
VOUT (V)	5	High-level voltage (digital output)
VCM (V)	2,6	Input common-mode voltage
CLK_SAMP (MHz)	1	Sampling clock frequency
CLK_COMP (MHz)	14	Comparator clock frequency

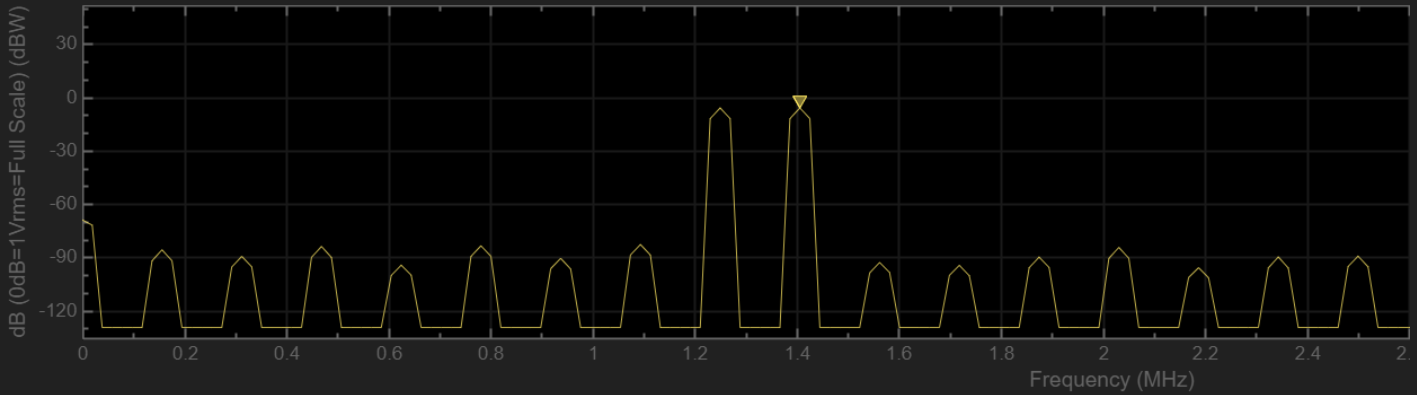
System-Level Model: SAR ADC DC Testbench



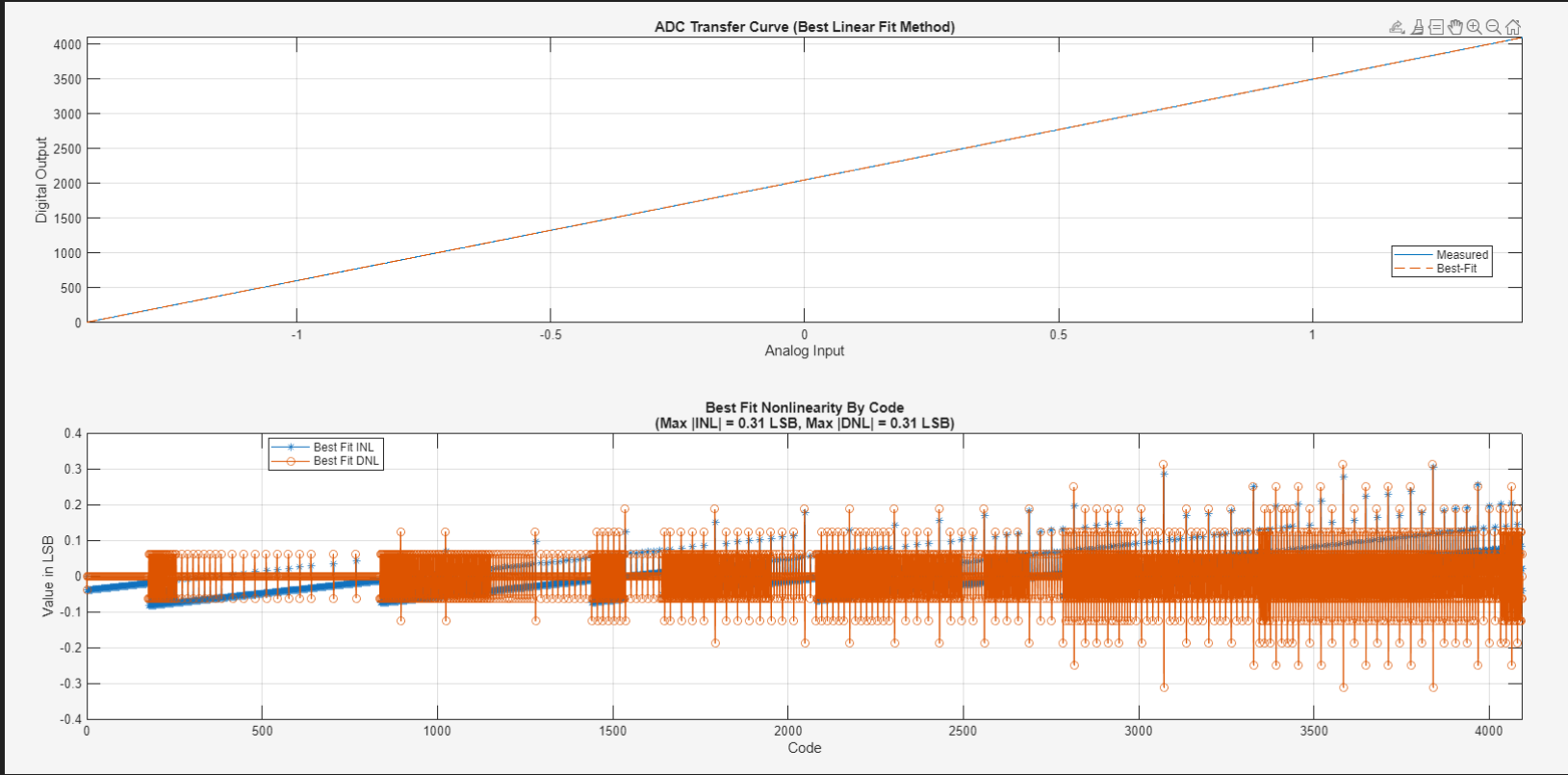
SAR ADC System-Level Model Setup



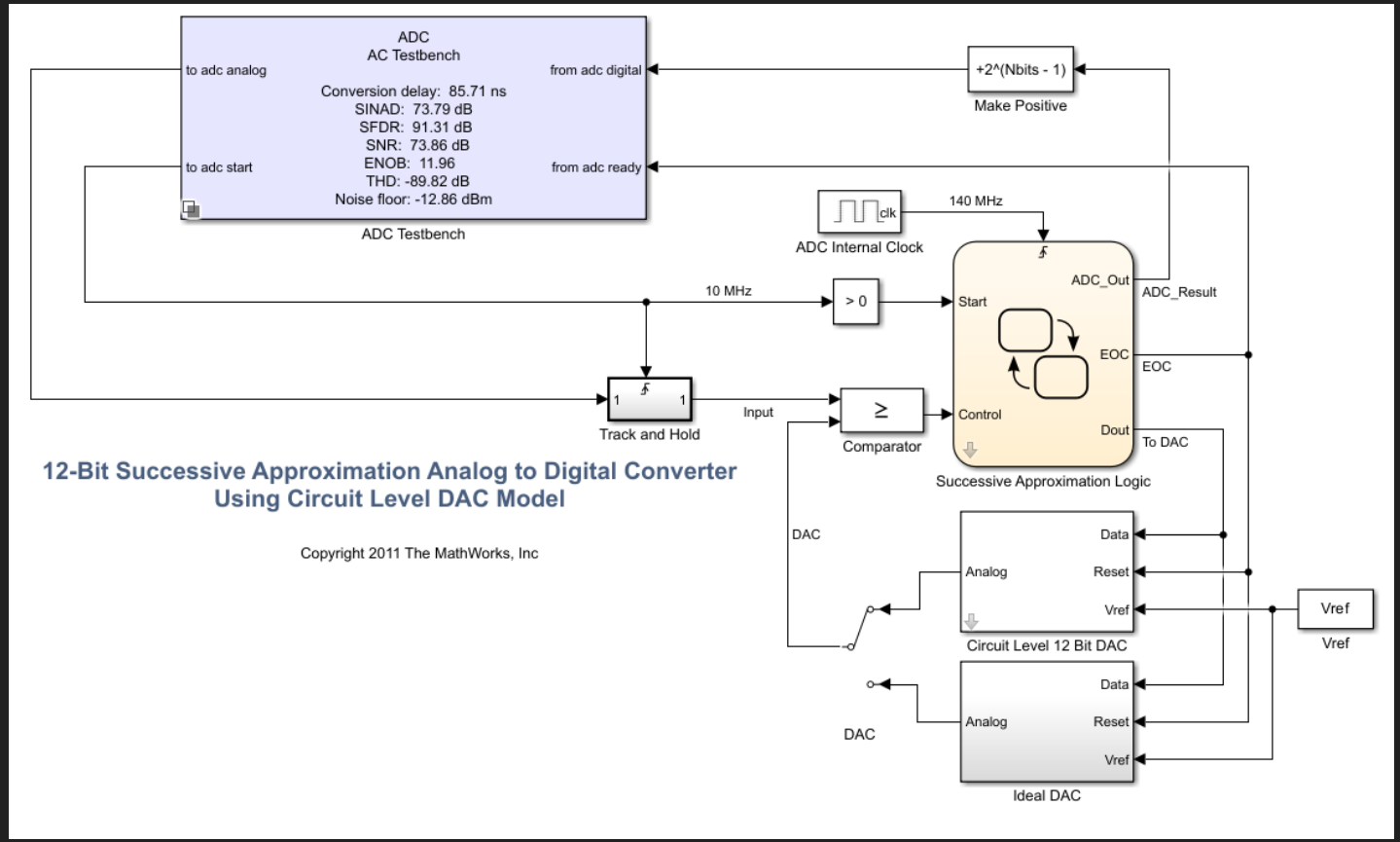




System-Level Model: SAR ADC DC Testbench



System-Level Model: SAR ADC AC Testbench



Timeline

Month	Phase	Description
Sep-25	System & Behavioural Modelling	• 12-bit SAR ADC system level modelling • AC & DC testbench. • Define the high-level architecture
Oct-25	Comparator & S/H Design	• Design the comparator. • Design the sample-and-hold (S/H) circuit. • Perform DC, transient, and noise simulations
Nov-25	Capacitor DAC & Reference	• Define the capacitor array architecture (e.g., binary-weighted/split). • Design and add the reference buffer.
Dec-25	Full ADC Integration (Pre-Layout Simulation)	• Integrate the comparator, S/H, DAC, and reference buffer. • Add the SAR logic & NAND Gate. • Full performance simulations
Jan-26	Block-Level Layout Design	• Layout the comparator • Layout the DAC array • Layout the S/H circuit and reference buffer. • Run Design Rule Check
Feb-26	Top-Level Layout Assembly	• Assemble all blocks at the top level. • Optimize block placement for area efficiency

References

- A. Jayaraj, N. Nitin Gujarathi, I. Venkatesh and A. Sanyal, "0.6–1.2 V, 0.22 pJ/bit True Random Number Generator Based on SAR ADC," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 10, pp. 1765-1769, Oct. 2020, doi: 10.1109/TCSII.2019.2949775.
- C. -C. Liu, S. -J. Chang, G. -Y. Huang and Y. -Z. Lin, "A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure," in IEEE Journal of Solid-State Circuits, vol. 45, no. 4, pp. 731-740, April 2010, doi: 10.1109/JSSC.2010.2042254.
- https://github.com/IHP-GmbH/IHP-AnalogAcademy.git
- H.-L. Kuo, C.-W. Lu, and P. Chen, "An 18.39 fJ/Conversion-Step 1-MS/s 12-bit SAR ADC with Non-Binary Multiple-LSB-Redundant and Non-Integer-and-Split-Capacitor DAC," *IEEE Access*, vol. 9, pp. 5651-5669, 2021, doi: 10.1109/ACCESS.2020.3048979.