Intel® SoC Watch for Windows* Release Notes

(for Internal use only)

October 2025

Version 2025.7

Intel Corporation

www.intel.com

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Contents

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Version History

These are the main releases of Intel® SoC Watch:

Date	Revision	Description
April, 2019	2.10.1	This release corrects an error in a JSON-formatted help file.
June, 2019	2.11	Added feature to show settings for display panel low power modes (-f dpst). Updates support for Tiger Lake PCH and adds Teton Glacier Optane support. Includes some support for Cascade Lake-Xeon. Improves handling of unrecognized CPUs, reporting S-state when hibernation occurs, and other bug fixes.
September, 2019	2019.12	Added support for Intel PCH code named Comet Lake V. Initial support for Jasper Lake Plus . Added features vr-pwr-state and display-rr. Improved sata-lpm DevSlp Capabilities reporting, cpu-pkgc-dbg, and PCH metrics for various platforms. Modified pch-ip-active percentage calculation. Modified hw-cpu-pstate reporting.
October, 2019	2019.13	Added feature s0ix-subs-status to NDA for Intel platform code named Tiger Lake. Fixed issue in ddr-bw and hw-cpu-cstate for Intel platform code named Tiger Lake. Fixed issue in hw-cpu-pstate for Intel platform code named Ice Lake.
November, 2019	2020.1	Added support for collecting metrics on Intel discrete graphics cards code named DG1. Added NDA support for Intel platform code named Elkhart Lake and Intel PCH code named Mule Creek Canyon. Added support for Intel platform code named Spring Hills. Added support for Intel platform code named Tiger Lake -H. Fixed issues in pcie-lpm, pcie-ltr and display-rr among others. Fixed several features for Intel platform code named Lakefield.
February, 2020	2020.2	Added collection of tool usage analytics. Added support for Rocket Lake, Alder Lake, Cooper Lake, Tiger Lake -H PCH and JSP-N PCH. Extended support of Snow Ridge and Ice Lake Xeon to NDA along with various features. Added new internal feature hgs-feedback and pch-ivr-state. Added features pch-slps0, pch-slps0-dbg to External. Enhanced Continuous Monitoring API. Improved error messages and help output. Enhanced driver security. Improved many metrics.
June, 2020	2020.3	Change in pch-ip-active behavior. Added feature s0ix-subs-dbg. Added (NDA) support for Intel platforms code named Cooper Lake-Xeon, Jasper Lake Plus, and Ice Lake Xeon -D. Added VMD support to PCIe features. Many bug fixes, including corrections in tcss-state, s0ix-subs-status, dpst, display-rr.

Date	Revision	Description
		Added support for most metrics on Alder Lake.
July, 2020	2020.3.1	Added NDA support for Intel platforms code named Rocket Lake and Sapphire Rapids. Bug fixes
September, 2020	2020.3.2	Corrected and extended support for Alder Lake. Added NDA support for Intel platform code named Alder Lake and Intel® Arc Discrete Graphics Card. Added soc-temp for Intel platform coded named Tiger Lake (B0) and updated pch-platform-ltr and pch-ip-status. Added ddr-bw and soc-temp for Intel platform coded named Tiger Lake -H. Bug fixes including correcting hibernation detection. Added cpu-pkgc-dbg for Intel platform code named Jasper Lake Plus.
October, 2020	2020.4	Added external support for Intel platform code named Tiger Lake. Added topology label in reports for some metrics. Re-named feature cpu-gpu-concurrency to cpu-igpu-concurrency. Removed support for older platforms. Also removed socperf. This version is for external package release only.
November, 2020	2020.5	Includes all changes noted above for v2020.4 release. Changed hw-cpu-pstate to report frequencies per thread rather than per core. Added term *integrated* to hw-igfx-cstate and hw-igfx-pstate report titles. Fixes for PCH metrics on Intel platforms code named Tiger Lake and Alder Lake.
April, 2021	2021.1	Added system name, OS name, and Intel PMT GUID to output reports. Included throt-rsn and other sampled count results in Automation_Summary. Re-ordered feature reports in summary output. Added Intel PMT metrics support for additional SKUs of Intel platform code named Alder Lake. Added Intel PMT features (for pkg C debug, bandwidth, LTR, and temperatures) and non-PMT features (for power limits) for Intel platforms code named Alder Lake and Tiger Lake. Added DC6V state to display-state for Alder Lake. Added basic support for Meteor Lake, Alder Lake -N, and Granite Rapids. Added support for Raptor Lake (-S). Added support for Intel® Arc Discrete Graphics Card . Added NDA support for PCH on Intel platform code named Alder Lake (-P, -M). Improvements/fixes for pch-ip-active, pch-ip-status, TCCold reporting, PCIe device discovery, empty summary reports, and more. Modified WakeupAnalysis report and added percentage table.
May, 2021	2021.1 .1	Fixed tcss-state for Intel platforms code named Tiger Lake -H and Alder Lake.

Date	Revision	Description
		Fixed cpu-pkgc-dbg for Intel platform code named Alder Lake.
July, 2021	2021.2	Extended Raptor Lake recognition, added ADL -N PCH, and ATS -M support. Fixed pcie-lpm PEG and VMD issues. Added dgfx-dstate for Intel discrete graphics code named DG2. Added PCx LTR threshold report to soc-ltr for Intel platforms code name Tiger Lake and Alder Lake. Added Intel PMT metrics perf-limit-rsn, ipu-state, llc-state, osreq-pkg-cstate, pkg-llc-flushed (internal only) for Tiger Lake and Alder Lake. Enhanced WakeupAnalysis report with idle time per process. Improved ia-throt-rsn support when Windows* OS secure modes are enabled. Fixed panel-srr recognition of when PSR2 is enabled on Intel platform code named Alder Lake.
September, 2021	2021.3	New feature s0ix-subs-req for Intel platform code named Alder Lake (-P). Added internal support for Intel PMT metrics on Raptor Lake. Bug fixes including correctness issues in pcie-lpm, pcie-ltr, cpu-pkgc-dbg, perf-limit-rsn, and several dgfx features.
October, 2021	2021.3.1	Improved support for platforms with many sockets and/or discrete graphics cards. Modified option --update-usage-consent.
November, 2021	2021.4	Added NDA support for Intel platforms code named Raptor Lake (non-PMT features) and Alder Lake -N. Added external support for Intel platforms code named Rocket Lake and Tiger Lake -H. Added external support for Intel platforms code named Ice Lake -X and Cooper Lake -X. Added some PCH features for Meteor Lake. Multiple bug fixes including correctness issues in s0ix-subs-dbg, sata-lpm, xhci-lpm, and dgfx-soc-ltr.
December, 2021	2021.4.1	Modified cpu-pkgc-dbg to report more detailed package C-state blocking reasons on Intel platform code named Alder Lake. Improved tool stability.
February, 2022	2022.1	Added external support for Intel platform code named Alder Lake and Intel® Arc Discrete Graphics Card . Added support for more Meteor Lake features (cpu-pkgc-dbg, PCH metrics) and initial support for Lunar Lake. Added NDA support for display-state. Bug fixes, including handling when VTIO is enabled.
April, 2022	2022.2	Added support for additional Meteor Lake features (from Intel PMT). Bug fixes including correctness issues in Intel platform code named Alder Lake feature cpu-pkgc-dbg and PCH metrics.
June, 2022	2022.3	Added support for additional Meteor Lake features. Added support for Intel® Arc Discrete Graphics Card 256 EU.

Date	Revision	Description
		Bug fixes including fix for collecting feature panel-srr irrespective of PSR flag status at initial collection time.
August, 2022	2022.4	Multiple bug fixes including correctness issues in Meteor Lake features.
September, 2022	2022.5	Enabled support for hgs-feedback for Meteor Lake, Raptor Lake and Alder Lake. Bug fixes including data correctness in Intel PMT based residency metrics.
November, 2022	2022.6	Report complete topology path on hybrid systems. Added support for IOE DIE features in Meteor Lake. Added support for PCH features in Meteor Lake -S. Bug fixes for data correctness.
January, 2023	2023.0	Deprecation of Google Analytics support. Added support for Intel server platform code named Emerald Rapids server. Added support for Intel platform code named Lunar Lake and additional metrics support (new PCH and Intel PMT metrics) for Intel platform code named Meteor Lake. Added (NDA) PCH and CDie (from Intel PMT) metrics support for Intel platform code named Meteor Lake. Bug fixes for data correctness.
February, 2023	2023.1	Added (NDA) PCH and Intel PMT metrics support for Intel platform code named Meteor Lake (B-step). Bug fixes for data correctness.
April, 2023	2023.2	Added external support for Intel platform code named Raptor Lake. Added external support for Intel server platform code named Sapphire Rapids -Xeon. Added support for Intel platform code named Arrow Lake. Added support for limited Intel PMT metrics on Intel platform code named Lunar Lake. Added support for Intel discrete graphics card named Alchemist Refresh. Added PCIe metrics support on Intel platform code named Meteor Lake -S. Added support for external PCH metrics on Intel platform code named Meteor Lake -S. Fixed issues in PCH metrics on Intel platform code named Meteor Lake. Bug fixes including BSOD on systems with integrated graphics disabled when running igfx features. .
June, 2023	2023.3	Added NDA support for Intel server platforms code named Emerald Rapids -Xeon and Granite Rapids -Xeon. Added additional features support for Intel platform code named Lunar Lake (from PMT and PCH). Added tcss feature support for Intel platform code named Meteor Lake. Bug fixes including issues in vpu-bw, vpu-dstate-res, pch-ip-active, s0ix-subs-* features, sata-lpm.

Date	Revision	Description
August, 2023	2023.4	Added support for Intel Platform code named Arrow Lake H (6+8) and Intel discrete graphics card code named Battlemage. Deprecated support for pch-ip-status and sa-freq from MTL onwards. Additional features support for Intel platform code named Lunar Lake. Bug fixes including BSOD when VTIO is enabled, issues in s0ix-subs-* features, etc. Notification about limiting the scope of certain group features including sys in future release.
August, 2023	2023.4.1	Added limited NDA support for Intel platform code named Lunar Lake. Fixed Intel PMT XML configuration file issue in Intel platform code named Lunar Lake. Bug fixes.
September, 2023	2023.4.2	Fixed an issue NDA only to avoid BSOD on Intel platform code named Lunar Lake.
October, 2023	2023.5	Change in scope for certain group features including -f sys. Added support for Intel platform code named Panther Lake. Updated Intel Vision Processing Unit (VPU) nomenclature to Intel Neural Processing Unit (NPU). Bug fixes
November, 2023	2023.6	Added external support for Intel server platform code named Emerald Rapids-Xeon. Added NDA support for Intel platform code named Arrow Lake and Intel server platform code named Sierra Forest-Xeon. Additional feature support for Intel platform code named Lunar Lake. Bug Fixes
December, 2023	2023.7	Enhanced wakeup analysis histogram report Additional features support for Intel platforms code named Lunar Lake and Arrow Lake. Bug fixes including summary report not generated for longer duration collections, data correctness in telemetry features for Intel platform code named Lunar Lake.
January, 2024	2024.0	Enabled (external) additional features support on Intel platform code named Meteor Lake. Enabled (NDA) additional features support on Intel platforms code named Meteor Lake -S, Arrow Lake -S and Lunar Lake. Enabled limited support for Intel platform code named Wildcat Lake. Enabled limited support for Intel server platform code named Diamond Rapids. Bug Fixes including reporting an error message when Intel discrete graphics card is in D3.
February, 2024	2024.1	Enabled s0ix-subs-res support on Intel platform code named Panther Lake -P/-H.

Date	Revision	Description
		Bug fixes including data correctness issues in NPU features on Intel platform code named Lunar Lake and Intel discrete graphics card named Battlemage.
April, 2024	2024.2	Added a text disclaimer about validation for early access platforms. Enabled additional PCD features support for Intel Platform code named Panther Lake -P/-H. Introduced new feature switch tcss-state-res for Intel Platform code named Meteor Lake onwards. Added warning to users for using deprecated or older telemetry GUIDs. Deprecation of support for older atom based features. Bug Fixes
May, 2024	2024.3	Enabled support for Intel platform code named Arrow Lake U. Enabled external support for Intel discrete graphics code named Ponte Vecchio. Enabled limited support for Intel server platform code named Clearwater Forest. Added support for latest telemetry GUIDs on Intel platforms code named Arrow Lake and Lunar Lake. Enabled additional PCD features support on Intel platform code named Panther Lake -H/-P. Bug Fixes
July, 2024	2024.4	Enabled limited support for Intel platform code named Nova Lake. Enabled support for Intel platform code named Arrow Lake S B0 stepping. Enabled Intel PMT based and PCD based features on Intel platform code named Panther Lake. Removed support for option pch-lvl from the feature pch-ip-active. Bug fixes including data correctness issue in the feature sata-lpm.
July, 2024	2024.5	Enabled limited support for Intel discrete graphics card named Battlemage G31. Removed support for Intel discrete graphics card named Battlemage G10. Added NDA support for Intel ARC discrete graphics card [320EU and 288EU] (Intel discrete graphic card code named Battlemage G21) .
September, 2024	2024.6	Added external support to Intel platforms code named Elkhart Lake, Arrow Lake and Lunar Lake. Added limited NDA support for Intel platform code named Panther Lake. Added additional features to Intel platform code named Panther Lake. Enhanced the feature s0ix-subs-dbg in Intel platform code named Panther Lake to support B/D/F of the reported components. Bug Fixes
October, 2024	2024.7	Enabled support for the latest OOBMSM telemetry GUID on Intel ARC discrete graphics card [320EU and 288EU] (Intel discrete graphics card code named Battlemage G21)

Date	Revision	Description
		Additional features external support on Intel Platform code named Lunar Lake Added support for option --result-slice-range. Enhanced summary report to include S0ix LPM capability of the system. Bug Fixes
November, 2024	2024.8	Bug Fixes
December, 2024	2024.9	Enabled additional features on Intel platforms code named Panther Lake -H, Wildcat Lake and Nova Lake. Added NDA support for feature s0ix-subs-dbg on Intel platform code named Panther Lake -P. Bug Fixes.
January, 2025	2025.0	Enabled additional features support on Intel platform code named Wildcat Lake. Added NDA support for feature cpu-pkgc-cfg on Intel platforms code named Meteor Lake onwards. Added support for latest telemetry GUIDs on Intel platform code named Arrow Lake. Bug fixes including an issue with the help output.
February, 2025	2025.1	Enabled external support for Intel® Arc™ B-series graphics. Enabled external support for the feature memss-pstate on Intel platform code named Lunar Lake. Enabled additional features NDA support on Intel platform code named Panther Lake. The support includes Intel PMT based features. Bug fixes
April, 2025	2025.2	Added external support for Intel server platforms code named Granite Rapids and Sierra Forest. Enabled additional features support on Intel platform code named Nova Lake and Intel server platform code named Diamond Rapids. Enabled limited support for Intel platform code named Bartlett Lake which is a derivative of Intel platform code named Raptor Lake. Bug fixes including issues in TCSS, s0ix-subs-dbg features.
April, 2025	2025.3	Added support for latest Pcode telemetry GUID on Intel support for Intel® Arc™ B-series graphics. Enabled support for Intel discrete graphics card named Battlemage G31.
May, 2025	2025.4	Added support for latest Pcode telemetry GUID on Intel support for Intel® Arc™ B-series graphics. Added support for latest Pcode telemetry GUID for Intel discrete graphics card named Battlemage G31. Enabled additional features support for Intel platforms code named Wildcat Lake and Nova Lake. Bug fixes including refining pcie-ltr feature.

Date	Revision	Description
July, 2025	2025.5	Enabled additional features support (including Intel PMT based features) on Intel platform code named Nova Lake. Enabled additional features NDA support for Intel platform code named Panther Lake PCD P. Enabled NDA support for Intel platforms code named Panther Lake PCD H and Wildcat Lake. Re enabled support for PCIe based features on Windows OS 26100 or higher when Enhanced security is turned on. Bug fixes.
August, 2025	2025.5.1	Removed support for PCIe features when VTIO is enabled to avoid system BSOD.
September, 2025	2025.6	Improved the topology report for hybrid platforms including core type. Enabled NDA support for Intel discrete graphics card code named Battlemage G31. Enabled NDA support for Intel PMT based features on Intel platform code named Wildcat Lake. Enabled PCH based features support on Intel server platform code named Granite Rapids Workstation. Bug fixes.
October, 2025	2025.7	Added support for additional PCH / PCD features on Intel platform code named Nova Lake -H/-S. Enabled external support for Intel platform code named Panther Lake. Bug Fixes.

Customer Support

For technical support, visit the internal SoC Watch Users Group on Yammer: https://engage.cloud.microsoft/main/org/intel.com/groups/eyJfdHlwZSI6Ikdyb3VwIiwiaWQiOiIzNTI5MzUxMTY4MCJ9/all

1 Introduction

Intel® SoC Watch is a data collector for power-related data that can help identify issues on a platform that prevent entry to power-saving states. Captured metrics include:

- System sleep states
- CPU and GPU sleep states
- Processor frequencies
- Temperature data
- Device sleep states
- IO controller link states and latency reporting
- Platform Controller Hub activity

You can correlate the collected data and visualize over time using Intel®VTune Profiler.

This document provides system requirements, installation instructions, issues and limitations, and legal information.

To learn more about this product, see:

- New features listed in the New in This Release section below, or in the help.
- Reference documentation listed in the Related Documentation section below
- Installation instructions can be found in the Installation Notes section below.
- For a detailed quick start guide to running the tool, see the *Intel SoC Watch User's Guide* in your installed documentation.

Optimization Notice
Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice. Notice revision #20110804

New in This Release

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The 2025.7 release (*socwatch* driver v2.20.3, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled external support for Intel platform code named Panther Lake. *0cff599*
- Enabled support for pch-ip-active and pcd-ip-active features on the Intel platform code named Nova Lake -H/-S. Starting from Nova Lake platform, the `--option pch-count-always` has been removed because the energy reporting counters now increment by default regardless of the system package states. *920ea88, a3cf3c1*
- Enabled support for features pcd-pcieg5-ip-active and pch-pcieg5-ip-active on Intel platform code named Nova Lake -H/-S.*f2f0962*
- Enabled support for pcd-dmi-ip-active feature on Intel platform code named Nova Lake -S. This feature reports activity of DMI components.*f2f0962*

3 System Requirements

Supported Architectures

Intel SoC Watch supports these Intel® microarchitecture or platform code names:

- Elkhart Lake
- Jasper Lake Plus
- Sky lake
- Kaby Lake
- Cannon Lake
- Coffee Lake
- Whiskey Lake
- Amber Lake
- Comet Lake
- Ice Lake
- Lakefield
- Tiger Lake
- Rocket Lake
- Alder Lake
- Raptor Lake
- Meteor Lake
- Lunar Lake
- Arrow Lake
- Granite Rapids-Xeon
- Sierra Forest
- Emerald Rapids
- Panther Lake
- Wildcat Lake
- Nova Lake
- Bartlett Lake
- Skylake-Xeon
- Cascade Lake-Xeon
- Ice Lake-Xeon
- Sapphire Rapids-Xeon
- Spring Hill
- Cooper Lake-Xeon
- Diamond Rapids-Xeon
- Clear Water Forest

Intel SoC Watch supports these Intel® Discrete Graphics code names:

- DG1
- Intel® Arc™ A-series graphics
- Intel® Arc™ B-series graphics
- Arctic Sound Mainstream
- Arctic Sound Performance [untested on Windows* OS]
- Ponte Vecchio
- Alchemist Refresh
- Battlemage G31

Minimum System Requirements

You can run Intel SoC Watch on these 64-bit operating systems with administrator permissions:

- Windows* 10 (desktop)
- Windows* 11

4 Where to Find the Release

Go to Intel Registration Center (https://registrationcenter.intel.com) to download the latest internal version of Intel SoC Watch for Windows*OS.

5 Installation Notes

Intel® SoC Watch for Windows* OS is available from the Intel Registration Center. Download the Internal Intel SoC Watch zip file and unzip in a folder of your choice.

Configure Intel SoC Watch for use by opening a command window and executing the following command:

```
set PATH=<install-dir>\socwatch\64;%PATH%
```

Prerequisites for Intel® Platform Monitoring Technology (PMT) Metric Collection Using Intel SoC Watch

Ensure Intel Platform Monitoring Technology driver is loaded in the system to be able to collect Intel® PMT-based metrics from Intel Client platforms starting from Tiger Lake onwards.

If the Intel® PMT driver is not found in the system, for Platforms starting from Meteor Lake, the Intel® PMT driver is available as a part of Intel One BKC. The latest driver can be obtained from https://onebkc.intel.com/#/home. To troubleshoot any issues in the Intel® PMT driver please visit https://wiki.ith.intel.com/display/WOSEXT/Intel+PMT+Wiki and for any help, please reach out to winpmt@intel.com.

Installing WDTF to Enable --auto-connected-standby

Use of the `--auto-connected-standby` option requires the Windows* OS Driver Test Framework (WDTF) to be installed on the target system. WDTF is found in the Windows Driver Kit (WDK). Below are instructions.

1. Get the latest WDK from Microsoft https://docs.microsoft.com/en-us/windows-hardware/drivers/download-the-wdk. Follow only the instructions for installing the WDK.
2. After installing the WDK, open an administrative command prompt in this folder: *C:\Program Files (x86)\Windows Kits\10\Testing\Runtimes*
3. Enter the following command to install WDTF:

```
msiexec /i "Windows Driver Testing Framework (WDTF) Runtime
Libraries-x64_en-us.msi" /l* WDTFInstall.log WDTFDir=c:\wdtf
WDTF_SKIP_MACHINE_CONFIG=1
```

Prerequisite for running collections with connected-standby

To run connected-standby tests ensure the OS has test signing mode enabled. Refer to https://learn.microsoft.com/en-us/windows-hardware/drivers/install/the-testsigning-boot-configuration-option for instructions on enabling test mode on Windows OS.

Default Installation Folders

Install standalone version:

When you install the standalone version of Intel® SoC Watch, the default installation folder is the location where the package was unzipped.

6 Fixed Issues

Release 2025.7 has a fix for these issues:

- Re enabled the support of features pcie-ltr and pcie-lpm when Enhanced Sign-In Security (a.k.a., Virtualized Trusted IO or VTIO) is enabled on the system. However this support is only available on Windows build 26100 or after. *b2319aa*
- Fixed an issue in the pcie-lpm and pcie-ltr features where devices were not being detected correctly on the Intel platform code named Nova Lake. *23ebe87*
- Fixed an issue on Intel platform code named Panther Lake, where an incorrect message was reported stating no graphics device was present when one was actually present. *63154c1*
- Enabled the support to report CD ROM devices and their activity in the feature sata-lpm. *63154c1*
- Fixed a data correctness issue in the feature sxix-subs-res on Intel platform code named Nova Lake. This feature now reports the sxix substates when system enters S3 or S4 state. *7a8287e*
- Fixed a data correctness issue in the feature pch-slps0 on Intel platform code named Nova Lake -S. *e908451*

7 Known Issues

Bandwidth

- The presence of EDRAM on a system may not be detected by Intel SoC Watch. This is known to occur when the accelerator card VCA2, which contains EDRAM, is present.
- Total DDR bandwidth does not include EDRAM. On systems using EDRAM, the `ddr-bw` feature report may have a discrepancy between the total data reads and writes and the total component requests. The Data Reads+Data Writes will be significantly higher than the total IA+GT+IO requests, because the EDRAM requests are not included. There is no software access to a counter for the traffic between EDRAM and DDR currently.

PCH Active, SlpS0, and other PCH Metrics

- The pch-ip-active feature requires Energy Reporting (ER) to be enabled. In early silicon, ER might not be turned on by default. This affects the tcss, io-bw, and saf-ip-active features as well. If you need to collect this information, enable ER manually in the BIOS.
- The Chassis 2.2 C2p2 counters have a bug on the Intel platforms code named Lunar Lake and Meteor Lake.
- The s0ix-subs-dbg feature is not fully validated, and the s0ix-subs-status feature is not validated on the Intel platform code named Lunar Lake.
- Prior collections of the feature pch-ip-active cannot be re-processed using Intel SoC Watch v2024.4 with -i option. Fixes have introduced incompatible format changes. Use an older version of SoC Watch to re-process older collections.
- Feature pch-ip-active counter for SCS-eMMC does not increment (always shows 0) on Intel platform code named Jasper Lake. This is a hardware issue that will not be fixed.
- The -f pch-ip-active reporting of time in hibernation (shown as Unknown) may be up to 10 seconds greater than the actual hibernation time reported at the top of the summary report. This occurs because we don't have samples precisely at hibernation entry/exit. Rather, we have the last sample taken before a request to enter hibernation and after returning from hibernation. Because there is time other than hibernation, we label the time Unknown. Most metrics are collected at 100ms intervals, so the time for Unknown in these is very close to the time reported at the top of the summary which is based on the time of hibernation entry and exit events. But for pch-ip-active, we have a long delay (5 seconds) between samples to avoid keeping the system awake. This can result in a much more noticeable time difference between its time in Unknown compared to the report hibernation time. The last sample might precede the hibernate by 5 seconds and follow hibernate by as much as 5 seconds, resulting in as much as a 10 second difference.
- Issues on Intel platform controller hub (PCH) code named Ice Lake PCH-LP:
  - Feature pch-ip-active report for Physical Mode Lane function and rate assignment is incorrect, showing all lanes assigned to function PCIe/DMI and rate PCIe G1. The hardware register containing that information is not being set resulting in all 0's, which map to those values.
  - Feature pch-ip-active reporting is incorrect for Ungated ISH SRAM. The status is not being set making it appear to be always on and never power-gated (value reported is always 20). (https://hsdes.intel.com/resource/1506770789)

PCIe, XHCI, SATA, LPSS

- The pcie-lpm feature’s Root Port vs CLKREQ Mapping table is incorrect on all latest platforms starting from Intel platform code named Meteor Lake. Do not use this table for any analysis. Investigation to fix this issue is in progress.

- Higher PC2R residency is seen when the collections include -f pcie features. This happens because these features collect a lot of information about LPM and LTR devices, which can prevent these devices from entering the D3 state..
- Re-processing xhci-lpm or sata-lpm data collections obtained with prior versions of Intel SoC Watch using v2021.4 (or newer) with the -i option will not produce result files. This is due to format changes introduced by recent fixes, resulting in incompatibility. To re-process older collections, use the corresponding older version of SoC Watch.
- The features pcie-lpm and pcie-ltr reports may include "Unknown Device" or "Unknown End Point" in the device names list. These may be devices or end points with nothing attached.In such cases, you should ignore the data reported for them.
- Root Port vs CLKREQ Mapping not available on some Intel platforms code named Coffee Lake. The -f pcie-lpm feature's Root Port vs CLKREQ Mapping information has been hidden by hardware on some platforms. In this case, all values read are invalid so the following message is reported: Root Port vs CLKREQ Mapping is not available on this platform (0xFFFFFFFF values read by all the counters). There is no workaround for this issue.
- CLKREQ Mapping does not recognize disabled port. The –f pcie-lpm feature’s Root Port vs CLKREQ Mapping table does not recognize disabled ports resulting in CLKREQ # 0 being shown for disabled ports.
- It has been observed that SATA does not enter DevSleep when the in-box ACHI driver of the window is configured for HIPM only. If Intel® Rapid Storage Technology (Intel® RST) driver is used, which is configured to use HIPM+DIPM, entry to DevSleep does occur. If ACHI driver is configured for HIPM+DIPM, entry to DevSleep can be achieved.
- GbE device controller link state names are shown as PCIe link states in the PCIe LPM report for -f pcie-lpm, which includes GbE device controllers. The GbE link state K0 is listed as L0, and K1 as L1 in that report.
- Feature -f xhci-lpm will report a "no device attached" error message when the actual problem is that either the XHCI host controller or XHCI device driver does not provide the information needed to discover the device.
- Feature lpss-ltr is disabled on Intel platforms code named Cannon Lake, and Ice Lake, and newer. Registers for this data are not documented for platforms after Intel platforms code named Kaby Lake.
- Intel SoC Watch collection can prevent SATA devices from entering DevSlp. This occurs because Intel SoC Watch accesses the disk periodically to store the collected data, which can prevent the device from entering DevSlp. As a workaround, run Intel SoC Watch from a RAM disk to avoid disk access.

C-States / P-States

- On newer platforms starting from the Intel platform code named Tiger Lake, the Latency Response Time MSRs are not enabled in the BIOS. As a result, the cpu-pkgc-cfg feature will report 'No IRT' for all Pkg C-States in the CPU Package C-State Latency Summary table.
- On Intel platform code named Meteor Lake, features cpu-pkgc-dbg-res and cpu-pkgc-dbg do not contain the table "Pkg C-state Entrance Count". Use feature –f cpu-pkg-cstate-cnt to collect package C-state entrance counts.
- On Intel platform code named Alder Lake, the hardware will stop reporting residency in the Core C7 C-state MSR for Atom cores, resulting in that counter always showing 0. The Atom Core C6 residency counter provides the total residency for C6+C7. The feature hw-cpu-cstate does not handle this change yet. To work around this issue, ignore the Atom Core C7 residency (CC7) and use CC6 to represent CC6+CC7. In a future release, SoC Watch will support different handling for Atom cores and then reflect this change in its Core CPU C-state report.
- On Intel platforms code named Alder Lake, the Intel Atom® Cores over-count residency in the Core C-state C6. The C6 counter does not stop counting when the C7 state is entered. This results in the -f hw-cpu-cstate Core C-state reporting (for Intel Atom® Cores only) to give incorrect data for both CC0+CC1 and CC6 if that Core has CC7 residency. To manually correct the report: CC6 = CC6 - CC7, and (CC0+CC1) = (CC0+CC1) + CC7.

- Prior to Intel SoC Watch v2020.5, feature -f hw-cpu-pstate reported time in P0 (turbo) states when turbo was disabled. This issue occurred on platforms where SoC Watch printed a warning about inaccurate P-state reporting. The problem was fixed by modifying -f hw-cpu-pstate to report P-states per thread rather than per core.
- The RC6 residency reported by -f hw-gfx-cstate is reporting higher than actual time in RC6 state when entering PC2 or greater package C-state on Intel platforms code named Alder Lake and Jasper Lake Plus. This causes RC0 time to be incorrect as well. A firmware fix is required to correct this issue. (HSD #16011606938, 16010900499).
- When collecting feature `-f hw-igfx-cstate` on Intel platforms code named Tiger Lake, the RC6 residency counters have been seen to report unreasonable data as detected by comparing the residency time to the sample duration. When this variance exceeds 2%, a warning is displayed with the Graphics C-state Summary Residency report and the reported data is suspect.
- When collecting a trace of residency data from hardware counters (i.e., using -m), the summarized residency data could be 2-3% inaccurate due to error propagation in the accumulation of each sample's calculated residency. Collecting without -m results in greater accuracy because only a single sample is taken. However, long collection duration could result in a counter rollover, and that will not be detected without the use of -m.

Discrete Graphics

- In Intel ARC discrete graphics card [320EU and 288EU] (Intel discrete graphic card code named Battlemage G21), residency values when collected with "-m" is incorrect. We suspect the issue is due to the frequency of incrementing counter.
- In Intel ARC discrete graphics card [320EU and 288EU] (Intel discrete graphic card code named Battlemage G21), residency reported will be inaccurate when the device goes into D3. Currently there is no way of determining the D3 state via telemetry.
- If a feature includes counters from multiple telemetry GUIDs and one of the telemetry block GUIDs is unloaded or missing, the entire feature will not be collectible. In such cases, you will be notified, and an empty report will be generated.
- The dgfx features for bandwidth and temperature are not reporting correct values when using certain firmware. On DG2, they may report only 0 values. These counters have been temporarily disabled in firmware for Intel discrete graphic cards code named DG2 (128EU A-step, 512EU B-step/C-step). Reading the counters interfered with C-state entry. This will be fixed in firmware but the version was not known at the time of this release. To resolve this issue, please try latest firmware versions when available.

S States & D States

- The ACPI dstate feature sometimes shows D3Hot for certain devices when it should display D3Cold. To work around this issue, cross-reference the metric with the -f pcie-lpm metric. To be certain of the state of a device, check the PCIe LPM Summary table (-f pcie-lpm). If the link is in the L2/L3/Down state, the device is in D3Cold. If the link is in the L1.1/L1.2 state, the device is in D3Hot.
- Occasional missing reports for acpi-dstate , os-cpu-cstate and other OS/ACPI metrics which are based on OS event trace data. This issue occurs when there are insufficient OS event trace sessions available to Intel SoC Watch when a collection was started. The Windows* 10 OS released in 2020 has increased the number of event trace sessions it is using, thereby reducing the number available to other processes like SoC Watch. Win10 OS 21H1 build 20170 reduces the number of sessions it uses, which will reduce the frequency this issue will occur. SoC Watch v2020.3.2 displays the following error messages when this issue is detected: *Warning: Cannot enable ETW provider in the trace file XXXX_extraSession.etl. Insufficient system resources exist to complete the requested service. Warning: Failed to start EtlCollector.* To resolve the problem, Event Trace Sessions must be made available either by trying again to see if other processes have closed their sessions, or running Windows Performance Monitor to view the Data Collector Sets/Event Trace Sessions that are running and stopping one of them. (Note that AgaveBootTrace is needed by Intel's Powerhouse Mountain tool.)

Intel® PMT metrics

- An issue related to data correctness has been identified in the npu-pstate feature on Intel platform code named Lunar Lake. The root cause lies in the utilization of a distinct clock ratio by the NPU firmware. Unfortunately, this information is abstracted to the pcode, resulting in data inaccuracies.
- Data correctness issue is noticed in the feature display-pstate in Intel platform code named Meteor Lake where the cdclk frequency is not rightly reported by pcode.
- Due to Intel confidentiality, the Package C sub states information on Intel platform code named Lunar Lake is not exposed to NDA. If you are an Intel engineer supporting NDA customers, please obtain the Internal vs. NDA mapping for Package C debug purposes from the Intel SoC Watch team.
- Approximately 2-5% difference in Package C state is noticed between the Intel PMT feature cpu-pkg-cstate-res and MSR based feature hw-cpu-cstate on Intel platform code named Lunar Lake. This discrepancy occurs because the pcode does not report the pkg C exit latency time in telemetry SRAM for PC6 and PC10. Only the substate residencies are reported.
- With Async calls made to the Intel PMT driver, we noticed a discrepancy between the number of counters in the HAS and the size of the telemetry region defined in the PMT driver on Intel platform code named Meteor Lake.

  Certain counters such as LLC_FLUSHED_RESIDENCY (supported in the feature cdie-llc-flushed-res), PKGC_BLCK_MODE_DEMOTE_CAUSE_PCU_NOT_DRAINED and PKGC_BLCK_MODE_DEMOTE_CAUSE_SB_BRIDGE_NOT_BLOCKED (supported in the feature cpu-pkgc-dbg) are not present in the telemetry space. We have removed support for these counters because we suspect that we were previously reading incorrect values for them.
- The package C-State reported through the Intel PMT feature cpu-pkg-cstate-res for Intel platform code named Meteor Lake reports incorrect data when -m is used in the command line. The issue is a firmware bug. Collect hw-cpu-cstate for accurate data.
- The feature memss-pstate returns 0 when SAGV is disabled on Intel platforms code named Meteor Lake and Arrow Lake due to a Punit RTL bug that will not be fixed in these platforms.HSD #22018530289
- The feature mem-state on Intel platform code named Meteor Lake is reporting abnormal values. This is due to a counter enabling bit not set by firmware. Work is in progress to fix this issue.HSD #14020078802, #14020079710
- The feature vpu-dstate-res has been adjusted to calculate residencies after accumulating counter values read throughout collection. The inferred state is calculated using these accumulated values. The trace file will only have the accumulated data reported. And since the counters are updated with a delay by firmware, there is potential for slight inaccuracy in residency data. Data samples are acquired periodically (order of 10s of milliseconds). If the intended workload used for measurements is too short in total duration, the data might be missed by the collecting software. Please use workloads of sufficient duration for accurate detection.
- On Intel platform code named Meteor Lake, below SOCN counters have not been implemented:

  - GT_ENGINE_BUSY_RESIDENCY
  - GT_RC0_IDLE_RESIDENCY
  - DISPLAY_IO_READ_BANDWIDTH
  - DISPLAY_IO_WRITE_BANDWIDTH
  - DISPLAY_VC1_BANDWIDTH
  - RC6_ENTRY_OVERHEAD
  - RC6_WAKE_OVERHEAD

  As a result of this, below SoC Watch features were disabled to avoid reporting incorrect data:

  - display-bw
  - display-vc1-bw
  - igfx-busy
  - igfx-rc0-idle
  - igfx-rc6-entry-ovhd
  - igfx-rc6-wake-ovhd

- On Intel platform code named Meteor Lake, "PROCHOT_COUNTER" has not been implemented for Compute Die (CDie). As a result of this, this counter will not be captured by the feature cdie-perf-limit-rsn-cnt.
- For feature cdie-perf-limit-rsn-res, there is a transition counter, but no residency counter for LLC_POWER. And, for feature soc-perf-limit-rsn-cnt, there is a residency counter, but no transition counter for IPU_THERM. These are omissions in the MTL telemetry HAS and not with SoC Watch.
- On some platforms all Intel PMT-based features are shown as Unknown. This occurs when the Intel PMT device driver is not loaded or when the Intel PMT discovery data is incorrect. To trouble shoot: Check if the Intel PMT driver (*intelPMT.sys*) is present. If present but not loaded, check if Intel PMT device 10 is enabled in BIOS: Boot to BIOS and enable this bit (menu names may vary slightly for different BIOS): *Intel Advanced -> System Agent -> Device CrashLog (device 10) -> Enable*.
- On Alder Lake platforms, hidden feature -f pmt-cpu-pkgc-dbg data is unreliable after the first exit from S0ix (Modern Standby). If the system is rebooted the counters begin counting properly again until resuming from the S0ix occurrence.
- The feature soc-ltr requires C-step for Intel platform code named Alder Lake in order to collect non-zero LTR values. Even then, the TypeC LTR values may still report only 0.
- Intel PMT metrics (e.g., cpu-pkgc-dbg, io-bw, disp-bw, etc) may be reported as unsupported and not appear in help on Intel platform code named Alder Lake. This occurs when the Intel PMT driver required to access this data is not loaded on the target platform. *Note: Collection of these features requires driver intelPMT.sys which is available in Windows* OS Cobalt builds beginning with EEAP build #21318.* (Device Manager will show failure to load (yellow bang) Intel Platform Monitoring Technology Driver due to error introduced by microcode patch 0x15. Firmware version with fix is not known at the time of this release, see HSD's: 16012983281, 22012672089.)
- Collection of metrics from Intel PMT data are not supported on Alder Lake-S and Alder Lake-P A-step.

Telemetry GUID maintenance

Intel SoC Watch will only support the most recent telemetry firmware revision provided by the platform BKC in order to remain current and ensure optimal performance. This would mean that SoC Watch supports only the most recent PMT GUIDs that are supported on the BKC. It is advised that users utilize the most recent tool version in conjunction with the newest telemetry revision.

However, certain users may need to continue operating with previous firmware versions. For these cases, it's suggested to collect telemetry data using the older versions of the tool. Be aware that using an outdated tool version may result in missing out on critical updates and enhancements.

Miscellaneous

- Entering connected standby using the -z option is supported only on Windows 11 with WDTF version 10.0.26100.0 installed, due to Microsoft's requirements. For older Windows OS versions, use an older version of the tool.
- Older collections of the feature s0ix-subs-res cannot be reprocessed with Intel SoC Watch v2024.0 or newer. This was due to code enhancement which affects the backward compatibility.
- When a low sampling interval (for example 1ms) is provided along with --polling, SoC Watch will poll as close to that interval as possible but the interval may not be exact. Recommended lowest sampling interval is 15ms. If the device goes into a sleep state during the collection, SoC Watch cannot run, and will only get samples when it wakes up, so the time between the device going to sleep and then waking up will be the sampling interval.
- The CPU usage percentage in SoC Watch may differ slightly from what you see in Windows Performance Analyzer.
- Stress testing on ADL N with modern standby cycling (more than 100 cycles) is known to cause a hang. This issue is very random and not reproducible. The team is aware of this issue and we recommend not to run multiple MS cycling with SoC Watch.
- Feature hgs-feedback can be collected only on Windows 11 (build > 220000).

- If –f connected-standby was collected on a target platform with Intel SoC Watch v2021.2 or older, *cstracedrv.sys* must be removed before any collection using SoC Watch v2021.3 or newer. To remove *cstracedrv*, execute command `socwatch --disable-cstrace` then reboot the system. SoC Watch v2021.4 will display an error message and terminate if an incompatible *cstracedrv* driver is detected (this error will occur even if -f connected-standby is not specified in the command line). The *cstracedrv* driver enables feature -f connected-standby and was modified in SoC Watch v2021.3 making it incompatible with older versions of SoC Watch. The *cstracedrv* driver is automatically installed when feature -f connected-standby is executed for the first time on a platform (or when option `--enable-cstrace` is used prior to first use of -f connected-standby). Unlike the *socwatchdrv*, it remains installed at the end of collection and is reloaded after a reboot in order to capture complete information for connected standby reporting. The option `--disable-cstrace` is provided to stop the *cstracedrv* from being reloaded after every reboot, and must be followed by a reboot to complete the process before running the next *socwatch* collection command.

  NOTE On some systems (possibly due to OS version) a running older *cstracedrv* driver cannot be unregistered by a new *socwatch.exe* (i.e., use of option `--disable-cstrace` with the new version of *socwatch* on a *cstracedrv* installed by an older version of *socwatch*, will result in an error indicating that the driver cannot be stopped). If this occurs, a system crash (BSOD) will occur on reboot. To avoid the crash on reboot, you must manually delete the cstrace driver (*C:\Windows\System32\drivers\cstracedrv.sys*) and edit the registry *(regedit)* to delete its registry entry (*Computer\\HKEY_LOCAL_MACHINE\\SYSTEM\\CurrentControlSet\\Services\\cstracedrv*) before rebooting.

- Hibernation time will not be detected if Intel SoC Watch is unable to start the required event trace log. The time in hibernation will be incorrectly attributed to the inferred state, which is usually the active state (e.g. C0). The following warning message indicates this condition: *Warning: Cannot enable ETW provider in the trace file XXXX_extraSession.etl. Insufficient system resources exist to complete the requested service. Warning: Failed to start EtlCollector.* This occurs when there are insufficient ETW sessions available due to other process collecting event traces at the time Intel SoC Watch collection was started.
- When polling is specified, the time interval for some samples may occasionally be double the time specified by -n. This occurs when the system timer expires slightly before the full time interval has completed, which results in the time check for next sample to fail resulting in no sample being taken until the next timer expires.
- Intel SoC Watch may take a long time to return after the collection period has ended. This is due to a long post processing phase, that begins after collection duration has ended. The feature that adds the most time to this post-processing time is -f os-cpu-cstate (included in groups: cpu, cpu-cstate, cpu-os), especially when -m (--max-detail) is included. The os-cpu-cstate feature results in a large amount of event trace (ETL) data when collecting for long periods, and processing ETL data is time consuming. The use of the -m option with -f os-cpu-cstate causes generation of an additional Wakeup analysis report (_WakeupAnalysis.csv) which increases post-processing time even more. To reduce post-processing time, consider whether you need the OS data. All features that are prefixed with "os-" have a "hw-" counterpart feature name. The OS-based data provides residency based on when the OS requested C-state or P-state changes, whereas the hw-based data is time the hardware actually spent in the states. Therefore, you may not need to collect both types of data. If you require collecting the OS-based data for long periods you may want to use the --no-post-processing option during collection to postpone SoC Watch's data processing phase until after you have copied all the .etl files SoC Watch generated during collection to a system with higher-performance, then use the -i option to generate summary and trace files more quickly. See Intel SoC Watch User's Guide for details on use of these options.
- If collecting a large number of metrics and requesting multiple types of results files to be generated on the same command line, Intel SoC Watch may report the following, *Warning: Could not post process metric data: Too many open file handles. Results may be incomplete for some metrics. Try post processing results with only one -r option at a time. If the problem persists; try collecting fewer metrics.* There will be some missing reports in the results files that are generated if this occurs. The work around is

to specify only one -r file type at collection time or collect fewer metrics. After collection, use -i option with each of the remaining file types to generate the additional result files. This issue is also seen in server platforms with more cores.

- When using -z (--auto-connected-standby), the following failed message is displayed by WDTF, but can be ignored when followed by the enter /exit messages from WDTF as shown below:

  ```
  Loading Wex.Logger.dll from systemdata.cpp linep 922 failed.

  WDTF_SYSTEM : INFO : Attempt Entering Connected Standby At (hh:mm:ss): 13:4:35 ,
  Wake Time In Milliseconds: 20000

  WDTF_SYSTEM : INFO : Exiting Connected Standby. Elapsed time (hh:mm:ss): 0:0:20
  ```
- On platforms with HyperV enabled, the sum of the CPU C-state idle residencies will not match CPU P-state idle residency time. The issue occurs because HyperV does not allow setting of the anythread bit, resulting in incorrect core-level reporting of both C-state and P-states.
- Metrics report Unknown 0 when `-m` is not used and hibernation occurs. Metrics with a snapshot default collection mode, such as CPU C-state, will show the Unknown state with 0 time and the remaining states will not sum to the total collection duration if the system entered hibernation during the collection and the `-m` option was not specified. The snapshot metrics are only collected at the start and end of a collection by default, but finding hibernation time requires samples taken throughout the collection. Including `-m` will cause continuous sampling to occur for all metrics. When hibernation occurs, a message reporting time spent in hibernation appears at the beginning of the summary report. The Unknown state is then included for all appropriate metrics and the time in hibernation is included in that state. Refer to the *Intel SoC Watch User's Guide* "Options Quick Reference" section to learn which metrics have a snapshot collection mode by default.
- Package level power data (-f pkg-pwr) is reported incorrectly for Cascade Lake-Xeon (AP) which has multiple Die in the CPU package. Intel SoC Watch labels the power as per package but it is actually per Die. There is no package level power.
- Syntax errors in the command line may not report a visible error message. If a collection did not run and you are not seeing any error message, add option `-d 2` to your command line to get more information.
- Insufficient system resources error seen on occasion when collecting OS event trace metrics such as `acpi-dstate`. The system error "WARNING: Cannot enable provider in the trace file <etl filename>" has been reported when collecting metrics that enable event trace logging. This error prevents ETL logging from being started and is usually caused by a background process consuming system resources. Use Task Manager to find and remove such processes then try the collection again.
- Devices that are added/removed after cstracedrv has been started will be unknown to the tool. If devices are added or removed after the first use of `-f connected-standby` or `--enable-cstrace`, the connected-standby reporting will not take that device into account. Workaround: use `--disable-cstrace` to uninstall the cstracedrv, reboot, then re-install the driver for it to see the change in devices.
- Hyper-V and Virtualization-based Security (VBS) prevent some metrics from being collected. Intel SoC Watch detects when Hyper-V and Virtualization-based Security is enabled on the platform, reports a warning message on the console and disables metrics that are blocked by these settings. When Hyper-V and VBS are enabled `cpu-gpu-concurrency` cannot be collected. On Intel platforms code named Ice Lake, `edram-state` and `comp-max-temp` metrics cannot be collected as well.
- If a command window is closed (using either the X button or Alt-F4) while the socwatch process is running, or the Task Manager is used to kill the socwatch process, then the behavior of a subsequent run of Intel SoC Watch becomes unknown. The proper way to terminate Intel SoC Watch is using Ctrl-C. A collection driver may be left in an undefined state when Intel SoC Watch is abruptly terminated because there is no OS event to allow proper cleanup. This can cause the next Intel SoC Watch collection to result in anything from bad data to a system crash. If a driver is left running, it must be removed. You can reboot the system to clear a driver or use the following set of commands to check if the driver is running, stop it, and then delete it:`sc query socwatchdrv; sc stop socwatchdrv; sc delete socwatchdrv`.

Intel® VTune™ Profiler Visualization

- Feature -f s0ix-subs-req generates a static table that cannot be visualized in Intel® VTune™ Profiler. Its data is excluded when generating the import file (-r vtune).
- TypeC Subsystem metrics reported by -f tcss-state cannot be imported into Intel® VTune™ Profiler. These results are currently excluded by -r vtune when generating the import file. They were causing a crash in VTune.
- Importing a collection that includes feature –f dgfx-pwr to Intel® VTune™ Profiler may fail with "Database interface, Precompute error". This issue was first seen with Intel® VTune™ Profiler v2020 Update 3.
- When using Intel® VTune™ Profiler to view ddr-bw data collected by Intel SoC Watch, the Intel VTune Profiler summary report may not match the SoC Watch summary report. If this occurs, the SoC Watch summary results are correct. This issue has been seen on platforms prior to Intel platform code named Tiger Lake.
- The Intel VTune Profiler System Summary does not report the rated frequency for the CPU when viewing results from data collected by Intel SoC Watch, such as Throttling Analysis. Instead, it reports 1GHz which is the clock frequency used in the calculations for processing the SoC Watch data.
- Collections containing PCIe metrics (pcie-ltr, pcie-lpm) cannot be imported to Intel VTune Profiler. A corrupted .pwr file message will result if an import is attempted. The issue is under investigation.
- If the bandwidth is 0 Mb throughout the collection for a particular bandwidth type, Intel VTune Profiler will not show a timeline entry for it. The timeline is shown only if there is at least one non-zero value.
- In some cases, the summary CSV results produced by Intel SoC Watch can vary from the summary results shown by Intel VTune Profiler even though they represent the same collection. For example, the summary CSV file may report a specific cpu-pstate residency of 50.78% and Intel VTune Profiler may report the same cpu-pstate residency as 50.8%.
- Some metrics are not supported for visualization in Intel VTune Profiler. When `–r vtune` is specified, unsupported metrics will be excluded from the .pwr file. When this occurs, a message is printed to the console for each metric that was collected but not included in the .pwr file. The unsupported metric is `cpu-pkgc-dbg`. If there were no supported metrics in the collection, no .pwr file is created.
- In order to visualize graphics C-states that are reported as Render and Media, the table headers in the trace file (generated with option -r int), must be manually modified, adding *Render* and *Media* to the appropriate C0, C1, and C6 column headers.

8 Related Documentation

The release contains these documents:

- Intel® SoC Watch User Guide for Windows* OS

9 Previous Release Notes

Version 2025.6

New

The 2025.6 release (*socwatch* driver v2.20.3, *cstracedrv* driver v2.5.0) contains these changes:

- Improved the topology report of the hybrid systems. The summary report now provides information about the core type (P Core, E core, L/P core).*e48a075*
- Added NDA support for Intel discrete graphics card code named Battlemage G31. Support is enabled for the following features
  - dgfx-gt-perf-limit-rsn
  - dgfx-media-perf-limit-rsn
  - dgfx-vram-perf-limit-rsn
  - dgfx-vram-srr
  - dgfx-mods-res
  - dgfx-sgunit-dstate
  - dgfx-audio-dstate
  - dgfx-pcie-dstate
  - dgfx-pkg-cstate
  - dgfx-pcie-link-state
  - dgfx-afm-cstate
  - dgfx-display-ltr
  - dgfx-pkgc-dbg
  - dgfx-bw
  - dgfx-temp
  - dgfx-media-cstate
  - dgfx-gt-cstate

  999e82b
- Added limited NDA support for Intel platform code named Nova Lake S. Support enabled for the following features.
  - acpi-dstate
  - acpi-sstate
  - core-temp
  - cpu-igpu-concurrency
  - cpu-pkgc-cfg
  - ddr-bw
  - device-acpi-calls
  - display-state
  - hgs-feedback
  - hw-cpu-cstate
  - hw-cpu-hwp
  - hw-cpu-pstate
  - hw-igfx-pstate
  - ia-throt-rsn
  - igfx-throt-rsn
  - os-cpu-cstate
  - os-cpu-pstate
  - os-gfx-cstate

- panel-srr
- pkg-pwr
- pwr-limits
- ring-throt-rsn
- sata-lpm
- timer-resolution
- xhci-lpm

aef8652

- Added support for the following PCH based features on Intel server platform code named Granite Rapids Work Station.
  - pch-slps0
  - pch-ip-active
  - s0ix-subs-res
  - s0ix-subs-req
  - s0ix-subs-dbg
  - s0ix-subs-status
  - pch-platform-ltr

404001f

- Added NDA support for Intel PMT based features for Intel platform code named Wildcat Lake. The support is added for these features.
  - cluster-cstate-res
  - core-cstate-res
  - core-temp
  - cpu-pkgc-dbg
  - d2d-pstate
  - ddr-virtual-bw
  - display-pstate
  - display-vc1-bw
  - display-volt
  - gt-temp
  - hbo-bw
  - hw-igfx-cstate-cnt
  - hw-igfx-cstate-res
  - hw-igfx-pstate
  - igfx-volt
  - llc-temp
  - media-cstate-res
  - media-pstate
  - media-volt
  - mem-state
  - memss-pstate
  - memss-volt
  - mufasa-bw
  - noc-d2d-bw
  - noc-gt-bw
  - noc-io-bw
  - noc-pstate
  - noc-volt
  - npu-bw
  - npu-dstate-cnt
  - npu-dstate-res
  - npu-pstate

- npu-pwr
- npu-volt
- partial-slp-cnt
- partial-slp-res
- pl-limited-res
- psyspl-limited-res
- ring-pstate
- ring-volt
- santa-bw
- soc-perf-limit-rsn-cnt
- soc-temp

8bd28b9

- Added support for the following features on Intel platform code named Nova Lake. Refer to User Guide for metric description.
  - vr-temp
  - soc-temp
  - psys-temp
  - cdie-core-temp
  - ccf-temp
  - soc-perf-limit-rsn-cnt
  - soc-pl-limited-cnt
  - soc-psyspl-limited-cnt
  - hw-igfx-cstate-cnt
  - media-cstate-cnt
  - ipu-cstate-cnt
  - partial-slp-cnt
  - cdie-perf-limit-rsn-cnt
  - cdie-ring-cnt
  - cdie-hammer-throt-res
  - cdie-ring-res
  - cdie-perf-limit-rsn-res
  - pcd-s0ix-subs-dbg
  - pch-s0ix-subs-dbg
  - pcd-sxix-subs-res

  7202adb, 3beb10c, ee99ce6, 4ebf9d9, 2d93cd6

Fixed

Release 2025.6 has a fix for these issues:

- Fixed an issue that caused s0ix blocker counters to report over counting in certain extended collection scenarios on Intel platforms code named Panther Lake and Wildcat Lake. *2adf9d9*
- Fixed a data correctness issue in the feature panel-srr on Intel platform code named Panther Lake. For achieving accurate result use the option `--option display-wakelock` which will keep the display on to provide panel self refresh residency. However, this will keep the system from entering deeper display state (DC6).*999e82b*
- Updated the CNVi counter information in the feature pcd-ip-active which includes counter definition and removal reserved counters on Intel platform code named Wildcat Lake. *0a932f3*
- Fixed a data correctness issue in the feature io-bw on Intel platform code named Wildcat Lake. *0a932f3*

Version 2025.5

New

The 2025.5 release (*socwatch* driver v2.20.2, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled support for the following Intel PMT and PCH based features on Intel platform code named Nova Lake:
  -
    - cclk-pstate
    - cclk-volt
    - cdie-ccp-pstate
    - cdie-ccp-volt
    - cdie-cstate-cnt
    - cdie-cstate-dbg
    - cdie-cstate-res
    - cdie-ltr
    - cdie-llc-flushed-res
    - cdie-ring-pstate
    - cdie-ring-volt
    - cdie-vccia-pwr
    - cpu-pkg-cstate-cnt
    - cpu-pkg-cstate-res
    - cpu-pkgc-dbg
    - ddr-virtual-bw
    - display-pstate
    - display-volt
    - hbo-bw
    - hw-igfx-cstate-res
    - hw-igfx-pstate
    - idi-bw
    - igfx-volt
    - io-bw
    - ipu-cstate-res
    - ipu-pstate
    - ipu-volt
    - llc-bw
    - media-cstate-res
    - media-pstate
    - media-volt
    - mem-state
    - memss-pstate
    - memss-volt
    - mufasa-bw
    - noc-cdie-bw
    - noc-d2d-bw
    - noc-display-bw
    - noc-gt-bw
    - noc-ipu-bw
    - noc-media-bw
    - noc-ms-bw
    - noc-npu-bw
    - noc-pstate
    - noc-volt
    - npu-pwr
    - osreq-pkg-cstate-res
    - partial-slp-res
    - pch-s0ix-subs-res
    - pch-slps0
    - psys-pwr

  - santa-bw
  - soc-ccp-pstate
  - soc-ccp-volt
  - soc-hammer-throt-res
  - soc-ltr
  - soc-perf-limit-rsn-res
  - soc-psyspl-limited-res
  - soc-vccia-pwr
  - vccgt-pwr
  - vccecore-pwr
  - vccsa-pwr
  - vnnaon-pwr

  032a8b1, 0c71d6e, c006de8, 4150dbd, 3387ad6, 8c959af, 8fd3b37, eae4561, 2d9bbd9, 2e2922e, 96a10d9, 8886709
- Re enabled the support of features pcie-ltr, pcie-lpm and xhci-lpm when Enhanced Sign-In Security (a.k.a., Virtualized Trusted IO or VTIO) is enabled on the system. However this support is only available on Windows build 26100 or after. c24f3d0
- Enabled NDA support for the features pcieg5-ip-active, saf-ip-active on Intel platform code named Panther Lake PCD P. *c1ce856*
- Enabled NDA support for the feature hw-igfx-cstate-res (from Intel PMT) on Intel platform code named Panther Lake PCD P. *c1ce856*
- Enabled NDA support for the following features on Intel platform code named Panther Lake PCD H.
  - pcie-ltr
  - pcie-lpm
  - pcd-slps0
  - pcd-ip-active
  - pcd-platform-ltr
  - s0ix-subs-res
  - s0ix-subs-status
  - s0ix-subs-dbg
  - saf-ip-active
  - pcieg5-ip-active
  - tcss-state-res
  - tcss-state-cnt
  - tcss-state-dbg
  - tcss-ltr-cnt

  e77860b
- Added limited NDA support for Intel platform code named Wildcat Lake. This includes support for the following features:
  - acpi-dstate
  - acpi-sstate
  - connected-standby
  - core-temp
  - cpu-igpu-concurrency
  - ddr-bw
  - device-acpi-calls
  - display-rr
  - display-state
  - hgs-feedback
  - hw-cpu-cstate
  - hw-cpu-hwp
  - hw-cpu-pstate

- hw-igfx-cstate
- ia-throt-rsn
- igfx-throt-rsn
- os-cpu-cstate
- os-cpu-pstate
- os-gfx-cstate
- panel-srr
- pcd-ip-active
- pcd-slps0
- pcie-lpm
- pcie-ltr
- pkg-pwr
- pwr-limits
- ring-throt-rsn
- s0ix-subs-dbg
- s0ix-subs-status
- s0ix-subs-res
- saf-ip-active
- tcss-ltr-cnt
- tcss-state-cnt
- tcss-state-dbg
- tcss-state-res
- sata-lpm
- timer-resolution
- xhci-lpm

6e70fca

- Added s0ix LPM configuration to the summary report header for Intel platforms code named Panther Lake and Wildcat Lake. *25ef562*

Fixed

Release 2025.5 has a fix for these issues:

- Fixed a data correctness issue due to scale factor for the features partial-slp-res and Intel PMT based bandwidth features on Intel platforms code named Panther Lake and Wildcat Lake. *ce4f3cb*
- Fixed an issue which caused the feature s0ix-subs-res on Intel platform code named Wildcat Lake to return incorrect data due to reading wrong offsets. *087d1ba*

Version 2025.4

New

The 2025.4 release (*socwatch* driver v2.20.2, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled support for the latest Pcode telemetry GUID (0x1e2f8202) for Intel® Arc™ B-series graphics. This includes support for G7 state for the feature dgfx-pkg-cstate.*2923979*
- Enabled support for the latest Pcode telemetry GUID (0x1e2f8302) for Intel discrete graphics card code named Battlemage 31. This includes support for G7 state for the feature dgfx-pkg-cstate.*2923979*
- Enabled support for the following Intel PMT based features on Intel platform code named Wildcat Lake:
  - cluster-cstate-cnt
  - cluster-cstate-res
  - core-cstate-res
  - cpu-pkg-cstate-cnt
  - cpu-pkg-cstate-res
  - cpu-pkgc-dbg
  - d2d-pstate

  - ddr-virtual-bw
  - display-pstate
  - display-vc1-bw
  - display-volt
  - gt-temp
  - hbo-bw
  - hw-igfx-cstate-res
  - hw-igfx-cstate-cnt
  - hw-igfx-pstate
  - idi-bw
  - igfx-volt
  - llc-temp
  - media-cstate-cnt
  - media-cstate-res
  - media-pstate
  - media-volt
  - mem-state
  - memss-pstate
  - memss-volt
  - mufasa-bw
  - noc-cce-bw
  - noc-d2d-bw
  - noc-gt-bw
  - noc-io-bw
  - noc-media-bw
  - noc-pstate
  - noc-volt
  - npu-bw
  - npu-dstate-cnt
  - npu-dstate-res
  - npu-pstate
  - npu-pwr
  - npu-volt
  - partial-slp-cnt
  - partial-slp-res
  - perf-limit-rsn
  - pl-limited-res
  - psys-pwr
  - psyspl-limited-res
  - ring-pstate
  - ring-volt
  - santa-bw
  - soc-ltr
  - soc-perf-limit-rsn-cnt
  - soc-pl-limited-cnt
  - soc-psyspl-limited-cnt
  - soc-temp
  - vccgt-pwr
  - vccia-pwr

  ea7fd87
- Added support for the following Intel PMT based features on Intel platform code named Nova Lake:
  - pcd-slps0
  - npu-dstate-res

- npu-dstate-cnt
- npu-bw
- npu-pwr
- noc-npu-bw
- npu-volt
- npu-pstate

ccadb33

- Added additional B/D/F information for the component REF-PLL for the feature s0ix-subs-dbg on Intel platform code named Panther Lake.*612fc37*
- Improved the -r json to support a format which users can import into Perfetto visualizer. Currently this option is hidden.*b676f06*

Fixed

Release 2025.4 has a fix for these issues:

- Refined pcie-ltr metric to report "Not Received" to the component LTR information when No LTR message is received from the device.*4993c02*
- Fixed a data correctness issue on tcss-state-res feature on Intel platform code named Panther Lake.*c9f063b*
- Disabled the feature hw-igfx-cstate on Intel platform code named Panther Lake due to a bug in the hardware counters and enabled the feature hw-igfx-cstate-res to report the residency values via Intel PMT.*68b8b8c*

Version 2025.3

New

The 2025.3 release (*socwatch* driver v2.20.1, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled support for the latest Pcode telemetry GUID (0x1e2f8201) for Intel® Arc™ B-series graphics.
- Enabled support for Intel discrete graphics card code named Battlemage 31. The support is added for rev 2 Pcode Telemetry GUID (0x1e2f8301) and rev16 Ocode Telemetry GUID (0x5e2f8311). Features supported include

  - dgfx-volt,
  - dgfx-current,
  - dgfx-pwr,
  - dgfx-gt-perf-limit-rsn,
  - dgfx-media-perf-limit-rsn,
  - dgfx-vram-perf-limit-rsn,
  - dgfx-vram-srr,
  - dgfx-mods-res,
  - dgfx-sgunit-dstate,
  - dgfx-audio-dstate,
  - dgfx-pcie-dstate ,
  - dgfx-pstate-status,
  - dgfx-pkg-cstate,
  - dgfx-pcie-link-state,
  - dgfx-afm-cstate,
  - dgfx-display-ltr,
  - dgfx-pkgc-dbg,
  - dgfx-bw,
  - dgfx-temp

  b11e308

Fixed

Release 2025.3 has a fix for these issues:

- This is a limited release for Intel® Arc™ B-series graphics support.

Version 2025.2

New

The 2025.2 release (*socwatch* driver v2.20.1, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled support for Intel platform code named Bartlett Lake. This is a derivative of Intel platform code named Raptor Lake and the platform will be identified as RPL. *822c2f4*
- Added support for features pkg-pwr and dram-pwr on Intel server platform code named Diamond Rapids. These are Intel PMT based features on this platform. *2dd96bd*
- Added external support for Intel server platforms code named Granite Rapids and Sierra Forest. *ba550ab*
- Enabled support for the features display-rr, display-state, panel-srr and hw-igfx-pstate features on Intel platform code named Nova Lake. *cb587ef*
- Added support for the feature pcd-s0ix-subs-res on Intel platform code named Nova Lake, including the 0x29787064 telemetry GUID for this Intel PMT-based feature. 678a363
- Reenabled support for CC1 state on hw-cpu-cstate feature on platforms starting from Intel platform code named Lunar Lake. *c5cea16*

Fixed

Release 2025.2 has a fix for these issues:

- The latest fixes have introduced incompatible format changes to the feature pcie-lpm. Use an older version of SoC Watch to reprocess older collections. *7ea1f1a*
- Updated the feature panel-srr to report correct states on Intel platforms code named Lunar Lake and Panther Lake. *46dc517*
- Fixed an issue that affected the collection of feature saf-ip-active on Intel platforms code named Panther Lake and Wildcat Lake. *4d62e9b*
- Fixed an issue in feature display-rr where the refresh rate was incorrectly reported in certain scenarios on Intel platforms code named Meteor Lake, Arrow Lake and Lunar Lake. *6bc84f6*
- Fixed an issue which reported incorrect LTR values for VMD remapped PCIe devices on Intel platform code named Arrow Lake -S. *b04adb8*
- Fixed an issue in s0ix-subs-dbg on Intel platform code named Panther Lake that caused counters to display repeated values. *6a4d7c7*
- Fixed issue in feature s0ix-subs-dbg on Intel platform code named Panther Lake where the order of the blocker requirements were reversed. *41e3704*
- Fixed an bug that caused data correctness issues in tcss based features in certain scenarios. *d81a962*

Version 2025.1

New

The 2025.1 release (*socwatch* driver v2.20.1, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled external support for the feature memss-pstate on Intel Platform code named Lunar Lake. This feature provides insights to memory subsystem frequency.*c7cba1d*
- Enabled external support for Intel® Arc™ B-series graphics. The support includes the following features:
  - dgfx-pcie-dstate
  - dgfx-pkg-cstate
  - dgfx-media-cstate
  - dgfx-pwr

  70fbfb4
- Enabled NDA support for the following features on Intel platform code named Panther Lake. Support includes the following features:

- pcie-ltr
- pcie-lpm
- ccp-pstate
- ccp-volt
- cluster-cstate-res
- core-cstate-res
- cpu-igpu-concurrency
- cpu-pkgc-dbg
- d2d-pstate
- ddr-virtual-bw
- display-pstate
- display-state
- display-vc1-bw
- display-volt
- gt-temp
- hbo-bw
- hw-cpu-pstate
- hw-igfx-cstate
- hw-igfx-cstate-cnt
- hw-igfx-pstate
- ia-throt-rsn
- igfx-throt-rsn
- igfx-volt
- ipu-cstate-res
- ipu-pstate
- ipu-volt
- llc-temp
- media-cstate-res
- media-pstate
- media-volt
- memss-pstate
- memss-volt
- mufasa-bw
- noc-d2d-bw
- noc-gt-bw
- noc-io-bw
- noc-pstate
- noc-volt
- npu-bw
- npu-dstate-cnt
- npu-dstate-res
- npu-pstate
- npu-pwr
- npu-volt
- perf-limit-rsn
- pkg-pwr
- pl-limited-res
- psyspl-limited-res
- pwr-limits
- ring-pstate
- ring-throt-rsn
- ring-volt
- santa-bw
- soc-ltr

- soc-temp
- io-bw
- s0ix-subs-status
- tcss-state-res
- tcss-state-cnt
- tcss-ltr-cnt
- tcss-state-dbg
- pcd-platform-ltr

5baf0ac, 8a2de4e

Fixed

Release 2025.1 has a fix for these issues:

- The latest fixes have introduced incompatible format changes to the feature xhci-lpm. Use an older version of SoC Watch to reprocess older collections. *d86ec81*
- Fixed an issue in the feature pcieg5-ip-active causing incorrect lane rate mappings to be reported. *0d3643f*

Version 2025.0

New

- Added support for Lane Rate mapping for the PCIe Gen 5 components supported in the feature pcieg5-ip-active feature. This data will be reported in a new lane mapping table. *1cf4848*
- Added support for latest telemetry GUIDs (0x1306a0b4, 0x1306a1b4, 0x1a06a002 and 0x1a06a102) for Intel platform code named Arrow Lake. *627619d*
- Enabled support for PCD based features on Intel platform code named Wildcat Lake. Support includes the following features:
  - pcie-ltr
  - pcie-lpm
  - pcd-platform-ltr
  - tcss-state-res
  - tcss-entry-cnt
  - tcss-ltr-cnt
  - tcss-state-dbg
  - io-bw
  - saf-ip-active
  - s0ix-subs-status

  32146e9, 373fb98, 8b5efc1, cd059f7, 92725c3, 3cb8e5d
- Added NDA support for feature cpu-pkgc-cfg on Intel platforms Meteor Lake onwards. *dc4236f*
- Added the feature hw-igfx-pstate as a part of the group feature gfx. *3cb8e5d*

Fixed

Release 2025.0 has a fix for these issues:

- Fixed an issue that caused the feature sata-lpm to not detect SATA devices on the Intel platform code named Nova Lake. *c2ff71e*
- The latest fixes have introduced incompatible format changes to the feature sata-lpm. Use an older version of SoC Watch to reprocess older collections. *158d7a0*
- Fixed an issue that caused help output to not display all options properly. *10e712b*
- Fixed an issue that caused certain dgfx metrics to show invalid data if the device was in D3 during collection. *f88cb4d*

Version 2024.9

New

The 2025.0 release (*socwatch* driver v2.20.1, *cstracedrv* driver v2.5.0) contains these changes:

The 2024.9 release (*socwatch* driver v2.20.1, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled support for the additional features on Intel platform code named Nova Lake. Support includes the following features:
  - ddr-bw
  - hgs-feedback
  - igfx-throt-rsn
  - ia-throt-rsn
  - ring-throt-rsn
  - cpu-pkgc-cfg
  - pwr-limits
  - pwr-limits-locks
  - cpu-igpu-concurrency

  b9afc0d, 89d1d79
- Enabled support for PCD based features on Intel platform code named Wildcat Lake. Support includes the following features:
  - pcd-slps0
  - pcd-ip-active
  - s0ix-subs-dbg
  - s0ix-subs-status

  b83f9a8, 1b72e06
- Enabled support for Intel PMT based temperature features on Intel platforms code named Lunar Lake and Panther Lake. The support includes the following features:
  - soc-temp (on Intel platform code named Panther Lake)
  - llc-temp
  - gt-temp

  1051a24
- Enabled support for the features s0ix-subs-dbg and s0ix-subs-status on Intel platform code named Panther Lake -H. *926cf1b*
- Enabled NDA support for the feature s0ix-subs-dbg on Intel platform code named Panther Lake -P. *7dad20d*

Fixed

Release 2024.9 has a fix for these issues:

- Fixed a data correctness issue on the feature tcss-state-res. *fc008ea*
- Fixed an issue that caused incorrect data to be reported when the features pcie-ltr and pcie-lpm were collected together. Fixes have introduced incompatible format changes. Use an older version of SoC Watch to reprocess older collections. *74464e9*

Version 2024.8

New

The 2024.8 release (*socwatch* driver v2.20.1, *cstracedrv* driver v2.5.0) contains these changes:

- This is primarily a release for bug fixes.

Fixed

Release 2024.8 has a fix for these issues:

- Fixed a bug that caused the feature hw-cpu-pstate to not collect on Intel server platforms code named Granite Rapids, Sierra Forest, Diamond Rapids, and Clearwater Forest. *14f67c6*

- Fixed multiple issues in the s0ix-subs-dbg feature on Intel Panther Lake platform. The updates include: accurate reporting of blocker reasons residency, correction of units for breaker reasons (now reported as residency), and accurate reporting of S0ix requirements for components. *8f0dbad, df7b27, a58b96c*
- Fixed an issue in the feature s0ix-subs-status where the component "OSSE-PGD0' was reported twice in the summary report. *3c19b41*
- In feature pcie-lpm, the Root Port CLKREQ mapping table now differentiates between a CLKREQ value of '0' and the unavailability of CLKREQ by showing 'N/A' instead. *df9fda8*
- Fixed an issue in feature sata-lpm which caused capabilities to be reported incorrectly. *634bfbf*

Version 2024.7

New

The 2024.7 release (*socwatch* driver v2.20.1, *cstracedrv* driver v2.5.0) contains these changes:

- Enhanced the summary report to include the system S0ix LPM states capability in the system information section. *9f3855c*
- Added support for latest OOBMSM telemetry GUID (0x5e2f8211) for Intel ARC discrete graphics card [320EU and 288EU] (Intel discrete graphics card code named Battlemage G21). *0a09cb5*
- Updated the way Intel SoC Watch handles temporary files. The temp directory called 'socw_tmp' is now created at C:\Windows\TEMP.*bfecca1*
- Added support for new features partial-slp-res and partial-slp-cnt for Intel platform code named Panther Lake.

  These features provide the power gated residencies and entrance counts of the IP's present in SOC N.

  f5cf66e
- Enabled external support for additional features on Intel platform code named Lunar Lake. The following features are now supported

  - cpu-pkgc-dbg
  - cluster-cstate-res
  - npu-pwr
  - npu-bw
  - npu-dstate-res
  - hw-igfx-pstate
  - soc-temp

  c716603
- Added a new option `--result-slice-range` to summarize a specific time segment of a collection. This new option can be used with the `-i` option to summarize a time slice from a prior collection for a particular section of interest. Refer to the User's Guide for usage details. *5ac1ef0*

Fixed

Release 2024.7 has a fix for these issues:

- Fixed several issues with the feature sata-lpm that caused SATA devices to not display properly in the summary report. *97e67df*
- Improved the Summary report to print number of packages and modules in decimal format. *7807f44*
- Fixed issues in several PCD / PCH based features that caused unknown states to be reported incorrectly during hibernation. *4ec997d*
- Updated telemetry XMLs on the platform code named Panther Lake to fix data correctness issues. The telemetry GUIDs are not updated. *4a28a7f*
- Fixed an issue where lane mappings were incorrectly reported for feature pcd-ip-active on Intel platform code named Panther Lake. *5d9e47f*
- Fixed an issue in the feature pcd-platform-ltr on Intel platform code named Panther Lake to report additional counters which were previously missing. *9c06c75*
- Fixed an issue that caused incorrect component names to be displayed for the feature s0ix-subs-dbg on Intel platform code named Panther Lake. *5e3ac6a*

- Fixed a data correctness issue that caused incorrect residency values to be reported for dstate and perf-limit-rsn features in Intel discrete graphics card code named Battlemage G21. *414ce32*
- Fixed an issue that caused no warning to be issued when insufficient samples were taken to produce output tables for collections made on Intel discrete graphics card code named Battlemage G21.*236868b*

Version 2024.6

New

The 2024.6 release (*socwatch* driver v2.19.10, *cstracedrv* driver v2.5.0) contains these changes:

- Added limited NDA support for Intel platform code named Panther Lake -P. This includes support for the following features:
  - acpi-dstate
  - acpi-sstate
  - connected-standby
  - core-temp
  - cpu-igpu-concurrency
  - ddr-bw
  - device-acpi-calls
  - display-rr
  - display-state
  - hgs-feedback
  - hw-cpu-cstate
  - hw-cpu-hwp
  - hw-cpu-pstate
  - hw-igfx-cstate
  - ia-throt-rsn
  - igfx-throt-rsn
  - os-cpu-cstate
  - os-cpu-pstate
  - os-gfx-cstate
  - panel-srr
  - pcd-ip-active
  - pcd-slps0
  - pkg-pwr
  - pwr-limits
  - ring-throt-rsn
  - s0ix-subs-res
  - sata-lpm
  - timer-resolution
  - xhci-lpm

  The platform is not fully validated.*0319ebf*
- Enhanced the s0ix-subs-dbg feature to support component B/D/F information on Intel platform code named Panther Lake. Components which do not have a B/D/F associated with it is marked N/A. *94bd7b1*
- Enabled a new feature tcss-state-dbg on Intel platforms code named Lunar Lake and Panther Lake. This feature reports TCSS state blocking time, wake reasons, and blocking causes.*5d3d273, 3f163aa*
- Enabled additional Intel PMT based features on Intel platform code named Panther Lake. Support includes the following features:
  - mufasa-bw
  - hbo-bw
  - santa-bw
  - noc-io-bw
  - ddr-virt-bw

9b4beb8

- Added external support for Intel platforms code named Lunar Lake, Arrow Lake, Elkhart Lake.*7844979, ee8f48a, f8b4ec3*
- Added external support for features ia-throt-rsn, igfx-throt-rsn and ring-throt-rsn on Intel platform code named Meteor Lake.*10a97b9*
- Removed support for features dgfx-pkg-cstate-status and dgfx-cstate-status on Intel discrete graphics cards code named DG1. *ecd48e6*

Fixed

Release 2024.6 has a fix for these issues:

- Fixed a bug that caused the feature hw-cpu-pstate to not collect on Intel platforms code named Panther Lake and Nova Lake.*4d9cca4, df7800f*
- Enhanced the granularity of the active time reporting for PCIe devices in the pcie-lpm feature by including the specific PCIe generation link speeds at which they are active.*7c107f0*
- Fixed a data correctness issue in the feature pcd-ip-active on Intel platform code named Panther Lake that caused the counter TCSS-VCCTPC-PGD to report incorrect value.*87ae5dc*
- Improved data correctness of the features soc-pch-platform-ltr, ioe-pch-platform-ltr and ext-pch-platform-ltr on Intel platforms code named Meteor Lake -S and Arrow Lake -S.*bf85648*
- Fixed an issue which prevented the detection and reporting of VMD remapped devices by the features pcie-lpm and sata-lpm on Intel platform code named Arrow Lake. *108f874, 84a62c3*
- Fixed an issue with the feature sata-lpm that hindered the detection of SATA devices connected to higher port numbers only on Intel platform code named Arrow Lake.*84a62c3*

Version 2024.5

New

The 2024.5 release (*socwatch* driver v2.19.9, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled limited NDA support for Intel ARC discrete graphics card [320EU and 288EU] (Intel discrete graphic card code named Battlemage G21). Support includes following features
  - dgfx-afm-cstate
  - dgfx-gt-cstate
  - dgfx-gt-perf-limit-rsn
  - dgfx-media-cstate
  - dgfx-media-perf-limit-rsn
  - dgfx-mods-res
  - dgfx-pcie-dstate
  - dgfx-pcie-link-state
  - dgfx-pkg-cstate
  - dgfx-pkgc-dbg
  - dgfx-soc-ltr
  - dgfx-vram-perf-limit-rsn
  - dgfx-vram-srr

  b124370
- Enabled limited support for Intel discrete graphics card named Battlemage G31. The support includes only OOBMSM telemetry features. The supported features are dgfx-bw, dgfx-gt-cstate, dgfx-media-cstate and dgfx-temp. *2d049f2*
- Added support for latest OOBMSM telemetry GUID (0x5e2f8210) for Intel discrete graphic card code named Battlemage G21. *2d049f2*
- Removed support for Intel discrete graphic card code named Battlemage G10. *2d049f2*

Fixed

Release 2024.5 has a fix for these issues:

- This is a limited release to support Intel graphics card code named Battlemage in NDA.

Version 2024.4

New

The 2024.4 release (*socwatch* driver v2.19.9, *cstracedrv* driver v2.5.0) contains these changes:

- Added limited support for Intel platform code named Nova Lake. The feature support includes: hw-cpu-cstate, hw-cpu-pstate, pkg-pwr, pl-limits, core-temp, sata-lpm, xhci-lpm, acpi sstate, acpi dstate, os-cpu-cstate, os-cpu-pstate. *adfab87*
- Added support for Intel platform code named Arrow Lake S 20A B0 target. *2173273*
- Added support for Intel server platform code named Diamond Rapids D. *fd150c0*
- Enabled support for the feature tcss-state-cnt that reports the entrance count for TCSS states on Intel platform code named Lunar Lake. This feature is also a part of tcss-state group. *b59d84d*
- Enabled the following Intel PMT based features and PCD based features support on Intel platform code named Panther Lake P/H. Please check user guide for detailed explanation on each of these features
  - cpu-pkg-cstate-res
  - cluster-cstate-res
  - cpu-pkgc-dbg
  - cluster-cstate-cnt
  - soc-ltr
  - cpu-pkg-cstate-cnt
  - npu-dstate-res
  - npu-dstate-cnt
  - npu-bw
  - npu-pwr
  - psys-pwr
  - vccia-pwr
  - vccgt-pwr
  - hw-igfx-pstate
  - soc-perf-limit-rsn-cnt
  - soc-pl-limited-cnt
  - soc-psyspl-limited-cnt
  - hw-igfx-cstate-cnt
  - media-cstate-cnt
  - ccp-pstate
  - ccp-volt
  - d2d-pstate
  - display-vc1-bw
  - display-volt
  - idi-bw
  - igfx-volt
  - ipu-pstate
  - ipu-volt
  - media-cstate-res
  - media-pstate
  - media-volt
  - mem-state
  - memss-pstate
  - memss-volt
  - noc-cce-bw
  - noc-d2d-bw
  - noc-gt-bw
  - noc-ipu-bw

  - noc-media-bw
  - noc-pstate
  - noc-volt
  - npu-volt
  - npu-pstate
  - perf-limit-rsn
  - psyspl-limited-res
  - ring-pstate
  - ring-volt
  - soc-temp
  - s0ix0-subs-dbg
  - tcss-ltr-cnt
  - tcss-state-cnt
- The feature s0ix-subs-dbg from the Intel platform code named Panther Lake onwards, will include information about requirements for entry into each of the s0ix states per component and the Bus / Device / Function (B/D/F) information of the component if applicable. The feature s0ix-subs-req will no longer be supported for newer platforms. Support for reporting B/D/F is yet to be enabled. Work is in progress. *76b1acc, e11fb0f*
- The option pch-lvl is removed from the pch-ip-active feature. Active residency information for all ER-enabled components will now be reported in the pch-ip-active feature. As a result, the pch-ip-active-all feature is considered redundant and has been removed. This change applies to all variants of the pch-ip-active feature: soc-pch-ip-active, ioe-pch-ip-active, ext-pch-ip-active, and pcd-ip-active. *7fd96e5*

Fixed

Release 2024.4 has a fix for these issues:

- Fixed a data correctness issue in the sata-lpm feature when port 0 is disabled and SATA devices are connected to other ports. *545a969*
- Fixed an issue in detecting Intel server platform code named Diamond Rapids. 4960a65
- Fixed a bug that prevented the OPI-DMI counter from being reported for the ext-pch-ip-active feature in Intel platforms code named Meteor Lake S and Arrow Lake S. *23b0175*
- Fixed a data correctness issue seen in platforms supporting multiple Intel PMT GUIDs in a single platform specifier. *2ca50ff*

Version 2024.3

New

The 2024.3 release (*socwatch* driver v2.19.9, *cstracedrv* driver v2.5.0) contains these changes:

- Added external support for Intel discrete graphics code named Ponte Vecchio. *c07f6bd*
- Added support for Intel platform code named Arrow Lake U. *a378a5a*
- Added support for latest telemetry GUIDs (0x3072005 and 0x3072105) for Intel platform code named Lunar Lake. 67f04a8
- Added support for latest telemetry GUIDs (0x1306a0b3, 0x1306a1b3, 0x1a06a001 and 0x1a06a101) for Intel platform code named Arrow Lake. *5897539*
- Added NDA support for features pch-ip-active and soc-temp on Intel platform code named Lunar Lake. *1e908be*
- Added support for the feature cdie-llc-flushed-res on Intel platform code named Arrow Lake. This feature will be only available on systems with latest telemetry revisions. 5897539
- Added limited support to Intel server platform code named Clearwater Forest. *fc62b64*
- Added support for the following features on Panther Lake P/H platforms. Please check user guide for the description of these features
  - io-bw
  - pcd-platform-ltr
  - s0ix-subs-status

  - pcieg5-ip-status
  - pcie-lpm
  - pcie-ltr

  b705545, cb28332, 951db73, 500e08a
- Enhanced the feature io-bw by including more component specific bandwidth information on Intel platform code named Lunar Lake. *b705545*
- Enhanced histogram report for feature platform-ltr to include 40us, 250us, 350us and 750us time buckets. *cb28332*
- Deprecated support for telemetry GUIDs (0x3072002 and 0x3072102) for Intel platform code named Lunar Lake. Refer to Known Issues section for the tool version that supports these GUIDs. *67f04a8*
- Debug symbols for the driver are now available in http://symbols.intel.com/symproxy/. Users can add this to the WinDbg by adding symbols server link into File --> "Symbol Path Path ..." dialog. *444e8be*

Fixed

Release 2024.3 has a fix for these issues:

- Fixed data correctness issue for the feature soc-temp on Intel platforms code named Meteor Lake, Arrow Lake and Lunar Lake. *2d12069, f705683*
- Fixed a data correctness issue for the feature mem-state on Intel platform code named Lunar Lake. *6491109*
- Updated the feature cpu-pkgc-dbg to improve the counter description for Display Engine based debug counters on Intel platform code named Lunar Lake. *a699bd9*

Version 2024.2

New

The 2024.2 release (*socwatch* driver v2.19.9, *cstracedrv* driver v2.5.0) contains these changes:

- A new switch called tcss-state-res has been introduced. It reports TCSS device residency on Intel platforms, code named Meteor Lake and onwards. The purpose of this feature is to ensure that the IOM (Input/Output Manager) is awakened before sampling. Residency counters are now sampled only twice: once at the start and once at the end of the collection process. This change enhances data accuracy.

  If waking up the IOM is not desired, --option disable-iom-wakeup can be used with the tcss-state-res feature.

  The tcss-state feature now behaves like a group switch.*5feec6f, e776790*

  In a future release, support for tcss-state-cnt will be enabled which will report the entrance counts into various residency states.
- Added NDA support for the feature soc-ltr on Intel platform code named Lunar Lake.*df199e2*
- Added support for the feature soc-temp that reports temperature of various components such as PCH, System Agent, IPU, DE, NPU and Media on Intel platform code named Lunar Lake.*7b81929*
- Added a group switch dgfx-cstate to support the features dgfx-media-cstate and dgfx-gt-cstate on Intel graphics card code named Battlemage.*7b81929*
- Enabled support for the following features on Intel platform code named Panther Lake.

  - pcd-ip-active (-all)
  - pcd-slps0
  - saf-ip-active
  - s0ix-subs-dbg
  - tcss-state-res

  7c1333e, 8947968, 6946f7a
- A text disclaimer has been included regarding limited validation in summary output for newer platforms that have not yet been powered on or are in the early system bring-up phase. This ensures transparency and acknowledges the current state of validation for these platforms. *366a32b*

- Support for the following metrics has been deprecated in this release: pmc-ip-status, pmc-ip-pg-res, cnv-active, cnv-ltr, nc-dstate, sc-dstate, pmc-ip-d3-res, pmc-ip-d0i3-res, pmc-ip-d3-occ, pmc-ip-d0i3-occ. These features were mostly atom based. *bfb35e3*

Fixed

Release 2024.2 has a fix for these issues:

- Fixed an issue that caused collection to continue for a short duration after `-z`(connected standby) fails. Intel SoC Watch will now exit with a warning pertaining to the failure. *411df53*
- Fixed an issue where the feature display-state caused system crashes when Intel integrated graphics was disabled/not present. *d1e79ef*
- Fixed a data correctness issue for the feature npu-dstate-res on Intel platform code named Meteor Lake. This issue was seen as data samples can arrive swapped. *d7c4ff6a*
- Fixed a data correctness issue for the feature ipu-pstate on Intel platform code named Lunar Lake.*bd43da5*
- Users will now see a warning printed when the system under test has older or deprecated telemetry GUIDs. Visit known issue section for more information.*e62d58f*
- Deprecated support for older telemetry GUIDs on Intel platform code named Meteor Lake. Only the latest telemetry GUIDs are supported for embargoed platforms. *38c720a*

Version 2024.1

New

The 2024.1 release (*socwatch* driver v2.19.7, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled support for the feature s0ix-subs-res on Intel platform code named Panther Lake -P/-H. *a023acf*
- Added support for latest telemetry GUIDs (0x3072003 and 0x3072103) for Intel platform code named Lunar Lake. *b700a14*

Fixed

Release 2024.1 has a fix for these issues:

- Fixed a potential BSOD that was caused by not restoring IRQLs when accessing a non-paged memory . *5f5d972*
- Fixed scale factor value for the features npu-bw and npu-dstate-res on Intel platform code named Lunar Lake which caused data incorrectness. *d475667, b700a14*
- Updated the feature dgfx-gt-cstate to read RC0 and infer RC6 and feature dgfx-media-cstate to read MC0 and infer MC6 on Intel discrete graphic card BattleMage. This is because RC6/MC6 telemetry counters use a different scale factor from RC0/MC0. *739b3e4*
- Fixed an issue that printed duplicate PMT platform specifier entries in summary report when multiple GUIDs are supported on a particular platform or discrete graphics card. *63a60ea*

Version 2024.0

New

The 2024.0 release (*socwatch* driver v2.19.6, *cstracedrv* driver v2.5.0) contains these changes:

- Added limited (non PMT and PCD) support for Intel platform code named Wildcat Lake. *337804a*
- Added limited support to Intel server platform code named Diamond Rapids. *aa13b7d*
- Enabled support for the feature io-bw on Intel platform code named Lunar Lake. This feature reports total read and write bandwidth from I/O component. *8ca91e4*
- Enabled additional features (NDA) support for Intel platform code named Lunar Lake. The following features are now supported.
  - cpu-pkgc-dbg
  - cluster-cstate-res
  - media-cstate-res

- npu-dstate-res
- perf-limit-rsn
- pl-limited-res
- psyspl-limited-res
- memss-pstate
- ipu-pstate
- display-pstate
- npu-pstate
- media-pstate
- hw-igfx-pstate
- noc-pstate
- d2d-pstate
- ring-pstate
- ccp-pstate
- memss-volt
- ipu-volt
- display-volt
- npu-volt
- media-volt
- igfx-volt
- noc-volt
- ring-volt
- ccp-volt
- noc-gt-bw
- noc-d2d-bw
- idi-bw
- npu-bw
- display-vc1-bw
- hw-igfx-cstate-cnt
- media-cstate-cnt
- npu-dstate-cnt
- npu-pwr

af940a2

- Removed NDA support for the feature cpu-pkg-cstate-res on Intel platform code named Lunar Lake as it exposes Intel confidential data.
- Enabled additional features (NDA) support for Intel platforms code named Meteor Lake -S and Arrow Lake -S. The following features are now supported.

  - ext-pch-platform-ltr
  - ext-s0ix-subs-res
  - soc-s0ix-subs-req
  - ext-s0ix-subs-req
  - ext-s0ix-subs-status
  - cdie-perf-limit-rsn-res
  - cdie-perf-limit-rsn-cnt
  - cdie-core-cstate-res
  - cdie-core-cstate-cnt
  - cdie-ccp-llc-bw

cec7236

- Enabled additional features (external) support for Intel platform code named Meteor Lake. The following features are now supported.

  - cpu-pkg-cstate-res
  - cpu-pkgc-dbg

- npu-dstate-res
- npu-dstate-cnt
- npu-bw
- soc-temp
- io-bw
- cdie-cstate-res
- cdie-cstate-dbg
- cdie-ccp-llc-bw

bbdf9ed

Fixed

Release 2024.0 has a fix for these issues:

- Fixed a memory deallocation issue in the Windows driver that may have led to sporadic crashes. *606576d*
- Intel SoC Watch will now display an error message when Intel discrete graphics card is in D3 indicating features cannot be collected. The message now reads "NOTE: Cannot collect feature: <Feature Name>. The device is in D3!". *d5bc089*
- Fixed a data correctness issue for the feature ext-pch-ip-active on Intel platforms code named Meteor Lake -S and Arrow Lake -S. *79101c9*
- Fixed an issue where DMI-PLL counters were not reported properly for soc-pch-ip-active-all feature on Intel platform code named Meteor Lake -S. *7358261*

Version 2023.7

New

The 2023.7 release (*socwatch* driver v2.19.4, *cstracedrv* driver v2.5.0) contains these changes:

- Added support for newer Windows* OS flavors such as Windows SV3. *15467f6*
- Enabled NDA support for features pcie-lpm and pcie-ltr for Intel platforms code named Arrow Lake and Lunar Lake. *52b39cc*
- Enhanced Wakeup Analysis histograms report for feature os-cpu-cstate to include 7ms and 10ms time buckets. *504efab*
- Added features hw-igfx-pstate and igfx-volt to the group feature igfx. *4f2b5e0*
- Enabled support for features pch-slps0-cfg and pch-slps0-dbg for Intel platforms code named Lunar Lake. *8b413b9*

Fixed

Release 2023.7 has a fix for these issues:

- Fixed an issue where summary reports were not generated on Intel platforms Meteor Lake or newer for longer collections. This was due to a low level regression on how buffered events were handled. *8ec3bc8*
- Fixed data correctness issues for breaker counters in features ioe-s0ix-subs-dbg and ext-s0ix-subs-dbg on Intel platform code named Meteor Lake. *4f2b5e0*
- Updated the PMT XML for Intel platform code named Lunar Lake. The change is done to ensure the XML matches with the pcode. The change should potentially fix any data correctness issue seen in telemetry based features. *91b649d*
- Fixed an issue which caused the feature ioe-s0ix-subs-req not collectible on Intel platform code named Meteor Lake. *a5315e1*

Version 2023.6

New

The 2023.6 release (*socwatch* driver v2.19, *cstracedrv* driver v2.5.0) contains these changes:

- Added external support for Intel server platform code named Emerald Rapids-Xeon. *6789b67*

- Added a new feature saf-ip-active on Intel platform code named Lunar Lake to report the active time of System Agent fabric components. These components will not be active beyond Package C6. *5861ccc*
- Disabled MMIO based hw-igfx-pstate due to data correctness issues and enabled the Intel PMT based hw-igfx-pstate on Intel platform code named Lunar Lake. *f1749bd*
- Removed support for features npu-context-priority and noc-disp-bw on Intel platform code named Lunar Lake as the counters read for these features are no longer supported in firmware. *f1749bd*
- Added support for below features on Intel platform code named Lunar Lake. These features provide entrance count data for various IP's C state residency. *3580733*
  - soc-perf-limit-rsn-cnt
  - soc-pl-limited-cnt
  - soc-psyspl-limited-cnt
  - hw-igfx-cstate-cnt
  - media-cstate-cnt
  - npu-dstate-cnt
  - cluster-cstate-cnt
  - cpu-pkg-cstate-cnt
- Added support for below features on Intel platform code named Lunar Lake. These features provide PMT power statistics.*35ee97e*
  - psys-pwr
  - vccia-pwr
  - vccgt-pwr
  - npu-pwr
- In order to enable power management, added ability for SoCWatch driver to wake up the PMT device at the beginning of collection and then explicitly put it back to sleep when done at the end of the collection. *700cad4*
- Added -f bldt switch to capture ETW events from the following providers:
  - Microsoft-Windows-Kernel-Interrupt-Steering
  - Microsoft-Windows-Sleepstudy
  - Microsoft-Windows-Kernel-PnP-Rundown
  - Microsoft-Windows-Kernel-Processor-Power
  - Microsoft-Windows-TCPIP

  00595f4

Fixed

Release 2023.6 has a fix for these issues:

- Fixed an issue that caused the features pch-slps0, pch-ip-active(-all) and tcss-state not collectible on Intel platforms code named Meteor Lake and Lunar Lake. The issue occurred when these features were collected standalone instead of a group feature. *5ea854b*
- Fixed an issue where IOE and EXT chipsets were not detected on Intel platform code named Arrow Lake - S. *c4402b4*
- Fixed incorrect mappings of certain Power gated components for the feature soc-pch-ip-active(-all) on Intel platform code named Meteor Lake (-M/P). *fea063f*
- Fixed an issue that caused incorrect data to be reported for the feature soc-ltr on Intel platform code named Meteor lake. *22df8df*
- Fixed a bug that caused the feature pch-platform-ltr to report erroneous data on Lunar Lake platforms. *b27ac8a*
- Added updates to the Windows driver support for newer OS versions, to improve stability and possibly fix random crashes. *3a16ea8*
- Fixed a bug in feature s0ix-subs-status which was reporting incorrect mappings on Intel platform code named Meteor Lake and Intel platform code named Lunar Lake. *db9e2ce, 94398c6*
- Fixed a bug in feature mem-state where an error was being reported about setting OS Telemetry bits on Intel platform code named Lunar Lake.*3b9870f*

- Fixed scaling factor for -f npu-pstate which caused reported frequencies to be ~1% lower than actual on Intel platform code named Meteor Lake.*3116517*
- Reformatted tables for features s0ix-subs-status and s0ix-subs-dbg on all platforms to better display counters based on counter class.*8f23c52*

Version 2023.5

New

The 2023.5 release (*socwatch* driver v2.19, *cstracedrv* driver v2.5.0) contains these changes:

- Updated the scope of existing group features to make it more meaningful. To provide better value addition, new feature groups are introduced while certain older groups are removed. Some key changes are noted below. The description of these groups are updated in user guide.
  - Reduced the "sys" group to only contain metrics that support physical components of the system (CPU, GPU). The firmware based metric support is moved out of this group.
  - The group "pch-all" is renamed to "chipset-all" to be inclusive of all the chipset dies in disaggregated architecture and to include s0ix based metrics.
  - The groups "sstate" and "pch" are removed and all the metrics supported in the group are moved to new group "chipset-all".
  - Improved the group "ring" to include all ring and llc based metrics.
  - The group "cdie-cstate" is renamed to "cdie" and now includes all Compute die based features in platforms with disaggregated dies.
  - The group "sa-pstate" now includes memss-pstate, ring-pstate, display-pstate and ipu-pstate. This is added as sa-freq is deprecated in newer platforms.
  - The groups "llc", "volt" and "pstate" are removed as they do not provide any special value add to the users.

  b82601
- Added limited support (non PMT and PCH) support for Intel platform code named Panther Lake. *880d6e*
- Added support for latest telemetry GUIDs (0x3072002 and 0x3072102) for Intel platform code named Lunar Lake. *11762e*
- Enabled support to discover new discrete graphics card PMT endpoints along with older host system endpoints. This enables support for PMT metrics for Intel discrete graphics card code named Battlemage. *1e45cf*
- Updated Intel Vision Processing Unit (VPU) nomenclature to Intel Neural Processing Unit (NPU) to conform with company and industry standards.*9119b7*
- Implemented the feature display-vc1-bw for Intel platform code named Lunar Lake. This provides information about display vc1 non coherent reads. *a40429*
- Implemented the feature display-rr for Intel platform code named Lunar Lake. *16a633*
- Removed support for the feature noc-vpu-bw for Intel platform code named Lunar Lake. The counters for this feature are not implemented in pcode. *a40429*

Fixed

Version 2023.4.2

New

The 2023.4.2 release (*socwatch* driver v2.18, *cstracedrv* driver v2.5.0) contains these changes:

- This is an NDA only release with driver changes to remove PMT interface support for Intel platform code named Lunar Lake .

Release 2023.4.2 has a fix for these issues:

- Fixed an issue that caused BSOD when the latest PMT driver Interface was accessed in Intel platform code named Lunar Lake. We have currently disabled the PMT interface for NDA build for the platform Lunar Lake as there is a probability of BSOD and the team is still working on the fix. PMT based metrics for this platform are not yet supported in NDA build and therefore, will not cause any user visible changes

Version 2023.4.1

New

The 2023.4.1 release (*socwatch* driver v2.17.5, *cstracedrv* driver v2.5.0) contains these changes:

- Added limited NDA support for Intel platform code named Lunar Lake. This includes support for features hw-cpu-cstate, hw-cpu-pstate, s0ix-subs-res, pch-platform-ltr, pcie-lpm, hw-igfx-cstate, hw-igfx-pstate and cpu-gpu-concurrency *fa36f2b*
- Added support for feature mem-state on Intel platform code named Lunar Lake. *d929b4*

Fixed

Release 2023.4.1 has a fix for these issues:

- Fixed an issue which caused SoC Watch to read incorrect address for PMT based metrics on Intel platform code named Lunar Lake. Previously, the XML collaterals were incorrectly generated which is fixed now. *0d0a7cc*
- Fixed a bug that removed support for the feature s0ix-subs-res on Intel platform code named Lunar Lake.*9e987ff*
- Fixed a data correctness issue with Modphy Lane 3 value in the feature ioe-pch-ip-active on Intel platform code named Meteor Lake P.*5191e8*

Version 2023.4

New

The 2023.4 release (*socwatch* driver v2.17.5, *cstracedrv* driver v2.5.0) contains these changes:

- Added support for Intel platform code named Arrow Lake -H (6+8). *be5627*
- Added support for Intel discrete graphics card code named Battlemage. Below lists the features currently supported. *b3ad4f*

  dgfx-gt-perf-limit-rsn

  dgfx-media-perf-limit-rsn

  dgfx-adm-perf-limit-rsn

  dgfx-vram-perf-limit-rsn

  dgfx-vram-srr

  dgfx-mods-res

  dgfx-pcie-link-state

  dgfx-sgunit-dstate

  dgfx-audio-dstate

  dgfx-pcie-dstate

  dgfx-afm-cstate

  dgfx-adm-cstate

  dgfx-volt

  dgfx-current

  dgfx-pwr

dgfx-pstate-status

dgfx-pkg-cstate

dgfx-pkgc-dbg

dgfx-soc-ltr

dgfx-gt-cstate

dgfx-media-cstate

dgfx-temp

dgfx-pstate-status

dgfx-bw

- Enabled additional features support for Intel platform code named Lunar Lake. The following features are now supported. *d9a261, 872691, eac3f7, c057de, 260e31, 28c57d*

  pch-platform-ltr

  s0ix-subs-req

  tcss-state

  s0ix-subs-status

  pcie-ltr

  pcie-lpm

  noc-gt-bw

  noc-d2d-bw

  idi-bw
- The feature pch-ip-status is deprecated for platforms starting from Intel Platform code named Meteor Lake. This feature reads PPFEAR registers which provide power gated status of components at a given point in time. These were useful for low power debug when s0ix residency debug reasons were unavailable in older generations. Customers are encouraged to use the features s0ix-subs-status and s0ix-subs-dbg which provide more detailed information for low power analysis. *15355b*
- Removed "Supported CPU Frequencies (P/T-states)" table from the feature hw-cpu-pstate. *4fd1e6*
- Removed support for feature sa-freq for platforms starting from Intel platform code named Meteor Lake. The register used for collecting data for this metric is not implemented in BIOS. Refer the below table for alternate features that provide equivalent data from telemetry aggregator space. *5df53a*

Feature Name	Frequency Data
memss-pstate	qclk freq
display-pstate	cdclk freq
ipu-pstate	IPU-PS freq
ring-pstate	ring-uclk freq

- Added support for Chassis 2.2 LTR counters in the features soc-pch-platform-ltr and ioe-pch-platform-ltr for Intel platform code named Meteor Lake. *9933a8*
- Added support for tile telemetry GUID 0xb15a0ede for Intel discrete graphics card code named Ponte Vecchio. The support for older GUID is removed. The HBM read write data is now for the entire HBM subsystem. *9edf50*
- Added support for latest telemetry GUIDs (0x3072001 and 0x3072101) for Intel platform code named Lunar Lake. Support for older GUIDs (0x3072000 and 0x3072100) are removed. *419696*
- The scope of group feature sys will be reduced in future versions of SoC Watch to collect a pruned set of system features. This redefinition of the sys feature is being done to reduce undue collection overhead as well as have a more focused feature set. The group features device, sstate will be replaced with more

meaningful groups to support all relevant metrics. Few groups which currently do not provide any value addition to existing groups will be removed, this includes volt, pstate etc. More details will be made available when these changes are introduced.

Fixed

Release 2023.4 has a fix for these issues:

- To prevent a system crash, the following features are disabled when Enhanced Sign-In Security (a.k.a., Virtualized Trusted IO or VTIO) is enabled on the system: xhci-lpm, pcie-lpm and pcie-ltr. To use these features, turn off "Memory integrity" under "Core Isolation" in the Windows Security control panel or disable VTIO in the BIOS. *841426*
- Fixed an issue where certain PMT based residency metrics had issue with data correctness for non-64 bit counters. The data rollover was incorrectly handled. *49fa59*
- Fixed a bug which caused the feature ioe-s0ix-subs-res to report values lower than soc-s0ix-subs-res in the Intel platform code named Meteor Lake -M/P. *134dda*
- Fixed multiple issues in the feature s0ix-subs-dbg on Intel platforms code named Meteor Lake and Lunar Lake . The fixes include:
  - Updating the breaker counter size from 32 bits to 16 bits.
  - Inverting the LPSS / ITSS blocker counters definition. Now, if the counters increment, its considered non blocking.
  - Updating the scale factor for blocker counters from 10 ms to 30.5us per tick.
  - Removing setting of policy bit. Previously setting this on default, enabled the breaker counters to count even when the system was not in PC10 state, which is an undesired functionality.

  531e569
- Fixed an issue with the feature sata-lpm where incorrect controller B/D/F information were displayed for the SATA devices. *9506233*
- Fixed a bug where unknown devices were displayed when no SATA disks are connected to the system. If there are no SATA disks connected to the system, users will not be able to collect feature sata-lpm and will see a warning- "WARNING: No sata devices found on this system". *3ceaec8*
- Fixed an issue in s0ix-subs-res on Intel platform code named Lunar Lake where incorrect registers were read earlier. *3235b4*
- Fixed a table ordering issue in the feature cpu-pkgc-dbg for Intel platform code named Lunar Lake. *b119e7*
- Fixed inaccurate descriptions of CNVI counters in the feature ext-pch-ip-active-all on Intel platform code named Meteor Lake -S. Also, removed CNVI8-10 counters due to firmware bug. *d1315f5*
- Updated counter names for features soc-pch-ip-active and ioe-pch-ip-active on Intel platform code named Meteor Lake -P/M.
  - ICC-CLKOUT-DBUFF-SRC-6 counter was removed from SoC die.
  - ICC-CLKOUT-DBUFF-SRC-0/1/2 counters were renamed to ICC-CLKOUT-DBUFF-SRC-6/7/8 on IOE die.

  e9826d2

Version 2023.3

New

The 2023.3 release (*socwatch* driver v2.17.3, *cstracedrv* driver v2.5.0) contains these changes:

- Added NDA support for Intel server platforms code named Emerald Rapids-Xeon and Granite Rapids-Xeon. *b27a1b, 4e9a98*
- Enabled a list of PMT and PCH based metrics on Intel platform code named Lunar Lake. Below lists the features currently supported in Lunar Lake. The user guide provides the description of these features.

  acpi-dstate

  acpi-sstate

ccp-pstate
ccp-volt
cluster-cstate-res
connected-standby
core-cstate-res
core-temp
cpu-igpu-concurrency
cpu-pkg-cstate-res
cpu-pkgc-cfg
cpu-pkgc-dbg
d2d-pstate
ddr-bw
device-acpi-calls
display-pstate
display-state
display-volt
io-bw
hgs-feedback
hw-cpu-cstate
hw-cpu-pstate
ia-throt-rsn
igfx-throt-rsn
igfx-volt
ipu-pstate
ipu-volt
media-cstate-res
media-pstate
media-volt
memss-pstate
memss-volt
noc-cce-bw
noc-display-bw
noc-pstate
noc-volt
noc-vpu-bw
os-cpu-cstate
os-cpu-pstate
os-gfx-cstate

panel-srr

pch-ip-active

pch-slp-s0

perf-limit-rsn

pkg-pwr

pl-limited-res

psyspl-limited-res

pwr-limit-locks

pwr-limits

ring-pstate

ring-throt-rsn

ring-volt

s0ix-subs-dbg

s0ix-subs-res

sata-lpm

soc-ltr

timer-resolution

vpu-bw

vpu-context-priority

vpu-dstate-res

vpu-pstate

vpu-volt

xhci-lpm

- Enabled the feature tcss-state on Intel platform code named Meteor Lake. *7859c3, a68182*
- Enhanced the feature sata-lpm to also display SATA devices on the secondary bus on Intel platforms starting with Meteor Lake -S. *91c514*
- Updated Windows driver to use Windows API for PCI reads/writes. This enhancement allows collection of various metrics which were previously disabled when Enhanced Sign-In Security (a.k.a., Virtualized Trusted IO or VTIO) was enabled on the system. This affects the following features: s0ix-subs-dbg, s0ix-subs-req, xhci-lpm, pcie-lpm, pcie-ltr, pch-ip-active, and pch-ip-status. *502c22*
- Removed support for PMT based features on Intel platform code named Meteor Lake (A step).*8d32af*

Fixed

Release 2023.3 has a fix for these issues:

- Fixed an issue which reported Windows 11 systems as Windows 10 systems. *cd2521*
- Fixed an issue where IOE chipset was not detected properly when TCSS device is in TC Cold on Intel platform code named Meteor Lake. *1d8b57*
- Updated feature vpu-dstate-res to account for delayed updating of counters by software. This improves the residency reporting accuracy compared to previous implementation. Older collections of this feature cannot be reprocessed with Intel SoC Watch v2023.3 or newer.*9c130d*
- Fixed scale factor value for the feature vpu-bw on Intel platform code named Meteor Lake which caused data incorrectness. *cc91dc9*
- Fixed data ordering issues for s0ix-subs-status features on Intel platform code named Meteor Lake. *1f0a07*

- Fixed an issue in the feature soc-pch-ip-active on Intel platform code named Meteor Lake where the power gated counters were reported as counts instead of residency. The feature now reports additional counters which were earlier missing due to this bug. *1368c6*
- Fixed an issue where feature soc-pch-ip-active was not collectible on Intel platform code named Meteor Lake -S. *a8cba1*
- Corrected reporting of feature ioe-pch-ip-active on Intel platform code named Meteor Lake -P. The feature now reports the counter HSIO-MPFPW5-0-PLLA which was earlier missing. *b74901*
- Fixed an issue that caused the features soc-s0ix-subs-status, ioe-s0ix-subs-status, soc-pch-ip-active and ioe-pch-ip-active to report PCIe controllers on incorrect dies on Intel platform code named Meteor Lake. *71dd66*
- Fixed an issue in the feature s0ix-subs-req that caused the summary table headers to have a prefix "SOC" on systems with single PCH die. *b4f935*
- Enabled the feature sata-lpm to identify SATA disks across multiple controllers. Previously these devices were identified as unknown. Also added controller B/D/F and port information to residency and count tables. *b94073*
- Fixed an issue on PMT based bandwidth metrics on Intel platforms code named Meteor Lake and Lunar Lake where the data was collected only at the beginning and end of collection instead of sampling at regular intervals. *afc1a0d*

Version 2023.2

New

The 2023.2 release (*socwatch* driver v2.17.0.0, *cstracedrv* driver v2.5.0) contains these changes:

- Added external support for Intel Platform code named Raptor Lake and Intel server Platform code named Sapphire Rapids -Xeon. *988d0d, d514f0*
- Added support for Intel Platform code named Arrow Lake. The cores are identified as Lion Cove (LNC) for big cores and Skymont (SKT) / Crestmont (CMT) for Atom. *3c4af4, 576456*
- Added support for Intel discrete graphics card code named Alchemist Refresh. *787ea0*
- Enabled support for the following PMT features on Intel platform code named Lunar Lake.
  - cpu-pkgc-dbg
  - cpu-pkg-cstate-res
  - cluster-cstate-res

  The feature cluster-cstate-res reports the residency of the hybrid cores. Cluster 0 refers to big cores and cluster 1 refers to Atom.

  The package C state metric also reports the package C sub states (PC6.1, PC6.2, PC10.1, PC10.2 and PC10.3).

  a44633, 8df29c, 723346
- Enabled support for features pcie-lpm and pcie-ltr on Intel platform code named Meteor Lake -S. *9d0c98*
- Expanded the feature pcie-lpm to also display PCI devices on the secondary bus (128 by default) on Intel platform code named Meteor Lake-S onwards. *74739d*
- Added Modphy lane assignment and rate tables to features soc-pch-ip-active, ioe-pch-ip-active, and ext-pch-ip-active for Intel platform code named Meteor Lake. *6df0ac2*
- Added NDA support for features ioe-pch-ip-active and ioe-pch-slps0 on Intel platform code named Meteor Lake. *9a543e*
- Added support for external PCH on Intel platform code named Meteor Lake -S, the support includes the following features:
  - ext-s0ix-subs-dbg
  - ext-s0ix-subs-res
  - ext-s0ix-subs-status
  - ext-pch-platform-ltr
  - ext-pch-slps0-dbg
  - ext-pch-slps0-cfg

- ext-s0ix-subs-req
- ext-pch-ip-active
- ext-pch-ip-active-all
- ext-pch-slps0

edb313, e307d2, cda963, 2cd94b

- Added s0ix breaker counters to the features soc-s0ix-subs-dbg, ioe-s0ix-subs-dbg, ext-s0ix-subs-dbg on Intel Platform code named Meteor lake.

  Note that these counters may not correspond exactly with blocker counters as they are implemented in firmware as opposed to the blocker counters implemented in hardware. The firmware only updates them on s0ix exit to PC0, so the numbers in them may not reflect expected results.

  dfd702
- Removed support for PMT features vpu-cstate-res, vpu-cstate-cnt, vpu-context-priority on Intel platform code named Meteor Lake as the counters used for these features are not implemented in firmware. *f19e8e*

Fixed

Release 2023.2 has a fix for these issues:

- Fixed an issue on some Intel platform code named Meteor Lake -S or legacy systems with integrated graphics disabled which could cause crashes or possible wrong data for features hw-igfx-cstate, hw-igfx-pstate, panel-srr, display-rr, display-state, and dpst. *955e7f, 90e139*
- Fixed issue on ADL-N where BSOD was occurring while running help command.

  This bug was due to a regression of an earlier fix that disabled the features known to cause a crash when Enhanced Sign-In Security (a.k.a., Virtualized Trusted IO or VTIO) is enabled on the system. *7e9d67*
- Fixed an issue on Intel platform code named Meteor Lake where the features soc-s0ix-subs-status and ioe-s0ix-subs-status did not output tables. *c1c154*
- Fixed an issue on Intel platform code named Meteor Lake -S which caused mismatched counter output for the feature soc-pch-ip-active. *4c2d97*
- Fixed an issue on Intel graphics cards code named DG2 and ATS-M which caused inaccurate frequencies for P-States. *52bfdb*
- Fixed an issue in feature ioe-pch-ip-active on Intel platform code named Meteor Lake which caused incorrect data. *9a543e*
- Fixed an issue in feature ioe-s0ix-subs-req for Intel platform code named Meteor Lake -S where the metric was not being collected. *2cd94b*
- Updated scale factor value for the features vpu-volt and vpu-pstate on Intel platform code named Meteor Lake to match with specification document. *f19e8e*

Version 2023.1

New

The 2023.1 release (*socwatch* driver v2.16.12.0, *cstracedrv* driver v2.5.0) contains these changes:

- Added NDA support for features soc-pch-ip-active and soc-pch-slps0 on Intel platform code named Meteor Lake. *b60b84*
- Added NDA support for PMT features on Intel platform code named Meteor Lake (B-step). This includes SoC and CDie residency, bandwidth, voltage, temperature, pkgc debug metrics. *48fcce*
- Enabled support for features ioe-pch-ip-active and ioe-pch-slps0 on Intel platform code named Meteor Lake. *12abf1*
- Added support for feature gcd-cstate-res on Intel platform code named Meteor Lake (B-step). *44443b*

Fixed

Release 2023.1 has a fix for these issues:

- Fixed an issue on Intel platform code named Meteor Lake -S which prevented PCH features with the 'soc-' prefix from working. Also rewrote the PCH detection to allow for all 3 Meteor Lake chipset dies (SOC, IOE, and PCH-S) to be detected properly. *5169fa*
- Fixed an issue in features cpu-pkgc-dbg-res and cpu-pkgc-dbg on Intel Platform code named Meteor Lake which caused the metrics not report all the cannot go deeper and high residency reasons table. This fix is available only on the latest firmware. *5a6f11*
- Fixed an issue where feature soc-pch-ip-active was not collectible on Intel platform code named Meteor Lake. *b60b84*
- Fixed an issue that caused hw-cpu-cstate residency values to be inaccurate on platform code-named Meteor Lake. *a3a0d64*

Version 2023.0

New

The 2023.0 release (*socwatch* driver v2.16.12.0, *cstracedrv* driver v2.5.0) contains these changes:

- Added limited support for Intel platform code named Emerald Rapids Server. *11edbf*
- Enabled initial set of features for Intel platform code named Lunar Lake. This includes support for the following features: cpu-pkgc-cfg, ddr-bw, pwr-limits, pwr-limit-locks, ia-throt-rsn, igfx-throt-rsn, ring-throt-rsn, core-temp, os-cpu-cstate, hw-cpu-cstate, connected-standby, hw-igfx-pstate, hw-igfx-cstate, sata-lpm, hgs-feedback, xhci-lpm. *18ab52*
- Added a new feature gcd-cstate-res that reports residency information for Graphics Companion Die (GCD) on Intel platform code named Meteor Lake (A-step). *cb1b60*
- Added a new feature mem-state to report residency in low power memory states for Intel platform code named Meteor Lake (B step). *813ca6*
- Enabled support for features soc-pch-ip-active and soc-pch-slps0 on Intel platform code named Meteor Lake. *ba43fd*
- Enabled support for feature display-rr on Intel platform code named Meteor Lake. *30b4bf*
- Enabled NDA support for features display-state, IOE-PCH features ioe-s0ix-subs-res, ioe-s0ix-subs-status, ioe-s0ix-subs-dbg on Intel platform code named Meteor Lake. *a310ffb*
- Expanded NDA PMT metrics support in Intel platform code named Meteor Lake (A step) to include features from CDie.*a205ac3*
- Removed Min/Max IRT table from the feature cpu-pkgc-cfg summary report on Intel platforms code named Tiger Lake and newer as the counters read to collect this data are not supported. *5c627e*
- Removed support for feature comp-max-temp in Intel platform code named Meteor Lake. *18ab52*
- Support for feature cpu-pkg-cstate-res metric on Intel platforms code named Alder Lake, Raptor Lake and Meteor Lake has been removed as the package c-state information reported by this feature is already available through hw-cpu-cstate feature. *02de7a*
- Support for Google Analytics has been removed. *ddf09f*

Fixed

Release 2023.0 has a fix for these issues:

- Removed support for DC6 and DC6V states in feature display-state for Intel platform code named Meteor Lake as the transition protocol from DC5 to DC6 is not supported anymore. *5c64e2*
- Fixed an issue in feature pcie-lpm where "Rootport vs. CLKREQ #" table was reporting inaccurate data on Intel platform code named Meteor Lake. Feature now reports accurate data due to corrected register offsets. *4b7c4a*
- Fixed scale factor value for the feature display-pstate in Intel platform code named Meteor Lake (B-step) which caused data incorrectness. *0bf7fa*
- Fixed issues in the features soc-s0ix-subs-dbg and ioe-s0ix-subs-dbg on Intel platform code named Meteor Lake. Previously wrong addresses were used for reading the data and the enable bit to read the counters were not set. *7cd8c6, 07e696d*
- Fixed a bug in the command-line parsing of long options. *6896aaa*

- Fixed an issue on Intel platform code named Meteor Lake -S with SoC South PCH detection that resulted in SoC PCH features being uncollectible or reporting incorrect data. *3614ca*

Version 2022.6

New

The 2022.6 release (*socwatch* driver v2.16.12.0, *cstracedrv* driver v2.5.0) contains these changes:

- Report complete topology path in the 'CPU native model' section of summary header on hybrid systems instead of just core ID. *e7eaea*
- Add support for new method of querying PMT driver for endpoints. *a946f9*
- Add support for dgfx collections with new CtaChildDriver which allows for queries in D3 without causing BSOD. *a946f9*
- Added support on Intel Platform code named Meteor Lake for IOE-PCH features -f ioe-s0ix-subs-status, -f ioe-pch-platform-ltr, -f ioe-s0ix-subs-res, -f ioe-pch-slps0-cfg, -f ioe-pch-slps0-dbg. IOE PCH features are only supported on the latest firmware. SoCWatch will throw an error message to update the firmware if older versions are used. *548f91*
- Added support on platform code named Meteor Lake -S for SoC-PCH features: -f soc-s0ix-subs-res, -f soc-s0ix-subs-dbg, -f pch-slps0, -f pch-ip-active, -f soc-s0ix-subs-status, -f soc-pch-ps-on, -f soc-pch-slps0-dbg, and -f soc-pch-slps0-cfg. *fe7fa9, ba0d2f*
- Added support on Intel Platform code named MTL –M/P for SoC-PCH features -f soc-s0ix-subs-status, -f soc-pch-slps0-dbg and -f soc-pch-slps0-cfg. *ba0d2f*
- Added support for group switches -f s0ix-subs-req, -f s0ix-subs-res, -f s0ix-subs-dbg for multiple PCH dies on Intel Platform code named Meteor Lake. *199524*
- Added an additional table "S0ix Substate Status Summary - Sampled: Ever Observed", to the -f s0ix-subs-status feature. *bb5dc5*

Fixed

Release 2022.6 has a fix for these issues:

- Fixed an issue with scale factor on voltage metrics on Intel Platform code named Meteor Lake. Earlier a wrong scale factor was used in voltage calculation which affected data correctness of these metrics.*10e8d4*
- Fixed an issue in the feature -f acpi-dstate in which some devices were erroneously reported in the D3Hot state which should have been in D3Cold. *5a7a36*
- Fixed -f pch-ip-active on platform code named Meteor Lake (M/P) to report correct SLPS0 residency. *421fb6*
- Fixed an issue which caused SoCWatch to report an empty summary file when -r vtune command was provided.This issue was seen when CPU brand name was longer than 64 characters. *c568d5*
- Fixed an issue which caused the feature -f ddr-comp-bw to report large erroneous values. *01de32*
- Fixed an issue in -f display-pstate on Intel Platform code named Meteor Lake that caused huge values to be reported.*9eb4e4c*
- Fixed an issue in -f hw-dgfx-pstate on Intel discrete graphics code named DG2 and Arctic Sound Mainstream (M75 and M150) that affected data correctness.*9eb4e4c*

Version 2022.5

New

The 2022.5 release (*socwatch* driver v2.16.9.0, *cstracedrv* driver v2.5.0) contains these changes:

- Enabled support for feature hgs-feedback on Intel platforms code named Meteor Lake, Raptor Lake and Alder Lake. *938e0d*

Fixed

Release 2022.5 has a fix for these issues:

- Fixed an issue with os-cpu-cstate and os-cpu-pstate that caused empty result file. Now, an entry Unknown will be displayed in the summary table regardless of whether hibernation or standby occurred whereas, earlier, it would only be displayed in those cases. *c891630*
- Added note summary report table for acpi-dstate explaining how to interpret results in the event of questionable data.*8e635c*
- Fixed an issue on Intel Platform code named Meteor Lake where big core model ID in the summary report was reported as N/A when the device was configured with LP5 memory. Now the big core model ID is reported as RWC which is as expected. *42d074*
- Fixed an issue which caused all the PMT counters in Intel platform code named Meteor Lake to return incorrect data due to reading wrong offsets. *ce10b2*
- Fixed a regression where some PMT-based residency metrics (such as dgfx-cstate, dgfx-pkg-cstate) would display '0' residency for inferred states on all endpoints other than the first. *7aa3bf*
- Enhanced the error message for the features s0ix-subs-req and soc-s0ix-subs-req when bad data is received. The error message now reads "ERROR: Failed to parse s0ix LPM Requirements from raw data. Check that the SSRAM is populated correctly on your platform." *235c2e*
- Fixed a bug in the summary output for the feature pcie-ltr where the "N-Snp Lat Override Value" and "Snp Lat Override Value" values incorrectly reported "No Req" rather than the expected override latency values. *1919b2*
- Removed support for feature s0ix-subs-req on Intel Platform code named Alder Lake -N. It was not an intended feature on that platform.*235c2e*

Version 2022.4

New

The 2022.4 release (*socwatch* driver v2.16.9.0, *cstracedrv* driver v2.5.0) contains these changes:

- Added relevant error message when the result directory is not writable and causes SoC Watch to exit. The message "ERROR: Cannot create output files. Check if you have write permissions to result directory." is displayed when this occurs. *044efb2.*
- Added begin and end time stamps of collection in the SoC Watch results header output. *6b121a0.*
- Enabled support for new firmware for Intel discrete graphics code named Ponte Vecchio. The latest PVC firmware has these PMT GUIDs 0xfdc76195 and 0xb15a0edd for root and tile telemetry, respectively. *a2c41e9*

Fixed

Release 2022.4 has a fix for these issues:

- Fixed -f cpu-pkgc-dbg on Intel platform code named Alder Lake to read correct telemetry counters. Previously these were not in line with pcode. *6d2528f*
- Fixed -f pch-ip-active on Intel platform code named Meteor Lake, to report the table "PCH Active State (as percentage of PMC Active plus SLP_S0 Time) Summary: Residency (Percentage)" which was missing previously and removed duplicate SLP-S0 entries. *459f650*
- Fixed -f sa-freq on Intel platform code named Meteor Lake to use correct bitmask to read the address of the counter. *8863dd3*
- Fixed -f hw-igfx-pstate on Intel platform code named Meteor Lake to report correct Graphics P-state values. The register reporting the Graphics P-state has changed in Meteor Lake because the Graphics and Media counters are now separate. *16ed11f*
- Changed the ordering of memory read and write counts for -f ddr-bw on Intel platform code named Meteor Lake. *5109852*
- Fixed issues in Intel platform code named Meteor Lake for -f soc-s0ix-subs-dbg, -f soc-pch-platform-ltr and -f soc-s0ix-subs-res to read correct counter addresses. Added configuration file entries which were missing for Intel platform code named Meteor Lake for -f soc-s0ix-subs-res that caused zero values in the output table. *330dd81*
- Type C Subsystem features -f tcss-state and -f tcss-cfg-status are disabled in this release for Intel Platform code named Meteor Lake, for an issue which is not fixed yet. Collection of these features cause BSOD. *300ff90*

- Updated existing Intel Platform code named Lunar Lake metrics to behave like Alder Lake metrics until right documentation is available. Changed Lunar Lake config file to inherit Alder Lake metrics. *5e6269c*
- For Intel discrete graphics code named DG2, fixed bandwidth counters which were previously double counting resulting in bandwidth values higher than actual values. *c092386*
- Fixed an issue in trace output where column headers weren't following the same format in tables for certain metrics. *20e036d*
- Removed extra commas from a note in the summary table for -f ddr-bw. *fc871d4*
- Fixed an issue where both -t and -p options when specified together were not working as documented. *1ef27dd*

Version 2022.3

New

The 2022.3 release (*socwatch* driver v2.16.9.0, *cstracedrv* driver v2.5.0) contains these changes:

Fixed

Update release 2022.3 has a fix for these issues.

- Fixed crash in collecting metrics on Intel platform code named Raptor Lake. Previously, when hardware reports duplicate host GUIDs to SoC Watch, collection was failing or wrong data was reported.
- Fixed issue in ordering of tables in summary report. Previously, the order was incorrect in some cases.
- Fixed -f panel-srr to collect regardless of the status of PSR flags. Previously, collection failed if PSR flag was not ON at initial collection time. As a result of this change, data collected prior to this release cannot be re-processed (-i) using this release.
- Fixed column headers for feature xhci-lpm to include units in certain columns. Previously, there were no units for these columns.

Version 2022.2

New

The 2022.2 release (*socwatch* driver v2.16.8, *cstracedrv* driver v2.5.0) contains these changes:

- New features enabled for Meteor Lake are listed below. **Collection of these metrics requires installation of a PMT driver that supports Meteor Lake.** The *intelPMT.sys* driver included in Microsoft Windows OS client releases only supports Tiger Lake, Alder Lake, and Raptor Lake platforms. A temporary PMT driver is available for Internal Use Only. You will find this driver at the Intel Registration Center (IRC) site where you download the Internal SoC Watch package, along with a README text file containing installation instructions.

Feature Name	Description
cdie-cstate-dbg	Die C-state block/wake causes for Compute Die
cdie-cstate-res	Residency in Die C-states (DC2.1, D2.2, D3.1, D3.2, D6) for Compute Die
cdie-cstate-cnt	Entrance counts for Die C-states for Compute Die
cdie-core-cstate-res	Residency in Core C-states (CC0, CC1, CC6) on Compute Die
cdie-core-cstate-cnt	Entrance count for Core C-state CC6 for Cores 0-5 on Compute Die. [Counters for additional cores planned for B0]
cdie-ccp-pstate	CDie Converged Core Perimeter (CCP) IA Module (0-7) approximate residency in P-states
cdie-ccp-volt	CDie Converged Core Perimeter (CCP) IA Module (0-7) voltage
cdie-ccp-llc-bw	CDie Converged Core Perimeter (CCP) to LLC Read and Write bandwidth

Feature Name	Description
cdie-ring-cstate-res	Residency in Ring C-states (C0, C3, C6) on Compute Die
cdie-ring-cstate-cnt	Entrance count for Ring C-states C3, C6 on Compute Die
cdie-ring-pstate	Ring approximate residency in P-states on Compute Die
cdie-ring-volt	Ring voltage requirement on Compute Die
cdie-llc-flushed-res	Residency in LLC-FLUSHED state on Compute Die
cdie-llc-flushed-cnt	Entrance count for LLC-FLUSHED state on Compute Die
cdie-ltr	LTR thresholds for Die C-states on Compute Die
cpu-pkgc-dbg-res	Pkg C-state block/wake causes
cpu-pkgc-dbg	Pkg C-state Cannot go deeper/High residency reasons
cpu-pkg-cstate-res	Residency in Package C-states (PC2-PC10). [Same as hw-cpu-cstate PCx residency but includes PC2R]
cpu-pkg-cstate-cnt	Entrance counts for Package C-states
pkg-llc-flushed-cnt	Entrance count for Package LLC-FLUSHED state [No residency counter available]
soc-core-cstate-res	Residency in SoC Core C-states (C0, C1, C6). [Same as hw-cpu-cstate CCx residency]
soc-core-cstate-cnt	Entrance count for SoC Core C-state CC6
soc-ccp-pstate	SoC Converged Core Perimeter (CCP) IA Module 0 approximate residency in P-states
soc-ccp-volt	SoC Converged Core Perimeter (CCP) IA Module 0 voltage
soc-ltr	SoC LTR thresholds for Package C-states and LTR values for Display, IPU, PCH, CDIE
pmt-hw-igfx-cstate-res	Residency for integrated GPU RC states (RC0, RC6). [This is a hidden feature, same as hw-igfx-cstate]
hw-igfx-cstate-cnt	Entrance count for integrated GPU RC6 state
igfx-pstate	Integrated GPU approximate residency in P-states
igfx-volt	Integrated GPU voltage
igfx-busy	Time integrated GPU engine truly busy
igfx-rc0-idle	Time after all streams indicated idle until integrated GPU requested RC6 entry
igfx-rc6-entry-ovhd	Time integrated GPU took to go through the RC6 flow (including context save) after all conditions to enter RC6 were met
igfx-rc6-wake-ovhd	Time spent between end of integrated GPU RC6 wake sequence and engine starting to execute
vpu-bw	VPU memory bandwidth

Feature Name	Description
vpu-dstate-res	Residency in VPU D-states (D0 Active, D0i2 Active, D0i2 Idle, D0i3/D3)
vpu-dstate-cnt	Entrance counts VPU D-states (D0 Active, D0i2 Active, D0i2 Idle)
vpu-context-priority	Residency in VPU context priority RealTime, Normal, Focus, Idle
vpu-cstate-res	Residency in VPU C-states (C0, C6)
vpu-cstate-cnt	Entrance count for VPU C-state C6
vpu-pstate	VPU approximate residency in P-states
vpu-volt	VPU voltage requirement
memss-pstate	Memory subsystem (QCLK) approximate residency in P-states
memss-volt	Memory subsystem voltage requirement
media-cstate-res	Residency in Media C-states (C0, C6)
media-cstate-cnt	Entrance count for Media C6
media-pstate	Media approximate residency in P-states
media-volt	Media voltage requirements
ipu-cstate-res	Residency in IPU PS and IS C-states (C0, C6)
ipu-cstate-cnt	Entrance count for IPU PS C6 and IS C6
ipu-pstate	IPU PS and IS approximate residency in P-states
ipu-volt	IPU PS and IS voltage requirements
display-pstate	Display (CDCLK) approximate residency in P-states
display-volt	Display voltage requirement
display-bw	Display IO bandwidth Reads and Writes
display-vc1-bw	Display VC1 bandwidth (non-coherent read)
ngu-pstate	Next Gen Uncore approximate residency in P-states
ngu-volt	Next Gen Uncore voltage requirement
io-bw	Total IO bandwidth Reads/Writes
noc-gcd-bw	Graphics Die to NOC bandwidth on Bridge0/1
noc-ioc-bw	IO Cache to NOC bandwidth on Bridge0/1
noc-vpu-bw	VPU to NOC bandwidth on Bridge0/1
noc-ipu-bw	IPU to NOC bandwidth on Bridge0/1
noc-display-bw	Display to NOC bandwidth on Bridge0/1
noc-media-bw	Media to NOC bandwidth on Bridge0/1
noc-hac-bw	HAC to NOC bandwidth on Bridge0/1

Feature Name	Description
noc-cce-bw	CCE to NOC bandwidth on Bridge0/1
noc-idi2cmi-bw	IDI2CMI to NOC bandwidth on Bridge0/1

- Some legacy features have not been enabled yet for Meteor Lake. These include: pch-ip-active, soc-temp, pcie-lpm, pcie-ltr, xhci-lpm. These are being updated now and will be in the next release.
- On Meteor Lake, feature ddr-bw is broken down into bandwidth per subchannel for each memory channel.
- For features cpu-pkgc-dbg, cpu-pkgc-dbg-res, pmt-cpu-pkgc-dbg, and dgfx-pkgc-dbg, the following changes have been made to the summary report:
  - Added table "Total Samples Received" that shows the number of samples collected and the interval between samples.
  - Changed the title from “C-States” to "C-State" to be consistent with other features.
  - Changed the descriptions for the wake reasons to be "Wake caused by" instead of "Package C-state Wake from".

Fixed

Release 2022.2 has a fix for these issues:

- Features that report sampled residency data have changed the table name from “Sampled: Residency” to “Sampled: Approximated Residency” to set appropriate expectations for the data found in that table. Sampled residency is calculated using sampled values that are weighted by the time between samples, which is generally much less accurate than data obtained from actual residency counters. The table name was changed to emphasize the difference.
- For Intel platform code named Alder Lake –N, metrics for the PCH are now reporting correct data. Previously, some Alder Lake –N PCH were identified as Alder Lake –M PCH resulting in incorrect data reported for pch-ip-active and other PCH metrics. The issue occurred when ID’s for PCH –M were re-purposed for PCH –N. This issue was observed because the pch-ip-active feature report did not include the eMCC active counter which is only defined for PCH –N. Also, the PCH ID was identified as –M rather than -N.
- On Intel platform code named Alder Lake, feature cpu-pkgc-dbg now reports all the wake reasons. Previously, the following were omitted from the "High Residency in" tables:

Table Name	Counter Name
High Residency in PKG C0	PC0-DEEP-WAKE-PCH-INT
	PC0-DEEP-WAKE-DISP-INT
High Residency in PKG C2	PC2-DEEP-WAKE-SNOOP
High Residency in PKG C2R	PC2R-DEEP-WAKE-PCH-MEM
	PC2R-DEEP-WAKE-USB-LTR
	PC2R-DEEP-WAKE-PMCMBOX
	PC2R-DEEP-WAKE-PWR-BUTTON
	PC2R-DEEP-WAKE-EC2PCH
	PC2R-DEEP-WAKE-TIMER
	PC2R-DEEP-WAKE-PECI
	PC2R-DEEP-WAKE-OPI-DMI-PEG-SQUELCH
	PC2R-DEEP-WAKE-DISPLAY-BUFFER
	PC2R-DEEP-WAKE-DISPLAY-LTR
	PC2R-DEEP-WAKE-PCODE

	PC2R-DEEP-WAKE-TAP
	PC2R-WAKE-IPU
	PC2R-DEEP-WAKE-FIVR-ERROR
	PC2R-DEEP-WAKE-TYPEC
	PC2R-DEEP-WAKE-GEN4-HANG
	PC2R-DEEP-WAKE-PMIP
Transient and Uncommon Reasons	PC2R-DEEP-WAKE-RESET

- On Intel platform code named Tiger Lake, feature -f cpu-pkgc-dbg now includes reporting for reason WAKE_PKGS in the “Transient and Uncommon Reasons” table if it occurs. Previously, it was not reported.

Version 2022.1

New

The 2022.1 release (*socwatch* driver v2.16.7, *cstracedrv* driver v2.5.0) contains these changes:

- Added support for Intel server platform code named Sierra Forest. (Does not include feature -f dram-pwr because counter no longer exists.)
- For Intel platform code named Alder Lake and Meteor Lake, renamed feature -f pmt-cpu-pkg-cstate to -f cpu-pkg-cstate-res and removed redundant reports. This feature reports CPU C-state (PCx) residency data read from PMT, which includes the PC2R state. These residency values will be almost identical to the PCx residency values reported by feature -f hw-cpu-cstate. These are read from MSRs, but do not include PC2R. This feature is included in group cpu-pkg-cstate.
- Added support for 50Hz and 120Hz displays to feature -f display-rr. Previously, 50Hz was included with 60Hz and 120Hz was ignored.
- Added Meteor Lake -M support for features: cpu-pkgc-dbg, pch-ip-lat-limit, pch-slps0-dbg, pch-slps0-cfg, pch-ip-status, pch-platform-ltr.
- Enabled Lunar Lake support for basic CPU metrics. (Initial support, not tested.)
- Enabled NDA PMT metrics on Intel platform code named Raptor Lake. These include: llc-bw, ipu-bw, typec-bw, io-bw, soc-temp and soc-ltr.
- Added NDA support for feature -f display-state. Display state provides (DC5, DC6, DC6V) entry counts.
- Added power-gated status counts for PCIe controllers (SPE, SPF, and SPG) to feature -f pch-ip-status for Intel platform code named Alder Lake -S.
- Added external support for Intel platforms code named Alder Lake. Note: Does not include Intel platform code named Alder Lake -N.
- Added external support for feature -f dgfx-pwr on Intel discrete graphics card code named DG2 EU128 and EU512.
- Enabled support for new firmware for Intel discrete graphics code named DG2 and Arctic Sound -M. Use the latest firmware to allow collection of all metrics SoC Watch supports. Fewer metrics are supported on older DG2 firmware. The latest DG2 and ATS-M firmware have one of these PMT GUIDs 0x4f9502 and 0x4f9302 for EU128 and EU512, respectively.
- For discrete platforms DG2 and ATS -M, feature -f dgfx-pkg-cstate-status has been removed. This reported point-in-time C-state information incorrectly because the counters do not function. The feature that reports C-state residency (-f dgfx-pkg-cstate) is still supported.
- Reverted change from prior release, allowing use of option `--update-usage-consent yes`, to permit collection of tool usage analytics. This is permissible now because the text explaining the "yes" consent has been added to the help output and the User's Guide so that it will be read before use of the option.
- Changed the help output to provide better guidance on the usage of options `--input` and `--output`. Changes are reflected in the User's Guide.
- Made feature -f pmt-cpu-pkgc-dbg a hidden metric for platforms RPL and ADL, the same as on TGL.
- Removed hidden feature -f pmt-cpu-pkgc-dbg from NDA.

- Support for Intel platforms code named Broxton -M, Apollo Lake (Broxton-P), and Gemini Lake will be removed in the next SoC Watch release.

Fixed

Release 2022.1 has a fix for these issues:

- To prevent a system crash, the following features are disabled when Enhanced Sign-In Security (a.k.a., Virtualized Trusted IO or VTIO) is enabled on the system: s0ix-subs-dbg, s0ix-subs-req, xhci-lpm, pcie-lpm, pcie-ltr, pch-ip-active, and pch-ip-status. To use these features, turn off "Memory integrity" under "Core Isolation" in the Windows Security control panel or disable VTIO in the BIOS.
- Fixed issue which resulted in *"NOTE: Hypervisor Enforced Code Integrity is enabled on this system.*", being displayed when it was not enabled. This happened on systems on which DeviceGuard (HVCI and VBS) registry keys were present but not actually set to enabled.
- Fixed issue so that use of -f cpu-pkgc-dbg (from mailbox) no longer turns off PMT counting for Block Cause, Block Category, and Wake Cause counters. Previously, use of -f pmt-cpu-pkgc-dbg on its own, after once using -f cpu-pkgc-dbg, would result in all 0 values for the Block Cause, Block Category, and Wake Cause tables.
- Fixed correctness issues in the results of feature -f hw-cpu-pstate on Intel server platforms code named Sapphire Rapids, Granite Rapids, and Sierra Forest.
- Fixed incorrect values for IVR states in -f pch-ivr-state feature. Also changed the order of the summary table to go from highest power (lowest voltage reduction) to lowest power (highest voltage reduction) and changed the "Active" state name to be "No IVR" for more accurate naming. The new table ordering is: No IVR, IVR3, IVR2, IVR1
- On Intel platform code named Alder Lake, modified feature -f soc-temp in NDA package to no longer report temperature data for PCH, IPU, and TYPEC. The data is not valid.

Version 2021.4.1

New

Update release 2021.4.1 (*socwatch* driver v2.16.7, *cstracedrv* driver v2.5.0) contains these changes:

- Modified feature -f cpu-pkgc-dbg to report more detail for package C-state blocking and waking reasons on Intel platform code named Alder Lake. These include the "Cannot go deeper than" and "High Residency in" reports available on prior platforms. Internal Note: All of these counters have not been validated. If you find inconsistency in what they are reporting, please email *SoCWatchDevelopers*.

Version 2021.4

New

The 2021.4 release (*socwatch* driver v2.16.6, *cstracedrv* driver v2.5.0) contains these changes:

- Added NDA support for Intel platform code named Raptor Lake (does not include features using the PMT data source).
- Added external support for Intel platforms code named Tiger Lake -H and Rocket Lake.
- Added external support for Intel server platforms code named Ice Lake -X and Cooper Lake -X.
- Added NDA support for Intel platform code named Alder Lake -N.
- Added recognition of CPU ID for Meteor Lake-S.
- Added new option `--revoke-usage-consent` to remove consent to share Intel SoC Watch usage data via Google Analytics. Use this option as an alternative to the interactive option `--update-usage-consent`. Modified option `--update-usage-consent` to no longer accept ‘yes’ as a command line parameter. This had allowed customers to give consent without seeing the terms of consent.
- Removed "Blocking reasons" column from the -f pch-slps0-dbg report. This column contained the counter name which was the negative of the state description shown in the “IP State” column. This caused confusion as to which condition the “In State” and “Not In State” columns referred to.
- Added support for -f s0ix-subs-res, -f s0ix-subs-status, and -f pch-slps0 for Meteor Lake -M.

- Improved message when hibernation occurs to make it clear that option -m must be added to the collection command line to get correct reporting for residency data.
- Improved WakeupAnalysis histograms report for feature -f os-cpu-cstate when –m is used. It now sorts Cores and Threads in numerical order.
- If –f connected-standby was collected on a target platform with Intel SoC Watch v2021.2 or older, *cstracedrv.sys* must be removed before any collection using SoC Watch v2021.3 or newer. To remove *cstracedrv*, execute command `socwatch --disable-cstrace` then reboot the system. SoC Watch v2021.4 will display an error message and terminate if an incompatible *cstracedrv* driver is detected (this error will occur even if -f connected-standby is not specified in the command line). The *cstracedrv* driver enables feature -f connected-standby and was modified in SoC Watch v2021.3 making it incompatible with older versions of SoC Watch. The *cstracedrv* driver is automatically installed when feature -f connected-standby is executed for the first time on a platform (or when option `--enable-cstrace` is used prior to first use of -f connected-standby). Unlike the *socwatchdrv*, it remains installed at the end of collection and is reloaded after a reboot in order to capture complete information for connected standby reporting. The option `--disable-cstrace` is provided to stop the *cstracedrv* from being reloaded after every reboot, and must be followed by a reboot to complete the process before running the next *socwatch* collection command.

  NOTE On some systems (possibly due to OS version) a running older *cstracedrv* driver cannot be unregistered by a new *socwatch.exe* (i.e., use of option `--disable-cstrace` with the new version of *socwatch* on a *cstracedrv* installed by an older version of *socwatch*, will result in an error indicating that the driver cannot be stopped). If this occurs, a system crash (BSOD) will occur on reboot. To avoid the crash on reboot, you must manually delete the cstrace driver (*C:\Windows\System32\drivers\cstracedrv.sys*) and edit the registry *(regedit)* to delete its registry entry (*Computer\\HKEY_LOCAL_MACHINE\\SYSTEM\\CurrentControlSet\\Services\\cstracedrv*) before rebooting.

- Updated gahelper to new version with curl v7.79.1 to resolve security risks. Also signed gahelper.dll with new certificate.
- Support for Microsoft Universal Windows (OneCore) has been removed.
- Support for feature -f edram-state has been removed for all platforms following Intel platform code named Coffee Lake. The feature was erroneously carried forward (eDRAM is not used in newer platforms) so any result reported for newer platforms was invalid.

Fixed

Update 2021.4.1 has a fix for these issues.

- Improved SoC Watch driver to reduce system crash occurrences. Modified driver to reduce the occurrence of BSOD caused by error DRIVER_IRQL_NOT_LESS_OR_EQUAL.

Release 2021.4 has a fix for these issues.

- Use of `--option pch-count-always` with feature -f pch-ip-active on platforms that do not support counting only while in PC10 (i.e., Elkhart Lake, Ice Lake, and older platforms) now results in a warning being displayed and collection continues. Previously, use of that option on platforms that did not support it would result in an error and immediate exit. The option can be ignored on these older platforms because the counters are always counting.
- Removed unsupported IP counters from feature -f pch-ip-active for Intel PCH code named Alder Lake. Counters removed for ADP-S: GEN3-PLL, OPI-PLL, MIPI-PLL, MPHY-PG-CORE-CMN-LANE, MPHY-SQUELCH, PSF3-PSF4-ACT-CNT-Gx, PSF1-PSF2-PSF5-ACT-CNT-Gx, MPHY-PER-LANE-CORE-PG, USB2-PER-LANE-SUS-PG, USB2-PER-LANE-CORE-PG, CNVi-PLL, SDXEMMC, UFS. Counters removed for ADP-P/N: PSF3-PSF4-ACT-CNT-Gx, PSF1-PSF2-PSF5-ACT-CNT-Gx, SCS-SDX, FIVR-VCCIO-ON, Ungated-USB-Ports.
- Fixed feature -f s0ix-subs-dbg to report hibernation time as "Unknown". Previously, hibernation time was included in the "Blocking" time.

- Reporting has been improved for features –f sata-lpm and -f xhci-lpm. Previously, the capabilities and state data reported could be wrong in certain circumstances. As a result of this change, data collected prior to this release cannot be re-processed (-i) using this release. The problem occurred due to a serialization issue.
- Fixed feature -f dpst so that re-processing (use of option -i) will report the active display and DPST information for the system on which the original collection occurred. Previously, this data was not stored, so when -i was used to re-process the collection files this information was being retrieved at the time the re-processing was done for the system on which the re-processing command was executed.
- For Intel discrete graphics card code named DG2, feature -f dgfx-pkgc-dbg now reports only the "Wake Cause" table. It no longer reports "Block Cause" and "Block Category" reasons because these counters are no longer valid (disabled by Pcode for performance reasons).
- Fixed incorrect reporting of the LTR values in feature -f dgfx-soc-ltr for DG2. Previously, the calculation for the reported LTR values was incorrect. As a result of this change, data collected prior to this release cannot be re-processed (-i) using this release.
- Fixed ordering of PCx states for the Threshold values reported by feature -f soc-ltr on Intel platform code named Alder Lake.
- Introduced a driver change to reduce the occurrence of DPC_WATCHDOG_VIOLATION timeouts which result in a system crash.
- Fixed Driver Verifier detected memory leak in feature -f edram-state which resulted in a system crash.

Version 2021.3

New

Update release 2021.3.1 (driver v2.16.2.1) is a bug fix release. For changes, please see Fixed Issues section.

The 2021.3 release (*socwatch* driver v2.16.0, *cstracedrv* driver v2.5.0) contains these changes:

- Added feature -f s0ix-subs-req on Intel platform code named Alder Lake (-P only). This feature reports the requirements for entry to S0ix.y states for each IP, including the Bus/Device/Function (B/D/F) IDs when applicable. This feature should be used in conjunction with feature –f s0ix-subs-dbg which shows residency of the requirements that are met. The requirements table is static so there is no trace data. The trace file indicates this with "Trace not applicable - table is static". The data also cannot be imported to Intel® VTune™ Profiler, so it is excluded when generating .pwr file (via -r vtune). Use of this feature requires firmware with PMC v1013, found in ADP-P IFWI 2021ww22.4.01 and newer.
- Added support for metrics from PMT data source on Intel platform code named Raptor Lake (-S and -P). These metrics include: cpu-pkgc-dbg, display-bw, io-bw, ipu-bw, ipu-state, llc-bw, llc-state, pcie-bw, osreq-pkg-cstate-blocked, osreq-pkg-cstate-res, perf-limit-rsn, pkg-llc-flushed, pkg-pwr-limit-exceeded, psys-pwr-limit-exceeded, soc-ltr, soc-temp, typec-bw, and hidden metrics ddr-comp-bw, pmt-cpu-pkg-cstate, pmt-current, pmt-power, pmt-volt. (Internal only support as functionality could not be verified at time of release.) NOTE: An updated *intelpmt* driver that recognizes Raptor Lake is required. These features will report as unknown if the updated *intelpmt* driver is not installed on the target platform.
- Use of feature –f connected-standby with v2021.3 SoC Watch requires removal of any older version of *cstracedrv.sys* installed on the target platform (due to an internal change). The *cstracedrv* driver is automatically installed when feature -f connected-standby is executed for the first time on a platform. Unlike the *socwatchdrv*, it remains installed at the end of collection and is reloaded after a reboot. To remove *cstracedrv*, execute the command: `socwatch --disable-cstrace` and then reboot the system. Intel SoC Watch will display a message and terminate for any collection if an old *cstracedrv* driver is detected.

Fixed

Update release 2021.3.1 has a fix for these issues.

- Enhanced support for platforms containing many sockets and/or discrete graphics cards. Previously, the data reported was limited to the first 10 sockets and/or discrete graphics cards found, but that limit has been removed.

- Modified option --update-usage-consent so that the purpose of the consent is always displayed before consent is given.

The release 2021.3 has a fix for these issues.

- Fixed feature -f cpu-pkgc-dbg on Intel platform code named Alder Lake and –f dgfx-pkgc-dbg on Intel discrete graphics cards code named DG1 and DG2. Previously, the labeling of the reasons in the Block Cause, Block Category, and Wake Cause tables was incorrect.
- Corrected feature -f pcie-lpm reporting of table "Root Port vs CLKREQ Mapping" on Intel platform code named Alder Lake-S, and extended the list of Root Port mappings for Alder Lake (–S and –P). Previously, all CLKREQ # values were showing a value of 31 and the mapping stopped at 32 entries. The error occurred due to a change in register offsets for ADP-S and an additional mapping register added for ADP PCH.
- Fixed regression in –f pcie-lpm and –f pcie-ltr for detection/reporting of NVMe re-mapped devices. The regression occurred in SoC Watch v2021.1 such that NVMe re-mapped devices did not appear in summary and trace reports.
- Fixed issues in features pcie-lpm and pcie-ltr and added reporting of device name and port B/D/F for both Root port and End point (when present). Previously, the device name and port B/D/F may have been incorrect in addition to incorrect capability and state information. Also, the previous report gave the End point name with Root port B/D/F. These changes mean that results collected with prior versions of SoC Watch cannot be correctly re-processed (-i option) using v2021.3.
- Fixed issue in feature –f display-rr link rate discovery for Intel platforms code named Tiger Lake and Alder Lake (using Gen11 and beyond with19.2 or 38.4 MHz crystal clock frequency). Previously, an error was reported.
- Feature –f s0ix-subs-dbg no longer reports the "Breaking Reasons” table. This table was incorrectly reporting the count as residency, so it has been removed until it can be corrected.
- Removed references to unused component (UFS1) from features s0ix-subs-dbg, s0ix-subs-status, and pch-slp0-dbg on Intel platforms code named Tiger Lake and Alder Lake.
- Fixed issue in calculating the residency time for features –f llc-state and –f ipu-state. Previously, the data being reported was scaled incorrectly.
- Feature -f perf-limit-rsn has been disabled for Tiger Lake and the calculation corrected for Alder Lake. The counter is wrong for Tiger Lake and the data as reported was not scaled correctly for Alder Lake.
- Corrected feature -f dgfx-volt reporting for Display on Intel discrete graphics cards code named DG1 and DG2. Previously, the data reported was not scaled correctly for the Display voltage only.
- Corrected feature -f dgfx-temp reporting for LLC and removed unused component on Intel discrete graphics card DG1 (A-step). Previously, the wrong offset was being read for LLC temperature and the unused IPU component temperature was being shown.
- Fixed issue in feature –f dgfx-vf-pwr on Intel discrete graphics cards code named Arctic Sound and Ponte Vecchio. Previously, values for VF1 power were reported incorrectly due to a data formatting issue.
- Data from feature -f core-scale can now be imported in Intel® VTune™ Profiler. Previously, an error was reported.
- Modified collection behavior for feature –f pch-ps-on. Previously, at the start of collection SoC Watch checked the BIOS CEC_EN setting to determine if the platform was configured to turn off the power supply when system requirements were met (i.e., determine if PS_ON# was enabled). If it was not enabled, the feature would report “PCH PS-ON# is not enabled on this system”. That check has been removed because the enabled setting will not occur until the platform is ready to turn off the power supply and SoC Watch would not be running at that time. Instead, the residency counter is sampled at the end of collection (more frequently if –m is specified) so that when SoC Watch is awakened it would collect any increment that occurred. This means that when 0 residency is reported it could be due to multiple reasons, so the following note has been added to that report: “Note: Unable to check if PS_ON has been enabled for this system. If residency is 0 then check BIOS setting for PS_ON enabling. If PS_ON is enabled in the BIOS then either the requirements for BIOS to set the bit allowing PS_ON may not be met or the runtime requirements were not met."
- Feature –f hgs-feedback has been disabled in this release, due to known error that is not yet fixed. It has been a hidden feature due to incomplete support for reporting HGS+ class index.

- Modified several recently added features that have accumulators as their data source to only read at start/end of collection unless –m option is specified. This data is equally accurate whether sampled or not so this change will reduce overhead for collections that do not require max detail. Previously, these features were always sampling. The features impacted are: ipu-state, llc-state, perf-limit-rsn, and pkg-llc-flushed.
- Aligned *socwatch* driver behavior for PCI/MMIO read/write operations across Windows and Linux OSes. Also, fixed behavior of write operations.

Version 2021.2

New

The 2021.2 release (driver v2.15.7) contains these changes:

- Extended support for Intel platform Raptor Lake to include another CPU Model ID (0xBF).
- Added support for ADL-N PCH.
- Added NDA support for the following features on Intel discrete graphics code named DG2 512EU B-step and DG2 128EU A-step and B-step. The distinction between DG2 128EU A-step and B-step has been removed because the support is the same. For best dgfx metric data, use latest firmware. (Firmware from ww28 was used to determine which features to expose in NDA because the results looked reasonable.):
  - -f dgfx-pkgc-dbg: Reports discrete graphics package C-states.
  - -f dgfx-bw: Reports discrete graphics bandwidth data for IDI_READS, IDI_WRITES and DISPLAY_VC1_READS.
  - -f dgfx-temp: Reports discrete graphics temperature for GT, DRAM, SA.
  - -f dgfx-pwr: Reports discrete graphics package energy.
  - -f dgfx-volt: Reports discrete graphics voltage.
  - -f dgfx-current: Reports discrete graphics current for SA, MC, DDR, GT.
- Modified features for Intel discrete graphics code named DG1 and DG2:
  - -f dgfx-current:
    - Added reporting of maximal virus current for additional IPs.
    - Table name was changed from "Current" to "Maximal Virus Current" so that it correctly labels the data being collected. Previously, the data was reported as current at a point in time, but that data is not available. The hardware sensor that reports current is broken, so point-in-time current data is not available.
    - Removed table "Sample Residency (Percentage)" because using sampled data to approximate residency can be misleading.
  - -f hw-dgfx-pstate:
    - Removed reporting of frequency for UNSLICE-LOWER for DG2 because it was not reporting valid data. This was intended for reporting unslice frequency at 1MHz granularity rather than 50MHz, but reports only 0 values.
- Added feature -f dgfx-dstate for Intel discrete graphics code named DG2 (stepping B-512 and A-128). This reports DG D-state residency for D3Hot and D3Cold-VRAM-SRR.
- Added PMT features for Intel platforms code named Tiger Lake and Alder Lake:
  - -f soc-ltr: Added reporting of LTR Threshold requirements for each package C-state. This feature also reports the LTR values for each IP at the time entry to a package C-state was being determined, so you can see which IP’s LTR would block entry to a particular package C-state. Note: Alder Lake C-step is required to get non-zero data in the LTR Values report. Also, the TypeC LTR value may still report only 0 values.
  - -f perf-limit-rsn: Reports residency of performance limiting reasons (Thermal/Power/EDP/Other) per IP (Core or Module, GT, LLC, IPU, Pkg). Also includes PROCHOT and VRHOT residency. This is a breakdown of the performance limiting (frequency throttling) reasons reported by features ia-throt-rsn, gt-throt-rsn, and ring-throt-rsn. (Internal only due to uncertainty in counter correctness.)
  - -f ipu-state: Reports active (C6) residency time in the Imaging Processing Unit's (IPU's) Input System (IS) or Processing System (PS).

- -f llc-state: Reports residency time in states C3 (LLC retention) and C6 (LLC flushed and off).
- -f osreq-pkg-cstate-res: Reports time that the OS requested each Package C-state. Part of group feature osreq-pkg-cstate. Residency is calculated as % of total collection duration.
- -f osreq-pkg-cstate-blocked: Reports time that the OS requested Package C-state was blocked. Part of group feature osreq-pkg-cstate. Residency is calculated as % of total collection duration.
- -f os-req-pkg-cstate: Use this group name to collect both of the above features. While this is currently a group name, we expect this to replace the individual feature names in a future release that combines reporting so that the blocked time can be reported as a % of the requested time.
- -f pkg-llc-flushed: Reports residency in Package C-state LLC_FLUSHED. This is a temporary feature. The reporting of LLC_FLUSHED will be included in a package C-state feature in a future release.
- -f core-scale: Reports per core scalability percentages that are calculated by the Punit as unstalled clocks divided by total active clocks.
- -f core-max-freq: Reports the per core maximum allowed frequency (P-Alpha).
- -f core-auto-freq: Reports the per core autonomous mode frequency target.
- -f pe-freq: Reports the Power Efficient (PE) frequency for IA and GT. (Not available on Tiger Lake due to counters not being implemented for reading from its PMT.
- -f core-freq-select-rsn: This is a group feature name that collects core-max-freq, core-auto-freq, and pe-freq features that together form the basis for decision on the P-state frequency selected.

- Enhanced WakeupAnalysis reported by feature –f os-cpu-cstate when –m is included:
  - Added table *Histogram of Overall Idle Duration per Process* to report histogram of the lengths of idle time between active time for each process. Three tables are produced that report Idle Hit Count, Idle Time in milliseconds, and Percentage of Total Collection time for each idle duration bucket.
  - Modified existing table *Histogram of Overall Busy Duration per Process* that reports histogram of the lengths of busy time per process to include partial busy times for processes that start prior to collection start or that end after collection ends. Also modified the percentage table to calculate percentage as ratio of total collection duration rather than total busy time for all processes. As a result, the table name changed from *Histogram of Overall Busy Duration per Process: Percentage of Total Busy Time* to *Histogram of Overall Busy Duration per Process: Percentage of Total Collection Time*. This makes the data comparable to the idle histogram report and it provides a consistent time basis for comparison of an individual process's % number from run to run. The previous percentage calculation gave a comparison between processes in a single run.
- Improved support for ia-throt-rsn and cpu-pkgc-cfg on newer platforms when Windows* OS security modes (HyperV, VBS, HECi) are enabled on the platform. This is now disabled only if the platform CPUID is not included in the installed Windows OS approved list for the required register. When this occurs, Intel SoC Watch will print a message indicating the feature that could not be collected. For example, "NOTE: Cannot collect feature: ia-throt-rsn (restricted by OS security settings)".
- Disabled hidden feature -f hw-cpu-pstate-per-core. This feature is being deprecated because it is not valid on platforms starting with Ice Lake. Please email SoCWatchDevelopers if there is a business need for continuing this support.
- Modified hidden PMT metrics for Alder Lake and Tiger Lake:
  - -f pmt-volt: Added reporting of voltage for additional IPs.
    - On TGL: per Core, Display, GT Slice, GT Unslice, LLC, and SA.
    - On ADL: per Module, GT Slice, GT Unslice, LLC, and SA. Note: Only SA is expected to have valid values because VR is external on ADL vs. TGL where it is internal.
  - -f pmt-current: Added reporting of maximal virus current for additional IPs.
    - On TGL: per Core, GT Slice, GT Unslice, LLC, and SA.
    - On ADL: per Module, GT Slice, GT Unslice, LLC, and SA. Note: Only SA is expected to have valid values because VR is external on ADL vs. TGL where it is internal.
- Updated Google Analytics library to resolve curl security issue.
- Changes that occurred in v2021.1 that were not recorded in those release notes are:
  - -f dgfx-ddr-bw was re-named to dgfx-bw because there are non-DDR bandwidths included in the report.

- -f dgfx-cstate-res was renamed to simply dgfx-cstate and report labels changed as follows:
  - Changed the report to label the inferred state as "RC0" rather than "Not RC6" since there are no additional states.
  - Added "GT" to more precisely label the C-states.

Fixed

Update release 2021.2 has a fix for these issues.

- Alder Lake platforms now show hidden PMT feature -f ddr-comp-bw in the help output. This is an internal only metric because the PMT counter for this data is under debug.
- Fixed correctness issue in feature -f s0ix-subs-dbg which is available on Intel platforms code named Tiger Lake, Alder Lake, and Elkhart Lake. A mask was missing resulting in the wrong data address being read.
- The report for PMT features -f pkg-pwr-limit-exceeded and -f psys-pwr-limit-exceeded no longer include *Not Exceeded* state. That state was being inferred and was an incorrect assumption. These features are available on Tiger Lake and Alder Lake platforms.
- Fixed detection of PSR2 enabled setting on Intel platform code named Alder Lake when an eDP display is active. Previously, there was an error in detecting when PSR2 was enabled which resulted in panel-srr being reported as unsupported. If the system does not have an active eDP display the tool reports "NOTE: eDP not detected. Panel self-refresh is not supported on this system."
- The following fixes are now in feature -f pcie-lpm and -f pcie-ltr:
  - When PEG external graphics cards are present on the system, feature -f pcie-lpm now correctly reports LPM link states (Lx) on platforms with Intel chipsets code named Cannon Point and newer. Previously, residency was reported as 100% Down state for PEG devices.
  - Corrected feature -f pcie-lpm reporting of LPM link states and -f pcie-ltr reporting of LTR values for VMD controllers when they are in D3. Previously, if the VMD controller entered the D3 state, the link state residency would be reported as Other and the LTR values would be extremely high. This was caused by the memory region being blocked while the VMD controller was in D3, which Intel SoC Watch has worked around.
  - VMD managed devices are now reported by features -f pcie-ltr and -f pci-lpm with the name "Intel VMD managed NVMe Controller (B:D:F)" that includes the Bus/Device/Function. Previously, they were reported as device 0x09AB.
  - These fixes make Intel SoC Watch v2021.2 incompatible for re-processing (using option -i) collections of pcie-lpm, pcie-ltr, or sata-lpm data collected with older versions of SoC Watch. Use an older version of SoC Watch to re-process older collections.
- Feature -f tcss-state report now has the TCCold (inactive) state at the end of the table. Previously, the TCCold state was in the middle of the table.
- PMT Feature -f cpu-pkgc-dbg now has the unit "counts" in the *Wake Cause* table. Previously there was no unit to reflect what the values indicated.
- Improved the Intel SoC Watch driver behavior so that it does not result in a BSOD when the Microsoft* Driver Verifier settings are enabled on the platform during collection. The problem occurred when the intelPMT.sys driver left the IRP in STATUS_PENDING. SoC Watch now returns an error when this occurs so that Driver Verifier does not flag an IO manager violation.
- The group feature name -f dgfx-pwr has been removed for DG2, only the individual feature with the same name remains, so it now appears in the help output only as an individual feature name. The features -f dgfx-psys-pwr-limit-exceeded and -f dgfx-pkg-pwr-limit-exceeded that had been in that group are included in groups dgfx-pwr-limit-exceeded, dgfx, and power.
- Command line option --log (-l) has been fixed. It was broken in v2021.1.
- Improved tool error handling to reduce silent tool failure during post-processing of collections that entered low-power states which resulted in no summary report.

Version 2021.1.1

New

Update release 2021.1.1 is a bug fix release. For changes, please see **Fixed Issues** section.

Fixed

Update release 2021.1.1 has a fix for these issues.

- Fixed reporting of TCx states in feature -f tcss-state for Intel platforms code named Tiger Lake -H and Alder Lake. The TCx state residency was reported incorrectly on those platforms due to a change in counter location that has been corrected in this release.
- Fixed feature -f cpu-pkgc-dbg for Intel platform code named Alder Lake. The IP "FMHC" is now correctly listed in the Block Cause table. Previously it was listed as a Block Category. Also, the Wake Cause table now labels the Total column with its unit of measure, "count". (Note: Use of this feature is delayed awaiting a firmware release that enables it.)

Version 2021.1

New

The 2021.1 release (driver v2.15.5) contains these changes:

- Added "experimental" PMT metrics support for Intel platform code named Alder Lake, SKUs S (B-step only), P, and M. Experimental means that these reports should be used with caution because verification of these features was not possible at the time of this release. *Note: Collection of these features requires driver intelPMT.sys which is available in Windows* OS Cobalt builds beginning with EEAP build #21318.* (Device Manager will show failure to load (yellow bang) Platform Monitoring Technology Driver due to error introduced by microcode patch 0x15. Firmware version with fix is not known at the time of this release, see HSD's: 16012983281, 22012672089.) :
  - cpu-pkgc-dbg: For debugging low residency in package C-states (reports blocking and waking reasons). This feature report is different from prior platforms. It reports residency values rather than counts, but no longer pairs the what and why for each reason. It reports three tables containing residency for Block Cause, Block Category, and Wake Cause. The Block Cause table indicates how long a particular component/IP was blocking entry to Package C-states below PC6. The Wake Cause table indicates how long the component/IP was causing wakeups from deeper states. The Block Category table reports residency for each blocking reason. When there are multiple causes and categories, the correlation is unclear. This will be improved for future platforms.
  - soc-temp: Reports SoC component temperatures (e.g., IA, GT, LLC, PCH, Module, PCIe, SA, IPU, TypeC)
  - ddr-comp-bw – Reports DDR bandwidth breakdown for IA, GT, and IO (total Reads+Writes). (Internal only and hidden due to unclear data source)
  - io-bw – Total IO bandwidth (Read/Write breakdown).
  - display-bw – Display IO bandwidth (Read/Write breakdown).
  - ipu-bw – Image Processing Unit IO bandwidth (Read/Write breakdown).
  - pcie-bw – PCIe Gen4 IO bandwidth (Read/Write breakdown).
  - typec-bw – TypeC IO bandwidth (Read/Write breakdown).
  - llc-bw – Per Core Last Level Cache (LLC) bandwidth and GT LLC bandwidth (Read/Write breakdown).
  - bw-all – Group name that collects all the above bandwidth metrics.
  - soc-ltr: Reports the Latency Tolerance Reported values for Display, IPU, PCH, TypeC subsystem, and PCIe. (Internal only)
  - pwr-limit-exceeded - Group name for -f pkg-pwr-limit-exceeded and -f psys-pwr-limit-exceeded. Reports time when package power limit (PLx) and platform power limit (PSYS PLx) is exceeded. (Internal only)
- Added PMT metrics support for Intel platforms code named Tiger Lake (B-step and newer). *Note: Collection of these features requires driver intelTA.sys or intelPMT.sys which is available in Windows* OS 20H1 builds or newer:*
  - pmt-cpu-pkgc-dbg: (These counters have not been validated on Tiger Lake.) This hidden feature is an alternative to cpu-pkgc-dbg on Tiger Lake, but replaces it on Alder Lake and beyond. See description of cpu-pkgc-dbg for Alder Lake.

  - soc-temp: Reports SoC component temperatures (e.g., IA, GT, LLC, PCH, Module, PCIe, SA, IPU, TypeC)
  - ddr-comp-bw – Reports DDR bandwidth breakdown for IA, GT, and IO (total Reads+Writes). (Internal only and hidden due to unclear data correctness)
  - io-bw – Total IO bandwidth (Read/Write breakdown).
  - display-bw – Display IO bandwidth (Read/Write breakdown).
  - ipu-bw – Image Processing Unit IO bandwidth (Read/Write breakdown).
  - pcie-bw – PCIe Gen4 IO bandwidth (Read/Write breakdown).
  - typec-bw – TypeC IO bandwidth (Read/Write breakdown).
  - llc-bw – Per Core LLC bandwidth and GT LLC bandwidth (Read/Write breakdown).
  - bw-all – Group name that collects all the above bandwidth metrics. This replaces the data collected with ddr-bw in v2020.5.
  - soc-ltr: Reports the Latency Tolerance Reported values for Display, IPU, PCH, TypeC subsystem, and PCIe. (Internal only)
  - pwr-limit-exceeded - Group name for -f pkg-pwr-limit-exceeded and -f psys-pwr-limit-exceeded. Reports time when package power limit (PLx) and platform power limit (PSYS PLx) is exceeded. (Internal only)
- Added support for PMT metrics collection on TGL-R (GUID 0x1701) and TGL-C (GUID 0x1602). (Internal Only)
- Added new (non-PMT) features for Intel platforms coded named Tiger Lake and Alder Lake:
  - ddr-bw: Modified ddr-bw to report total bandwidth per memory channel with Read/Write breakdown. This is collecting the same free running counters reported by EMON. Use feature group -f bw-all to collect the breakdown bandwidth data formerly reported by -f ddr-bw on Tiger Lake. (This data has been broken into separate features/tables so that it no longer totals unrelated bandwidth.)
  - pwr-limits: Reports package power limits (PL1-PL4) and platform (PSYS) power limits (PSYS PL1-PL2), Tau values (time allowed in a particular power limit), and the TjMax TCC offset. Both MSR and MMIO power limit settings are reported.
  - pwr-limit-locks: Reports package and platform power limit locks and enable status information.
- Added support for Alder Lake -N CPU (no PCH support yet). (Internal Only)
- Added NDA support for PCH on Intel platform code named Alder Lake (-P, -M) .
- Added NDA support for feature –f s0ix-subs-dbg on Intel platform code named Alder Lake (-S, -P, -M).
- Modified feature -f display-state to include entry count for state DC6V on Alder Lake. This state is only valid on ADL-P and ADL-M, and is always 0 on ADL-S. This is the low-power DC6 Video-playback state (display engine off + PSR2 + video playback). It requires a display that supports eDP.
- Added initial support for Meteor Lake (no support for PCH or PMT telemetry) (Internal Only):
  - Cores are identified as Redwood Cove (RWC) for big Core or Crestmont (CMT)for Atom.
  - Feature -f cpu-igpu-concurrency results are suspect.The GT-C0 MSR was not available, therefore residency reported for *iGPU Only* is always 0, and the *Both* and *Neither* values are suspect.
- Added support for Raptor Lake and Raptor Lake PCH-S. These have been enabled to support the same telemetry as Alder Lake, excluding metrics from PMT. (Internal Only)
- Added support for Granite Rapids (not tested). (Internal Only)
- Added the following information to the top of the summary and trace reports:
  - System Name
  - Operating System name and build number
  - Added GUID to PMT description (as hexidecimal value)
- Extended the message that is displayed when hibernation occurs to explain how the accuracy of hibernation time can be improved if needed, "Adding option -m can increase the accuracy of the time attributed to hibernation."
- The Automation_Summary report (generated when using -r auto) now includes summary data for features ia-throt-rsn, gt-throt-rsn, and ring-throt-rsn, as well as other features which contain the table “Summary – Sampled: Counts”.
- Modified order of feature reports within the summary file to bring relevant data closer together for faster reference.

- The _WakeupAnalysis.csv report (generated when -m is used with feature os-cpu-cstate) has been modified as follows:
  - Separate tables for Idle and Busy histograms that report counts and time. Previously, these histogram tables had count and time values in a single table. Table titles were changed as part of this separation.
  - Added table “Histogram of Overall Busy Duration per Process: Percentage of Total Busy Time” to provide % calculation for the corresponding “Busy Time” table.
- Feature -f pch-ip-active now includes table "PCH Active State (as percentage of PMC Active plus SLP_S0 Time)" on Intel platform code name Tiger Lake and beyond, when PCH active count policy is the default (i.e., count only if in PC10). This table reports the % of active time while in PC10 when the default policy is in effect. When –option pch-count-always is used, this table reports the % of total collection time. A note is included with the report which states which counting policy is in effect and whether the % is for total PC10 time or total collection time. Note that with the default counting policy, the PMC active time represents the time in PC10 prior to entry to any S0ix because it stops counting on entry to S0i2.0 or lower. SLP_S0 is the total time in S0ix.y states, during which PC10 is still in effect. Therefore, the sum of PMC active time and SLP_S0 time is the total PC10 time.
- Feature -f pch-ip-status now includes power gated status for SPE and SPF PCIe Controllers on Intel platform code named Tiger Lake (-H).
- Renamed several feature names for Intel discrete graphics card code named DG1:
  - dgfx-cstate is the new (simplified) feature name for -f dgfx-cstate-res
  - dgfx-pkg-cstate is the new (simplified) feature name for -f dgfx-pkg-cstate-res
  - dgfx-pkg-cstate-status is now a hidden feature due to unreliable data (Internal only)
- Added support for the following discrete graphics cards (collecting these metrics requires the CTA driver to be installed, see Installation Notes):
  - Intel discrete graphics card code named DG2 128EU (A-step) and DG2 512EU (B-step):
    - dgfx-bw: Memory bandwidth statistics for discrete graphics
    - dgfx-cstate: GT C-state (RCx) residency for discrete graphics
    - dgfx-cstate-status: GT C-state (RCx) status for discrete graphics (Internal only and now hidden due to unreliable data.)
    - dgfx-pkg-cstate: Package C-state (PCx) residency for discrete graphics (hardware measured)
    - dgfx-pkgc-dbg: Package C-state blocking and wake reasons for Package C-state entry and exit for discrete graphics (Internal only)
    - dgfx-pwr: Power statistics for discrete graphics
    - dgfx-current: Current statistics for discrete graphics (Internal only)
    - dgfx-temp: Temperature statistics for discrete graphics (Internal only)
    - dgfx-volt: Voltage statistics for discrete graphics
    - hw-dgfx-pstate: Graphics P-state frequency status for discrete graphics
    - dgfx-pkg-pwr-limit-exceeded: Package Power Limit exceeded residency for discrete graphics (Internal only)
    - dgfx-psys-pwr-limit-exceeded: Platform Power limit exceeded residency for discrete graphics (Internal only)
    - dgfx-soc-ltr: Latency Tolerance Reporting values for components on discrete graphics (Internal only)
    - Note: DG2 512EU A-step is not supported. There is a hardware issue which prevents access to PMT data.

Fixed

The 2021.1 release has a fix for these issues.

- Fixed feature –f tcss-state to correctly report residency in TCCold when no TypeC device is attached. Previously, TCCold time was reported as TC0Unblocked 100% when no device was attached. TCCold residency is now determine to be the actual hardware state when the IOM sets the IN_TCCOLD status register. This overrides the TCx state residencies reported by PUnit , which is unaware of IOM state

changes in and out of TCCold. TCCold will only occur if no device is attached. When a device is plugged in, the TypeC subsystem comes out of TCCold, the IOM clears the status register, and responds to TCx state requests from the PUnit. In this case, SoC Watch reports the residencies for the TCx states.
- Fixed error in feature -f acpi-dstate which resulted in empty result file if S3/S4 occurred during collection. SoC Watch failed during post-processing due to change in the OS events (first seen on early Windows 10X builds) when an S3/S4 entry event occurred during collection, such as closing the lid. In addition, time is now properly allocated to Unknown state for the S3/S4 time period.
- Improved error handling to reduce occurrences of empty or no .csv summary result files occurring at end of a collection without any error message.
- Fixed issue where SoC Watch would silently fail before producing any results, while post-processing a collection with feature –f connect-standby, if the system entered Modern Standby.
- Fixed error in feature -f pch-ip-active reporting of "Physical Mode Lane Assignment" table and “PCH Active Not Power Gated Counts Summary”] on Intel platforms code name Tiger Lake (-LP and -H). This was caused by an undocumented shift in counter offsets.
- Corrected reporting of feature -f pch-ip-active on Intel platform code name Alder Lake (-P). Added missing IP (UFSX2) counter, which shifted a large portion of IP names so that they are now correctly aligned with their counters (e.g., FIVR-VNN-ON), and fixed the Physical Mode Lane Assignment table.
- Feature -f sata-lpm now reports on SATA controllers configured in a VMD that includes more devices than the SATA.
- Fixed error in feature -f s0ix-subs-status on Intel platform code named Tiger Lake. The power gated counts were not labeled with the correct IP name. This was seen because the power gated status reported by features -f pch-ip-status and -f s0ix-sub-status did not match for the same IP.
- Modified feature -f s0ix-subs-dbg to collect this data using a different byte alignment. (A 4-byte aligned read is now used to avoid a firmware issue that occurred when reading these as 2-byte values, that could result in system hang). The reported results are the same, but the change means you cannot use option -i to re-process s0ix-subs-dbg reports from prior verions using SoC Watch v2021.1.
- Resolved an issue with feature -f s0ix-subs-dbg where the blocking reason counters would not increment if collected without feature -f pch-ip-active. Additional enabling settings were required.
- Fixed issue in -f pcie-lpm where collection failed with "couldn't enumerate PCI devices". Now it prints a warning on the console ("Failed to retrieve BDF for a pcie device"), and continues collection for other devices.
- Fixed features -f pcie-ltr and -f pcie-lpm Capabilities reports to include PEG entries. Discovery of the capability offset was changed to be dynamic to resolve the incorrect reporting and missing devices.
- Corrected discovery of device names to resolve reporting of unknown device which could occur when collecting both -f pcie-lpm and -f xhci-lpm.
- Improved error message given when re-processing a SoC Watch result with option -i <*result-name*> and the <*result-name*> parameter is missing. Previously, the error was unclear.
- Fixed feature -f display-state reporting of DC5 and DC6 entrance counts on Tiger Lake, Alder Lake, and Rocket Lake. SoC Watch is now using the counter offsets defined in the graphics Bspec for newer platforms, rather than the internally provided (undocumented) offsets used for the older platforms.
- Fixed feature -f pkg-pwr so that it collects samples at the expected intervals. Previously, samples were not collected at the polling interval specified by option -n when --polling was requested on the command-line.
- Fixed potential PMT data accuracy issues on Intel plaform code named Tiger Lake, where counter names could have been assigned to the wrong counter values in the reports.
- Removed trailing count value _1 from counter names previously seen in some reports from PMT metrics. The integer was added to help VTune-imported data be properly separated. However, this was not needed because VTune makes use of the topology to distinguish the data for bandwidth, power, package C-state and graphics C-State reports.

Version 2020.5

New

Release v2020.5 includes these changes:

- Intel® SoC Watch reports now include additional topology information in column headers and row entries for some features. A change was required to differentiate data reported for multiple discrete graphics cards of the same type and discrete graphics card with multiple tiles. This change extended into the reporting of CPU and integrated graphics metrics due to the common underlying tool framework. The topology components are separated by "/" and the number of components in the topology string will vary depending on the topology of the target platform. For example:
  - For CPU metrics you now see " CPU/Package_0/Core_0" shown where in prior releases it was simply "Core_0".
  - For integrated graphics, you now see "iGPU/Graphics" rather than "Graphics".
  - For discrete graphics, you now see "dGPU/DG1_173:0:0/Tile_0" where the numbers are Bus:Device:Function (B/D/F) for the PCI device on the card where the data is read. The B/D/F is appended to uniquely identify the source of the data. Note: The B/D/F appended for DG1 and DG2 data is for the P2SB PCI device on the card. This will be different from the PCI device for graphics on the card.
  - Metrics that are system level or from PCH are unchanged.
- Feature -f hw-cpu-pstate now summarizes and reports CPU P-states per thread (logical processor) rather than per core. The per core summary gave inaccurate results on all new platforms that are running with Hyper-Threading, starting with Intel platform code named Ice Lake. The inaccuracy occurs because the any-thread bit is no longer supported by hardware. Previously, SoC Watch displayed a warning about inaccurate P-state data and suggested use of –polling option as a work around on those platforms. Additional notes:
  - This change resolves occasional hardware counter correctness issue which resulted in SoC Watch displaying a warning about invalid P-state data because different counters are now used. The APERF/MPERF counters are now used to collect frequency data in place of the unreliable FIXED_CTR1/FIXED_CTR2.
  - Added hidden option -f hw-cpu-pstate-per-core to get the old report for use on platforms prior to Ice Lake, where P-state collection per Core is still valid. This feature will report inaccurate results if used on Ice Lake or newer platforms unless the --polling option is included. Note: Features hw-cpu-pstate and hw-cpu-pstate-per-core are mutually exclusive. Attempting to collect both in the same run will result in an error.
  - Hidden feature name –f hw-cpu-pstate-per-thread has been removed since that functionality is now in feature –f hw-cpu-pstate.
- Changed feature name -f cpu-gpu-concurrency to -f cpu-igpu-concurrency to make it clear this refers to integrated GPU vs. discrete GPU. The table name was changed accordingly to "CPU-iGPU Concurrency Summary".
- Changed table names for features -f hw-igfx-cstate and -f hw-igfx-pstate to include "Integrated". Previously, these output tables did not identify the results as Integrated Graphics vs. Discrete Graphics.
- Added support for Intel platform code named Tiger Lake to external package. This includes PMT features -f ddr-bw and -f soc-temp, which are defined within the SoC Watch configuration file, the PMT XML file is not included in the external package.
- Added support for collecting package power data on Intel discrete graphics card code named DG1 (-f dgfx-pwr) to external package. Collection of this feature requires the presence of a driver that is available when running on platforms with DG1 in the Intel DevCloud.This support is not available on platforms running Windows* OS because there is no public PMT driver for Windows OS.
- Added note to the report for feature -f os-cpu-pstate to explain the appearance of -1 as a frequency value. When no P-state change event occurs for one or more threads, the following message is written at the start of the report: "Note: No OS P-state event is generated for a thread if it does not change frequency during the collection period. Frequency is reported as -1 when this occurs."
- For Intel platforms code named Jasper Lake and Elkhart Lake:
  - Added features -f display-rr and -f dpst.
- For Intel platform code named Alder Lake:
  - Updated feature -f s0ix-subs-dbg to include more components in NDA version.

  - Added reporting of the HGS+ application Class index if HGS+ is supported and enabled. This support is not available until ADL B-step and therefore has not been fully tested.
  - Enabled ddr-bw for ADL-S B-step and ADL-P in SoC Watch, however collection requires new IntelTA.sys driver which was still under test at time of this release, so this feature has not been tested yet.
  - Enabled support for ADP-P and ADP-M PCH metrics. Not tested.
- For Intel platform code named Tiger Lake:
  - Hidden feature -f pmt-pwr now includes VCCIN power, and the separate feature -f pmt-vccin-pwr has been removed.
- For Intel discrete graphics cards DG1 and DG2:
  - Feature -f dgfx-pwr now includes VCCIN power data and the separate feature -f dgfx-vccin-pwr has been removed. This data is still suspect and therefore only included in the Internal version.
- Groups sys and sstate now include feature -f s0ix-subs-dbg. That feature had been removed as a workaround to an issue that was fixed.
- Updated SoC Watch driver to work with new IntelTA.sys driver, as well as older version of that driver. This is required for collection of PMT telemetry on Tiger Lake with newer builds (21H1) of Win10 desktop OS.
- Removed .msi install package from NDA and External SoC Watch packages. This was only used to acknowledge the EULA, and its removal reduces SDL requirements. Acknowledgment of EULA by NDA customers now occurs at the download site, and was approved by legal.
- Removed support for collection of PMT metrics on Tiger Lake A-step due to conflicting XML definition files with B-step.
- Support for the following older platforms has been removed in this release: Intel platforms code named Anniedale, Valleyview, Cherry Trail, Haswell, and Broadwell. socperf is also removed.

Fixed Issues

Release v2020.5 has a fix for these issues.

- Re-enabled features -f acpi-sstate, -f pch-slps0-dbg, -f pkg-pwr, and -f dram-pwr in external package.
- Use of feature -f ia-throt-rsn on Intel platform code named Tiger Lake is disabled when Windows* OS Hypervisor Enforced Code Integrity (HECI) is enabled. Enabling this security mode results in some register access being blocked unless allowed by the Windows* OS.
- Fixed SoC Watch driver so it no longer fails Driver Verifier bugcheck DRIVER_IRQL_NOT_LESS_OR_EQUAL.
- For Intel platform code named Alder Lake-S:
  - Fixed pch-slps0 which was under reporting residency. A firmware fix was made using an alternate register.
  - Changed CNVi(Pulsar)-PLL label to CNVi-PLL in the report from feature -f pch-ip-active. The Pulsar reference was incorrect.
- Modified feature pch-ip-active for Intel platforms code named Tiger Lake and Alder Lake to add components and align component names with those in the External Design Specification (e.g., added LPSS using name *Intel Serial IO*). Any items marked reserved in the EDS are only visible in the Internal version of pch-ip-active.
- Removed OPI-PLL residency reporting from feature pch-ip-active for Intel PCH code named Tiger Lake-H (in Intel platforms code name Rocket Lake-S and Tiger Lake-H). That IP is not valid for this PCH and the counter gave erroneous data.
- Fixed feature -f dgfx-volt so that it no longer reports an empty result file. There was an error in the NDA version of the configuration file.
- Fixed issue seen on Win10x OS after installing SoC Watch where the Device Manager showed a ‘yellow bang’ for the socwatch driver after reboot. The error was due to defining the SoC Watch driver load to occur on demand when it must be load on boot (in the .inf). SoC Watch collections still functioned correctly when this warning occurred.

Version 2020.4

Release v2020.4 was released only as an External package. All changes for v2020.4 are included in the v2020.5 release notes.

Version 2020.3.2.1

Update release v2020.3.2.1 is the same binary linked with CTA driver v1.0.1.0 library. CTA driver v1.0.1.0 supports collection on both DG1 and DG2 discrete graphics cards. This version of SoC Watch will not work with CTA driver v1.0.0 and older versions of SoC Watch will not work with CTA driver v1.0.1.0. SoC Watch will report dgfx metrics as unsupported if the CTA driver with the matching version is not found.

Version 2020.3.2

New

Release v2020.3.2 includes these changes:

- New platform support:
  - Added (NDA) support for Intel platform code named Alder Lake.
  - Added feature -f s0ix-subs-status for Intel platform code named Alder Lake.
  - Added (NDA) support for collecting dgfx metrics on Intel discrete graphics card code named DG2. (PMT GUID 0x4f93 indicates DG2 512EU A-Stepping was detected).
    - Supported metrics include: GT RC6 residency, GT Slice and Unslice frequency, package C-State residency, GT and display voltage, and package power.
    - The internal package includes the following metrics which were not reporting reliable data at the time of release: Package C-state debug blocking and wake reasons, GT and SoC domain thermals, PSYS power, GT and SoC domain current, Package C-State Status.
  - Added support for SATA devices remapped under Intel® Volume Management Device (VMD). They were not detected earlier causing Soc Watch to report "No Sata devices found on this system". Now SoC Watch detects SATA devices remapped under VMD and reports the LPM values.
  - Added support for collecting features -f ddr-bw and -f soc-temp on Intel platform code named Tiger Lake -H. (PMT GUID 0x1700 indicates Tiger Lake P/H).
  - Metrics for discrete graphics have been added to groups, so that they are collected easily when a DG card is present in the platform. Feature dgfx-temp was added to -f temp and feature dgfx-pwr was added to -f power.
  - Removed support for pch-platform-ltr on Intel platform code named Broadwell.
  - Added status reporting of Energy Efficient Turbo Disable configuration for feature -f cpu-pkgc-cfg. Setting this bit disables the Turbo P-States energy efficiency optimizations. When disabled, SoC Watch reports "Energy Efficient Turbo Disable: Yes". Otherwise, SoC Watch reports "Energy Efficient Turbo Disable: No"
- Bug fixes.

Fixed Issues

Release v2020.3.2 has a fix for these issues.

- Improved support for Intel platform code named Alder Lake:
  - Added missing features -f pch-slps0 and -f cpu-pkgc-dbg.
  - Feature -f pch-platform-ltr was updated to add new IPs: THC0, THC1, SPF , and SPG
  - Resolved incorrect identification of heterogeneous cores reported near the top of the SoC Watch summary report. Previously, the logical core count incorrectly assumed Hyper-Threading applied to all physical cores.
  - Feature -f pch-ip-status was updated to include new IPs: NPK, MPFPW(1-6), ENDBG, FIA, FIA(1- 2), U3FPW(2-3), SPF, GBETSN1, TAM, GBETSN, THC0 and THC1.
  - Feature -f s0ix-subs-status was updated with new IPs.
- Improved support for Intel platform code named Tiger Lake:

  - Feature -f platform-ltr was updated to add new IPs: THC0, THC1, and SPF (Intel platform code named Tiger Lake PCH-H only). Also, the following unsupported IP's were removed: CPPM, CAM, and WIGIG.
  - Feature -f pch-ip-status was updated to include new IPs: FIA, GBETSN1 (Intel platform code named Tiger Lake PCH-H only), TAM, GBETSN, THC0, THC1, and SRROM.
  - Added missing MODPHY Lane function and rate mapping for "PCIe2nd" to feature -f pch-ip-active.
- Improved support for Intel platform code named Elkhart Lake (PCH code named Mule Creek Canyon):
  - Feature -f pch-ip-active was updated to support recent energy reporting firmware offset changes for B0 stepping. These changes also fixed support for MODPHY lane assignment and rate reporting. Changes occurred on Elkhart Lake B0 CPU with IFWI WW32.2.0 or newer.
- Feature -f pch-ip-status was updated to correct IP name to P2SB from PS2B for all platforms.
- Improved support for Intel platform code named Jasper Lake Plus:
  - Added missing feature -f cpu-pkgc-dbg.
  - The summary report was corrected to show the Intel PCH code name Jasper Lake (JSP) PCH rather than "Unsupported" (seen in NDA package).
- Hibernation was incorrectly detected for platforms entering Modern Standby, resulting in time being attributed to the Unknown state for metrics which reported residency data. Data in reports that exhibit this behavior are not reliable, but re-processing a collection (using -i option) with this version of SoC Watch will result in correct residency data.
- Added note explaining D3Unknown state to report for feature -f acpi-dstate.
- Fixed Driver Verifier violation in SoC Watch Driver caused by allocating executable memory.
- Removed feature -f s0ix-subs-dbg from groups -f sys and -f sstate as workaround to crash/hangs seen on Intel platforms code named Tiger Lake and Rocket Lake after that feature was added to those groups in SoC Watch v2020.3.
- A warning message is now displayed when SoC Watch is not able to start the ETW Event trace sessions required to collect metrics that are based on data from event trace logs (i.e., acpi-dstate, acpi-sstate, os-cpu-cstate, os-cpu-pstate, timer-resolution, and device-acpi-calls). The message is *Warning: Cannot enable provider in the trace file XXXX_extraSession.etl. Insufficient system resources exist to complete the requested service. Warning: Failed to start EtlCollector.* When this occurs, there will be missing reports in the SoC Watch output files. To resolve the problem, Event Trace Sessions must be made available either by trying again to see if other processes have closed their sessions, or running Windows Performance Monitor to view the Data Collector Sets/Event Trace Sessions that are running and stopping one of them. (Note that AgaveBootTrace is needed by Intel's Powerhouse Mountain tool.)

Version 2020.3.1

New

Release v2020.3.1 includes these changes:

- New platform support:
  - Added (NDA) support for Intel platform code named Rocket Lake.
  - Added (NDA) support for Intel platform code named Sapphire Rapids.

Fixed Issues

Release v2020.3.1 has a fix for these issues.

- Support for graphics metrics collected on Intel discrete graphics card code named DG1:
  - Added support for collecting dgfx metrics on DG1 B0-stepping which were previously reported as "unknown". SoC Watch was using the incorrect XML file name telemetry_0x0000490e01.xml when actual file name was telemetry_0x00490e01.xml. This XML GUID number aligns with IFWI version 2020ww26_05_01 and later.
  - Fixed discrepancy in -f dgfx-cstate-res feature causing the C-states output report to be labeled incorrectly as "PRESIDENCY".
  - Restored feature -f hw-dgfx-pstate. This was inadvertently removed from the NDA package.
- Support for Intel platform code named Alder Lake:

  - Feature -f pch-ip-active changed the counter reported as the REF PLL. The REF PLL counter is now GEN2(REF)-PLL, renamed from USB3PXP GEN2 PLL. The counter GEN5(REF)-PLL was incorrect and is no longer reported.
  - Feature -f pch-ip-active has removed broken counters CNVi-WF-LMAC1, CNVi-WF-LMAC2, and CNVi-WF-UMAC from its report.
- Support for Intel platform code named Tiger Lake:
  - -f ddr-bw reporting has been modified and IO_BANDWIDTH is no longer reported. The display and IO bandwidth counters reset when exiting Pkg C-states. This resulted in spikes in the data reported by SoC Watch because each drop in value was handled as a counter overflow. The counter reset is now handled, although a small under reporting of bandwidth may occur due to the difficulty of distinguishing a reset from overflow. The IO_BANDWIDTH data is not reported because it cannot be correctly calculated. That counter resets to an indeterminate value, rather than 0, so the occurrence of a reset cannot be detected.
  - Restored metrics -f comp-max-temp and -f edram-state which were inadvertently removed from NDA package.
  - Fixed issue where an empty (0k) summary .csv report was generated when feature -f acpi-sstate (included in groups -f sys and -f sstate) was collected. The issue was seen for collections that entered S0ix/Modern Standby. Post-processing would silently fail due to incorrect assumption about ETL event order that resulted in failure to initialize.
- Removed -f pch-slps0-dbg feature for Intel platform code named Elkhart Lake (with Intel PCH code named Mule Creek Canyon). Use feature -f s0ix-subs-status instead.
- Fixed error in feature -f s0ix-subs-status that caused incorrect reporting of S0i3.0 residency as 100%.
- Fixed issue where files generated using phm_csv result type format were corrupt when the number of columns exceeded 256.
- Added missing feature -f cpu-pkgc-dbg for Intel platform code named Rocket Lake.
- Fixed issue where the per process file handle limit on Linux systems was being reached resulting in too many open file error occurring during post processing of a collection. This was seen for collections on platforms with hundreds of cores.
- SoCWatch now returns an error code when an error occurred while parsing the command-line. Previously, a command line parsing error returned 0.

Version 2020.3

New

Release v2020.3 includes these changes:

- Change in behavior of counters for PCH Active metrics reported by feature -f pch-ip-active. Starting with Intel platform code named Tiger Lake, the PCH active counter behavior has changed to only increment if the PCH IP is active after entry to Pkg C10. This makes it easy to see which IP on the PCH is active after entry to PC10 state, which may be blocking entry to SLP_S0 (Modern Standby). Thus, Intel SoC Watch reports will show 0 activity for all PCH IP counters if the platform never enters PC10, even though the PCH IPs may have been active during that time. Due to this change in counter behavior the following changes have occurred, and are seen on all platforms unless otherwise indicated:
  - Removed report PCH Active State (as percentage of PCH Active Time) Summary: Residency which used the PMC counter as the denominator for percentage calculation. The PMC counter may no longer represent total PCH active time. It is unclear if this report was useful since these percentages could not be used relative to any other metric's percentage calculations, so dropping it to simplify reporting.
  - Added report PCH Active State Summary: Residency which uses total collection time (delta between first and last sample timestamps) as the denominator for percentage calculation. This aligns with all other metric's which report residency.
  - Renamed report PCH Active State (as percentage of PCH Wall Time) Summary: Residency to be PCH Active State (as percentage of PMC Active plus SLP_S0 Time). This report produces a more accurate percentage calculation for total active time compared to the total collection time that comes from using the delta between timestamps.

  - Suppressed PCH Active State (as percentage of PMC Active plus SLP_S0 Time) report on platforms where the PCH activity counters are not always counting (i.e., Tiger Lake PCH and newer) since the PMC counter will not represent total PCH active time if it does not increment until after PC10 entry occurs.
  - Suppressed PCH Active State (as percentage of PMC Active plus SLP_S0 Time) on Mule Creek Canyon PCH because the SLP_S0 counter is not supported.
  - Added hidden --option pch-count-always, that will change the PCH activity (ER) counter behavior to the legacy behavior which is to always count when PCH is active. This option is supported on TGL and newer platforms, in Internal and NDA package, but not documented because of the impact it can have on the powercfg sleepStudy report. (Note: This option is not being shared broadly for the following reason. If the legacy counting policy is set when a system enters Modern Standby, the sleepStudy report will capture misleading activity counts for TGL and newer platforms. If the system's sleepStudy data is part of a field study collection, it will introduce bad data into the database.)
  - Added a check to ensure the PCH ER counters are configured to count after entry to SLP_S0 (i.e., ER_HALT_SLPS0 is set to default) to ensure that IP activity is counted during entry to the S0ix substates, which will be reflected in the PCH Activity reported by -f pch-ip-active.
- New platform support:
  - Added (NDA) support for Intel platform code named Ice Lake Xeon-D.
  - Added (NDA) support for Intel platform code named Cooper Lake-Xeon.
  - Added (NDA) support for Intel platform code named Jasper Lake Plus.
  - Added (NDA) support for Intel PCH code named Jasper Lake-N and Ice Lake-N.
- Improved support for Intel platform code named Tiger Lake:
  - Added new feature -f s0ix-subs-dbg which reports residency for reasons blocking entry into deeper S0ix sub-states or breaking out of (waking from) S0ix sub-states.
  - Added initial support for some Intel ® Volume Management Device (VMD) configurations to PCIe features -f pcie-lpm and -f pcie-ltr. See Known Issues section for details.
  - Memory bandwidth feature (-f ddr-bw) is supported on Intel platform code named Tiger Lake with Bstepping when running on Windows* OS 20H1 builds or newer.
  - Added IA, GT, and IO Bandwidth reporting to this feature.
  - The driver required for accessing telemetry aggregator data (IntelTA.sys) is included in that OS and will successfully load on platforms with Tiger Lake B-stepping (not on A-stepping).
  - The latest IFWI is required for Tiger Lake B-stepping for accurate bandwidth data.
  - Intel SoC Watch should report PMT GUID 0x1601 on Tiger Lake B-stepping
- Extended support for Intel platform code named Alder Lake:
  - Enabled PCH metrics: pch-ip-status, pch-ip-active, s0ix-subs-res, s0ix-subs-dbg, pcie-lpm, pcie-ltr, sata-lpm, xhci-lpm. (-f s0ix-subs-status has not been enabled yet)
  - Added new hidden feature, -f pch-ps-on, to report PS_ON (power supply on) residency. This metric has not been verified, so it is not yet shown in help. (Note: Will report as unsupported feature if PS-ON has not been enabled in BIOS.)
  - Enabled -f hgs-feedback. (Note: Not yet extended for HGS+ to report classification ID.)
  - Enabled support for -f igfx-hw-pstate metrics.
  - No support -f cpu-pkgc-dbg or -f ddr-bw metrics until ADL B-stepping. The legacy counters for CPU Pkg C debug were not carried forward to ADL and the memory bandwidth legacy counters became invalid starting with Tiger Lake. Both metrics have replacement counters in the PMT (Platform Monitoring Technology, aka telemetry aggregator), however, that support was not implemented in Astepping
- Enabled feature -f pch-slps0 on Intel platform code named Lakefield.
- Enabled support for -f ddr-bw and -f igfx-hw-pstate metrics for Intel platform code named Rocket Lake.
- Extended support for graphics metrics collected on Intel discrete graphics card code named DG1:
  - Collecting dgfx metrics on DG1 B0 is supported. PMT SRAM layout changed.
  - Collection from PMT (aggregated telemetry, formerly CTA) metrics (e.g., ddr-bw) and discrete graphics (dgfx*) metrics simultaneously on Intel platform code named Tiger Lake with DG1 is supported.

  - GUIDs associated with collecting data from PMT enabled targets are displayed on the console (e.g., PMT=0x490e,0x1600) and the device name is included in the summary report (e.g., PMT: Discrete Graphics DG1, PMT: Tiger Lake (B) PMT). This information must be included if reporting issues.
- The --help command now lists option --no-post-processing which can be used to delay post-processing. If this is specified on the collection command line, no summary .csv file will be generated at the end of that collection. To generate a summary result or any other result file later, re-process the collection using the -i option. Delaying post-processing of large collections (i.e., many metrics and/or long collection duration) until the intermediate collection files (.sw2 or .etl) have been copied to a more powerful system can significantly reduce the post-processing time.
- Intel SoC Watch can be executed without administrative privilege when re-processing results from a previous collection using option -i.
- Enabled use of tool-specific options for Powerhouse Mountain (-f phm -r phm-csv) in External package to allow Enterprise Battery Life Diagnostic tool access to them. These options are hidden, not seen in help.
- The following old platforms will have support removed in the next release: Intel platforms formerly code named Valleyview, Cherry Trail, Haswell, and Broadwell. (Note: The pch-ip-active feature is currently broken for the Broadwell platform and will not be fixed.)
- Support for socperf collection of signal-based metrics ended with Intel platform code named Cherry Trail (and limited support for Intel platform code named Apollo Lake), therefore it will be removed in the next release. This will result in removal of all signal-based metrics: all-approx-bw, cpu-ddr-mod0-bw, cpu-ddrmod1-bw, disp-ddr-bw, dram-srr, gfx-ddr-bw, io-bw, isp-ddr-bw, netip-bw, and netip-partials-bw.

Fixed Issues

Release v2020.3 has a fix for these issues.

- Fixed missing table reported by feature -f pkg-pwr when re-processing collection. Previously, the Package Limits table for -f pkg-pwr was not reported when using -i to re-process a result.
- Removed -f comp-max-temp from feature groups sys and temp. There can be a conflict in the data source access mechanism when collecting features -f comp-max-temp or -f edram-state simultaneously with -f cpu-pkgc-dbg which is included in several groups as well. (The conflict is in use of the BIOS Mailbox - seen mainly on Linux OS, but possible on Windows OS.)
- Corrected reason description for -f cpu-pkgc-dbg counter PC3-PEG-NOT-BLOCKED (ID 111) to read "PEG is not blocked" on Intel platform code named Tiger Lake (U/Y). Previously, the description reported this as "DMI is not blocked".
- Max Pkg C-state reported by -f cpu-dbg-cfg has been corrected for Intel platforms code named Lakefield, Tiger Lake, Elkhart Lake, and Jasper Lake Plus. Previously, this was always reported as C0/C1. For BIOS setting of Auto for maximum Pkg C-state, the deepest state is used (e.g., Pkg C10). (The location of the bits had changed for these platforms.)
- Added warning for missing ETW events to help identify situations when reports will be missing or inaccurate for features based on event trace data (i.e., acpi-dstate, acpi-sstate, os-cpu-cstate, os-cpupstate, os-gfx-cstate). The message "Warning: Lost events detected" is displayed when this occurs. The message includes the number of lost events and the Intel SoC Watch .etl file impacted. This problem usually occurs if another application has its own ETW logging session running at the time an SoC Watch collection is started, resulting in contention for the NT Kernel logging session. Re-running the SoC Watch collection will resolve the issue if the other logging session has stopped. Alternatively, logman stop "NT Kernel Logger" can be used prior to running SoC Watch, which will have repercussions on the other application's logging. Note that the missing ETW event issue has been reported on Intel IT managed laptops, caused by background DCA processes.
- Improved error/warning messages by adding "SoCperf" to messages related to issues involving the socperf driver.
- Re-enabled metrics for public platforms in OneCore Windows* OS packages (NDA and Internal). A regression in the previous release caused metrics for external platforms (e.g., SKL, KBL, ICL) to be omitted from the OneCore Windows* OS packages, only NDA or Internal platforms were supported (e.g., TGL, LKF, EHL).
- Modified Physical Mode Lane Assignment reported by -f pch-ip-active . A lane without a connection now has its function and rate reported as "Undefined" rather than "Unknown".

- Removed features -f pch-slps0 and -f pch-slps0-dbg for Intel platform PCH code named Mule Creek Canyon. The old telemetry is not supported for the Mule Creek Canyon PCH, these metrics have been replaced by -f s0ix-subs-res and -f s0ix-subs-status, respectively. The sum of the S0ix.y residencies is equivalent to SLP_S0 residency.
- Aligned report names for -f acpi-sstate to be the same across operating systems. The new name is "ACPI S-State". Previously, "Platform ACPI S-State" was used for Linux* OS and derivatives and "System SState (OS)" was used for Windows* OS.
- Improvements in -f display-rr:
  - Corrected link rate reporting on platforms using Intel Gen11 integrated graphics. Previously, the link rate was reported as 0 MHz.
  - Added 20Hz to supported refresh rates.
- Fixed issue where -f pch-slps0 was inadvertently changing the PCH Energy Reporting clock rate from 1us to 122us for Intel platform PCH code named Tiger Lake and Mule Creek Canyon. This would cause the PCH to underreport its energy use to the CPU. The clock rate was corrected by the PMC if PC10 entry occurred.
- Feature -f pch-ip-active was reporting activity incorrectly for Intel platform PCH code named Mule Creek Canyon. The base additional offset was wrong and there were missing IP blocks. There was also an issue in the FW that blocked enabling of the ER activity counters that was fixed.
- Added support for Cannon Lake PCH to external builds to support use of -f pch-slps0 on public platforms that include the CNP PCH. The core platform support for Cannon Lake was included as well.
- Fixed Intel SoC Watch crash when re-processing -f pch-slps0-cfg results using -i.
- Fixed -f tcss-state reporting:
  - Corrected TCx residency reporting for Intel platform code named Tiger Lake. TC0 residency data was too high. (Offsets for counters had changed.)
  - TC0 Blocking and Unblocking states are now identified. The Blocking state means Pkg can go as deep as PC8. Unblocking means Pkg can go from PC0 to PC3.
  - On Intel platform code named Ice Lake, there is a single value for TC0, inferred as the remainder of collection duration, because there is no counter for TC0. Also, the TC3 state is not used so it is omitted from the report.
  - On Intel platform code named Tiger Lake, TC0 Blocking counter is provided and TC0 Unblocking is inferred. The TC3 and TC4 states are not used, so they are omitted from the report.
  - Removed TCCold from the list of TCx states. It is a separate state from the TCx states, and it cannot be read without waking the system from TCCold, so it is not reported.
- Modified and corrected -f s0ix-subs-status metric for Intel platforms code named Tiger Lake, Lakefield, and Elkhart Lake:
  - Fixed several errors in data collection which resulted in incorrect data being reported.
  - Changed table format to use a single table containing all IP and states rather than a separate table for each state. This aligns with the format used for the new -f s0ix-subs-dbg feature and other PCH IP status/dbg metrics which report similar state data.
  - Changed to reading state from more accurate (live) status registers. Previously, read status registers that would only update under certain conditions.
  - The s0ix-subs-status table is a summary of point-in-time samples for each IP/agent being in the required state for entry to S0ix low power states. The s0ix-subs-dbg feature reports approximate time that the IP/agent is not in the required state.
- Fixed over-reporting of D3Cold residency by -f acpi-dstate feature. Previously, once a device entered D3Cold, all time after that was added to D3Cold residency no matter what state change occurred.
- Fixed issue where Intel SoC Watch would hang or crash when collecting many metrics and requesting multiple result file types (-r). Now you will see error messages indicating that too many files are open or the file system is not writable. To work around this issue, specify only one -r file type at collection time or collect fewer metrics. After collection, use -i option with each of the remaining file types to generate the additional result files.

- Removed feature -f connected-standby from showing as a supported feature for the OneCore Windows OS package. That feature requires an extra driver (cstracedrv) which has not been ported to Universal Windows. If the feature is specified, the warning message has been improved to give the name of the driver that is missing.
- Added detection of when display information is unavailable for feature -f dpst on Intel platform code named Tiger Lake with DG1 card installed. Now the feature is reported as unsupported rather than reporting bad data.
- Increased supported processor count from 256 to 512 and added a check so that the socwatch driver fails to load with a debug message if count is exceeded. Previously, a system crash occurred when collecting on a platform with 448 logical processors.
- Disabled loading of Telemetry Aggregator XML file in external build since those metrics are not supported externally.
- Added missing description in help output for -f sa-freq.
- Re-enabled (NDA) support for PCIe metrics (-f pcie-lpm, -f pcie-ltr) for Intel platform code named Ice Lake PCH (ICP-H, ICP-N) and Intel platform PCH code named Mule Creek Canyon.
- Disabled integrated graphics metrics (hw-igfx-cstate, hw-igfx-pstate, igfx-throt-rsn, cpu-gpu-concurrency) when a discrete graphics card is installed and integrated graphics is disabled. A message is displayed to the console when --help is used to indicate when integrated graphics is disabled.
- Improved messages reported when metrics from PMT (e.g., ddr-bw) cannot be reported. These messages are displayed on the console and in the summary .csv file help to identify the issue:
  - If the PMT GUID reported by the FW does not match any XML configuration file bundled in the Intel SoC Watch package, this warning message is displayed: WARNING: Metrics relying on the Platform Monitoring Technology driver are disabled for PMT:< GUID >. The required XML configuration file is missing or the platform is not supported.
  - If a counter name for a metric is not found in the XML, this error message is displayed: ERROR: The PMT specification XML <xml_full_path> is corrupted or incompatible with the PMT endpoint < GUID >. PMT metrics on that endpoint cannot be collected.
- Due to anomalies in the hardware counters for CPU C-state and CPU P-state (-f hw-cpu-cstate, -f hw-cpupstate), several warnings are now reported to notify users of the problem. (Prior to v2020.2, bad data was caught and silently omitted from the summary because it was believed to be a rare occurrence.) The new warnings appear on the console and in the summary .csv file, they include:
  - Warning: Zero FIXED counter value <value> found. Warning: CPU C/P state results will be inaccurate.
  - Warning: CPU P-state results may not be accurate on this platform. Please specify --polling to get accurate CPU P-state results.
  - Warning: Detected HW counter value did not increment as expected (FIXED-CTR: <value> < previous value <value> . CPU C-state residency for CC0 and CC1 will be inaccurate. CPU P-state frequencies will be inaccurate.
- Fixed issue where Intel SoC Watch returned silent failure for -export-help option on a Tiger Lake platform with DG1 card installed. SoC Watch did not handle the presence of both the PMT and DG1 telemetry sources.

Version 2020.2

New

Release v2020.2 includes these changes:

- **Added collection of SoC Watch usage analytics**. After installing Intel SoC Watch, upon first use, a dialog box prompts you to allow the collection of non-personal information about the system and SoC Watch command line used in this and future collections (i.e., to opt-in). If allowed, this data is sent to Intel if the system is connected to the internet at the end of the SoC Watch collection. If the data cannot be sent for any reason, the data is deleted. The data will not accumulate on the system. Use these command line options to respond to the dialog box:
  - To opt-in or change a former decision to opt-in: `--update-usage-consent yes`

  - To opt-out or change a former decision to opt-out: `--update-usage-consent no`
  - To skip prompt and disable usage collection (regardless of a prior opt-in): `--skip-usage-collection`
- **New platform support:**
  - Added support for Rocket Lake. (Internal Only. Limited testing, pre-Si.)
  - Added support for Cooper Lake. (Internal Only. Not tested on hardware.)
  - Added Alder Lake basic support, no PCH metrics. (Internal Only. Limited testing, pre-Si.)
  - Added (NDA) support for Intel platforms code named Snow Ridge and Ice Lake Xeon.
- **Features extended to additional platforms:**
  - Added (NDA) support for -f pch-ip-active on Intel PCH code named Tiger Lake -H.
  - Added (NDA) support for -f cpu-pkgc-dbg on Elkhart Lake.
  - Added (NDA) support for -f s0ix-subs-status on Intel platforms code named Lakefield.
  - Extended panel-srr and display-rr support for Intel platforms code named Tiger Lake. (Gen12 graphics display).
  - Added (NDA) support for features s0ix-subs-res, s0ix-subs-status, pch-ip-active* and pch-ip-status for Intel PCH code named Mule Creek Canyon. (*The pch-ip-active report may be all 0's, the issue is being worked.*)
  - Added support for Jasper Lake -N PCH, enabling pch-slps0*, pch-ip-active*, pch-ip-status, pch-ip-lat-limit, and pch-platform-ltr features. JSP-N is a derivative of ICP-N without eMMC and CNVi.
- **New features:**
  - -f pch-slps0: Reports residency in lowest power sleep state, SLP_S0 (s0i3/Modern Standby). (added to public release)
  - -f pch-slps0-dbg: Reports blocking reasons (IP state conditions) that may be preventing entry to lowest power sleep state, SLP_S0 (s0i3/Modern Standby). (added to public release)
  - -f hgs-feedback: Hardware Guided Scheduling feedback feature exposes the power and performance efficiency numbers that the hardware provides to the OS. The OS uses these to make scheduling decisions as to which type of Core to use on hybrid platforms (e.g., Lakefield). It is not included in any group. (Internal Only)
  - -f pch-ivr-state: PCH Idle Voltage Reduction (IVR) state feature reports residency in the idle voltage states. It is supported on Tiger Lake platforms (both -LP and -H PCH). It is not included in any group. (Internal Only)
  - Added event trace providers (Microsoft-Windows-Energy-Estimation-Engine, Microsoft-Windows-WMI-Activity) that are enabled by -f phm option to enable Intel Enterprise Battery Life Diagnostic Tool.
- **Change in counter behavior for the -f pch-ip-active metric starting with Intel PCH code named Tiger Lake**. The PCH IP active counters reported by this feature now only increment when the system is in PC10. This increases its usefulness in identifying which IPs on the PCH are active when the system is trying to enter the S0ix sub-states (S0ix.y). The PCH activity is only a blocker after the CPU (Package) has entered its deepest sleep state (PC10), and that is when the counters increment for the Tiger Lake PCH. For older PCH, these counters increment without regard to the Package C-state so it is not clear which IP are active after entry to PC10. Note that this means the Tiger Lake PCH active counters will show 0% active if the system does not enter PC10, but that does not mean the PCH was not active.
- **Improved error messages and help:**
  - Improved error message when attempting to run SoC Watch as non-administrative user. Added explicit check for running as administrator. If check fails, report error "Failed to install Intel(R) SoC Watch driver. Please run with administrator privileges." Other failures to install the driver result in the error "Failed to install Intel(R) SoC Watch driver. Please reboot the system and try again."
  - Clarified -f pkg-pwr report's Note regarding multi-DIE topology: "Die-level power is included in package power on platforms with a multi-die CPU topology." There is no breakdown for energy at the Die-level.
  - Improved help output by aligning terminology and form used across the features.

- **Enhanced security of SoC Watch drivers**. The drivers now limit access to only those registers or memory intended by the tool development team for collecting platform power and performance information.
- **Enhanced Continuous Monitoring (Profiling) API:**
  - Improved security by changing the usage model so that the calling process is the server which forks the socwatch process as a client. The server process must have root privilege to successfully launch the socwatch process. The command line option to launch a socwatch server process has been removed.
  - The API example program has been updated to reflect the change. In addition, the example program's command line parsing now works for both Windows or Linux OS with an improved help output.
  - You can now pull results from a continuous collection at arbitrary time intervals. There is no longer a requirement to pull results at least once every second.
  - Removed the distinction between 'blocking' and 'non-blocking' pull calls within the API . Now, all calls are non-blocking.

Fixed Issues

Release v2020.2 has a fix for these issues.

- Improvements for dgfx* features (for DG1):
  - Fixed issue in -f dgfx-cstate-res and -f dgfx-pkg-cstate-res where time being reported was too large. (Hardcoded the XTAL clock frequency to 38.4MHz due to broken register value.)
  - Fixed collection of RC6 state residency so that it is not sampled unless -m option is used.
  - Collecting DG1 metrics requires an updated CTA driver.
- Improvements for hw-cpu-pstate:
  - Attempting to collect feature -f hw-cpu-pstate-per-thread simultaneously with -f hw-cpu-pstate will now result in an error message in order to prevent erroneous data reports. These features are mutually exclusive because of conflicting hardware settings. Previously, collection would continue and produce incorrect results.
- Improvements for hw-cpu-cstate:
  - For Intel platforms code named Sapphire Rapids, added missing Core C1 and Package C7 states. (Limited testing, pre-Si.)
  - Resolved system crash when collecting -f hw-cpu-cstate when Windows* OS Virtual Secure Mode (VSM) is enabled. Enabling VSM results in some register access being blocked unless allowed by the OS (i.e., white-listed) for specific platforms. New platforms that have not been white-listed yet will crash, so the tool must workaround or disable metrics affected. (including Intel platforms code named Tiger Lake and Elkhart Lake, Rocket Lake and Jasper Lake). For hw-cpu-cstate the Core C1 register is blocked, so C1 cannot be reported separately resulting in Core C0+C1 being reported instead.
- Improvements for -f cpu-pkgc-dbg:
  - Corrected Ice Lake, Elkhart Lake, and TGL-H (CPU) reporting
  - Fixed problem causing "Cannot go deeper than" and "High Residency in" tables to be missing
- Improvements for -f pch-ip-active*:
  - Reverted tables to report percentage of PCH Active Time and percentage of Wall Time. Wall time is the sum of PCH Active time + PCH Not Active time (PMC counter + SLP_S0 counter) and this gives a more precise % number, compared to using collection duration. (A broken PMC counter for Tiger Lake PCH had caused the change to use collection duration, which has been resolved.)
  - Removed unused ModPHY lanes 12-15 and added missing lane function mappings for Intel PCH code named Tiger Lake -LP.
  - Fixed reporting of HP-PLL and MAIN(AUD)-PLL activity, which were swapped, and added ModPHY lane function mapping for CSI3 (6) for Intel PCH code named Tiger Lake.
  - Added missing lane function mappings for Intel PCH code named Cannon Point.
  - Resolved issue where PMC and other IP were incorrectly reported as 0% active for Intel PCH code named Lakefield. (Firmware after ww43 changed the counter offsets.)

  - Updated counter offsets for Mule Creek Canyon PCH according to latest information. (Marginal testing due to limited access to hardware.)
- Fixed issue with -f pch-ip-status where CSME power gated was incorrectly reporting No. (CSME power gated was reporting Yes with Internal SoC Watch package, but No with NDA package due to copy error in configuration file which has been resolved.)
- Fixed reporting for s0ix-subs-res and s0ix-subs-status features for Mule Creek Canyon PCH (in Elkhart Lake platform), updating counter addresses.
- Corrected -f display-state feature so that it always collects the DC5 and DC6 entry counts and samples the DC5/DC6 enable status, then shows a total count for each enabled status. Previously, the enable status was only read at the start of collection and if not enabled, the entire feature was disabled and nothing would be collected. Now, the DC5 and DC6 entrance counters will be collected without regard to the enable status. In this release, the enable status data is only available as a total count, but will be included in a sample trace file in a future release. (Note: On Tiger Lake, it has been observed that the entrance counters reset to 0 if the system enters S0i2.0.)
- Fixed issue where use of --interval option with value of 1 (e.g., -n 1 -m) resulted in only one sample being collected.
- Improved regularity of time interval between samples when using --polling on Windows OS. The actual time interval between samples is still slightly greater than requested interval due to overhead. (The timer now operates within the application rather than the driver, similar to the Linux implementation.)
- Fixed -f sa-freq reporting for CDCLK frequency on Intel platforms code named Tiger Lake. (Added missing table look up for 192MHz.)
- For Snow Ridge platforms, corrected number of cores per module (changed to 4).
- Removed extra tables reported for features igfx-throt-rsn, ia-throt-rsn, and ring-throt-rsn, and added Total Samples Received table, to align with tables reported for similar features.

Version 2020.1

New

Release v2020.1 includes these changes:

- Intel® SoC Watch v2021.1 has been updated to include a security update in its OneCore package. Users of the OneCore package should update to the latest version. (The security update for the desktop package was included in v2019.12.)
- Added initial support for collecting metrics from discrete graphics card code named DG1 installed in Intel architecture platforms. Specific drivers are required as noted below (collection only supports one DG1 card currently). Use the help (-h) option to get a complete list of Intel SoC Watch feature names supported for the target platform. Features that collect data for discrete graphics DG1 have "dgfx" in their name. The legacy graphics metrics, for integrated graphics, have been renamed to include "igfx" in their name, and use of "gfx" alone is now a group feature name that includes both integrated and discrete graphics metrics. Use of the group name will collect whatever is available. Below is the list of currently supported metrics for DG1:
  - dgfx-cstate-res: DG1 residency in graphics C-state (RC6)
  - dgfx-cstate-status: DG1 sampled graphics C-states (RC0, RC1, RC6)
  - hw-dgfx-pstate: DG1 sampled P-State operating frequency for Slice and Unslice
  - dgfx-ddr-bw: DG1 display VC1 memory bandwidth (read and write)
  - dgfx-pkg-cstate-res: DG1 residency in package C-states (PCx)
  - dgfx-pkg-cstate-status: DG1 sampled state for: package C-state (PCx), display state (DCx), PCIe state (Cx), and memory subsystem state (Cx).
  - dgfx-pkgc-dbg: Approximate residency for DG1 package C-state reasons blocking entry to deeper PCx states and causing wakeup from deeper PCx states.
  - dgfx-pwr: DG1 sampled package energy usage. Internal support includes sampled PSYS energy usage.
  - dgfx-vccin-pwr: DG1 sampled VCCIN energy usage.
  - dgfx-temp: DG1 sampled temperatures for: system agent (SA), image processing using (IPU), and graphics processor (GT).

  - dgfx-volt: DG1 sampled voltage values for Unslice. Internal support includes Slice voltage values.
  - dgfx-current: DG1 sampled current values for Slice and Unslice
- Feature group names added for discrete graphics metrics are: dgfx, hw-dgfx-cstate, dgfx-pkg-cstate. Use the help (-h) output to list what is included in each group.
- Feature groups that were modified to include discrete graphics metrics are: gfx, gfx-cstate, gfx-pstate, gfx-hw, hw-gfx-cstate, hw-gfx-pstate. Use of these group names will collect for whichever graphics is discovered in the system.
- Reverted feature os-gfx-cstate to an individual feature name, removing feature name os-igfx-cstate. A distinction was not needed, both integrated and discrete graphics can be collected from OS event trace logs using this feature.
- Collection of DG1 data requires the following hardware and drivers to be installed on the target system under analysis:
  - DG1 card
  - Intel graphics driver with support for the DG1 card (refer to DG1 BKC for details)
  - Intel CTA driver that provides access to the Converged Telemetry Architecture defined for DG1 (refer to Installation Notes chapter for download and installation instructions)
- Added support for Intel platform code named Elkhart Lake and Intel PCH code named Mule Creek Canyon for NDA. Metrics that could not be verified for correctness have been omitted from this release (cpu-pkgc-dbg, pch-ip-active, pch-ip-status). These are present in the Internal package but should be used with caution.
- Added initial support for Intel platform code named Spring Hills. This has not been validated. Internal only.
- Added support for Intel platform code named Tiger Lake-H. The PCH metrics for its chipset are not supported at this time.

Fixed Issues

Release v2020.1 has a fix for these issues.

- Feature -f pcie-ltr now reports "N/A" in its Capabilities summary report when the device's capability information is not available. Previously, the summary reported "No" when a device had entered D3 Cold and its capability data was not available.
- Fixed regression in feature -f pcie-lpm which caused incorrect reporting for residency in L1 substates for NVME devices. The regression occurred in v2.11, and manifested as always reporting 100% time in state L0s for NVME devices.
- Fixed an issue affecting Intel platform code named Tiger Lake where unexpected tables were seen in the output for "-f debug-cpu-cstate".
- Fixed an issue where "-f lpss-ltr" was not working on some platforms.
- Fixed a regression introduced in v2019.13 where feature "-f s0ix-subs-res" was not available for Intel platform code named Lakefield.
- Fixed an issue affecting Intel server platform code named Ice Lake-Xeon where C-states shown for Package and Core did not match the supported states. Core C1 and Package C7 were added, Core C7 was removed.
- Fixed an issue affecting Intel platform code named Lakefield where feature "-f pch-ip-active" was using an incorrect base address for the underlying energy reporting counters. The firmware change that requires the base address to change has not been released yet.
- Fixed an issue where feature "-f display-rr" was showing incorrect link rate and refresh rate on some platforms.
- Fixed an issue affecting Intel platform code named Lakefield where feature "-f cpu-pkgc-dbg" was missing tables.
- Fixed issue resulting in some platforms being reported as Intel platform code name Amber Lake that should have been Intel platform code name Kaby Lake. The data reported was correct, only the code name was incorrect.

Version 2019.13

New

Release v2019.13 includes these new features.

- Added (to NDA) new feature (-f s0ix-subs-status) to report low power mode requirements status for S0ix substates for Intel platforms code named Tiger Lake. Use -f s0ix-subs-res to see residency in the S0ix low power states (s0i2.0-s0i2.2 and s0i3.0-s0i3.4).

Fixed Issues

Release v2019.13 has fixes for these issues:

- Fixed problem in hw-cpu-pstate on Intel platform code named Ice Lake where P-state data was missing for some Cores.
- Fixed issue in ddr-bw feature for Intel platform code named Tiger Lake that manifested as extremely large bandwidth values being reported.
- Corrected possible error in hw-cpu-cstate reporting of Core C0 and C1 residency on Intel platform code named Tiger Lake. (Core C0 could have been wrong on systems that enabled Hyper-Threading technology, but that has been resolved.) Also added reporting for Core C6 residency.

Version 2019.12

New

Release v2019.12 includes these new features.

- Intel® SoC Watch has been updated to include functional and security updates. Users should update to the latest version.
- Changed Intel SoC Watch version numbering format. This release (v2019.12) is the release that follows v2.11.0 (the driver continues to use the 2.xx version number format).
- Added support for Intel PCH code named Comet Lake V (CMP-V)
- Added support for Intel platform code named Jasper Lake Plus. Support for the JSP PCH is not yet added. (This is early support, not tested.)
- Added (to NDA) new feature (-f s0ix-subs-res) to report S0ix substate residency for Intel platforms code named Lakefield and Tiger Lake. These platforms add S0ix low power states s0i2.0-s0i2.2 and s0i3.0-s0i3.4. The sum of these power states is equivalent to SLP_S0. Use this as a workaround for the unsupported pch-slps0 feature on Lakefield platforms.
- Added (to NDA) new feature (-f dpst) to report if Display Power Saving Technology (DPST) is enabled, corresponding level, and if Enhanced Power Savings Mode (EPSM) is enabled. It also reports the South Backlight (SBL) duty cycle frequency percentage. This is supported for Intel PCH code named Sunrise Point, Cannon Point, and Ice Lake.
- New feature (-f display-rr) to report display refresh rate information. The report includes the display resolution, link rate, Lower Refresh Rate (LRR) version (if available and LRR change detected), and histogram of the refresh rates. Supports Gen9 (KBL, CNL, CML) and Gen11 (ICL) LRR 1.0 pixelclock based refresh rate monitoring. Does not yet support LRR 2.0/VRR (vblank stretching) or LRR 2.5 (static pixelclock, vblank stretching).
- Improved -f sata-lpm **Capabilities** table by adding columns that report status for *DevSlp Capable* and *Devslp Enabled*. The *DSP* (Device Sleep Present) column has been renamed to *DevSlp Port Ena*. So now, *DevSlp Port Ena* indicates that the platform has enabled DevSleep for that particular SATA port (typically done in BIOS). Whereas, *DevSlp Capable* and *Devslp Enabled* indicate if the disk itself supports DevSleep. The new information helps detect the case where a disk without DevSleep support is plugged into a DevSleep enabled port (DSP=1).
- New feature -f vr-pwr-state for Intel platforms code named Ice Lake (requires firmware ww20 or newer). Reports residency percentage and time in Voltage Regulator (VR) power states PS0-PS3. When the Package is in C3 state, the PSx state is unknown. This metric cannot be collected in conjunction with -f

edram-state or -f comp-max-temp due to hardware limitation. If the platform enters hibernation, the Unknown residency time will include both the PS unknown state and hibernate time. These will be separated in the next release.
- Completed NDA support for Intel platform code named Tiger Lake. These features are now supported: hw-gfx-cstate, hw-gfx-pstate, panel-srr , pch-ip-active, edram-state, sata-lpm and cpu-gpu-concurrency.
- More blocking reasons added to -f cpu-pkgc-dbg reports for Intel platforms code named Comet Lake and Whiskey Lake. The new reasons show the specific component (DMI/OPI, PEG, IPU, GMM, or internal device) that is not blocked when cannot go deeper than PC2 or PC3.
- PCH IP Active Residency tables changed in -f pch-ip-active feature. A new table **PCH Active State Summary** has replaced the **PCH Active State (as percentage of PCH Wall Time) Summary** table. The new summary report calculates the residency as a percentage of the collection duration time. The old table used PMC + SLP_S0 counters as the measure of overall time. On Intel platforms code named Tiger Lake, these counter may count at the same time, invalidating this use. For consistency, the change in tables has been done for all platforms since the difference in calculated percentages is insignificant for other platforms.
- Graphics
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- s have been renamed to create a distinction between integrated and discrete graphics data collection (in preparation for DG1 support). The original feature names are still valid, but have become group names that include both integrated (legacy) and discrete graphics data on platforms that support both. The name changes are as follows:
  - hw-gfx-cstate -> hw-igfx-cstate; hw-gfx-cstate is now a group name
  - os-gfx-cstate -> os-igfx-cstate; os-gfx-cstate is now a group name
  - hw-gfx-pstate -> hw-igfx-pstate; hw-gfx-pstate is now a group name
  - gfx-throt-rsn -> igfx-throt-rsn; gfx-throt-rsn is now a group name
- Metrics from Tiger Lake Telemetry Aggregator that have duplicate legacy metrics remain hidden and have been renamed from prefix "aggr" to "ta" added to the legacy name (ta-cpu-pkg-dbg, ta-cpu-pkg-cstate, ta-pkg-pwr). The TA metrics are expected to replace or extend the legacy metrics when access to the TA data is more reliable. For now, they serve as a means of checking data correctness.

Fixed Issues

Release v2019.12 has fixes for these issues:

- Resolved Microsoft Windows State Separation compliance issue in the SoC Watch driver include in the SoC Watch OneCore OS package.
- Improved support for Intel PCH code named Mule Creek Canyon. Updated the offsets to align with current specification for PCH Activity counters used in -f pch-ip-active.
- Fixed low RC6 residency reported by -f hw-gfx-cstate. The error could occur when collecting without -m for longer than 11 minutes due to undetected counter overflow. The problem has been resolved by always collecting over time so that overflow can be detected and handled.
- Feature -f cpu-pkgc-dbg has been updated for Intel platforms code named Ice Lake and Tiger Lake U. Some block and wake reasons had changed resulting in missing reasons and incorrect labeling of counts.
- Feature -f pch-ip-lat-limit has been fixed for Intel platforms code named Tiger Lake. The clock rate had changed resulting in incorrect residency calculation.
- Feature -f pch-ip-active has been updated for Intel platforms code named Tiger Lake. Counter names were corrected and new counters added (HP-PLL, CNVi-IOSF-SB, CNVi-IOSF-P, and power domains EXTVNN, EXTV1p05).
- Feature -f pch-ip-active could report Active residency percentage up to half less than actual percentage in the "as percentatge of Wall Time" table on Intel platforms code named Tiger Lake. This was due to a change in the counters (PMC + SLP_S0) used to calculate that percentage, such that they could both count at the same time. That table has been replaced with a table that uses collection duration time to calculate the percentage (see *New in this Release* section).
- Fixed -f pch-ip-active feature for Lakefield. Base address for these counters had changed.

- Improved accuracy of -f hw-cpu-pstate reporting. On platforms where the hardware is controlling the processor frequency there can be an extremely high rate of change (i.e., Intel platforms code named Skylake and newer). When this occurs, using the periodic sampling of point-in-time frequency state as an estimate of time in each P-state can be extremely inaccurate. To correct this inaccuracy on these platforms, this feature now samples the average frequency calculated by the hardware that is controlling that frequency, to get a more realistic measure of residency in P-states. Since an average frequency value is read, the table now shows a range for all the P-state values rather than specific frequency P-states. In addition, the table reporting approximate average and actual average has been removed since the approximate average is no longer being collected. Note: On Intel platforms code named Ice Lake and Tiger Lake that have Intel Hyper-Threading Technology enabled, a hardware limitation requires use of --polling option to get accurate results for this metric. The following message is reported if the polling option is required: *CPU P-state results may not be accurate on this platform. Please specify --polling to get accurate CPU P-state results.*

  We are working on removing this requirement. An experimental option is available in engineering builds following release 2019.12, which resolves the problem by reporting P-states per-thread rather than per-Core.
- Feature -f hw-cpu-cstate no longer combines Core C0+C1 residency on Intel platforms code named Ice Lake. The Core C1 residency is now being read allowing C0 residency to be inferred as a separate value.
- Fixed issue in the -f dpst feature seen on Intel platforms code named Ice Lake. Incorrect data was being reported due to reading wrong address size.
- Removed GT-LLC-CLOCK-ACTIVE from the -f ddr-bw table for Intel platforms code named Tiger Lake. This was not a bandwidth counter.
- The -f connected-standby feature now appears in the help on all platforms where it is supported.
- Continuous profiling mode has been improved. It now supports longer collection durations, cleaned up child process termination, and resolves issues which resulted in empty data being returned.

Version 2.11

New

Release v2.11 includes these new features.

- Added limited NDA support for Intel platform code named Tiger Lake. These features are not supported because they could not be validated at the time of this release: hw-gfx-cstate, hw-gfx-pstate, panel-srr , pch-ip-active, edram-state, sata-lpm and cpu-gpu-concurrency. These metrics are available in the internal package, but were reporting only zero values at the time of this release.
- Updated Tiger Lake PCH Active (ER) counters.
- Tiger Lake platform introduces telemetry aggregator as a new source for debug metrics. Access to this data requires an additional driver, which is controlled by Microsoft, and will eventually become available in their Windows* 10 OS pre-release builds for 1H20. Metrics using that source have been implemented in this release of Intel SoC Watch. Once the necessary driver is made available, the new feature option for this data will be shared. It will collect: CPU Pkg C debug block/wake reasons that are time-based (vs. the count-based data currently provided), Pkg C state residency (duplicates legacy MSR counters), and memory bandwidth (replaces the legacy counters). Additional metrics available from the telemetry aggregator will be reported in the next Intel SoC Watch release.
- Improved PCIe reporting by adding support for latest NVMe device (Teton Glacier Optane) and handling multiple devices with the same name in pcie-ltr and pcie-lpm reporting by appending the Root Port number.
- Added new feature -f dpst to report if Display Power Saving Technology (DPST) is enabled, corresponding level, and if Enhanced Power Savings Mode (EPSM) is enabled. It also reports the South Backlight (SBL) duty cycle frequency percentage. This is supported for the following PCHs: SPT, CNP, and ICP.
- Added limited support for Intel platform code named Ice Lake-Xeon.
- Removed support for Windows 8.1 OS.

Fixed Issues

Release v2.11 has fixes for these issues:

- ACPI S-state (-f acpi-sstate) and its associated groups (sys and sstate) now properly display a hibernation message when hibernation is detected during the collection.
- Improved reporting of an unrecognized CPU and PCH. The error message reports both IDs.
- On Intel server platforms code named Ice Lake, CPU C-state Core level reporting now combines CC0+CC1 (similar to client platforms).
- Corrected CPU C-state reporting for server platforms. Removed reporting of unused Core C3 state and Package C7-C10 state residency for Intel platforms code named Skylake-Xeon and newer from feature -f hw-cpu-cstate reports.
- Package power (-f pkg-pwr) feature no longer reports extremely large values if the system entered hibernation during collection.
- Previously, if the SoC Watch installation was corrupted such that the SoCWatchConfig.txt file was missing, a message displayed indicating unknown processor error. An improved error message now displays when the configuration file (SoCWatchConfig.txt) is missing or corrupt. For the internal package zip file, this file may not be copied because it contains the words Intel Top Secret. There are some registers included in this package requiring that classification. You may need to confirm need for this file or it will not be written on the target system.
- If multiple SATA disks had the same name they could not be distinguished in the -f sata-lpm trace file tables. The Disk name column in the Sampled Residency and Sampled Counts tables now include the BDF and Port number to uniquely identify each disk.
- Corrected an error in the Core ID reported in the Core P-State/Frequency table for Intel server platforms code named Skylake-Xeon. The tool now checks for the presence of a core so that frequency data is not attributed to wrong core ID.
- Updated detection of Amber Lake (new graphics ID) platform.
- Feature -f pch-ip-lat-limit now correctly handles hibernation during collection. Previously, the hibernation time was not getting calculated and put in the Unknown column; it was reporting 0 instead.

Version 2.10.1

New

Release v2.10.1 includes these changes compared to v2.10:

- This release corrects an error in a JSON-formatted help file. This fix is required to properly support the use of Intel SoC Watch by the Intel Powerhouse Mountain tool.

Version 2.10

New

Release v2.10 includes these new features.

- Added support for Intel platform code named Comet Lake PCH metrics. Includes support for CMP-LP and CMP-H.
- Added initial support for Intel platforms code named Cascade Lake (CLX-AP). The tested metrics include: `core-temp`, `c-state`, `p-state`, and `pkg-pwr`.
- Added support for Intel platforms code named Comet Lake.
- Added support for TypeC Subsystem feature `-f tcss-cfg-status`.
- Enhanced feature `-f tcss-cfg-status` to include report to show Port Mode Type (USB, DP, TBT, etc).
- Added option to summarize a time segment of a collection. The new option `--result-slice-range` can be specified with option `-i` to summarize a time slice from a prior collection for a particular section of interest. See the *Intel SoC Watch User's Guide* for usage details.
- Added throttling reasons feature (`-f ia-throt-rsn`) for Intel platforms code named Lakefield.
- Enhanced `-f hw-cpu-pstate` feature reporting to include *Core P-state/Frequency Histogram* summary, which makes it easier to see residencies in turbo and throttled frequency states.
- This release (v2.10) is the last to maintain support for Windows* 8.1 OS.

Fixed Issues

Release v2.10 has fixes for these issues:

- For Intel platforms code named Lakefield:
  - Feature `-f pch-active` was reporting only 0 values. This has been corrected.
  - Feature `-f pch-slps0` was reporting only 0 values. The feature has been disabled until a replacement counter is provided by the hardware. The companion feature `-f pch-slps0-dbg` has also been disabled.
- Resolved issue where `-f pmc-ip-pg-res` values were all reported as 0. The problem occurred only if `-f soc-temp` was collected at the same time. This has been fixed so that both metrics can be collected together.
- Removed redundant word "Residency" in titles for feature `-f acpi-dstate`. Titles previously shown as "ACPI D-State Residency Summary: Residency (Percentage and Time)" are now simply "ACPI D-State Summary: Residency (Percentage and Time)."
- Improved report format and labels for feature `-f device-acpi-calls`. Name space "_GPE" is always listed now, with 0 count indicating it was not observed. All other unique names spaces only appear if observed at least once. Other changes include: columns and rows are transposed and "by process" added to the title. In the trace file, the column headers were corrected.
- Resolved incorrect package power value reported on Intel platforms with multiple packages. A very large package power value was observed on Intel server platforms code named Skylake for metric `-f pkg-pwr` because the data was being read from different processors. This has been fixed.
- Resolved system crash seen on platforms that enable the Windows* OS virtualization-based security service Hyper Enforced Code Integrity (HVCI) when Intel SoC Watch was executed with the feature `cpu-pkgc-cfg` (which is included in groups such as `-f sys`). That data cannot be read when HVCI is enabled. The tool now detects when HVCI is enabled, displays a warning message, and disables collection of that feature if specified.
- Resolved issue preventing use of drive letter in a pathname used in an argument on the Intel SoC Watch command line.
- Fixed error in `-f acpi-dstate` D3 Cold residency caused by unusual occurrence of a D3 Hot/Cold transition event occurring when the prior state was not D3. The problem was observed as time in D3Cold that should have been D2.
- The logical core count displayed in Intel® VTune™ Amplifier summary page for an imported Intel SoC Watch collection is now correct.
- On Intel platforms code named Ice Lake, core C0 and C1 state residency could be inaccurate on hyper-threaded platforms. The issue was seen as a mismatch with residency in CPU P-state report for 0 (idle) frequency. The error occurs because of missing hardware support that enables counting the core activity from any thread. Since neither core C0 or C1 can be determined individually, the tool can only infer the sum of both. Therefore, the core C-State residency report gives a single value labeled C0+C1 on this platform, rather than C0 and C1 separately. A message is printed when this occurs.
- Corrected reporting for several frequency values in feature `-f sa-freq`. IPU-PS frequency was corrected for CNL and ICL. DDR-QCLK frequency was corrected for SKL, KBL, CML, CNL, and ICL. QCLK-REFERENCE was corrected for ICL.
- For Intel platforms code named Tiger Lake:
  - Updated TGL PCH activity counters reported by `-f pch-ip-active`. The Modphy function and rate mapping counters are not included (pending documentation on their location).
  - Corrected feature `-f s0ix-subs-res` to be associated with the TGL PCH rather than the TGL CPU. This allows that metric to be collected on the TGL Z0 platform (WHL CPU + TGL PCH)
- Corrected reporting of the pending status seen in feature `-f tcss-cfg-status` Port DHPD Status report. This required splitting that report into two reports, the second report gives the correct Port DHPD Pending Status.
- Fixed error in reporting SATA HIPM capability/enabled setting shown in `-f sata-lpm` feature.

Version 2.9

New

Release v2.9 includes the following new features.

- New metrics:
  - `-f tcss-state` reports TCx state residency and entry count for TypeC Subsystem added to NDA package.
  - `-f device-acpi-calls` summarizes device ACPI namespace calls by process. Useful in determining if 3rd-party device is causing interrupts (GPE namespace calls).
  - `-f s0ix-subs-status` replaces old name `-f s0ix-subs-sts`, to better align with other metric names.
- Improved organization of reports in `_trace.csv` report. All reports belonging to a feature are now grouped together.
- Improved informational messages:
  - Now display a message if the `-f display-state` feature's counters are not enabled.
  - Added CPU ID and PCH ID model/family/stepping values when reporting them as unknown.
- Modified `-f hw-cpu-cstate` reports as follows:
  - In Package C-state report, added following notes to make it clear that software cannot request to enter PC2 or PC3 states explicitly, these are used by hardware.

    Note: PC2 is non-architectural state - software cannot request to go to PC2 explicitly. PC2 can be a transient state between PC0 and deeper pkgC states.

    Note: PC3 is non-architectural state - software cannot request to go to PC3 explicitly.
  - In the Core C-state report, removed the C3 state for platforms that are not using it rather than always reporting 0. Core C3 is not used on 10nm platforms, which include CNL, ICL, LKF, and TGL.
- Multiple enhancements for `-f tcss-cfg-status` reporting, as follows:
  - Traced data reports no longer have blank spaces in unused columns. Instead, "N/A" is printed if the field is not applicable to the command being interpreted.
  - Changed GPP_B11 / PMALERT Interrupt reporting so that it is collected over time rather than once. Not clear from documentation whether this data will change, so made this adjustment in case it does change.
  - Added raw data values and the offset from which that data is collected to all tables where the tool is interpreting the bits. This allows direct viewing of the bits in case the interpretation of the bits change.
  - Removed column in traced data with redundant data.
  - Modified report headers to better identify contents and relate them to the TypeC subsystem.
- Intel SoC Watch driver for OneCore package is compliant with State Separation requirements.
- Added `-f sa-freq` support for Intel platforms code named Tiger Lake

Fixed Issues

Release v2.9 has a fix for the below issues.

- Removed column with redundant data in trace file reports for features `os-cpu-cstates`, `os-cpu-pstates`.
- Removed support for `pch-slps0` and `pch-slps0-dbg` from Intel platforms code named Lakefield and Tiger Lake. Those hardware counters are no longer supported. Sum the s0i2.0 and deeper states reported by feature `-f s0ix-subs-res` to calculate an equivalent residency indicator for Modern Standby.
- Feature `-f display-state` occasionally reporting huge numbers has been fixed. The issue was caused when the hardware counter occasionally set to 0xffffffff, that value is now discarded and the tool prints a message if it was seen.
- Feature `-f dram-pwr` was reporting two sets of tables, this redundancy has been removed.
- Corrected error causing `-f xhci-lpm` to report L1 Capability as 'No' when the device is L1 capable.

- PCH and PCIe metrics can now be imported to Intel® VTune™ Amplifier. (`-f cpu-pkgc-dbg` is still disabled)
- Intel® VTune™ Amplifier 2019 Update 2 no longer reports error during import if too many metrics are included in the `.pwr` file. Previously, if the `.pwr` file being imported included too many metrics the following error was seen: *Error 0x4000002a (Database interface error) - Precompute error.*
- PCH Activity feature (`-f pch-ip-active`) occasionally reported very large values on platforms with certain PCH. The SPT and KBL PCH activity counters update slower than expected requiring an adjustment that was not uniformly applied in the calculation. This has been fixed.
- CDCLK frequency was reported as double the actual frequency on Intel platforms code named Ice Lake. Corrected address and mapping to determine -f sa-freq metric's CDCLK frequency on Ice Lake platforms.
- Updated PCH activity counters for Intel platforms code named Ice Lake PCH ICP-N and PCH ICP-H.
- Updated `-f tcss-state` TCx state residency counters for Intel platform code named Tiger Lake.

Version 2.8

New

Release v2.8 includes the following new features.

- New support for the following Intel platform code names:
  - Pre-silicon Elkhart Lake with Mule Creek Canyon PCH support, no support yet for new IP. Limited testing.
  - Comet Lake CPU recognition (WHL configuration). No Comet Lake PCH yet. No testing. (Internal only)
  - Lakefield support now includes connected standby & PCH metrics support in NDA version.
- New features:
  - Feature `-f display-state` reports DC5/DC6 entrance counts. Previously, this report was part of `panel-srr` feature which required panel self-refresh to be enabled on the platform. `display-state` does not require panel self-refresh to be enabled. (Internal only)
  - New group name `-f display` includes features `display-state` and `panel-srr`.
  - Type C subsystem features `-f tcss-state` and `-f tcss-cfg-status`, and group name `-f tcss`, which includes both.
    - The `tcss-state` feature reports TCx state residency and entrance counts and is supported on Ice Lake, Lakefield, and Tiger Lake platforms.
    - The `tcss-cfg-status` feature reports subsystem version and status information in the summary file, and state change trace in the _trace file. It is only supported on Ice Lake platforms. The trace shown for this feature is different for tables "PCH Request FIFO Last Entry" and "IOM Firmware Current Task" in that they only show a sample if a change occurred from the previous sample, whereas other tables (and other metrics) show every sample taken. The `tcss-cfg-status` feature is still evolving, expect changes such as filtering for other tables. (Internal only)
- PCIe report improvements:
  - PCIe LPM Root port map now includes port 8.
  - PCIe LPM and LTR reports now include root port number in Device Name column values
- Added filter to `acpi-dstate` report to reduce devices listed (same as in v1.19 release). The filter is enabled by default, turn it off using `--option no-device-filter`.

Fixed Issues

Release v2.8 has a fix for the below issues.

- Cleaned up the s0ix-sstate report. Removed SYSTEM from column headers and entire Platform Residency Matrix table, which were not useful.
- Display warning if --program-delay option is not used in conjunction with --program option.

- Reorganized cpu-pkgc-dbg tables. Moved events that were blockers to more than one state into a separate table labelled appropriately. Previously, the same counter appeared in the tables for each state making it appear to have been a blocker with the same count for each state rather than a blocker of one or the other state. Specifically,
  - Event 11 moved into new table Cannot go deeper than PKG C2/R
  - Event 11 moved into new table High Residency in PKG C2/3
  - Event 66 moved into new table Cannot go deeper than PKG C6/9
- Changed registers used to read DC5/DC6 entrance counts reported by display-state.
- Feature pkg-pwr reports cleaned up to conform to other reports.
- Feature pch-ip-active now includes MODPHY lane translation for Intel platform code named Cannon Lake PCH (CNP-LP and CNP-H)
- Improved check for EDRAM presence. Previously, reported EDRAM as present on platforms when it wasn't.
- Resolved issue in `s0i3-sstate` report for residency and entry counts were huge on occasion. Issue occurred for collections started shortly after a system reboot, when counter had not been set to zero yet.
- PCH Slp_S0 residency reports did not match for `-f pch-slps0` and `-f connected-standby`. The error was in pch-slps0 if residency exceeded maximum 32-bit value. The value is now properly stored as 64-bit.
- Fixed problem where `-f ddr-bw` report was wrong on occasion when `-m` is not specified. The counters can overflow after just a few minutes of collection and this would not be caught if `-m` was not used. Therefore, these metrics are now always collected overtime, even when `-m` is not specified (snapshot mode is no longer available for ddr-bw). The issue has been seen most often on Intel platforms code named Ice Lake.
- Changed default for hotkey Alt-S to be disabled. Must use `--enable-alts` to turn it on thereby allowing use of Alt-S as alternative to Ctrl-C for stopping a collection. This hotkey combination is an issue with HOBL (Hours of Battery Life) Productivity workload in which Outlook uses Alt-S to send email, but that is caught by Intel SoC Watch as termination hotkey. In v2.7 there is an option (`--disable-alts`) to turn it off, which has been replace by the option to turn it on.
- For Intel platforms code named Lakefield, ddr-bw and gfx-cstate RC6 reporting has been corrected.

Version 2.7

New

Release v2.7 includes the following new features.

- Added Core P-state Average Frequency table to `-f hw-cpu-pstate` summary. A table reporting Core P-state Approximate Avg and Actual Avg frequency has been added to `-f hw-cpu-pstate` metric, similar to what was found in v1.19.1. Note that the Core P-State/Frequency Summary report shows sampled frequency Residency as a % of total collection time, but the Core P-State Average Frequency table is calculated as a % of Active (C0) time, excluding idle time. This is required in order to allow comparison of Approximate Avg to Actual Avg frequency as a measure of accuracy for the sampled data. (The Actual Avg frequency comes from registers Aperf/Mperf that accumulate average frequency during active time, providing the most accurate average frequency value.)
- Added option to delay start of program, `--program-delay`. If the `-p` option is used to launch a workload before collection, you can use `--program-delay <seconds>` to delay the starting of that program for the specified number of seconds. Collection will begin after the program starts unless the `-s` option is also given. When both are specified, Intel SoC Watch first waits for the number of seconds specified by the `program-delay` option then starts the program and waits for the amount of time specified by the `-s` option before starting data collection.
- Added guard against sampling bandwidth data too frequently on certain platforms. On Intel Atom® processors there is a minimum sampling interval when collecting bandwidth metrics based on signal counters. A warning will now be displayed when an interval smaller than the default 10 milliseconds is specified with option `-n`, and the default will be used instead.

- Added option to generate help output in JSON format. The option `--export-help` can be used to generate a JSON format help output file, useful in automating discovery of features available on a platform.
- Added new group names to make it easier to find and select features. These include:
  - `cpu-hw` Collects most CPU-specific metrics that are obtained from hardware data sources (`hw-cpu-cstate, hw-cpu-hwp, hw-cpu-pstate, ia-throt-rsn, cpu-gpu-concurrency, core-temp, soc-temp, cpu-pkgc-dbg, cpu-pkgc-cfg, ia-temp`)
  - `cpu-os` Collects all CPU specific metrics that are obtained from OS event traces (`os-cpu-cstate, os-cpu-pstate, timer-resolution`)
  - `cnv` Collects CNVi metrics (`cnv-active, cnv-ltr`). Note that this is seen on Intel Atom® processors only. On Intel Core™ processors the PCH metrics include CNV so there are no standalone CNV metrics.
  - `gfx-hw` Collects most GPU-specific metrics that are obtained from hardware data sources (`hw-gfx-cstate, hw-gfx-pstate, gfx-throt-rsn, cpu-gpu-concurrency, gt-temp`)
  - `gfx-os` Collects all GPU-specific metrics that are obtained from OS event traces (`os-gfx-cstate`)
  - `lpss` Collects all Low Power Subsystem I/O metrics (`lpss-ltr`)
  - `tcss` Collects all TypeC Subsystem metrics (`tcss-state, tcss-cfg-status`). Note that currently these are not visible in help since these have not been validated on functional hardware and must be used with caution since the data could be erroneous.
- Modified feature group names to include more features making it easier to get all relevant data. The changes are as follows:
  - `cpu`: Includes all of cpu-hw + cpu-os (more metrics than previously)
  - `gfx`: Includes all of gfx-hw + gfx-os (more metrics than previously)
  - `pch-all`: Includes pch-ip-lat with the default list of IPs. You can change the IPs by adding `--option lat-limit-ip` with the IPs you select from the list shown in help.
  - `temp`: Includes additional temperature metrics as available on the target platform (`sa-temp, comp-max-temp, gt-temp, ia-temp`)
  - `device`: Includes all I/O device metrics (`acpi-dstate, nc-dstate, sc-dstate, panel-srr, pcie, sata, xhci, lpss`)
  - `sstate`: Includes all system level state metrics as available for the target platform (`acpi-sstate, pch-slps0, pch-slps0-dbg, s0ix-sstate, s0i3-sstate, s0i3-sstate-dbg`)
  - `sys`: Includes most metrics, including the metrics in the expanded groups above plus bandwidth and package power. It does not include OS-based metrics which have a hardware equivalent, nor the PCH metrics. (`sstate + device + temp, cpu-hw, gfx-hw, ddr-bw|dram-bw, pkg-pwr, timer-resolution`)
- Feature `-f sstate` is now consistent across OSes. It is a group name that includes all metrics related to system idle states. On Intel Atom processors it includes S0ix or S0i3 states, whereas on Intel Core processors it includes pch_slpS0, pch_slpS0_dbg if supported by the target platform.
- Added energy metric for the Package. Feature `-f pkg-pwr` is now supported on Windows. This reports Joules and Watts used by the Package and comes from the Energy MSRs.
- Added support for Intel platforms code named Cherry Trail. This support has been enhanced from what was available in v1.19.1, the `-f s0ix-sstate` report has been extended to include eMMC, SDCard, and SDIO device status.
- Added option to disable the Alt-S hotkey. The key combination Alt-S was added as an alternative to Ctrl-C for terminating a collection. However, if a workload launched by Intel SoC Watch (option `-p`) uses Alt-S for its own purposes (ex: 3DMark benchmark) it will cause Intel SoC Watch collection to terminate prematurely. Use option `--disable-alts` to tell Intel SoC Watch to not interpret Alt-S as a command to stop collection.
- Added support for Intel platforms code named Amber Lake.

- Enabled support for Intel platforms code named Broxton (-M). Added support in Internal and NDA packages for small number of users still using this for early platform development. Note that the OneCore Intel SoC Watch package does not support collection of VISA metrics, so memory bandwidth and self-refresh metrics have been disabled in that package.
- Added Sleepstudy description to Intel SoC Watch report for debugging SLP_S0 blockers. Microsoft's powercfg Sleepstudy* report describes blockers to Modern Standby using terms approved for external use. Intel SoC Watch includes this description in the Blocking Reason column of its -f pch-slps0-dbg report, to guide users from an issue reported by Sleepstudy to the Intel SoC Watch equivalent with more information for further investigation. (Available on Intel platforms codenamed Cannon Lake and Ice Lake.)
- Added feature to report system configuration settings for PkgC states. Feature `-f cpu-pkgc-cfg` reports the configuration settings that control entry to Pkg C-states. This is useful to discover if a platform configuration is blocking entry to expected low power states or is not following Intel guidelines. This feature is not available if Windows Virtual Secure Mode is enabled on the platform.
- Added S0ix substate residency and status settings metrics. Intel platforms code named Lakefield and Tiger Lake have additional low power states, substates of S0ix. Features `-f s0ix-subs-res` and `-f s0ix-subs-sts` report s0ix.y substate residency and status settings, respectively. These are included in groups `sstate` and `sys`.
- CPU PkgC debug report uses internal description string rather than NDA. The internal version of Intel SoC Watch has replaced the NDA version of the blocking/wake reason descriptions with the internal description in the `-f cpu-pkgc-dbg` report. In many cases, these descriptions include more detail to help your understanding of the problem, but they cannot be shared directly with external customers. Detail was purposefully removed by the architect when creating the NDA version of the strings to protect Intel intellectual property. There are some cases where the internal description is less helpful. We will work to get internal descriptions improved in the hardware specification as the strings are being extracted directly from there.
- Added new features for TypeC Subsystem (TCSS) debug. New features `-f tcss-state` and `-f tcss-cfg-status`, have been added for Intel platforms code named Ice Lake to report residency in TCx states and configuration status of IOM and TCSS. These features are in the internal package only and do not appear in the help because these are untested metrics due to unavailability of functional hardware at the time of release. They are included as hidden metrics to enable users who have hardware to start testing and either benefit from them or report issues with them.
- Feature -f sa-freq now includes warning to describe potential inaccuracy that can occur when idling in Pkg C2 or C3. The system agent frequencies can change while in PC2 or PC3 states, but Intel SoC Watch will not collect any samples in those states. Therefore significant time in those states increases risk and degree of inaccuracy in the summary report. There is now a warning printed in this report to make users aware of this.
- Enabled support for Ice Lake PCH ICP-H and ICP-N. This is enabled in the internal package only due to very limited testing.

Fixed Issues

Release v2.7 has a fix for the below issues.

- Automation_Summary.csv file now includes all summary reports and column headers are unique. Corrected the issue where some tables from the summary report were not included in the Automation_Summary file. Also changed the column headers for all data to make them unique by prepending the table name, as seen in the summary file, to each column header.
- Corrected error in reporting ddr-bw. A regression from v1.19.1 occurred in reporting ddr-bw, which appeared most often on Intel platforms code named Ice Lake. The error resulted in significant under reporting of MB/sec in certain scenarios. This has been corrected.
- Improved error reporting for syntax errors on command line. Error messages are now reported on the console for command line syntax errors such as including an argument with -m or using invalid value for -r option.
- Corrected pathname for output file pathname that was being displayed on the console. When relative pathnames were specified with the -o option, the console message giving the complete pathname for the output file could be incorrect.

- Improved labeling of cores on systems with multiple packages. Windows OS numbers CPU cores contiguously across all packages. Previously, the set of cores on the second package might precede the cores from the first package, resulting in the core numbers being out of order in the report. This has been fixed so that package 0 cores are shown first followed by package 1, etc. Also, if a system has more than one package, the column header will include the package number prepended to the core number (ex: Package_0/Core_0). If the system has a single package, the column header does not change, and gives just the core number (ex: Core_0).
- Fixed issue which occurred when multiple NVMe devices were on a platform. When multiple NVME devices were present, the data for each could be swapped in the report.
- PCH metrics gave inconsistent results on Intel platforms code name Ice Lake. The address for the Ice Lake PCH metrics was changed by PMC patch 5 which caused inconsistency among the PCH metrics. Intel SoC Watch is now using the new location.
- Incorrect panel self-refresh data for PSR2. There was an error in reading residency for `-f panel-srr` when PSR2 was used. This has been corrected.
- XHCI LPM incorrectly reported a USB device when none was connected. The feature `-f xhci-lpm` did not report devices correctly when more than one host controller was present and no USB device connected. The second host controller was reported as a USB device. It now reports no XHCI devices connected and no report is generated.
- Resolved crash seen on Intel platforms code named Ice Lake with Virtual Secure Mode enabled. The features `-f edram-state` and `-f comp-max-temp` cannot be read when VSM is enabled on Ice Lake platforms, so these metrics are now disabled automatically and collection continues for other metrics.
- Improved reporting of comp-max-temp when PCH temperature unavailable. When PCH temperature data was unavailable, Intel SoC Watch was reporting it as 0 for `-f comp-max-temp`. This has been improved such that on Intel platforms with PCH code named Kaby Lake PCH-H and Cannon Lake PCH-H the PCH entry is removed (because PCH is not included in the MCP), and for all other PCH, if access to PCH metrics is disabled, a note is printed in the report indicating that is the reason for the 0 value displayed.
- Fixed several issues in handling filename argument to option `--log`. The handling of the filename argument for option `--log` has been improved so that it behaves like the `--output` option. Folders in the specified pathname will be created if they don't exist, use of "/" in pathname is allowed, and an error is reported if the file location is not writable rather than the tool crashing.
- Numbering of connected standby sessions is consecutive. Previously, numbering of connected standby sessions shown for `-f connected-standby` was shared with active sessions, which are not shown, so it appeared as if sessions were missing. This has been corrected.

Version 2.6/2.6.1

New

Update release v2.6.1 includes the following new features.

- Windows OneCore OS (WCOS) Intel SoC Watch package changes:
  - Includes DCHU compliant Intel SoC Watch driver.
  - Driver startup is different in WCOS build: 1) Intel SoC Watch executable checks if its driver is already installed and does not attempt to install it if found (desktop version always installs its driver), 2) Intel SoC Watch executable does not delete its driver at the end of a collection (desktop version always deletes its driver). This makes it possible to have a mismatched driver and executable. The summary report header displays the Intel SoC Watch application and driver version numbers to help identify such issues.
  - No VISA metric support in WCOS package at this time.
  - Restored the check for HyperV and Virtual Secure Mode (VSM) being enabled in the Intel SoC Watch package for WCOS. This check prevents metrics from being collected that are not available in that mode (e.g., cpu-gpu-concurrency) and would cause a system to crash.
- Modified the --version option output.

Release v2.6 includes the following new features.

- Added option to log console output to a file. Use option `--log <filename>` (short name `-l`) to log all console messages to a file.
- Added explanatory note to reports containing the Unknown value. For `-f hw-cpu-cstate` and `-f hw-cpu-pstate`, CPU C-State and CPU P-State reports now include a note explaining the meaning of the Unknown value that may appear in these reports. The residency table note is: "Unknown" state occurs when the system enters a platform idle state (ACPI S3 or S4). The wakeup table note is: "Unknown" wakeups mean the CPU wakeup reason could not be attributed to a known cause.
- Enhanced PCIe LPM reporting to include cycle router number and root port ID for better identification of NVMe (re-mapped) devices. This additional information is available for Intel platforms with Platform Controller Hub (PCH) code named Kaby Lake PCH-H and Cannon Lake PCH-LP and -H. (Support for Skylake PCH-LP is pending discovery of mapping documentation.)
- PCIE LPM feature's Root Port vs CLKREQ Mapping table has been extended with additional ports for Intel platforms with PCH code named Cannon Lake PCH and Ice Lake PCH.
- Reduced device ID checking for PCIe metrics. The `-f pcie-lpm` and `-f pcie-ltr` features will no longer result in unknown device ID warning. It is now assumed the devices will behave in expected fashion so that users are not burdened with having to add new device IDs manually.
- Added lane rate information to the PCH Active State report. The `-f pch-ip-active` feature now includes lane rate information in the Physical Mode Lane Assignment table for Intel platforms code named Ice Lake. Previously, the rate was listed as Unknown.
- Improved ordering of reasons reports for -f s0i3-sstate-dbg. The Exit Reasons summary table is now shown prior to the individual Exit Reason reports.
- Added support for new ICL CPUIDs for -H and -I SKUs (Internal only).
- Enabled s0i3-sstate-dbg feature for Intel platform code named Apollo Lake in NDA package. Addition for Intel platform code named Gemini Lake is pending release of this metric in external documentation.
- New feature to collect IA and GT bandwidth prior to last-level cache (Internal only). Feature `-f idi-bw` reports Reads and Reads+Writes per agent (Cores and GT) in-die-interconnect (IDI) traffic before the last-level cache (LLC). Use `-f ddr-bw` for post-LLC memory traffic. IDI traffic is per core as opposed to the aggregate number over all cores given for DRAM traffic, allowing deeper evaluation of: concurrent or multi-core workloads, effectiveness of LLC in filtering traffic from IA vs GT for a given workload, and fabric bandwidth limitations. This was requested for internal investigation purposes and is included in the internal package only.
- Added driver version to the summary report header. Summary reports now include the version of the Intel SoC Watch driver used to collect the data in addition to the application version number.
- Added Alt-S as a hot key alternative to Ctrl-C for Windows 10 Desktop OS.
- Removed several OS-based features from the `-f sys` group. The OS-based features which had a comparable hardware data (`os-cpu-cstate`, `os-cpu-pstate`, `os-gfx-cstate`) were removed from the group sys. Processing the OS-based ETL trace data is very time consuming for longer collections and often users do not need these OS-based metrics since the hardware metrics are more accurate. Removing these from the commonly used sys group reduces post-processing time and file size. Both OS and hardware based metrics are still included in the cpu and gfx group names, or can be explicitly added to the command line using their individual feature names.
- HWP reporting is no longer included in the `hw-cpu-pstate` feature. The `-f hw-cpu-pstate` feature now collects only Core P-state frequencies to allow finer-grained selection of which data to collect. Use the new feature `-f hw-cpu-hwp` to collect the HWP Guaranteed, Highest, Lowest, Most-Efficient Performance summary reports. The HWP feature is still included in the sys, cpu, and cpu-pstate groups.
- Added support for Intel platform code named Whiskey Lake.
- Intel platform code named Lakefield:
  - All metrics are supported except: edram-state, comp-max-temp, DCx states in panel-srr, and DMI capabilities in pcie-lpm.
  - Support included in NDA package, except for PCH activity metrics which are pending confirmation that they can be release externally.
  - pch-ip-active report only includes IPs present for Lakefield. Other IPs are excluded (e.g., GEN3 PLL, USB3 PLL, CNVi PLL).

  - pch-ip-active reports 8 DEKLPHY lanes rather than 16 MODPHY lanes.
  - pch-ip-active includes lane rate in the physical lane assignment report.
- Enabled temperature metrics for IA, GT, SA on Intel platforms code named Apollo Lake and Gemini Lake (included in NDA). The `ia-temp`, `gt-temp`, and `sa-temp` features are now enabled for Intel Atom® processors running Windows.
- Intel platform code named Tiger Lake (preSi, Internal only):
  - Enabled pch-slps0-config.
  - Added rate information to the physical lane assignment report for `-f pch-ip-active` feature.
- ETL data collected using `-f phm` now include constraints events from Microsoft-Windows-Kernel-Pep provider. This can be viewed by opening the ETL file using Microsoft's xperf or WPA tools.
- Windows OneCore OS (FactoryOS) support:
  - A separate package is available for use on platforms running FactoryOS
  - Driver is not yet UWD compliant, it will be.
  - All options are supported except: `-p`, `-z`
  - Hot key, Alt-S, is not supported
  - Use of Ctrl-C is not functioning, use timed collections instead.
  - All core metrics are supported, with minor differences as follows:
    - `-f acpi-dstate` report has no Class Name information, column will be blank.
    - `-f os-cpu-cstate` report will have reduced symbolic information
  - No VISA-based metrics are available on Intel Atom platforms
  - Intel SoC Watch application checks for an existing Intel SoC Watch driver in the `/system32/drivers` folder and uses it if found. This aligns with Windows OneCore OS usage model where the driver would be pre-installed with the OS. With this change, it is possible for the Intel SoC Watch application to use an older driver than what was packaged with the current release. Intel SoC Watch will execute with the older driver, but it may have reduced functionality due to lack of support or missing bug fixes in the older driver. In order to catch situations where an old driver is in use, the summary report header now includes the version of the driver as well the application version number.

Fixed Issues

Update release v2.6.1 has a fix for the below issues.

- Removed idi-bw support. An error was discovered in the v2.6 implementation and subsequently a decision was made that EMON will provide support.
- Occasionally cpu-gpu-concurrency data sums to >100%. This occurs when hardware over counts. SoC Watch now checks the timestamp delta and adjusts for over counting.
- Warning message is now displayed when you have specified metrics that cannot be collected at the same time due to hardware limitations. For example, features comp-max-temp and edram-state cannot be collected at the same time. Also, only one of the following metrics can be collected at a time: `pmc-ip-d0i3-occ`, `pmc-ip-d0i3-res`, `pmc-ip-d3-occ`, `pmc-ip-d3-res`, and `pmc-ip-pg-res`, `s0i3-sstate`, and `s0i3-sstate-dbg`. The warning message will indicate which metric is not being collected (e.g., Warning: Exceeded hardware telemetry counter limitation. Will not collect metric "XXXXX").
- Removed trailing hyphen from report titles in the trace output (e.g., Graphics Active State).
- Large collection durations specified with -t option are now handled correctly. Previously, a time value > 216 would be truncated.
- Platform LTR summary report correctly reports minimum LTR value. When an LTR value of 0 was collected, as seen in a trace file output, the summary did not report that as the minimum LTR. This has been corrected.

Release v2.6 has a fix for the below issues.

- Collecting `-f pcie-lpm` on a platform with a GbE device could result in significant tool overhead that reduced Pkg C10 residency. The problem has been resolved by reducing collection of the GbE controller link states from every 100ms to every 1 second. This is currently a fixed interval for GbE link state collection, not changed by using the `-n` option.

- Resolved Gfx C-State and P-state reporting errors seen on Intel platforms code named Ice Lake and Cannon Lake. The problem was caused by a change in register size. The problem manifested for hw-gfx-cstate as RC6=100% when running graphics workload, and all 0 P-states for hw-gfx-pstate.
- Gfx C-State Residency report was missing for short collections. If the GPU was inactive during the entire collection period the Gfx C-State Residency report would not appear in the summary file because no valid C-states are collected. Now `-f hw-gfx-cstate` will report a message in the report rather than omit the report entirely. The message is: Note: GPU was inactive during the entire collection. No valid gfx-cstate values were collected.
- Fixed error s0i3-sstate-dbg. The feature `-f s0i3-sstate-dbg` was reporting all zero data due to error in reading that data.
- Fixes specific to Intel platform code named Ice Lake:
  - Corrected reporting of `-f pch-ip-active`.
  - Enhanced `-f pch-ip-status` to include TBTLSX and add PECI to CSME aggregate (for PCH -H)
- Using `-f hw-cpu-cstate` feature with --polling option when collecting on a multi-socket server platform like SKX resulted in erroneous data reporting. The problem has been fixed.
- Summary totals reported by Intel® VTune™ Amplifier were different than what was found in the Intel SoC Watch summary report due to lost precision during the import of the trace data. The problem is fixed but requires the new .pwr files to be visualized using Intel VTune Amplifier 2018 Update 2 or newer. If still using an older version of Intel VTune Amplifier you will need to set environment variable PW_ENABLE_LEGACY_VTUNE=y before generating the .pwr file to be able to import it (reverting to loss of precision in the total values).
- Use `-r vtune` could result in empty .pwr file after successful collection. Some metrics are not supported for visualization in Intel VTune Amplifier (see Known Issues). Unsupported metrics have no data written to the .pwr file. Now, when there are no supported metrics in a collection, no .pwr file will be created rather than a 0 size file.
- Feature `pch-ip-status` now includes two missing PCIe controllers for Intel platforms with PCH code named Skylake-H and Kaby Lake-H.
- The console message indicating the data output was written to the result files is now written after completion of writing to that file.
- ACPI D-State Residency report no longer contains same device ID twice in the report as seen on some systems. Running collections for more than 30 minutes on systems with 3rd-party devices could result in the same device appearing twice in the ACPI D-State Residency report generated by `-f acpi-dstate`. Intel SoC Watch now handles the case when more than one ETL rundown event occurs for a device.

Version 2.5

New

- New PCH IP Latency Limit report available for big core platforms (NDA only). For Intel platforms code named Skylake and newer, the new feature `-f pch-ip-lat-limit` can be used to report the amount of time an IP is limiting the memory LTR request to the CPU (i.e., the IP's LTR is too short to allow entering deeper sleep state). The hardware support for this only allows monitoring three IPs at a time. You can select which IPs to monitor by including option `--option lat-limit-ip=[IP1, IP2, IP3]`. By default, SPA, SPB, and SPC are monitored. Use the `--help` option to get the complete list of IP available for the target platform's PCH. Additional IPs that can be monitored include: SATA, GBE, XHCI, ME, EVA, HD-AUDIO, ESPI, LPSS, CAM, SCC, and ISH. This feature is included in group names `pch` and `pch-all`.
- New PCH SLP_S0 Configuration report available for platforms with Intel PCH code names Cannon Lake and Ice Lake (Internal only). The new feature `-f pch-slps0-cfg` reports the target platform's actual configuration settings which control entry to SLP_S0. The report includes a table of qualifiers and whether it is required or not required for SLP_S0 to occur. It is not clear whether the setting can change over time, so the configuration state of each qualifier is sampled during the collection duration and counts are reported. A table of enablers is also reported as to whether it is enabled or not enabled during the collection. This feature is included in group names `pch` and `pch-all`.
- Intel platforms code named Gemini Lake are supported in External package now.

- Added `-f dram-bw` for Intel platforms code named Broxton.
- Added `-f cpu-pkgc-dbg` support for preSi Lakefield support. (Internal only)
- Added `-f pch-slps0-dbg` blocking and wake reasons for preSi Tiger Lake support. (Internal only)
- Enabled PCH metrics for import to Intel VTune Amplifier. PCH metrics `pch-ip-active, pch-slps0, pch-slps0-dbg, pch-ip-active-all` will now be included in the Intel VTune Amplifier import file generated with option `-r vtune` and viewed as a timeline after importing.
- Support for recognizing SKX and ICX servers has been enabled.

Fixed Issues

- Requesting graphics metrics on platforms that do not have a GPU no longer results in collection being terminated. A warning is displayed and collection continues if other metrics were specified.
- Unrecognized CPUIDs now report a more friendly error message and include the CPUID for easy reporting.
- Core C-States report of the total number of cores appeared incorrect on platforms with more than 8 cores. The number was being reported in hexadecimal, but without leading 0x. The number is now reported as decimal.
- Improved support for `xhci-lpm` feature on platforms with multiple XHCI host controllers. Various failures were seen on platforms with more than one XHCI host controller, all have been fixed. The failures reported were: 1) Intel SoC Watch crash, 2) unable to collect xhci-lpm error, and 3) XHCI Capabilities report had missing information.
- Issues resolved for Intel platforms code named Ice Lake:
  - Invalid Core C-State residency has been corrected. A warning is displayed if hardware counter values result in idle residency time exceeding collection duration, and active time (C0) is reported as 0.
  - Missing PCIe device IDs have been added.
  - Warning message is displayed if all counters for the PCIe CLKREQ mapping are reporting 0xff.
- Added handling in the GPU P-state feature for pre-Silicon environments that do not set LFM and HFM values. Intel SoC Watch crashes were seen on Lakefield and Tiger Lake simulations when `-f hw-gfx-pstate` data was requested because it required non-zero values in the LFM and HFM registers. It now reports a warning and disables that metric, allowing collection to continue if other metrics specified.
- Corrected collection duration time reported by Intel VTune Amplifier. After importing a collection trace file (.pwr) to Intel VTune Amplifier, its summary report could show a duration longer than the actual collection time that was reported correctly in the Intel SoC Watch summary file. The discrepancy has been fixed.
- Corrected `-f connected-standby` reporting of huge numbers when the CS Exit event was not captured in the trace log.
- Re-enabled OS CPU P-state reporting (`-f os-cpu-pstate`).
- Feature core-temp reports valid results on Intel platforms code named Cannon Lake.

Version 2.4/2.4.1/2.4.2

New

This Windows version of Intel SoC Watch marks the beginning of common command line interface and reporting format across supported operating systems on Intel® Core™ and Intel Atom® platforms. It is intercepting the Linux version at its 2.4 release point, hence the numbering that did not start at 2.0. Intel SoC Watch for each operating system now has the same command line options, result file formats, and features (metrics) that come from hardware-based data.

Windows users will see significant changes in style, format, and content of both summary and timeline result files. These changes are summarized below. While some command line option and feature names have changed since the last release, they are now the same across operating systems.

Release v2.4.2 includes the following:

- Added support for Intel platforms code named Apollo Lake with new stepping.

Release v2.4.1 includes the following:

- Added NDA support for Intel platform code named Ice Lake.

- Improved Ice Lake platform support: correcting `pch-platform-ltr` and `cpu-pkgc-dbg` offsets, adding PCIe device IDs, Root Port vs CLKREQ mapping, and adding wakeup reasons to `pch-slps0-dbg`.

Release v2.4 includes the following new features.

- Support for Intel platform code named Lakefield running Windows 10 OS (Internal only). Supported metrics are limited to those common across the heterogeneous cores. Use `-h` option to see the list of supported features.
- Support for Intel platform code named Tiger Lake (Internal only). Does not use telemetry aggregator as a data source yet.
- New feature group `sa-pstate` which includes `sa-freq` and new feature `ring-throt-rsn` which reports throttling reasons for the ring clock frequency that is include in the list of system agent frequencies. (Internal only)
- PCH Slp-S0 Debug report extended to include more blocking reason (Internal only). Additional blocking reason counters that are designated for internal use only, are now reported by feature `-f pch-slps0-dbg` for Cannon Lake PCH. These include: SDIO PLL Off, OC PLL Off, Main PLL Off, Audio ROSC Off, HPET XOSC CLKREQ, PMC ROSC Switch, AON2 ROSC Gated, CLKACK, USB2 SUS PG, Dynamic FLEX IO, TS DIS, ISH VNNAON Req, ISH VNN Req, CNV VNNAON Req, CNV VNN Req, NPK VNNAON Req, PMSYNC State Idle, PMC ARC Idle.

Summary of Changes in Intel SoC Watch for Windows v2.4 as compared to v1.19.1:

- Collection/processing behavior changes.
  - Default minimum collection interval for context switch mode collection has increased from 10ms to 100ms. This means fewer samples may be taken since at least 100ms must pass before another sample is read. When lots of context switching occurs, this will reduce overhead of collection and may reduce accuracy of metrics that come from status data sources. This was changed to be consistent across operating systems. You can change this default using the `-n` option.
  - GPU device ID is no longer matched against known IDs. Intel SoC Watch will no longer fail because of a new GPU ID, but there is a chance for system crash if a platform has a GPU that does not support reading metrics from expected locations.
  - GPU P-State (`-f gfx-pstate`) residency percentage is now given as a ratio of overall collection time. Previously, it was given as a ratio of GPU active time (RC0) so these residency results will not match between 1.19.1 and 2.4 versions unless a GPU is active during the entire collection. This was changed to be consistent across operating systems.
  - For all sampled metrics, the calculation for time-weighted averaging has changed. In v2.4, the entire time between samples is attributed to the current state collected. In v1.19.1, the time was split 50/50 between the prior state and current state. This was changed to be consistent across operating systems.
  - D-State (`-f acpi-dstate`) report lists all devices. The list of devices is no longer filtered. An option for filtering devices will be added later.
  - If hibernation occurs during collection, cannot compare reported residency percentages between 1.19.1 and 2.4. Residency percentage (%) calculations are always based on total collection time in 2.4, therefore if hibernation occurs the percentage calculation includes hibernation time. In 1.19.1, the hibernation time was not included, therefore percentages will be larger when time in state was actually the same. Intel Powerhouse Mountain residency percentages do not include hibernation time. Hibernation time is reported at the top of the summary, so you can manually adjust the percentages for proper comparison.
  - Cannot collect multiple levels of `pch-ip-active` metrics at the same time on Intel platforms code named Skylake and Kaby Lake. The special handling required to support simultaneous collection of multiple groups of PCH IP active metrics on Intel PCH code named Sunrise Point and Kaby Lake Point, has been discontinued. To keep tool collection overhead from interfering with low power states on platforms with these PCH, only one group of PCH active metrics can be collected at a time.
- Summary report changes.

  - Summary report is overwritten if output file name is not changed from run to run. Previously, new reports would be appended to an existing file.
  - More system information is included in the summary report.
  - GPU device is given as hex value only (not mapped to a name string).
  - All reports that come from OS event trace (ETW) logs have "(OS)" in their title. All other reports are based on data read from hardware sources.
  - Report ordering puts system level metrics at the top to better align with order of metrics viewed when debugging low power blockers.
  - Each metric report now consists of multiple tables because of the framework's generic handling of data types.
  - Collection statistics are now reported with each hardware metric in a report titled Total Samples Received. Previously, these statistics were gathered at the end of the summary file.
- CPU C-state Idle & Wakeup Analysis report changes.
  - This analysis is always generated when `-f os-cpu-cstate` metric is requested, previously `-r detail` was required.
  - The Wakeup summary reports are included in the summary `.csv`, rather than a separate `.txt` file.
  - The additional analysis reports are written in CSV format, previously was simple text.
  - The additional detail file is named <*basename*>`_WakeupAnalysis.csv`, previously was <*basename*>`.txt`.
  - The additional detail reports no longer include the following: Incorrect C-State Used, Histogram of Sleep Duration before Rescheduling, Histogram of Busy Duration Right After Wakeup, Call Stacks at Context Switches, Wakeup Events Summary, Wakeup Events by Previous Idle Duration, Wakeup Events by Busy Duration Right After Wakeups, Deferred Routine of Expired Timer, and Wakeup by Readied Thread.
- Trace (i.e., timeline) files have changed.
  - When writing over time (trace) files, the trace data for all metrics is written to a single file with suffix `_trace.csv`. Previously the trace data was in various files, including the consolidated table of certain metrics in `_hw_timeline.csv`, data from OS events in `_os_timeline.csv` file, and various metric-specific timeline files.
  - The trace data sets for each metric are appended sequentially, one after the other.
  - The trace file includes timestamp (column Continuous Time) and a Duration column which is the delta between the timestamps. A value of 0 duration is used to mark occurrences of hibernation.
  - The trace file is intended to be parsed for viewing graphically, and is not easily read by humans due to its length and non-consecutive ordering of tables. Powerhouse Mountain will be adapting to use this file. (Alternatively, use `-r vtune` to generate a file to import to Intel VTune Amplifier for viewing.)
  - Trace data for sata-lpm reports "Undefined" and "Other" rather than actual hex values as it did in v1.19.1.
- `Automation_summary.csv` file has changed.
  - Now contains all metrics collected for each run, rather than a predetermined set.
  - If the list of metrics collected is changed from the prior run, a new set of column headers is written to the file for the new data set. (The tool no longer tries to fix the set of metrics so that the columns for a particular system are constant despite metrics specified.)
  - To generate the automation summary file use `-r auto` rather than `--auto`.
- Command line option changes.
  - Help option `-h` is now dynamic, meaning that it only lists the features that are available for the platform on which it is executed, and the group names will only show those metrics as well. If a platform supports a metric but the metric is disabled by the system's configuration, it will be included in the help's feature list but a warning will be displayed if it is used.
  - New option name for displaying the CPUID, `--print-fms`(was`--cpuid`).
  - The `-r` option for choosing results formatting has different choices: `sum, vtune, int, auto`. Use `vtune` in place of `sww`, `int` in place of `detail`, and `auto` in place of `--auto`.

- The output option can be used to direct the summary results to be printed to the console as well as the summary file, use `-o console`.
- Long name for -z option has changed to --auto-connected-standby (was --cs-auto-enter).
- `--info` option now only reports LPIT table and whether enabled for connected standby (Internal only). All general information has been moved into the summary report so this option is no longer needed.
- Feature name changes:
  - `cpu-cstate`, `cpu-pstate`, `gfx-cstate`, `gfx-pstate` are now group names for collecting both hardware and OS based metrics. You can choose to collect only hardware or only OS data by selecting the individual metric names.
  - Clipping Reason reports have been renamed to Throttling Reasons. These reports are still included when using the new `cpu-pstate` and `gfx-pstate` group names, but they can also be specified individually. The new feature names are `ia-throt-rsn` and `gt-throt-rsn`. A new feature, `ring-throt-rsn`, has been added as well.
  - `sata-lat` is not available. The latency was determined by the tool issuing IO commands and calculating latency in advance of starting a collection for all other metrics, This may not be accurate and could perturb collection results so it has been removed.
  - `acpi-sstate` is the new feature name for collecting only system S states (Sx), which is an OS-based metric.
  - `sstate` is now a group name, which includes both OS (Sx) and hardware (S0ix) states on platforms that support both.
  - `connected-standby` option name must be spelled out, the `cs` abbreviation is no longer supported.
  - `cpu-gpu-concurrency` report includes only hardware-based data. The less accurate report based on OS event trace data has been discontinued.
  - `energy` feature is not supported. The data that had been available for general use, platform power data based on battery discharge event log and battery information is no longer supported. Internal users can request a configuration file to enable reporting of the Package, IA, and GT energy MSRs.
  - `dram-srr` support on Intel platform code named Kaby Lake has been discontinued from the Internal package as it cannot be confirmed to be valid.
- Modified metric names for consistency and distinction regarding use on platforms with Intel Core processors with discrete PCH vs. Intel Atom processors, details in table below.

In v1.19.1	In v2.4	What changed
`-f sstate`	`-f acpi-sstate -f s0i3-sstate`	Use the new individual name `acpi-sstate` if only want OS-based Sx states, or `s0i3-sstate` for hardware-based S0i3 state on platforms that support it. `sstate` is still valid as a group name.
`-f s0ix-dbg`	`-f s0i3-sstate-dbg`	Name adjustment.
`-f cs`	`-f connected-standby`	The cs abbreviation is not supported.
`-f platform-ltr`	`-f pch-platform-ltr`	Name adjustment.
`-f pch-active`	`-f pch-ip-active`	Name adjustment.
`-f pch-active-lvl*`	`-f pch-ip-active --option pch-lvl=[1|2|3a|3b|3c|3d|4|5]`	Different groups of PCH active metrics are now specified using `--option pch-lvl=`<*value*>.

In v1.19.1	In v2.4	What changed
-f pch-active-all	-f pch-ip-active-all	Name adjustment.
-f pmc-power-status	-f pmc-ip-status	Name adjustment.
-f pmc-pg-res	-f pmc-ip-pg-res	Name adjustment.
-f d0i3-res	-f pmc-ip-d0i3- res	Name adjustment.
-f d3- res	-f pmc-ip-d3- res	Name adjustment.
-f d0i3-occ	-f pmc-ip-d0i3-occ	Name adjustment.
-f d3-occ	-f pmc-ip-d3-occ	Name adjustment.
--cpuid	--print-fms	Name adjustment. Print CPUID in family/model/stepping format.
-n < # millisec>	-n < # millisec>	Default changed from 10 ms to 100 ms. Use -n 10 to revert to 1.19.1 sampling interval default.
-o <output file prefix>	-o console | <output file prefix>	Additional argument. Specify console to print summary report to console or give basename to use for the collection.
--cs-auto-enter -z	--auto-connected-standby -z	Long name for the -z option changed.
-r detail	-r int	Adjustment for option name and file name. Write over time (trace) file report to *_trace.csv. All metrics in single file rather than individual files for each metric.
-r sww	-r vtune	Adjustment for option name and file name. Write output to *.pwr file for import to Intel VTune Amplifier.
--auto	-r auto	Changed from its own option name to a result value type. All metrics written to the file rather than selected.
-ecst/-dcst --enable-cs-trace/--disable-cs-trace	--enable-cstrace/--disable-cstrace	Removed short names and modified long name.
-ess/-dss	Not available	Removed support for reporting certain metrics to powercfg SleepStudy. Support is available using an in-box driver.

In v1.19.1	In v2.4	What changed
`--enable-sleepystudy/ --disable-sleepstudy`		
`--info`	Not available for NDA/ External	Only displays LPIT info, all other info is always included in the summary report.

`-f sata-lat`
`-f thread-wait`
`-f syscall`
`-f battery`
`-f cpu-hdc`
`-f energy`
	Not available	These feature metrics are not supported in 2.4.

`-r snap-sum`
`-r hw-only`
`-r tl-compress`
`--query-name`
	Not available	These results post-processing options are not supported in 2.4.

`--log`
`--expert-help`
`--no-html`
`--no-callstack`
`--less-callstack`
`--csb-test`
`--uninst-driver`
`--wkup-filter-*`
`--use-*-timestamp`
`--idle-bucket`
	Not available	These advanced options are not supported in 2.4.

Fixed Issues

Update release v2.4.2 has the fix for the below issues.

- "Delaying collection" message will be displayed on the console when using the delayed start (`-s`) option. Previously, this message was only being displayed if debug messages were requested, and was incorrectly being displayed after "Started data collection" message.

Update release v2.4.1 has the fix for the below issues.

- Removed approximated report from `-f pch-slps0`. The approximated report tried to account for PMC clock throttling by relying on the PCH Active counter. But there are issues with the CNP PCH counter for both SLP-S0 and PCH PMC Active (see Known Issues section), which results in confusing or misleading results in this report, so it was removed.
- PCIe LPM reporting did not include GBE devices. Collecting link state data for GBE devices has been re-enabled.
- Additional PCIe device IDs added for Intel platforms code named Coffee Lake and Ice Lake.
- Improved syntax error reporting.

Release v2.4 has the fix for the below issues that were in v1.19.1.

- Improved hibernation support. Previously, some hardware counters used to collect data were not being reset after hibernation. This has been fixed.
- Updated Ice Lake `pch-ip-active*` and `cpu-pkgc-dbg` metrics. Incorporated updated hardware specifications for PCH activity counters and CPU Package C debug counters on Ice Lake PCH.
- Panel Self-refresh does not require explicit use of `-m` option. Panel self-refresh (`-f panel-srr`) data is always sampled now because it only uses hardware status data. Therefore, you do not have to explicitly include the `-m` option for it to work properly.

Acronyms and Terms

10

The following acronyms and terms are used in this document (arranged in alphabetic order):

Acronym/Term	Description
DDR	Double Data Rate
LPM	Link Power Management states
LPSS	Low Power SubSystem
LTR	Latency Tolerance Reporting
PCD	Platform Controller Die
PCH	Platform Controller Hub
PCIe	PCI Express
SATA	Serial Advanced Technology Attachment
Intel® PMT	Intel® Platform Monitoring Technology
PSR	Panel Self Refresh
SoC	System on Chip
TCSS	TypeC Subsystem
XHCI	eXtensible Host Controller Interfaces