

## **CS2323: Computer Architecture, Autumn 2023**

### **Homework-3: Processor Design**

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1. A six-stage pipelined processor has delays of 130, 125, 110, 132, 135, and 145 picoseconds for each pipeline stage. The registers used between pipeline stages have a delay of 12 picoseconds each. [3 + 2 marks]
  - a. Find the total time to execute 1000 independent instructions on this pipelined processor, assuming there are no pipeline stalls/hazards.
  - b. Find the total time to execute 1000 independent instructions on this pipelined processor, assuming that 20% of instructions incur a 1-cycle stall.
  
2. Consider a 5-stage pipelined processor P1 with a total latency of 800 ps, equally divided between the pipeline stages. P2 is an improved version of P1, which improves the ALU by supporting MULT instruction. Including the MULT instruction increases the ALU latency by 250 ps, with the latency of other stages being unchanged. Presence of MULT instruction also reduces the total number of instructions by 10% (as we can directly use MULT instead of realizing it through repeated ADD). Answer the following: [2 + 2 + 1 marks]
  - a. What is the minimum required clock period for processors P1 and P2?
  - b. Which processor (P1 or P2) would execute a given code in a smaller time?
  - c. If a piece of code has 5000 instructions on P1, find the total execution time of this code on P1 and P2.
  
3. Consider the code given below:  
    add x14, x12, x11  
    add x15, x14, x12  
    ld x13, 8(x13)  
    ld x12, 0(x14)  
    and x13, x15, x13  
    ld x11, 4(x13)  
    sd x13, 0(x15)
  - a. Insert NOPs for correct execution (assuming no forwarding or hazard detection is implemented). [3 marks]
  - b. Insert NOPs for correct execution (assuming data forwarding without hazard detection is implemented). [2 marks]

#### **Submission instructions:**

1. The assignment is to be done separately by each student.
2. Create a pdf file mentioning the reasoning/observations for the questions asked above.
3. The pdf file should be named YOUR\_ROLLNUM.pdf (e.g., CSYYBTECHXXXXX.pdf)
4. Deadline: 1-Nov-2023, 11.59 pm