Computer Architecture - CS2323

Homework-4

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1.

L1 - 8, 8

Program-1

Varying lines:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
1	0	2	0.7424	49	17	6500
2	0	2	0.7424	49	17	6500
3	0	2	0.7424	49	17	6500

Varying blocks:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	3	0.8636	57	9	6500
3	0	4	0.9242	61	5	6500
3	0	5	0.9545	63	3	6500

Varying ways:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	2	0.7424	49	17	6500
3	1	2	0.7424	49	17	6500

Program-2

Varying lines:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
1	0	2	0.0303	2	64	6500
2	0	2	0.0303	2	64	6500
3	0	2	0.04545	3	63	6500

Varying blocks:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	3	0.8636	57	9	6500
3	0	4	0.9242	61	5	6500
3	0	5	0.9545	63	3	6500

Varying ways:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	2	0.04545	3	63	6500
3	1	2	0.7424	49	17	6500

L1: 16, 16

Program 1

Varying lines:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
1	0	2	0.7481	193	65	25700
2	0	2	0.7481	193	65	25700
3	0	2	0.7481	193	65	25700

Varying blocks:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	3	0.8721	225	33	25700
3	0	4	0.9341	241	17	25700
3	0	5	0.9651	249	9	25700

Varying ways:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	2	0.7481	193	65	25700
3	1	2	0.7481	193	65	25700

Program -2

Varying lines:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
1	0	2	0.007752	2	256	25700
2	0	2	0.007752	2	256	25700
3	0	2	0.007752	2	256	25700

Varying blocks:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	3	0.007752	2	256	25700
3	0	4	0.01163	3	256	25700
3	0	5	0.9574	247	11	25700

Varying ways:

LINES	WAYS	BLOCKS	HIT RATE	HITS	MISSES	ACCESSES
3	0	2	0.007752	2	256	25700
3	1	2	0.007752	2	256	25700

2.

L1-8, 8

For program-1

WRITE-POLICY	WITH ALLOCATE	HIT RATE	HITS	MISSES	ACCESSES
Write-back	Yes	0.7424	49	17	6500
Write-through	Yes	0.7424	49	17	6500
Write-back	No	0.04545	3	63	6500
Write-through	No	0.04545	3	63	6500

For program-2

WRITE-POLICY	WITH ALLOCATE	HIT RATE	HITS	MISSES	ACCESSES
Write-back	Yes	0.7424	49	17	6500
Write-through	Yes	0.7424	49	17	6500
Write-back	No	0.04545	3	63	6500
Write-through	No	0.04545	3	63	6500

L1-16, 16

For program-1

WRITE-POLICY	WITH ALLOCATE	HIT RATE	HITS	MISSES	ACCESSES
Write-back	Yes	0.7481	193	65	25700
Write-through	Yes	0.7481	193	65	25700
Write-back	No	0.01163	3	255	25700
Write-through	No	0.01163	3	255	25700

For program-2

WRITE-POLICY	WITH ALLOCATE	HIT RATE	HITS	MISSES	ACCESSES
Write-back	Yes	0.01163	3	255	25700
Write-through	Yes	0.01163	3	255	25700
Write-back	No	0.01163	3	255	25700
Write-through	No	0.01163	3	255	25700

3.

L1 - 8, 8

ASSOCIATIVITY	HIT RATE	HITS	MISSES	ACCESSES
Direct mapped	0.01538	2	128	12900
2-Way set associative	0.7385	96	34	12900
Fully associative	0.7385	96	34	12900

L1 - 16, 16

ASSOCIATIVITY	HIT RATE	HITS	MISSES	ACCESSES
Direct mapped	0.006809	35	479	51300
2-Way set associative	0.7471	384	130	12900
Fully associative	0.7471	384	130	12900

Observations:

- Upon increasing the Lines in the cache configuration, it is observed that there is no significant change in the hit rate for Program-1 unlike Program-2.

In general, increasing the block size can improve the chances of cache hit and the number of hits, especially when there is spatial locality in the data. However, this advantage comes with the drawback of increased cache pollution and miss penalty due to larger block sizes which decreases the hits.

In the case of Program-1, the trade-off between these factors appears to have a neutral effect on the overall hit rate. The increase in block size has not significantly impacted the hit rate, suggesting that the trade-off might have balanced out.

In case of Program-2, there is a positive effect on the hit rate, and the number of hits has increased. This could be attributed to the presence of more spatial locality, overcoming the potential disadvantage of increased miss penalty.

- Upon increasing the Blocks in the cache configuration, it is observed that there is an increase in the hit rate.

In the both the Programs, increasing the number of blocks allows the cache to fetch more data or number of blocks at a time. This has a positive impact on the chances of a cache hit since a larger portion of the data is available in the cache, potentially reducing cache misses.

- Direct-Mapped Cache:
Direct-mapped caches may experience a reduction in hit rate due to conflicts, where multiple memory blocks map to the same cache set, potentially leading to more frequent cache misses.

Set-Associative Cache:
Set-associative caches offer greater flexibility, mitigating conflicts and often resulting in higher hit rates compared to direct-mapped caches.

Fully-Associative Cache:
Fully-associative caches offer maximal flexibility by allowing any memory block to be placed in any cache line. This freedom in block placement minimises conflicts, enabling higher hit rates compared to set-associative caches.

But there is no much increase from Set-Associative Cache to Fully-Associative Cache suggesting that the workload may not benefit significantly from the additional flexibility provided by a fully associative cache in these programs.

- Upon changing from L1: .dword 8, 8 to L1: .dword 16, 16 there is an increase in hit rate for Program -1and decrease for Program-2 and increase in total accesses for both the programs

In case of Program-1, there is an increase due to better alignment of memory accesses with cache lines, potentially improving spatial locality and reducing cache conflicts which may not be the case with program-2, in turn decreasing the hit rates

In case of both the programs, the loop present in the code runs more times due to the larger data size, leading to an increase in the total accesses.