

# Mobile Charger Lab Report

## EE3900: Linear Systems and Signal Processing

### Indian Institute of Technology Hyderabad

Velma Dhatri Reddy  
AI21BTECH11030

3 Nov 2022

#### 1. AIM

The aim is to make a mobile charger. The circuit must output 5 V DC to charge a mobile phone after taking 230 V AC as input.

#### 2. MATERIALS REQUIRED

- Breadboard
- Printed circuit board
- 12-0-12 Transformer
- 4 diodes
- $100 \mu\text{F}$  Capacitor
- 7805 Regulator
- Soldering iron
- Few electric wires
- Multimeter
- Cathode-ray oscilloscope
- USB cable
- Mobile phone

#### 3. CIRCUIT DIAGRAM

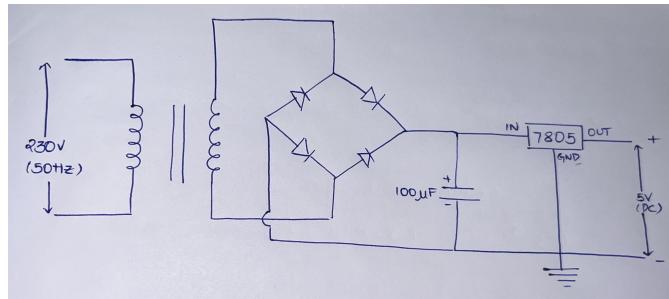


Fig. 3.1. Schematic diagram of the circuit

#### 4. CIRCUIT EXPLANATION

- 230 V AC main supply is step down by the transformer to 12 V AC. The peak voltage will thus be  $12\sqrt{2} \approx 20$  V (as these are RMS voltages). The transformed voltage is

$$v(t) = 12\sqrt{2} \sin(100\pi t + \phi) \text{ V} \quad (4.1)$$

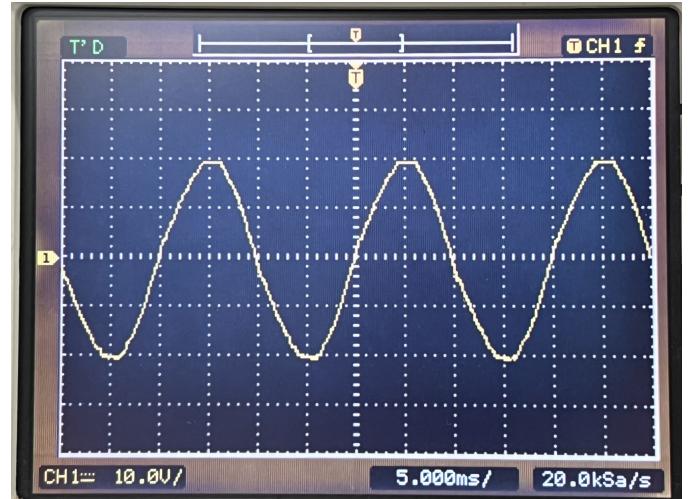


Fig. 4.1. Output AC waveform at transformer stage across  $T_1 T_0$  (18 V peak).

- The alternating current passes through a rectifier. The output is a DC wave whose peak is  $12\sqrt{2}$  V. The voltage at this stage is

$$v(t) = 12\sqrt{2} |\sin(100\pi t + \phi)| \text{ V} \quad (4.2)$$

- Here a capacitor is used as a low-pass filter to filter only the zero frequency component thereby converting the current into pure DC of  $12\sqrt{2}$  V

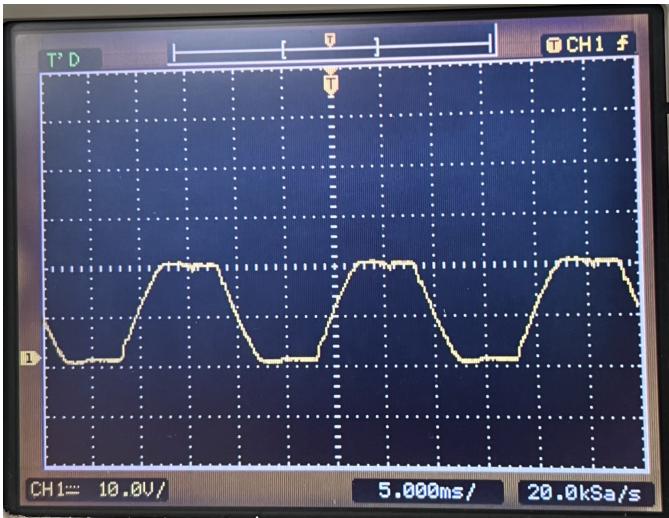


Fig. 4.2. Output half-wave rectified waveform across diode across AQ (18 V peak).

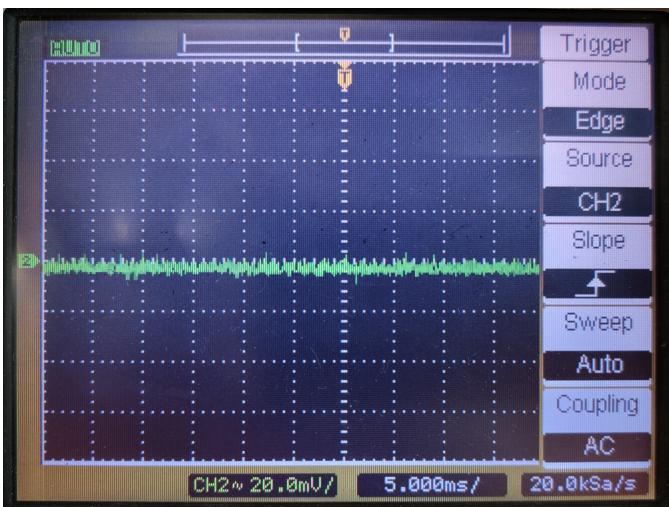


Fig. 4.3. Output AC ripple at regulator stage across OG (5 mV).

$$v(t) = 12\sqrt{2} \text{ V} \quad (4.3)$$

- The 7805 regulator is used to eliminate noise and stabilize the output and to convert it into 5 V DC which is used to charge the mobile

$$v(t) = 5 \text{ V} \quad (4.4)$$

## 5. OBSERVATIONS

We can verify that the output is 5 V DC using a multimeter and by using a cathode-ray oscilloscope (CRO) which shows a constant 5 V voltage. The CRO can be used to see the waveforms at various other stages in the circuit too.

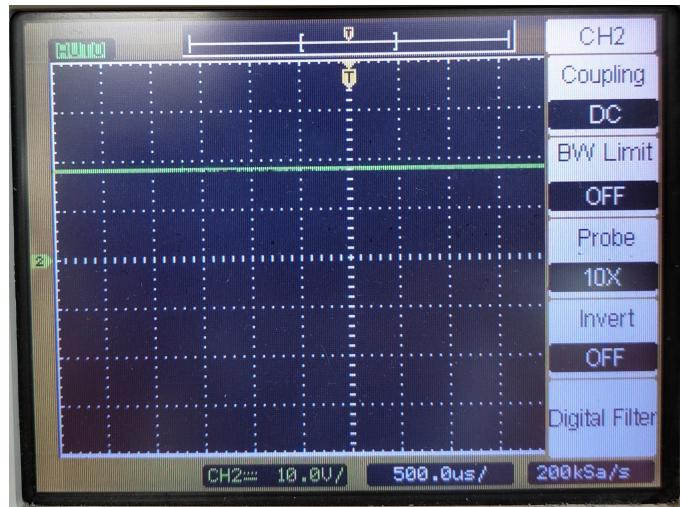


Fig. 4.4. Output DC waveform at filter stage across IS (18 V).

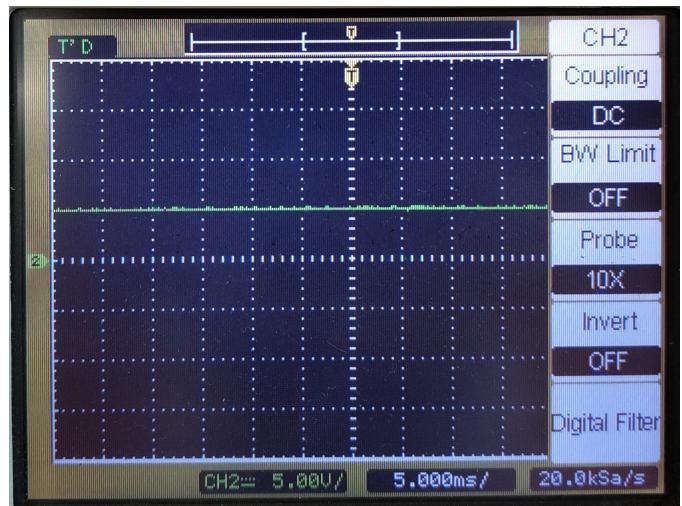


Fig. 4.5. Output DC waveform at regulator stage across OG (5 V).