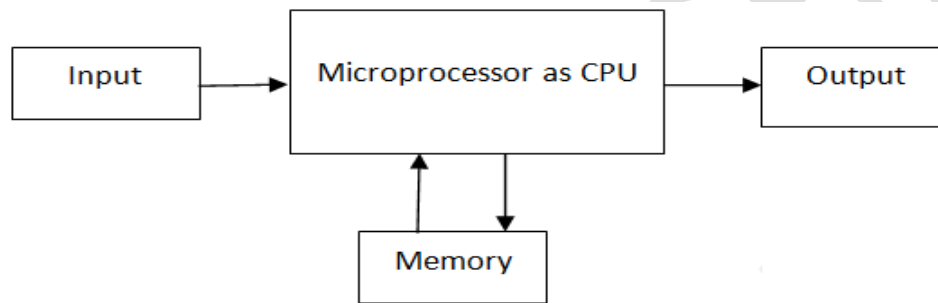


## Unit: II 8085 Microprocessor

### 2.1 Introduction:

- ✓ The 8085 microprocessor is an 8-bit microprocessor that was introduced by Intel Corporation in the year 1976.
- ✓ The 8085 microprocessor is designed to execute a set of instructions to perform various tasks in a computer system.
- ✓ The 8085 microprocessor operates at a clock speed of 3 MHz which is known as frequency.
- ✓ The frequency is inversely proportional to time, so time to execute one operation  $T = 1/3\text{MHz} = 1/(3 \times 10^6) = 0.33 \times 10^{-6} = 0.33 \text{ micro second}$ .
- ✓ To understand the basic concepts microprocessor device, it is easier to learn from a simple 8-bit processor than from a 64-bit processor.
- ✓ Following diagram shows microprocessor as CPU. A computer with a microprocessor is known as microcomputer.



**System bus:** The system bus is a communication path between the microprocessor and peripheral. There are three types of system bus in 8085 microprocessor: Address Bus, Data Bus and Control Bus.

**Address Bus:** It is a unidirectional bus which carries address of memory or I/O devices from where data is to be read or write according to control signal provided by microprocessor. Size of address bus is 16-bits. So, addressable memory of 8085 is 64 Kbytes ( $2^{16} = 2^6 \times 2^{10} = 64 \times 1024 = 64\text{K}$ ).

**Data Bus:** It is a bi-directional bus which is used to transfer 8-bit data between the microprocessor and memory or IO devices. The flow of data is depends on control signal.

**Control Bus:** It consists of various single lines carry synchronization signals between the microprocessor and memory or IO device. There are four lines which are used to generate memory read, memory write, I/O read, I/O write signals using control bus.

To communicate with a memory or I/O device, the microprocessor needs to perform the following steps:

Step 1: Identify the memory location or peripheral device (Using Address Bus)

Step 2: Provide timing and synchronization signals. (Using Control Bus)

Step 3: Transfer binary information to or from memory or peripheral device. (Using Data Bus)

### 2.2 8085 Pin Diagram & Pin Functions

- ✓ Fig (a) and (b) shows 8085 Pin Diagram and functional (Logical) pin diagram of 8085 microprocessor respectively.
- ✓ The signals of 8085 Pin Diagram can be classified into six groups according to their functions.
  - ✓ Address bus
  - ✓ Multiplexed Address/Data bus
  - ✓ Control and status signal
  - ✓ Power supply and frequency signals.

- ✓ Externally Initiated signals
- ✓ Serial I/O signals

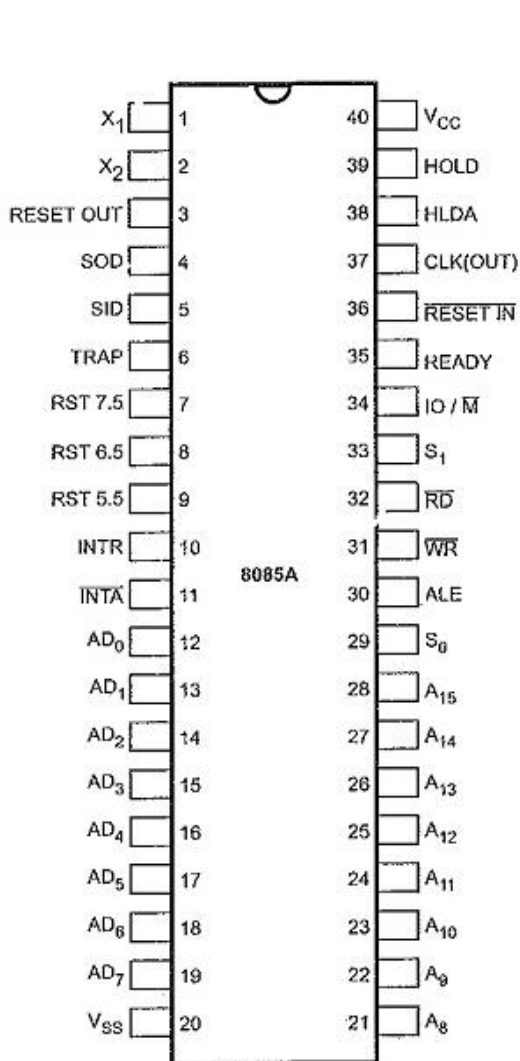


Fig.(a) Pin Diagram of 8085

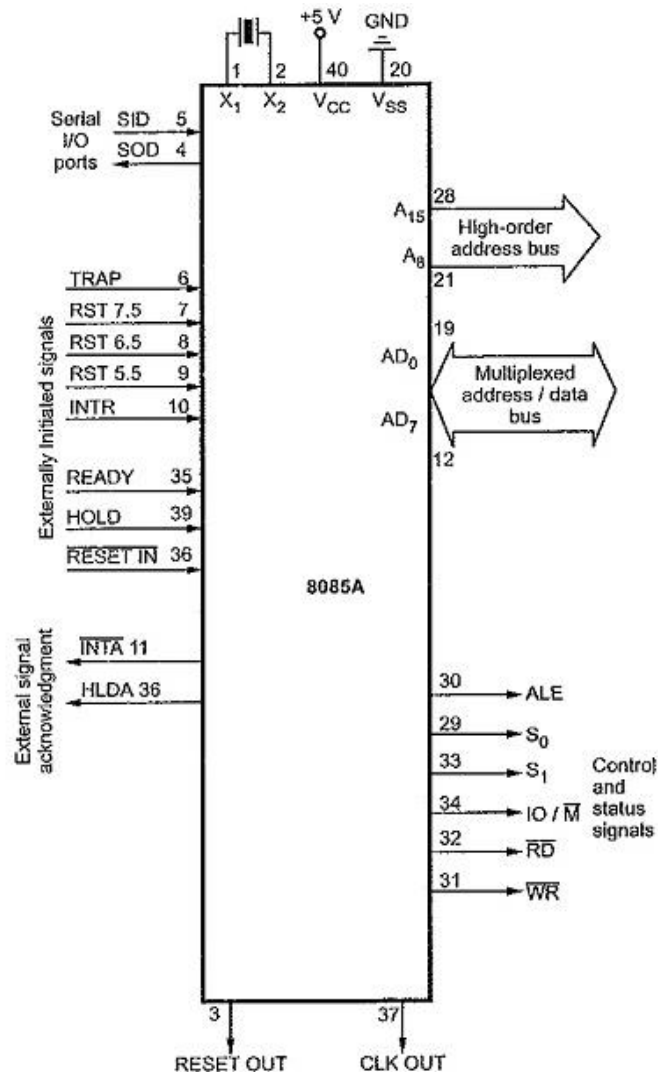


Fig.(b) Logical Pin Diagram of 8085

**Address bus:** This group consists 8-pins (A<sub>15</sub> to A<sub>8</sub>).

- ✓ The 8085 has 16 signal lines (pins) that are used as the address.
- ✓ These lines are split into two groups: A<sub>15</sub> to A<sub>8</sub> and AD<sub>7</sub> to AD<sub>0</sub>.
- ✓ The eight signal lines, A<sub>15</sub> to A<sub>8</sub> are unidirectional and used for the most significant bits, called higher order address bus.
- ✓ The signal lines AD<sub>7</sub> to AD<sub>0</sub>, are used for a dual purpose.

**Data bus / Multiplexed Address:**

- ✓ This group consists 8-pins (AD<sub>7</sub> to AD<sub>0</sub>).
- ✓ The 8085 has 8 data lines (D<sub>7</sub>- D<sub>0</sub>) which represent data and it is multiplexed with lower order address lines (A<sub>7</sub> to A<sub>0</sub>) to reduce the number of pins.
- ✓ These signal lines AD<sub>7</sub> to AD<sub>0</sub> are bidirectional.

**Control and Status signals:**

- ✓ This group consists **2 control signals** ( $\overline{RD}$  and  $\overline{WR}$ ), **3 status signals** ( $\overline{IO/M}$ ,  $S_1$  and  $S_0$ ) to identify the control signals, and **one special signal (ALE)** which is used to demultiplexed address and data bus. These signals are as follows:
- ✓ **Address Latch Enable (ALE) signal:** When signal on ALE pin becomes **high (1)**, then multiplexed address/data bus contains **lower order address** and when it becomes **low (0)** then the bits on  $AD_7$  to  $AD_0$  are considered as data bits. At every machine cycle, Signal on ALE become positive going pulse at first T-state and after that it becomes low.
- ✓ **Read ( $\overline{RD}$ ):** This signal is **enable** when **low (0)**. This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.
- ✓ **Write ( $\overline{WR}$ ):** This signal is **enable** when **low (0)**. This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.
- ✓  **$\overline{IO/M}$ :** This is a status signal used to differentiate between I/O and memory operations. When it is high, it indicates an I/O operation. When it is low, it indicates a memory operation. This signal is combined with  $\overline{RD}$  (Read) and  $\overline{WR}$  (Write) to generate I/O and memory control signals.
- ✓  **$S_1$ , and  $S_0$ :** These status signals can identify various operations like opcode fetch, memory read/write, I/O read, write, Interrupt acknowledgment etc.,

| Status signals    |       |       | Operation                          | Control Signals   |
|-------------------|-------|-------|------------------------------------|---|
| $\overline{IO/M}$ | $S_1$ | $S_0$ |                                    |   |
| 0                 | 0     | 1     | Memory Write ( $\overline{MEMW}$ ) | $\overline{WR} = 0$   |
| 0                 | 1     | 0     | Memory Read ( $\overline{MEMR}$ )  | $\overline{RD} = 0$   |
| 1                 | 0     | 1     | IO Write ( $\overline{IOW}$ )      | $\overline{WR} = 0$   |
| 1                 | 1     | 0     | IO Read ( $\overline{IOR}$ )       | $\overline{RD} = 0$   |
| 0                 | 1     | 1     | Opcode Fetch                       | $\overline{RD} = 0$   |
| 1                 | 1     | 1     | Interrupt Acknowledge              | $\overline{INTA} = 0$   |
| Tri-state         | 0     | 0     | Halt                               | $\overline{RD} = \overline{WR} = \text{Tri-state}$<br>$\overline{INTA} = 1$ |
| Tri-state         | X     | X     | Hold                               |   |
| Tri-state         | X     | X     | Reset                              |   |

Table: 8085 machine cycle Status and control signals

**Power supply and frequency signals:**

- ✓ This group consists of 2 power supply signals and 3 clock frequency signals.
- ✓ The 8085 requires only one +5 V power supply which is given by  $V_{cc}$ , (bit 1) and  $V_{ss}$  is connected to ground which represent bit-0.
- ✓ CLK OUT signal is used as a system clock for other devices.
- ✓ A crystal is connected between two pins  $X_1$ , and  $X_2$ , which generate crystal frequency 6 MHz.

**Externally Initiated signals**

- ✓ This group consists **6 interrupt related pins**, **2 pins** are used for **DMA transfer**, **2 pins** are used for **reset purpose** and **1 pin** is used for **synchronization**.
- ✓ There are Five interrupts pins TRAP, RST 7.5, RST 6.5, RST 5.5 and INTR and one Interrupt acknowledge pin ( $\overline{INTA}$ ).

TRAP: It is active high input signal. TRAP is non-maskable, vectored, high-priority interrupt. The request on TRAP pin can never be ignored by microprocessor. The vector address of ISR when

request on TRAP pin receive is 0024h.

RST 7.5, RST 6.5, RST 5.5: They are known as restart interrupts. These are maskable, vectored interrupts. Microprocessor can reject signals on these pins. Priority order of pins is 7.5, 6.5 and 5.5 (from high to low). Whenever any I/O device send request to microprocessor through any of these pins, microprocessor will calculate vector address of ISR using the code ( $7.5 \times 8$  in hex = 3C h). Vector address of RST 7.5, RST 6.5 and RST 5.5 are 003Ch, 0034h, 002Ch respectively.

INTR,INTA: It is a general purpose, maskable and non-vectored interrupt. It has lower priority among all interrupt pins. If interrupt occurs on INTR pin then vector address is to be received from external hardware. The 8085 sends acknowledgment to external hardware using INTA signal.

- ✓ Two pins for **DMA transfer** is **HOLD** and **HLDA**. It is used to transfer the control of system buses to other device like DMA controller. A HOLD input indicates that other device want to use the address and data bus. After receiving HOLD input, the 8085 completes the data transfer on buses, put RD, WR and IO/M in tri-state and acknowledge to peripheral devices through HLDA output that it will leave the control of buses in next clock cycle.
- ✓ The **READY** input signal is used to **synchronize** the operations with the slower peripheral devices. It is used by peripheral devices to inform the microprocessor that it is ready to send or receive data. When it is low, the microprocessor goes into wait state and then waits for response from device. When a device is ready to transfer the data, it sends READY signal high to microprocessor
- ✓ **RESETIN, RESET OUT**: The signal can be used to reset other devices. **RESETIN** is **active low** input signal. When it is low, microprocessor reset itself, the content of program counter is set to zero, and control buses are tri-stated. **RESET OUT** is **active high output** signal. The microprocessor can send the reset signal to other peripheral devices by RESET OUT pin to indicate that is being reset.
- ✓ **Serial I/O signals**: Two signals are used to implement the serial transmission: SID (Serial Input Data) and SOD (Serial Output Data). SID is input signal while SOD is output signal. In serial transmission, data bits are sent over a single line, one bit at a time, such as the transmission over telephone lines, serial printer etc.

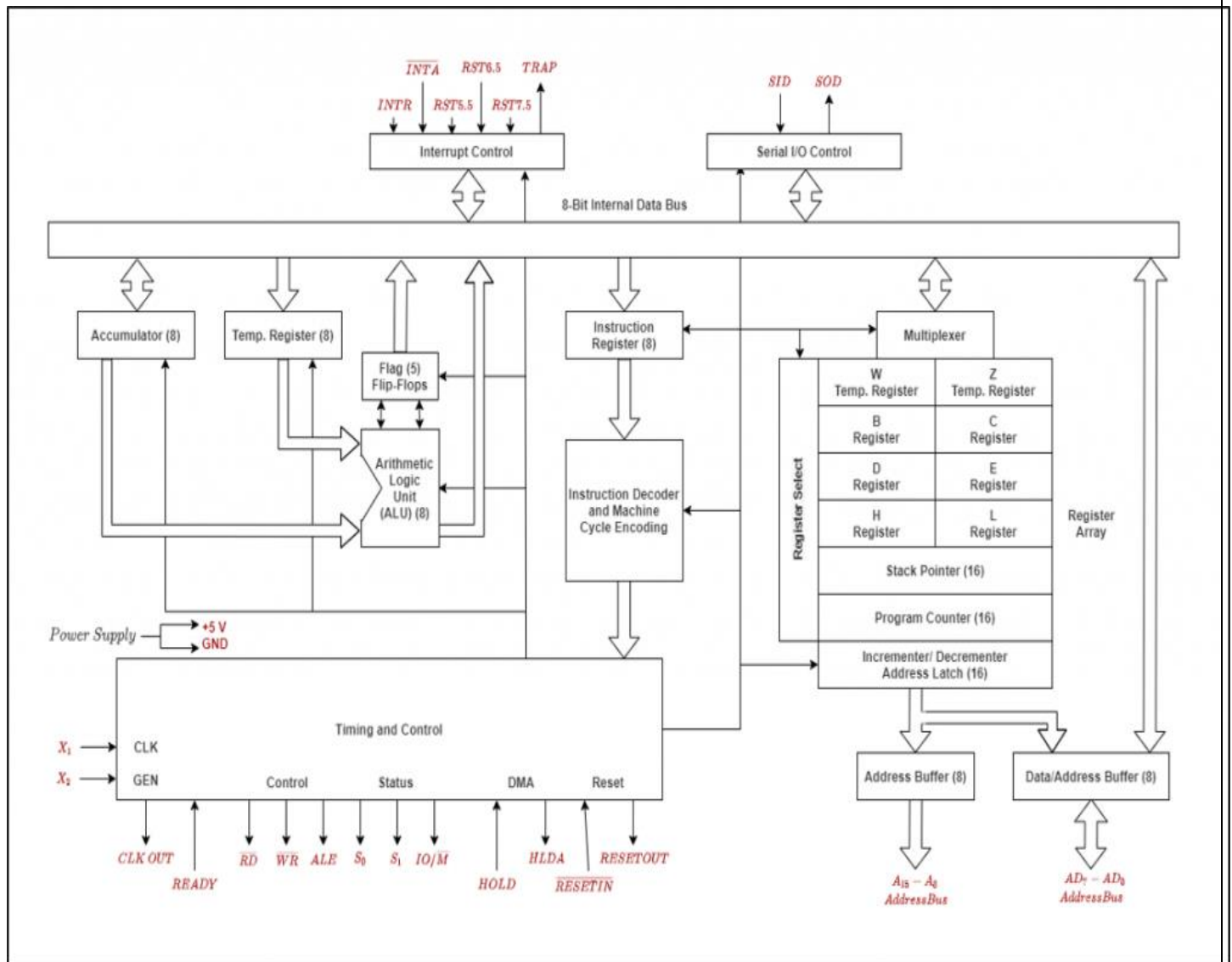
### 2.3 8085 Microprocessor Architecture

- ✓ It consists of various sections like the Arithmetic Logic Unit (ALU), Instruction Register, Instruction Decoder and machine cycle encoding, Timing and Control Unit. Register array, Interrupt control, Serial I/O control, Address Buffer and Address/ Data buffer.
- ✓ These components can transfer data inside the processor through 8-bit internal data bus.

**Arithmetic and Logic Unit (ALU)**: It is used to perform mathematical operations like addition, multiplication, subtraction, division, decrement, increment, etc. Different operations are carried out in ALU: Logical operations, Bit-Shifting Operations, and Arithmetic Operations.

**Instruction register** : It is an 8-bit register that contains the current instruction being executed. The instruction register is used by the microprocessor to decode and execute instructions.

**Instruction Decoder and Machine Cycle Encoding**: The content of instruction register is transferred to the instruction decoder and it is decoded to find the meaning of opcode. After decoding the instruction, Decoder directs the timing and control section to perform the sequence of events in order to complete the execution of current instruction.



### Timing and Control Unit:

Once the instruction decoder decodes the instruction, it sends necessary signals to timing and control section to perform necessary steps for instruction execution. It is responsible to provide various control signals to memory or I/O devices to perform external operation like memory read, memory write, I/O read, I/O write.

### Registers:

The 8085 has 8-bit and 16-bit internal registers which are used for different purpose. These registers are used to store data temporarily during the execution of a program and are accessible to the user through instructions.

- **Accumulator (A):** It is an 8-bit register. For all arithmetic and logic operations, one operand can be considered as Accumulator so it is also known as default register for arithmetic and logic instructions.
- **General-purpose registers:** There are six general-purpose registers. These registers can hold 8-bit values. These 8-bit registers are B, C, D, E, H, L. These registers work as 16-bit registers when they work in pairs like B-C, D-E, and H-L. Here registers W and Z are reserved registers.
- **Program Counter :** It holds the address value of the memory to the next instruction that is to be executed. It is a 16-bit register.
- **Stack Pointer (SP):** It is also a 16-bit register used to store the address of the top of stack.
- **Flag Register:** It is an 8-bit register where each bit register specifies one flag. The flag is 1-bit data and can be set/ reset based on arithmetic and logic operations and it can be used by Jump and CALL



instructions. There are Five flags used by 8085 microprocessor, Sign flag (S), Zero flag (Z), Auxiliary carry flag (AC), Parity flag (P), and Carry flag (CY).

**Interrupt control:** Whenever a microprocessor is executing the main program and if suddenly an interrupt occurs, the microprocessor shifts the control from the main program to process the incoming request. After the request is completed, the control goes back to the main program. There are 5 interrupt signals in 8085 microprocessors: INTR, TRAP, RST 7.5, RST 6.5, and RST 5.5.

**Priorities of Interrupts:** TRAP > RST 7.5 > RST 6.5 > RST 5.5 > INTR

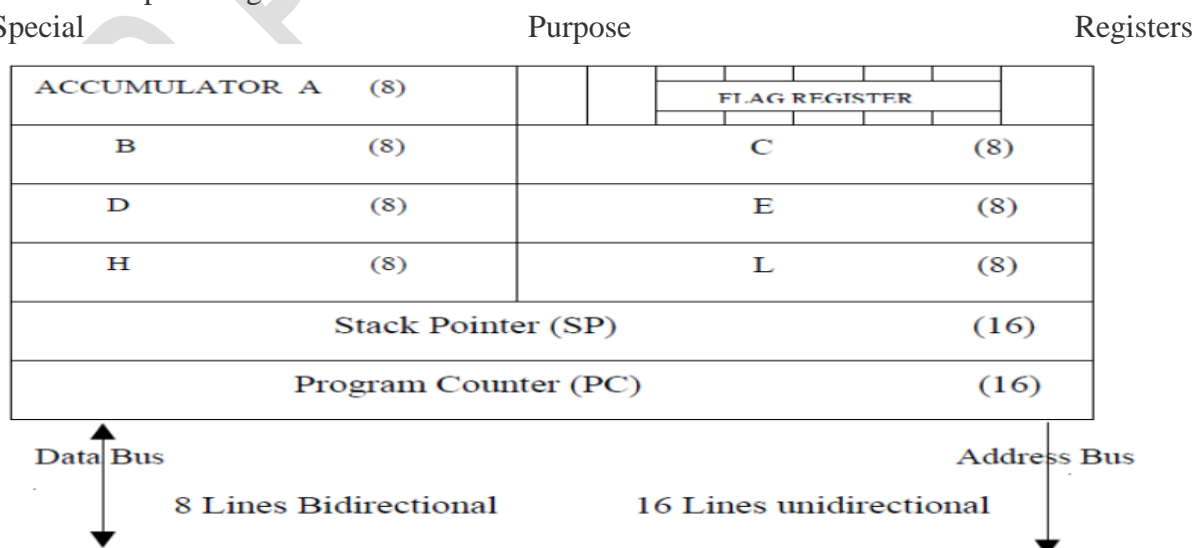
**Serial Input/output control:** It controls the serial data communication by using Serial input data and Serial output data. The 8085 has a serial I/O port (SID/SOD) for serial communication. Serial Input/output control in the 8085 microprocessor refers to the communication of data between the microprocessor and external devices in a serial manner.

**Address Buffer and Address/ Data buffer:** The contents of the stack pointer and program counter are loaded into the address buffer and address-data buffer. These buffers are then used to drive the external address bus and address-data bus. As the memory and I/O chips are connected to these buses, the CPU can exchange desired data to the memory and I/O chips. The address-data buffer is not only connected to the external data bus but also to the internal data bus which consists of 8-bits. The address data buffer can both send and receive data from internal data bus.

**Address bus and data bus:** The data bus is bidirectional and carries the data which is to be stored. The address bus is unidirectional and carries the location where data is to be stored. In the 8085 microprocessor, the address bus and data bus are two separate buses that are used for communication between the microprocessor and external devices.

## 2.4 Register Organization of 8085

- ✓ Registers are used by the microprocessor for temporary storage and manipulation of data and instructions.
- ✓ Total number of registers available is depending on the microprocessor.
- ✓ The 8085 has 8-bit and 16-bit registers used for storing data temporarily in program execution.
- ✓ Registers in 8085 can be classified in two categories:
  - General Purpose Registers
  - Special



**Register Organization of 8085**

**General purpose registers:**

- ✓ The 8085 has six general-purpose registers to store 8-bit data.

- ✓ These are identified as B, C, D, E, H, and L.
- ✓ These can be combined as register pairs BC, DE, and HL, to perform some 16-bit operation or store 16-bit data.
- ✓ These registers are used to store or copy temporary data during the execution of the program.
- ✓ When they are used as register pair in an instruction, then left register is used to store most significant byte (MSB) and right register is used to store least significant byte (LSB).
- ✓ Example, in DE register pair, the content of the D register is treated as the MSB, and the content of E register is treated as the LSB.
- ✓ For example, LXI H, 2030h instruction stores 20h into register H and 30h into register L.
- ✓ Generally Register C is used as counter register to iterate the loop in looping program.
- ✓ All general purpose register are used as second operands in arithmetic and logical instructions.

**Special purpose registers:**

- ✓ The special purpose register is used for specific purpose and can only be used by microprocessor.
- ✓ Special purpose register are: **Accumulator, Program Counter, Stack Pointer and Flag Register.**

**Accumulator (A):** Register accumulator is denoted by alphabet A.

- Register A is an 8-bit register used in 8085 to perform arithmetic, logical, I/O & LOAD/STORE operations.
- After performing arithmetical or logical operations, the result is stored in accumulator.
- In arithmetic and logic operations, one operand is compulsory stored in register A So it is also called as default register.

**Program Counter (PC):** It is a 16-bit register used by microprocessor to store address of next instruction fetch from memory.

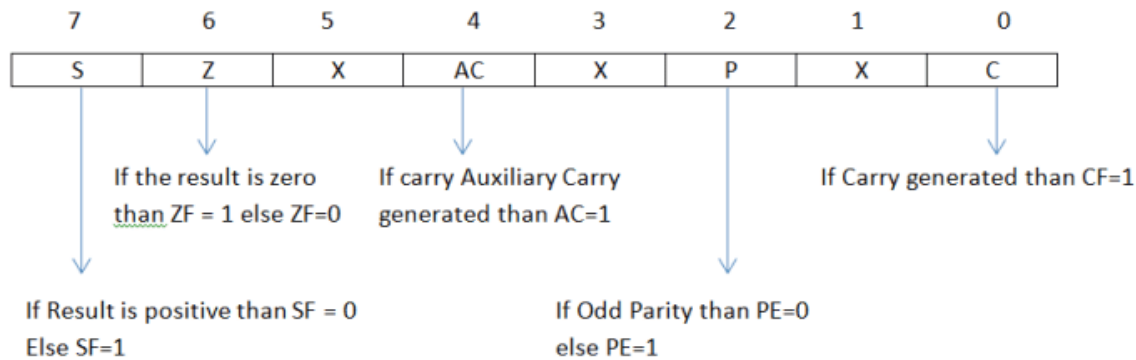
- Program is a sequence of instructions. While executing the program, microprocessor fetches the current instruction from the memory whose address is stored in PC and executes it.
- After fetching the instruction, content of PC is auto-increment by one, two or three depends on the size of instruction,
- For one-byte instruction it increments program counter by one, for two-byte instruction it increments program counter by two and for three-byte instruction it increments program counter by three.
- In case of JUMP and CALL instructions, address followed by JUMP and CALL instructions is placed in the program counter.

**Stack Pointer (SP):** The stack pointer is a 16-bit register used as a memory pointer.

- It points to a memory location in R/W memory, called the stack.
- A stack is a portion of RAM.
- Stack is temporary storage used by microprocessor to store return address while jump to the service routine/ stored procedure.

**Flag Register:**

- The flag register is a special purpose register and it is different from other registers in Microprocessor.
- It consists of 8 bits and only 5 of them are useful.
- The other three are left vacant and are used in the future Intel versions.



- **Sign flag(SF):** The sign flag indicates whether result generated is positive or negative. The sign flag is set to 1 whenever the result generated is negative. If the sign flag is set to 0 than the result generated is positive.
- **Zero Flag(ZF):** The zero flag indicates the result generated is zero or non-zero. If the result generated is zero than the Zero Flag is set to 1. If the result is non-zero than the ZF=0.
- **Auxiliary Carry Flag (AC):** The Auxiliary Carry flag is set to 1 whenever there is a carry or borrow at nibble in the data. If the carry generated from 4th bit to 5th bit or borrow is taken from 5th bit to 4th bit than the Auxiliary Carry Flag is set to 1.
- **Parity Flag(PF):** The Parity Flag is set to 1 when even parity of 1s into the result. The Parity Flag is reset to 0 when odd parity of 1s into the result.
  - If the number of 1s into the result is ODD than the parity flag is reset to 0.
  - If the number of 1s into the result is EVEN than the parity flag is set to 1.
- **Carry Flag(CF):** The Carry flag is set to 1 whenever there is a carry from MSB or borrow to MSB.

Example:

## 2.5 8085 Instruction Execution

- ✓ The programming used in 8085 microprocessor is known as assembly language programming.
- ✓ An assembly language is a type of low-level programming language that is used to communicate directly with a computer hardware.
- ✓ Assembly language program is converted into machine code by using assembler.
- ✓ Assembly language program is written using various instructions.
  - **Instruction:** An instruction of a microprocessor is a command given to the microprocessor to perform a specified operation on given data. Each instruction contains two part: Opcode and Operands.
  - **Opcode:** Opcode specifies which operation is to be performed by an instruction. It is also known as mnemonics code.
  - **Operands:** It specifies the data in instruction on which operation is to be performed
- ✓ **Instruction Cycle:**
  - The execution of each instruction involves a series of steps known as the instruction cycle.
  - It is the time taken by the processor to complete the execution of an instruction.
  - An instruction cycle consists of one to six machine cycles.
- ✓ **Machine Cycle:**



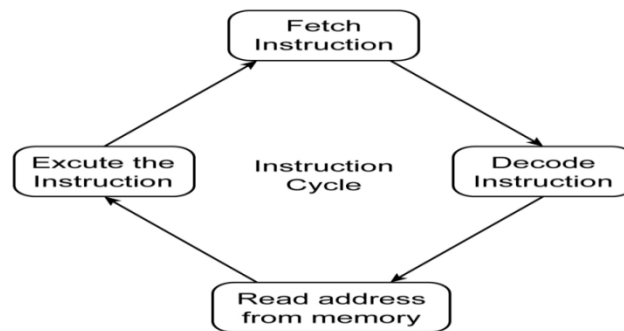
- In every instruction execution, there are some operations to be performed sequentially to complete instruction cycle.
- Such operations are represented by machine cycle.
- Examples are opcode fetch, memory read, memory write, I/O read, I/O write.
- Machine cycle consists of three to six T-states.
- Time required to complete one operation is known as machine cycle.

✓ **T-state:**

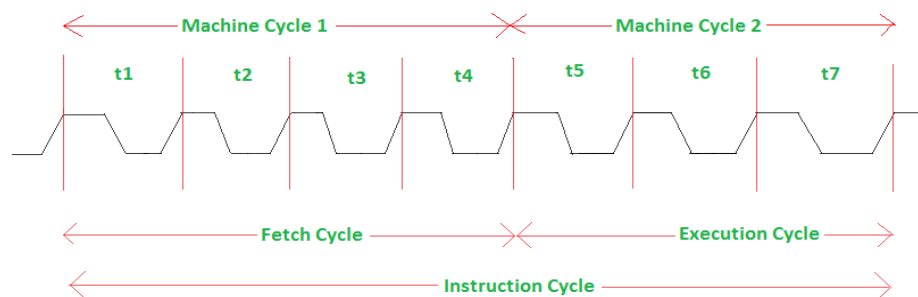
- Each operation is performed in synchronization with the internal clock.
- One clock pulse is called a T-state.
- The timing diagram is a graphical representation of the process in steps with respect to time.

✓ **Execution steps of Instruction cycle**

- **Fetch cycle:** It is used to fetch the next instruction opcode from the memory location whose address is stored in program counter (PC) and then stored in the instruction register.
- **Decode instruction:** Instruction Decoder section interprets the encoded instruction from instruction register.
- **Find effective address:** The address given in instruction is read from main memory and required data is fetched. The effective address depends on direct addressing mode or indirect addressing mode.
- **Execution cycle:** The microprocessor performs the operation specified by the opcode in instruction onto operands. It consists Memory read (MEMR), Memory write (MEMW), I/O read (IOR) and I/O write (IOW).



- ✓ Following Fig. shows the Instruction cycle and machine cycle. The fetch cycle takes 4 T-states and the execution cycle takes 3 T-states.

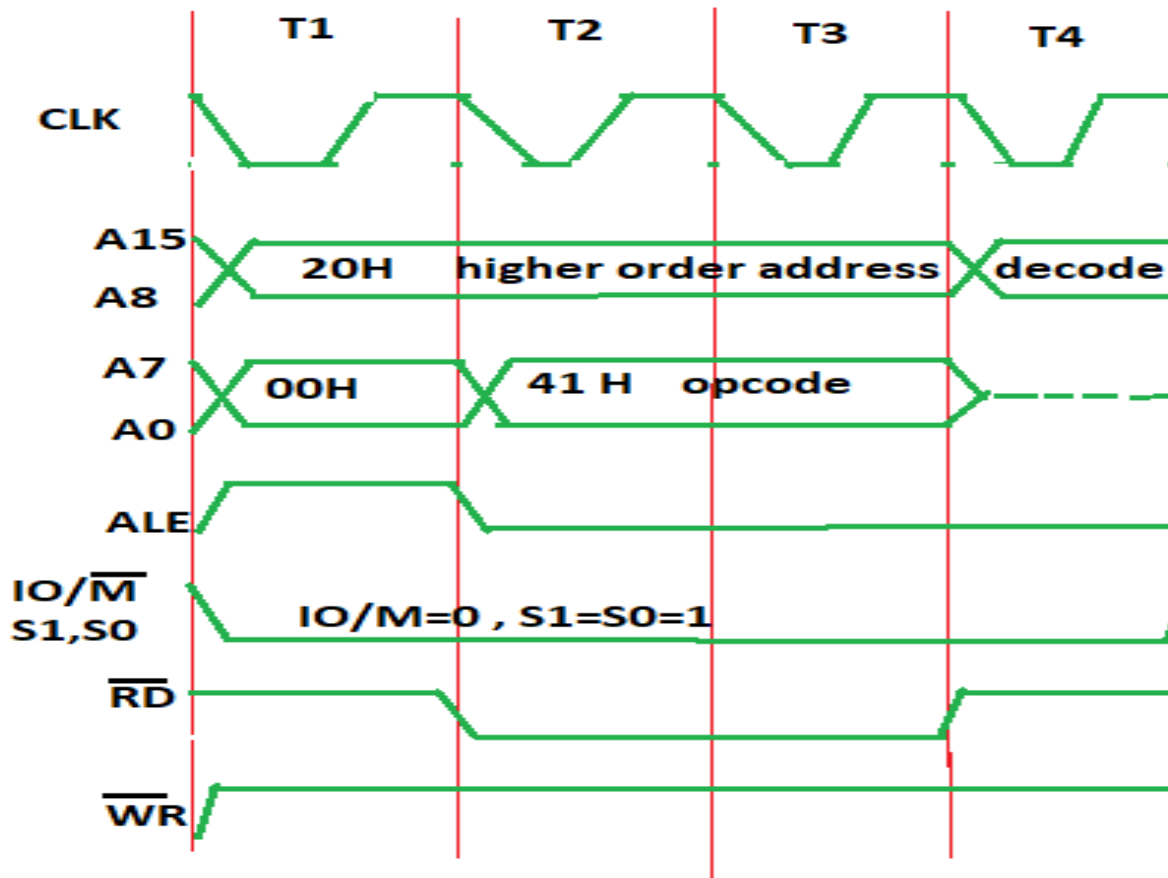


Instruction cycle in 8085 microprocessor

Example: Timing diagram of MOV Instruction in Microprocessor: MOV B, C

Here, MOV B, C so Opcode: MOV , Operand: B and C

- Only opcode fetching is required for this instruction .
- We need 4 T states for the timing diagram.
- The content of Program Counter which is 2000 h is placed on the address bus.
- At T<sub>1</sub>, the higher order address 20h is placed at A15 – A8.
- The lower order address 00h is placed at A7- A0, and ALE is active high.
- For the opcode fetch the IO/M (low active) = 0, S1 = 1 and S0 = 1.



- 00 – lower bit of address where the opcode is stored, i.e., 00.
- 20 – higher bit of address where the opcode is stored, i.e., 20.
- ALE – provides signal for multiplexed address and data bus. Only in t1, it is used as an address bus to fetch a lower bit of address
- RD (low active) – signal is 1 in t1 & t4 as no data is read by the microprocessor. Signal is 0 in t2 & t3 because here the data is read by a microprocessor.
- WR (low active) – signal is 1, no data is written by a microprocessor.
- IO/M (low active) – signal is 1 because the operation is performing on memory.
- S0 and S1 – both are 1 in case of opcode fetching.