Clock Implementation on Vaman FPGA using K-Maps and Multiplexing

Dhawal Saini

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Electrical Department
Indian Institute Of Technology, Hyderabad

Outline

Introduction

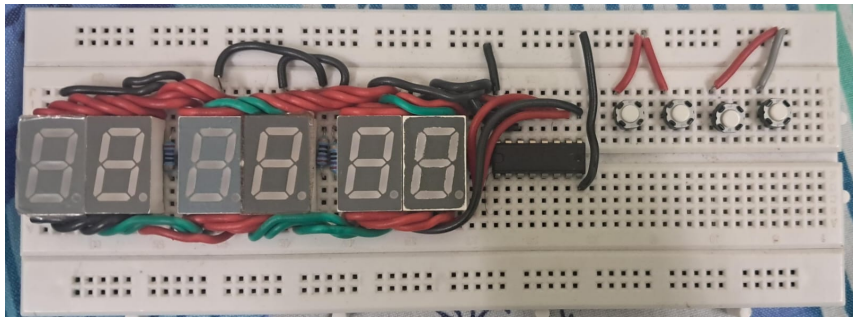
- Digital clock system implemented on Vaman FPGA
- Key features:
  - Uses Karnaugh maps (K-Maps) for time increment logic
  - Implements display multiplexing
  - Single BCD drives six 7-segment displays
- Implemented in Verilog HDL

Components

Component	Quantity
Vaman FPGA Board	1
7-Segment Displays	6
Push Buttons	4
IC 7447	1
Jumper Wires	30
Breadboards	2

Vaman Connections

- Button 1: PYGMY 1 (Pause/Play)
- Buttons 2-4: PYGMY 2-4 (Time Set)
- IC 7447 Inputs: PYGMY 5-8
- Display Control: PYGMY 9-14



Execution Steps

1. Clone repository:

```
git clone https://github.com/ysiddhanth/vaman.git
cd vaman/Clock/codes
```

2. Generate .bin file:

```
ql_symbiflow -compile -src . -d ql-eos-s3 -P pu64 -t
main -v main.v -p quickfeather.pcf
```

3. Program FPGA:

```
sudo python3 tinyfpgab --port /dev/ttyACM0 --appfpga main.bin
--mode fpga --reset
```

Increment Logic

Seconds Unit:

$$A_1 = \overline{W_1}$$
$$B_1 = (W_1 \wedge \overline{X_1}) \vee (\overline{W_1} \wedge X_1)$$

Seconds Tens:

$$A_2 = \overline{W_2}$$
$$B_2 = (\overline{Y_2} \wedge W_2) \vee (\overline{W_2} \wedge X_2)$$

Summary

- Successfully implemented digital clock on FPGA
- Key achievements:
  - Efficient K-Map based logic
  - Optimized display multiplexing
  - Flexible control interface
- Future enhancements:
  - Add date display functionality
  - Implement alarm features
  - Optimize power consumption