BOOTH MULTIPLIER:

(i) Power Utilization Report:

| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov 6 21:40:23 MST 2019
| Date : Mon Apr 22 14:31:26 2024
| Host : DHEEKSHITHA running 64-bit major release (build 9200)
| Command : report_power -file booth_multiplier_power_routed.rpt -pb booth_multiplier_power_summary_routed.pb -rpx booth_multiplier_power_routed.rpx
| Design : booth_multiplier
| Device : xc7a35tcpg236-1
| Design State : routed
| Grade : commercial
| Process : typical
| Characterization : Production

Power Report

Table of Contents
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1. Summary

Total On-Chip Power (W)	43.564 (Junction temp exceeded!)
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	43.078

Device Static (W)	0.486
Effective TJA (C/W)	5.0
Max Ambient (C)	0.0
Junction Temperature (C)	125.0
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA
+--------------------------+---------------------------------+
* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

+----------------+-----------+----------+-----------+-----------------+
| On-Chip | Power (W) | Used | Available | Utilization (%) |
+----------------+-----------+----------+-----------+-----------------+
Slice Logic	1.872	140	---	---
LUT as Logic	1.872	128	20800	0.62
Signals	2.096	156	---	---
I/O	39.110	32	106	30.19
Static Power	0.486			
Total	43.564			
+----------------+-----------+----------+-----------+-----------------+

1.2 Power Supply Summary

+-----------+-------------+-----------+-------------+------------+
| Source | Voltage (V) | Total (A) | Dynamic (A) | Static (A) |
+-----------+-------------+-----------+-------------+------------+
Vccint	1.000	4.373	4.032	0.341
Vccaux	1.800	1.484	1.431	0.053
Vcco33	3.300	11.053	11.052	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.000	0.000	0.000
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.010	0.000	0.010

MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.020	0.000	0.020
+----------+----------+----------+----------+----------+

1.3 Confidence Level

+---

| User Input Data | Confidence | Details | Action
|
+---

| Design implementation state | High | Design is routed |
|
| Clock nodes activity | High | User specified more than 95% of clocks |
|
I/O nodes activity	Low	More than 75% of inputs are missing user specification	Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
Device models	High	Device models are Production
Overall confidence level	Low	
+---
---

2. Settings

2.1 Environment

+----------+----------+
| Ambient Temp (C) | 25.0 |
| ThetaJA (C/W) | 5.0 |

Airflow (LFM)	250
Heat Sink	medium (Medium Profile)
ThetaSA (C/W)	4.6
Board Selection	medium (10"x10")
# of Board Layers	12to15 (12 to 15 Layers)
Board Temperature (C)	25.0
+------------------------+---------------------------+

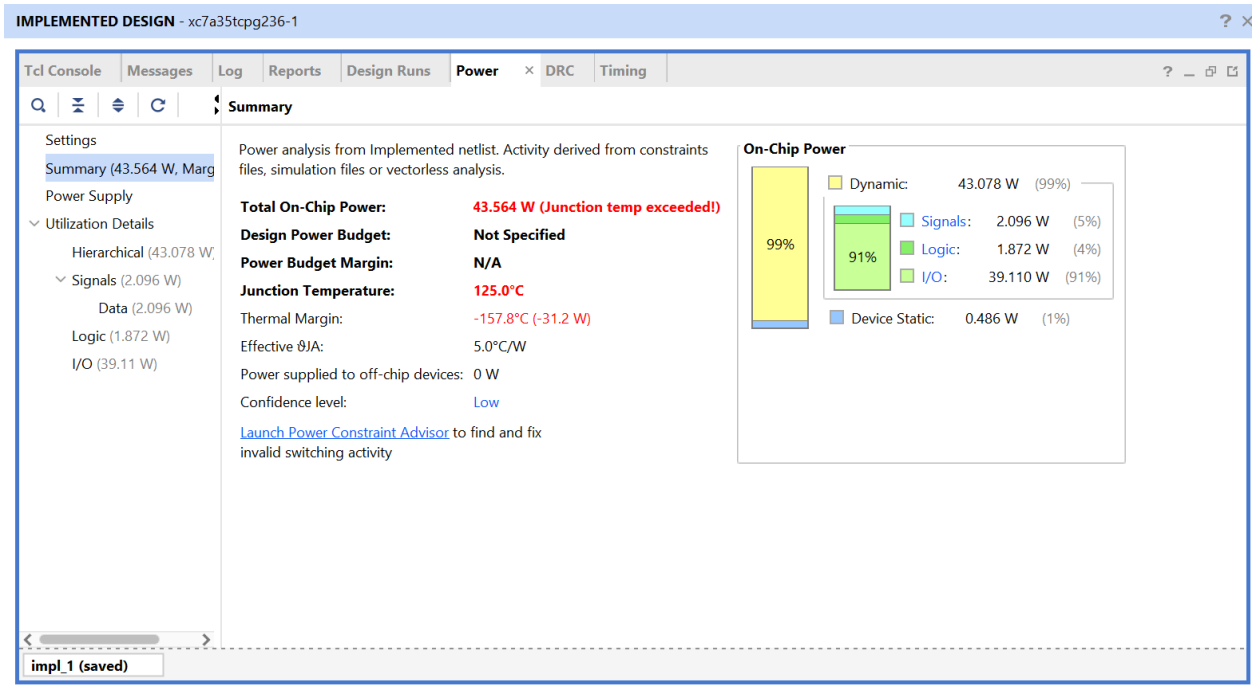
2.2 Clock Constraints

+-------+--------+-----------------+
| Clock | Domain | Constraint (ns) |
+-------+--------+-----------------+

3. Detailed Reports

3.1 By Hierarchy

+------------------+-----------+
| Name | Power (W) |
+------------------+-----------+
| booth_multiplier | 43.078 |
+------------------+-----------+



(ii) Clock Utilization Report:


```
------------------------------------------------------------------------------------
| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov  6 21:40:23 MST 2019
| Date         : Mon Apr 22 14:31:26 2024
| Host         : DHEEKSHITHA running 64-bit major release  (build 9200)
| Command      : report_clock_utilization -file booth_multiplier_clock_utilization_routed.rpt
| Design       : booth_multiplier
| Device       : 7a35t-cpg236
| Speed File   : -1  PRODUCTION 1.23 2018-06-13
| Design State : Routed
------------------------------------------------------------------------------------
```

Clock Utilization Report

Table of Contents

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1. Clock Primitive Utilization

+----------+------+-----------+-----+--------------+--------+
| Type | Used | Available | LOC | Clock Region | Pblock |
+----------+------+-----------+-----+--------------+--------+
BUFGCTRL	0	32	0	0	0
BUFH	0	72	0	0	0
BUFIO	0	20	0	0	0
BUFMR	0	10	0	0	0
BUFR	0	20	0	0	0
MMCM	0	5	0	0	0
PLL	0	5	0	0	0
+----------+------+-----------+-----+--------------+--------+

2. Global Clock Resources

+-----------+-----------+-----------------+------------+------+--------------+--------------------+-------------+---------------+--------------+-------+------------+-----+
| Global Id | Source Id | Driver Type/Pin | Constraint | Site | Clock Region | Load Clock Region | Clock Loads | Non-Clock Loads | Clock Period | Clock | Driver Pin | Net |
+-----------+-----------+-----------------+------------+------+--------------+--------------------+-------------+---------------+--------------+-------+------------+-----+

* Clock Loads column represents the clock pin loads (pin count)
** Non-Clock Loads column represents the non-clock pin loads (pin count)

3. Global Clock Source Details

+-----------+-----------+-----------------+------------+------+--------------+-------------+-----------------+-----------------+--------------+-------+------------+-----+
| Source Id | Global Id | Driver Type/Pin | Constraint | Site | Clock Region | Clock Loads | Non-Clock Loads | Source Clock Period | Source Clock | Driver Pin | Net |
+-----------+-----------+-----------------+------------+------+--------------+-------------+-----------------+-----------------+--------------+-------+------------+-----+

* Clock Loads column represents the clock pin loads (pin count)
** Non-Clock Loads column represents the non-clock pin loads (pin count)

4. Clock Regions: Key Resource Utilization

	Global Clock		BUFRs		BUFMRs		BUFIOs		MMCM		PLL		GT		PCI		ILOGIC		OLOGIC		FF		LUTM		RAMB18		RAMB36		DSP48E2	
Clock Region Name	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail
X0Y0	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1200	0	400	0	20	0	10	0	20
X1Y0	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1500	0	450	0	40	0	20	0	20
X0Y1	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1200	0	400	0	20	0	10	0	20
X1Y1	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1500	0	450	0	40	0	20	0	20
X0Y2	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1800	0	400	0	20	0	10	0	20
X1Y2	0	12	0	0	0	0	0	0	0	0	0	0	0	4	0	1	0	0	0	0	0	950	0	300	0	10	0	5	0	20

* Global Clock column represents track count; while other columns represents cell counts

5. Clock Regions : Global Clock Summary

All Modules

	X0	X1
Y2	0	0
Y1	0	0
Y0	0	0

Location of IO Primitives which is load of clock spine

Location of clock ports

WALLACE MULTIPIER:

(i) Power Utilization Report:

| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov 6 21:40:23 MST 2019
| Date : Mon Apr 22 14:46:52 2024
| Host : DHEEKSHITHA running 64-bit major release (build 9200)
| Command : report_power -file wallace_tree_multiplier_power_routed.rpt -pb wallace_tree_multiplier_power_summary_routed.pb -rpx wallace_tree_multiplier_power_routed.rpx
| Design : wallace_tree_multiplier
| Device : xc7a35tcpg236-1
| Design State : routed
| Grade : commercial
| Process : typical
| Characterization : Production

Power Report

Table of Contents
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1. Summary

Total On-Chip Power (W)	41.038 (Junction temp exceeded!)
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	40.552
Device Static (W)	0.486
Effective TJA (C/W)	5.0
Max Ambient (C)	0.0
Junction Temperature (C)	125.0
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)
Slice Logic	1.044	93	---	---
LUT as Logic	1.044	78	20800	0.38
Signals	1.781	109	---	---
I/O	37.727	32	106	30.19
Static Power	0.486			
Total	41.038			

1.2 Power Supply Summary

Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	3.230	2.889	0.341

Vccaux	1.800	1.434	1.380	0.053
Vcco33	3.300	10.661	10.660	0.001
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	0.000	0.000	0.000
Vcco15	1.500	0.000	0.000	0.000
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.010	0.000	0.010
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.020	0.000	0.020

1.3 Confidence Level

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is routed	
Clock nodes activity	High	User specified more than 95% of clocks	
I/O nodes activity	Low	More than 75% of inputs are missing user specification	Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
Device models	High	Device models are Production	
Overall confidence level	Low		

2. Settings

2.1 Environment

Ambient Temp (C)	25.0
ThetaJA (C/W)	5.0
Airflow (LFM)	250
Heat Sink	medium (Medium Profile)
ThetaSA (C/W)	4.6
Board Selection	medium (10"x10")
# of Board Layers	12to15 (12 to 15 Layers)
Board Temperature (C)	25.0

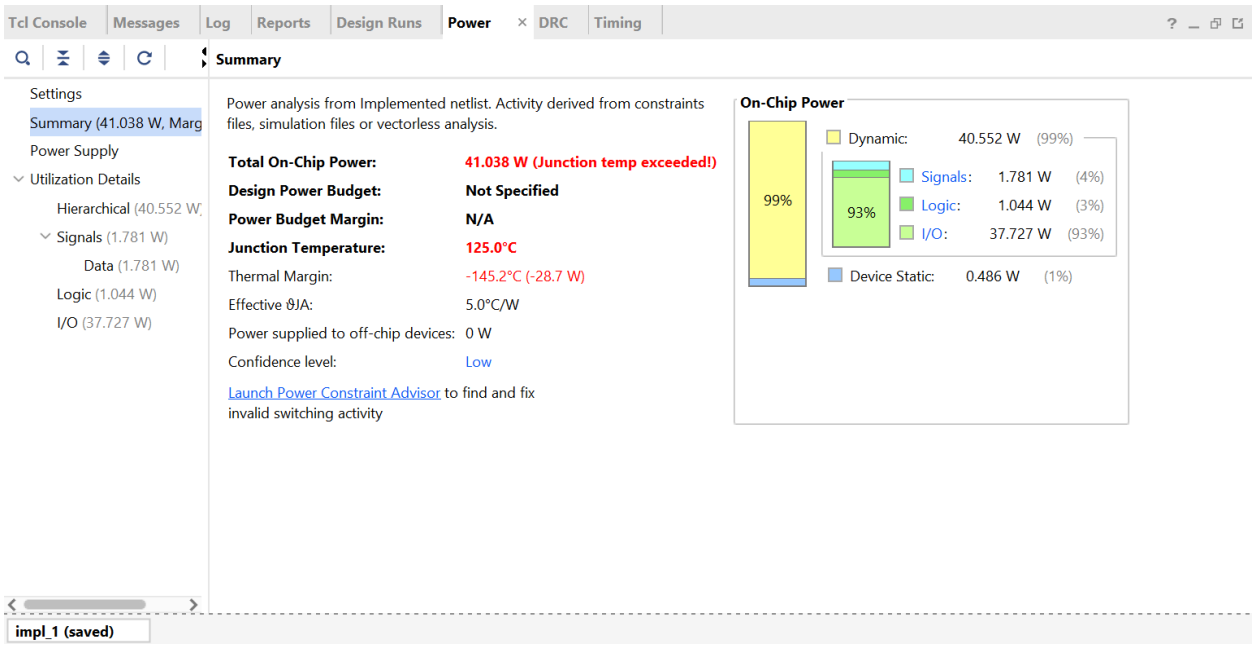
2.2 Clock Constraints

Clock	Domain	Constraint (ns)

3. Detailed Reports

3.1 By Hierarchy

Name	Power (W)
wallace_tree_multiplier	40.552



(ii) Clock Utilization Report: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| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov  6 21:40:23 MST 2019
| Date         : Mon Apr 22 14:46:52 2024
| Host         : DHEEKSHITHA running 64-bit major release  (build 9200)
| Command      : report_clock_utilization -file wallace_tree_multiplier_clock_utilization_routed.rpt
| Design       : wallace_tree_multiplier
| Device       : 7a35t-cpg236
| Speed File   : -1  PRODUCTION 1.23 2018-06-13
| Design State : Routed
------------------------------------------------------------------------------------------------
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Clock Utilization Report

Table of Contents

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1. Clock Primitive Utilization

+----------+------+-----------+-----+--------------+--------+
| Type | Used | Available | LOC | Clock Region | Pblock |
+----------+------+-----------+-----+--------------+--------+
BUFGCTRL	0	32	0	0	0
BUFH	0	72	0	0	0
BUFIO	0	20	0	0	0
BUFMR	0	10	0	0	0
BUFR	0	20	0	0	0
MMCM	0	5	0	0	0
PLL	0	5	0	0	0
+----------+------+-----------+-----+--------------+--------+

2. Global Clock Resources

+-----------+-----------+-----------------+------------+------+-------------+-------------------+-------------+---------------+-------------+-------+------------+-----+
| Global Id | Source Id | Driver Type/Pin | Constraint | Site | Clock Region | Load Clock Region | Clock Loads | Non-Clock Loads | Clock Period | Clock | Driver Pin | Net |
+-----------+-----------+-----------------+------------+------+-------------+-------------------+-------------+---------------+-------------+-------+------------+-----+
* Clock Loads column represents the clock pin loads (pin count)
** Non-Clock Loads column represents the non-clock pin loads (pin count)

3. Global Clock Source Details

+-----------+-----------+-----------------+------------+------+-------------+-------------+-----------------+-----------------+--------------+-------+------------+-----+
| Source Id | Global Id | Driver Type/Pin | Constraint | Site | Clock Region | Clock Loads | Non-Clock Loads | Source Clock Period | Source Clock | Driver Pin | Net |
+-----------+-----------+-----------------+------------+------+-------------+-------------+-----------------+-----------------+--------------+-------+------------+-----+
* Clock Loads column represents the clock pin loads (pin count)
** Non-Clock Loads column represents the non-clock pin loads (pin count)

4. Clock Regions: Key Resource Utilization

	Global Clock		BUFRs		BUFMRs		BUFIOs		MMCM		PLL		GT		PCI		ILOGIC		OLOGIC		FF		LUTM		RAMB18		RAMB36		DSP48E2	
Clock Region Name	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail	Used	Avail
X0Y0	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1200	0	400	0	20	0	10	0	20
X1Y0	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1500	0	450	0	40	0	20	0	20
X0Y1	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1200	0	400	0	20	0	10	0	20
X1Y1	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1500	0	450	0	40	0	20	0	20
X0Y2	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1800	0	400	0	20	0	10	0	20
X1Y2	0	12	0	0	0	0	0	0	0	0	0	0	0	4	0	1	0	0	0	0	0	950	0	300	0	10	0	5	0	20

* Global Clock column represents track count; while other columns represents cell counts

5. Clock Regions : Global Clock Summary

All Modules

	X0	X1
Y2	0	0
Y1	0	0
Y0	0	0

+----+----+----+

Location of IO Primitives which is load of clock spine

Location of clock ports

KOGGE STONE:

(i) Power Utilization Report:

| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov 6 21:40:23 MST 2019
| Date : Mon Apr 22 14:50:37 2024
| Host : LAPTOP-KRH96HJU running 64-bit major release (build 9200)
| Command : report_power -file kogg_power_routed.rpt -pb kogg_power_summary_routed.pb -rpx kogg_power_routed.rpx
| Design : kogg
| Device : xc7a35tcpg236-1
| Design State : routed
| Grade : commercial
| Process : typical
| Characterization : Production

Power Report

Table of Contents
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1. Summary

Total On-Chip Power (W)	4.892
Design Power Budget (W)	Unspecified*
Power Budget Margin (W)	NA
Dynamic (W)	4.804
Device Static (W)	0.088
Effective TJA (C/W)	5.0
Max Ambient (C)	60.5
Junction Temperature (C)	49.5
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

* Specify Design Power Budget using, set_operating_conditions -design_power_budget <value in Watts>

1.1 On-Chip Components

On-Chip	Power (W)	Used	Available	Utilization (%)

Slice Logic	0.066	15	---	---
LUT as Logic	0.066	13	20800	0.06
Signals	0.163	31	---	---
I/O	4.575	25	106	23.58
Static Power	0.088			
Total	4.892			

1.2 Power Supply Summary

Source	Voltage (V)	Total (A)	Dynamic (A)	Static (A)
Vccint	1.000	0.318	0.293	0.024
Vccaux	1.800	0.383	0.369	0.014
Vcco33	3.300	0.000	0.000	0.000
Vcco25	2.500	0.000	0.000	0.000
Vcco18	1.800	2.138	2.137	0.001
Vcco15	1.500	0.000	0.000	0.000
Vcco135	1.350	0.000	0.000	0.000
Vcco12	1.200	0.000	0.000	0.000
Vccaux_io	1.800	0.000	0.000	0.000
Vccbram	1.000	0.000	0.000	0.000
MGTAVcc	1.000	0.000	0.000	0.000
MGTAVtt	1.200	0.000	0.000	0.000
Vccadc	1.800	0.020	0.000	0.020

1.3 Confidence Level

User Input Data	Confidence	Details	Action
Design implementation state	High	Design is routed	
Clock nodes activity	High	User specified more than 95% of clocks	

I/O nodes activity	Low	More than 75% of inputs are missing user specification	Provide missing input activity with simulation results or by editing the "By Resource Type -> I/Os" view
Internal nodes activity	Medium	User specified less than 25% of internal nodes	Provide missing internal nodes activity with simulation results or by editing the "By Resource Type" views
Device models	High	Device models are Production	
Overall confidence level	Low		

2. Settings

2.1 Environment

Ambient Temp (C)	25.0
ThetaJA (C/W)	5.0
Airflow (LFM)	250
Heat Sink	medium (Medium Profile)
ThetaSA (C/W)	4.6
Board Selection	medium (10"x10")
# of Board Layers	12to15 (12 to 15 Layers)
Board Temperature (C)	25.0

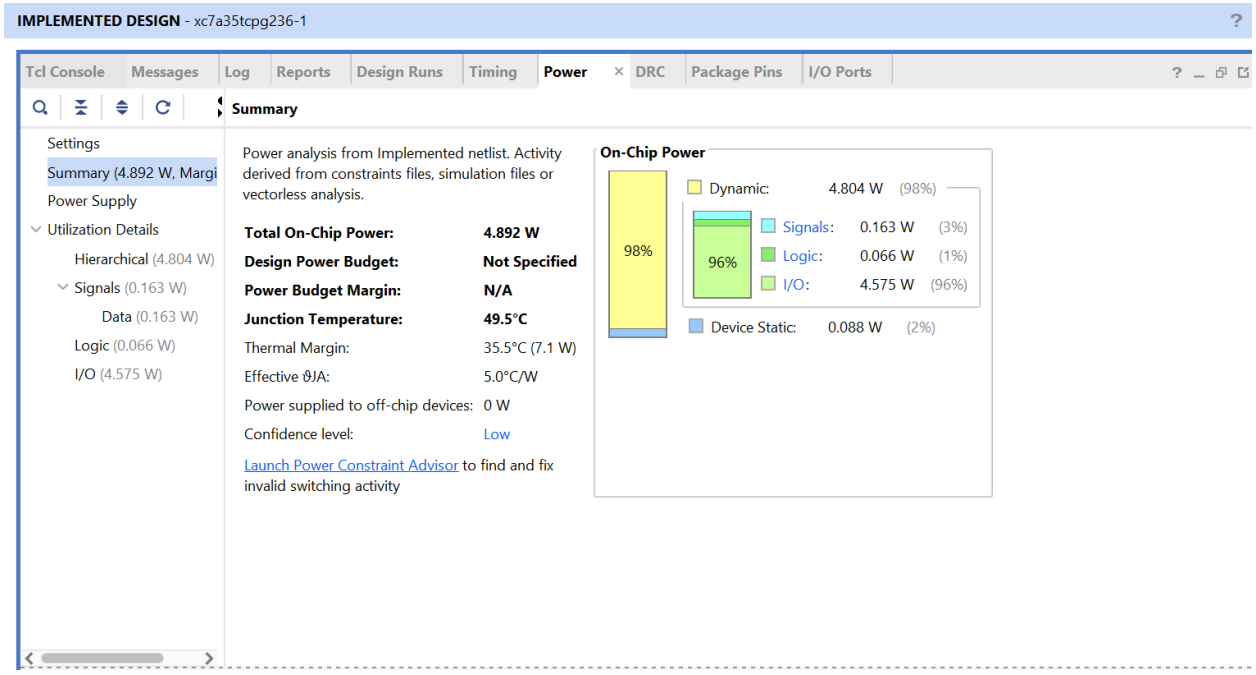
2.2 Clock Constraints

Clock	Domain	Constraint (ns)

3. Detailed Reports

3.1 By Hierarchy

+------+----------+
| Name | Power (W) |
+------+----------+
| kogg | 4.804 |
+------+----------+



(ii) Clock Utilization Report:

| Tool Version : Vivado v.2019.2 (win64) Build 2708876 Wed Nov 6 21:40:23 MST 2019
| Date   : Mon Apr 22 14:50:37 2024
| Host   : LAPTOP-KRH96HJU running 64-bit major release (build 9200)
| Command   : report_clock_utilization -file kogg_clock_utilization_routed.rpt
| Design   : kogg
| Device   : 7a35t-cpg236
| Speed File   : -1 PRODUCTION 1.23 2018-06-13
| Design State : Routed

Clock Utilization Report

Table of Contents
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1. Clock Primitive Utilization

+----------+------+-----------+-----+--------------+--------+
| Type | Used | Available | LOC | Clock Region | Pblock |
+----------+------+-----------+-----+--------------+--------+
BUFGCTRL	0	32	0	0	0
BUFH	0	72	0	0	0
BUFIO	0	20	0	0	0
BUFMR	0	10	0	0	0
BUFR	0	20	0	0	0
MMCM	0	5	0	0	0
PLL	0	5	0	0	0
+----------+------+-----------+-----+--------------+--------+

2. Global Clock Resources

+-----------+-----------+-----------------+------------+------+--------------+--------------------+-------------+---------
--------+--------------+-------+------------+-----+
| Global Id | Source Id | Driver Type/Pin | Constraint | Site | Clock Region | Load Clock Region |
Clock Loads | Non-Clock Loads | Clock Period | Clock | Driver Pin | Net |
+-----------+-----------+-----------------+------------+------+--------------+--------------------+-------------+---------
--------+--------------+-------+------------+-----+
* Clock Loads column represents the clock pin loads (pin count)
** Non-Clock Loads column represents the non-clock pin loads (pin count)

3. Global Clock Source Details

+-----------+-----------+-----------------+------------+------+--------------+-------------+-----------------+-----------
----------+--------------+------------+-----+

| Source Id | Global Id | Driver Type/Pin | Constraint | Site | Clock Region | Clock Loads | Non-Clock Loads | Source Clock Period | Source Clock | Driver Pin | Net |
+-----------+-----------+-----------------+------------+------+--------------+-------------+-----------------+---------------------+--------------+------------+-----+

* Clock Loads column represents the clock pin loads (pin count)
** Non-Clock Loads column represents the non-clock pin loads (pin count)

4. Clock Regions: Key Resource Utilization

+------------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+-------------+

| | Global Clock | BUFRs | BUFMRs | BUFIOs | MMCM | PLL | GT | PCI | ILOGIC | OLOGIC | FF | LUTM | RAMB18 | RAMB36 | DSP48E2 |
+------------------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+

| Clock Region Name | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail | Used | Avail |
+------------------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+

X0Y0	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1200	0	400	0	20	0	10	0	20
X1Y0	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1500	0	450	0	40	0	20	0	20
X0Y1	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1200	0	400	0	20	0	10	0	20
X1Y1	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1500	0	450	0	40	0	20	0	20
X0Y2	0	12	0	4	0	2	0	4	0	1	0	1	0	0	0	0	0	50	0	50	0	1800	0	400	0	20	0	10	0	20
X1Y2	0	12	0	0	0	0	0	0	0	0	0	0	0	4	0	1	0	0	0	0	0	950	0	300	0	10	0	5	0	20
+------------------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+------+-------+

* Global Clock column represents track count; while other columns represents cell counts

5. Clock Regions : Global Clock Summary

All Modules

	X0	X1
Y2	0	0
Y1	0	0
Y0	0	0

Location of IO Primitives which is load of clock spine

Location of clock ports