Unit I Biasing Methods and Amplifier Circuits

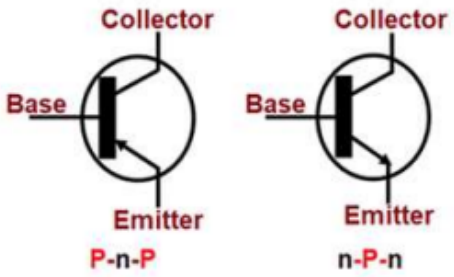
Bipolar Junction Transistor(BJT)

A transistor is a semiconductor device used to amplify or switch electronic signals and electrical power. It is composed of semiconductor material usually with at least three terminals for connection to an external circuit. A voltage or current applied to one pair of the transistor's terminals controls the current through another pair of terminals. Because the controlled (output) power can be higher than the controlling (input) power, a transistor can amplify a signal. Today, some transistors are packaged individually, but many more are found embedded in integrated circuits.

Most transistors are made from very pure silicon, and some from germanium, but certain other semiconductor materials are sometimes used. A transistor may have only one kind of charge carrier, in a field-effect transistor, or may have two kinds of charge carriers in bipolar junction transistor devices.

Bipolar junction transistor (BJT)

A bipolar junction transistor (BJT) is a type of transistor that uses both electrons and holes as charge carriers. A bipolar transistor allows a small current injected at one of its terminals to control a much larger current flowing between two other terminals, making the device capable of amplification or switching.



BJTs use two junctions between two semiconductor types, n-type and p-type, which are regions in a single crystal of material. The junctions can be made in several different ways, such as changing the Doping of the semiconductor material as it is grown, by depositing metal pellets to form alloy junctions, or by such methods as diffusion of n -type and p-type doping substances into the crystal.

Need for Biasing

Transistor Biasing is the process of setting a transistors DC operating voltage or current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

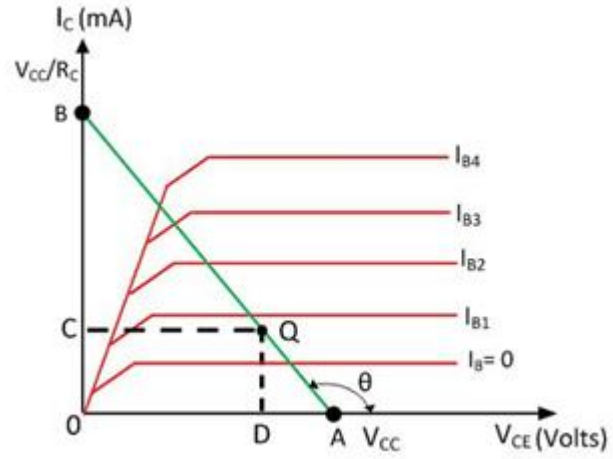
Establishing the correct operating point requires the selection of bias resistors and load resistors to provide the appropriate input current and collector voltage conditions. The correct

biasing point for a bipolar transistor, either NPN or PNP, generally lies somewhere between the two extremes of operation with respect to it being either “fully-ON” or “fully-OFF” along its DC load line. This central operating point is called the “Quiescent Operating Point”, or Q-point for short.

When a bipolar transistor is biased so that the Q-point is near the middle of its operating range, that is approximately halfway between cut-off and saturation, it is said to be operating as a Class-A amplifier. This mode of operation allows the output voltage to increase and decrease around the amplifiers Q-point without distortion as the input signal swings through one complete cycle. In other words, the output is available for the full 360o of the input cycle.

DC Load line and Bias point:

The DC load line is the load line of the DC equivalent circuit, defined by reducing the reactive components to zero (replacing capacitors by open circuits and inductors by short circuits). It is used to determine the correct DC operating point, often called the Q point.



Bias point of transistor:

- It the point on DC Load Line, which represents the DC current I_{CQ} through transistor and voltage V_{CEQ} across transistor in quiescent or steady state/DC condition.
- The co-ordinates of Q point are I_{CQ} and V_{CEQ}. Q = I_{CQ} , V_{CEQ}
- The position of Q point on DC load line depends on application of transistor. When transistor is used as an amplifier, operating point Q should set at the centre of DC load line to avoid distortion in output waveform.

Various Biasing Methods of BJT:

Base Biasing of a Common Emitter Amplifier

One of the most frequently used biasing circuits for a transistor circuit is with the self-biasing of the emitter-bias circuit where one or more biasing resistors are used to set up the initial DC values for the three transistor currents, (I_B), (I_C) and (I_E).

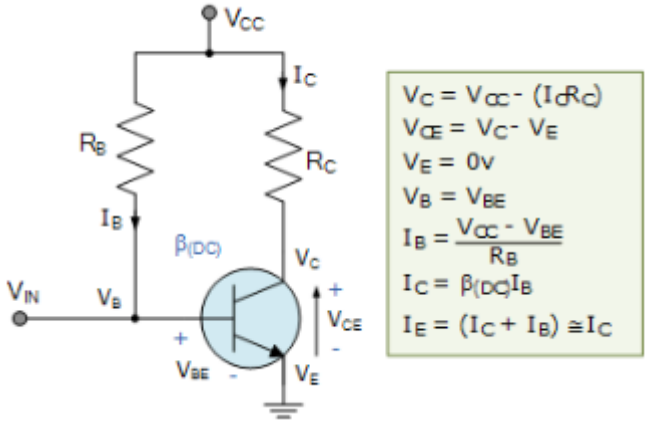
The two most common forms of bipolar transistor biasing are: Beta Dependent and Beta Independent. Transistor bias voltages are largely dependent on transistor beta, (β) so the biasing set up for one transistor may not necessarily be the same for another transistor as their beta values may be different. Transistor biasing can be achieved either by using a single feed

back resistor or by using a simple voltage divider network to provide the required biasing voltage.

The following are five examples of transistor Base bias configurations from a single supply (V_{cc}).

The circuit shown is called as a “fixed base bias circuit”, because the transistors base current, I_B remains constant for given values of V_{cc}, and therefore the transistors operating point must also remain fixed. This two resistor biasing network is used to establish the initial operating region of the transistor using a fixed current bias.

This type of transistor biasing arrangement is also beta dependent biasing as the steady-state condition of operation is a function of the transistors beta β value, so the biasing point will vary over a wide range for transistors of the same type as the characteristics of the transistors will not be exactly the same.



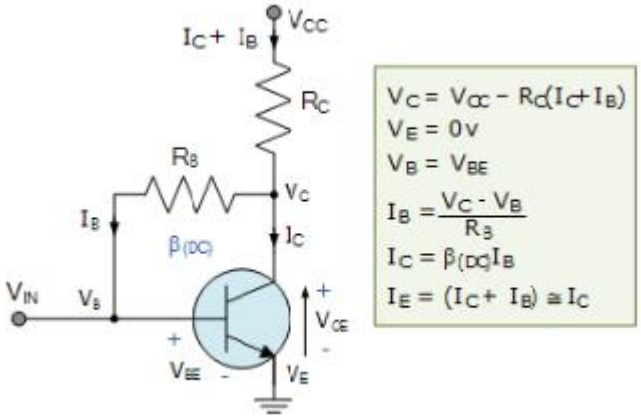
The emitter diode of the transistor is forward biased by applying the required positive base bias voltage via the current limiting resistor R_B. Assuming a standard bipolar transistor, the forward base-emitter voltage drop would be 0.7V. Then the value of R_B is simply: $(V_{CC} - V_{BE})/I_B$ where I_B is defined as I_C/β.

With this single resistor type of biasing arrangement, the biasing voltages and currents do not remain stable during transistor operation and can vary enormously. Also, the operating temperature of the transistor can adversely affect the operating point.

Collector Feedback Biasing a Transistor

This self biasing collector feedback configuration is another beta dependent biasing method which requires two resistors to provide the necessary DC bias for the transistor. The collector to base feedback configuration ensures that the transistor is always biased in the active region regardless of the value of Beta (β). The DC base bias voltage is derived from the collector voltage V_C, thus providing good stability.

In this circuit, the base bias resistor, R_B is connected to the transistors collector C, instead of to the supply voltage rail, V_{cc}. Now if the collector current increases, the collector voltage drops, reducing the base drive and thereby automatically reducing the collector current to keep the transistors Q-point fixed. Therefore, this method of collector feedback biasing produces negative feedback round the transistor as there is direct feedback from the output terminal to the input terminal via resistor, R_B.

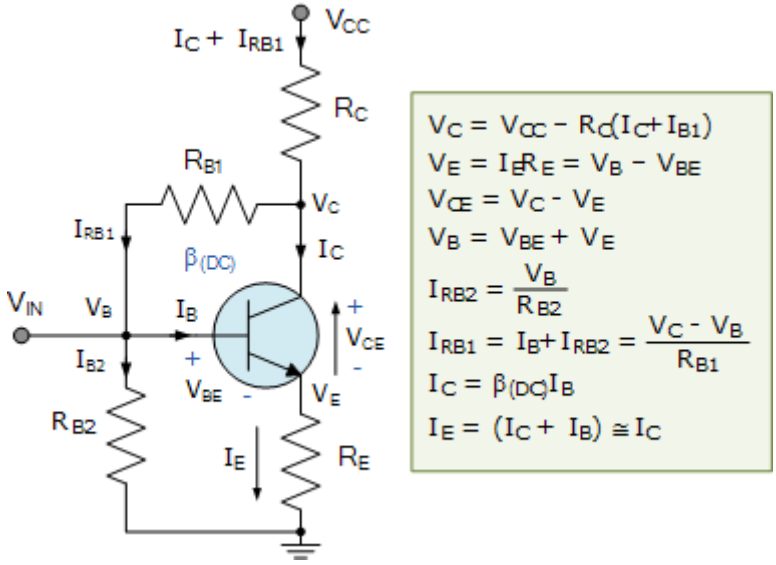


Since the biasing voltage is derived from the voltage drop across the load resistor, R_L, if the load current increases there will be a larger voltage drop across R_L, and a corresponding reduced collector voltage, V_C. This effect will cause a corresponding drop in the base current, I_B which in turn, brings I_C back to normal.

The opposite reaction will also occur when the transistors collector current reduces. Then this method of biasing is called self-biasing with the transistors stability using this type of feedback bias network being generally good for most amplifier designs.

Transistor Biasing with Emitter Feedback

This type of transistor biasing configuration, often called self-emitter biasing, uses both emitter and base-collector feedback to stabilize the collector current even further. This is because resistors R_{B1} and R_E as well as the base-emitter junction of the transistor are all effectively connected in series with the supply voltage, V_{CC}.



The downside of this emitter feedback configuration is that it reduces the output gain due to the base resistor connection. The collector voltage determines the current flowing through the feedback resistor, R_{B1} producing “degenerative feedback”.

The current flowing from the emitter, I_E (which is a combination of I_C + I_B) causes a voltage drop to appear across R_E in such a direction, that it reverse biases the base-emitter junction.

So if the emitter current increases, due to an increase in collector current, voltage drop I*R_E also increases. Since the polarity of this voltage reverse biases the base-emitter junction, I_B automatically decreases.

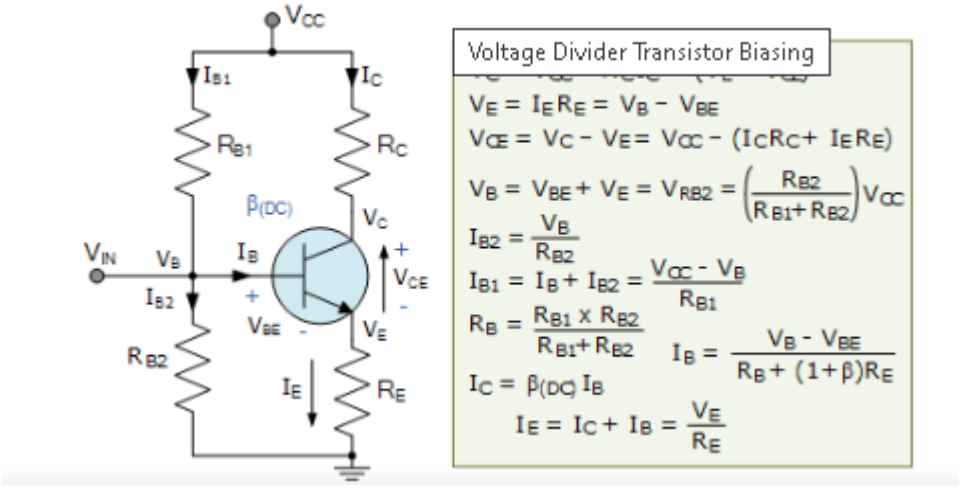
Generally, resistor values are set so that the voltage dropped across the emitter resistor R_E is approximately 10% of V_{CC} and the current flowing through resistor R_{B1} is 10% of the collector current I_C.

Thus this type of transistor biasing configuration works best at relatively low power supply voltages.

Voltage Divider Transistor Biasing

Here the common emitter transistor configuration is biased using a voltage divider network to increase stability. The name of this biasing configuration comes from the fact that the two resistors R_{B1} and R_{B2} form a voltage or potential divider network across the supply with their centre point junction connected the transistors base terminal.

This voltage divider biasing configuration is the most widely used transistor biasing method. The emitter diode of the transistor is forward biased by the voltage value developed across resistor R_{B2}. Also, voltage divider network biasing makes the transistor circuit independent of changes in beta as the biasing voltages set at the transistors base, emitter, and collector terminals are not dependant on external circuit values.



To calculate the voltage developed across resistor R_{B2} and therefore the voltage applied to the base terminal we simply use the voltage divider formula for resistors in series.

Generally, the voltage drop across resistor R_{B2} is much less than for resistor R_{B1}. Clearly the transistors base voltage V_B with respect to ground, will be equal to the voltage across R_{B2}.

The amount of biasing current flowing through resistor R_{B2} is generally set to 10 times the value of the required base current I_B so that it is sufficiently high enough to have no effect on the voltage divider current or changes in Beta.

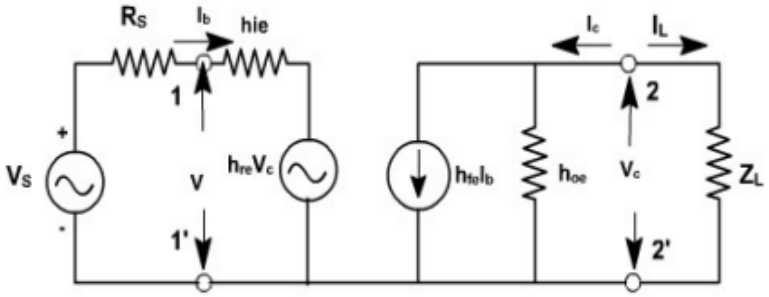
The goal of Transistor Biasing is to establish a known quiescent operating point, or Q-point for the bipolar transistor to work efficiently and produce an undistorted output signal. Correct DC biasing of the transistor also establishes its initial AC operating region with practical biasing circuits using either a two or four-resistor bias network.

Hybrid model of CE amplifier:

Every linear circuit having input and output terminals can be analyzed by four parameters (one measured in ohm, one in mho and two dimensionless) called hybrid or h Parameters. Hybrid means "mixed". Since these parameters have mixed dimensions, they are called hybrid parameters.

The circuit input terminals are the transistor base and emitter, and the output terminals are the collector and the emitter. So, the emitter terminal is common to both input and output, and the circuit configuration is termed common-emitter (CE).

There is a 180° phase shift between the input and output waveforms. This can be understood by considering the effect of a positive-going input signal. When υ_s increases in a positive direction, it increases the transistor base-emitter voltage (V_{BE}). The increase in V_{BE} raises the level of I_C, thereby increasing the voltage drop across R_C, and thus reducing the level of the collector voltage (V_C). The changing level of V_C is capacitor-coupled to the circuit output to produce the ac output voltage (υ_o). As υ_s increases in a positive direction, υ_o goes in a negative direction.



Current gain:

For the transistor amplifier stage, Ai is defined as the ratio of output to input currents.

$$A_i = \frac{I_L}{I_b} = \frac{-I_C}{I_b} \qquad (I_L + I_c = 0. \quad \therefore I_L = -I_c)$$

$$I_C = h_{fe} I_b + h_{oe} V_c$$

$$V_c = I_L Z_L = -I_c Z_L$$

$$\therefore I_c = h_{fe} I_b + h_{oe} (-I_c Z_L)$$

$$\text{or } \frac{I_c}{I_b} = \frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$\therefore A_i = -\frac{h_{fe}}{1 + h_{oe} Z_L}$$

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = - \frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output admittance:

$$Y_0 = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe} \frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $\quad R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0.$

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_0 = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_S) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

$$= A_V . \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i\, Z_L}{Z_i + R_s}$$

Gain and Frequency Response:

The voltage gain of a CE amplifier varies with signal frequency. It is because reactances of the capacitors in the circuit changes with signal frequency and hence affects the output voltage. The curve drawn between voltage gain and the signal frequency of an amplifier is known as frequency response. Below figure shows the frequency response of a typical CE amplifier.

The voltage gain drops off at low (< FL) and high (> FH) frequencies, whereas it is constant over the mid-frequency range (FL to FH).

At low frequencies (< FL) The reactance of coupling capacitor C_2 is relatively high and hence very small part of the signal will pass from amplifier stage to the load. Moreover, C_E cannot shunt the R_E effectively because of its large reactance at low frequencies. These two factors cause a drops off of voltage gain at low frequencies.

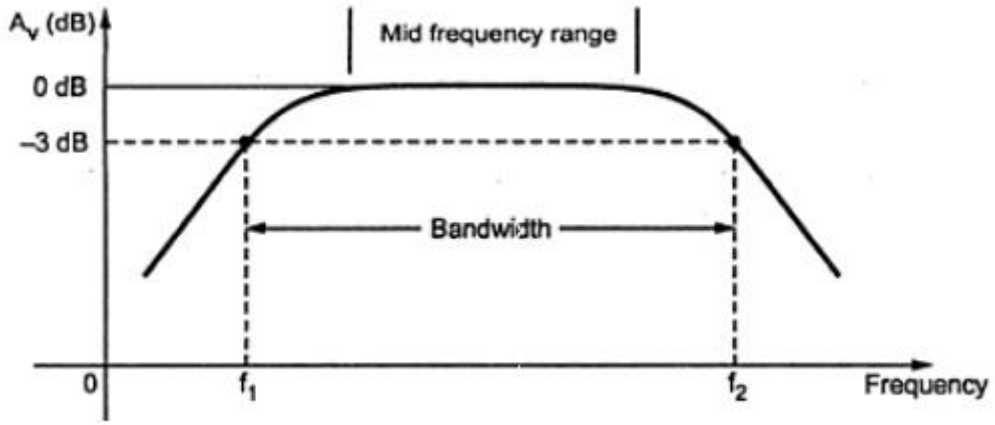


Fig. Normalized voltage gain vs frequency

At high frequencies (> FH) The reactance of coupling capacitor C_2 is very small and it behaves as a short circuit. This increases the loading effect of the amplifier stage and serves to reduce the voltage gain. Moreover, at high frequencies, the capacitive reactance of base-emitters junction is low which increases the base current. This frequency reduces the current amplification factor β. Due to these two reasons, the voltage gain drops off at high frequency.

At mid frequencies (FL to FH) The voltage gain of the amplifier is constant. The effect of the coupling capacitor C2 in this frequency range is such as to maintain a constant voltage gain. Thus, as the frequency increases in this range, the reactance of CC decreases, which tend to increase the gain.

Differential Amplifier:

The differential amplifier circuit amplifies the difference between signals applied to the inputs. There are two input voltages V_1 and V_2. This amplifier amplifies the difference between the two input voltages.

Common Mode Operation

In this mode, the signals applied to the base of Q1 and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in the Fig.

In phase signal voltages at the bases of Q_1 and Q_2 causes in phase signal voltages to appear across R E, which add together. Hence R E carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier.

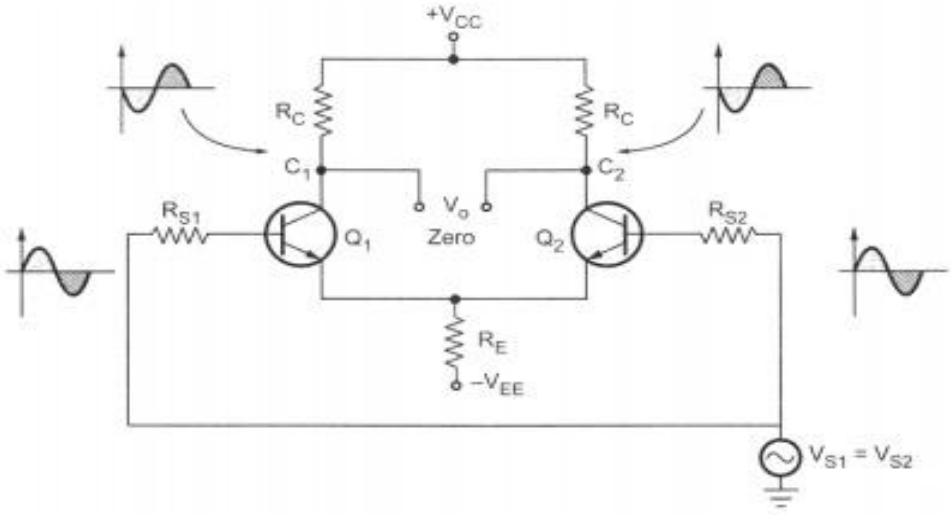


Fig. Common mode operation

While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q_1 and Q_2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase,

Fig. (20) - (20) = 0. Thus the difference output Vo is almost zero, negligibly small. ideally it should be zero.

Differential mode operation:

Differential Mode Operation In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180" out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig.

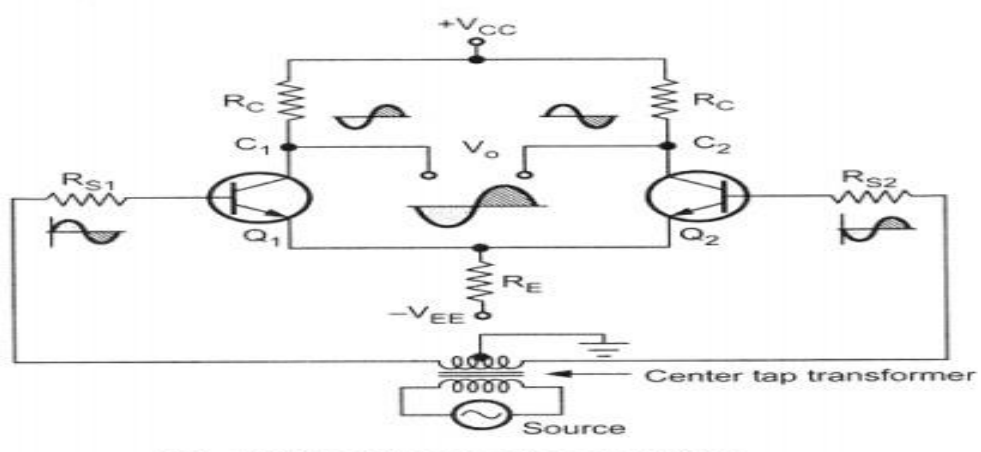


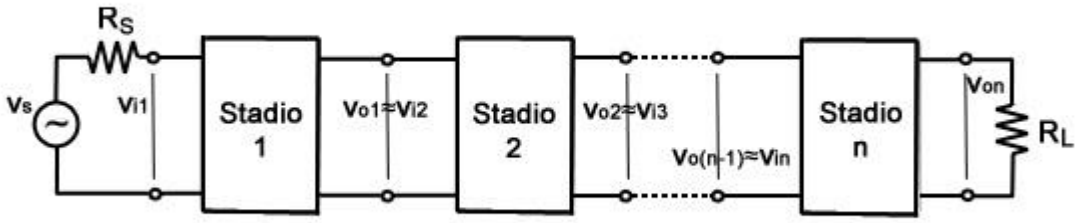
Fig Differential mode operation

Assume that the sine wave on the base of Q_1 is positive going while on the base of Q_2 is negative going. With a positive going signal on the base of Q_1, negative going signal develops on the collector of Q_1. Due to positive going signal, current through R_E also increases and hence a positive going wave is developed across R_E. Due to negative going signal on the base of Q_2, an amplified positive going signal develops on the collector of Q_2. And a negative going signal develops across R E, because of emitter follower action of Q_2. So signal voltages across R E, due to the effect of Q_1 and Q_2 are equal in magnitude and 180o out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance.

Hence R E in this case does not introduce negative feedback. While Vo is the output taken across collector of Q_1 and collector of Q_2. The two outputs on collector L and 2 are equal in magnitude but opposite in polarity. And Vo is the difference between these two signals, e.g. +10 - (-10) = + 20.Hence the difference output Vo is twice as large as the signal voltage from either collector to ground.

Multistage Amplifier:

A multistage amplifier is an electronic amplifier consisting of two or more single-stage amplifiers connected together. Output of a single stage amplifier is low. Therefore, all practical amplifiers are “multistage” i.e. they have more than one stage. The stages are connected(cascaded) with each other with some coupling device. Each stage consists of one transistor and the associated circuitry. One stage is coupled to the next stage such that the output of one stage becomes automatically the input of next stage.



The RC coupled amplifiers use resistance/capacitance coupling between two stages. The capacitance does not allow D.C. components of the amplified output of the preceding stage to the next stage. These are basic amplifiers used as audio and video amplifiers(with some changes). They are used to amplify voltage of the signal in the first few stages of the amplifier systems. The transformer coupled amplifiers use transformer as the coupling device. They perform two functions : (a) they block D.C. component and do not allow it to pass to the next stage. (b) They help in impedance matching with the load. It is to be mentioned here that these are used at the final stage of the amplification, where they are to be coupled with loudspeaker or the other load. In direct coupled amplifiers, the successive stages are directly coupled to each other. These are used for amplifying very low frequency signal (up to 10 Hz) and therefore, do not need any coupling for by-passing D.C.

Gain

The ratio of the output to the input of an amplifier is called gain. It may be:

Current gain, Ai = output current/input current = I_0/I_{in}

Voltage gain, Av = output voltage/input voltage = V_0/V_{in}

Power gain, Ap = output power/input power = P_0/P_{in}

Absolute gain :

The gain of an amplifier, when specified in number is called its "absolute gain". The gain of a multistage amplifier is equal to the product of the gains of its individual stages.

G = G1.G2.G3…..Gn.

Thus the total gain of an amplifier is equal to the product of the gains of its various stages. The gain in number is called "absolute gain".

Output of the first stage makes the input of the second stage, the output of the second stage makes the input of third stage and so on. The signal voltage V_s is applied to the input of the first stage. The final output V_0 is then available at the output terminals of the last stage.

The high 3-dB frequency for n-cascaded stages is fH and equal lo the frequency for which the overall voltage gain falls 3 dB i.e. $1/\sqrt{2}$ of its mid band value.

Multistage Amplifier Types

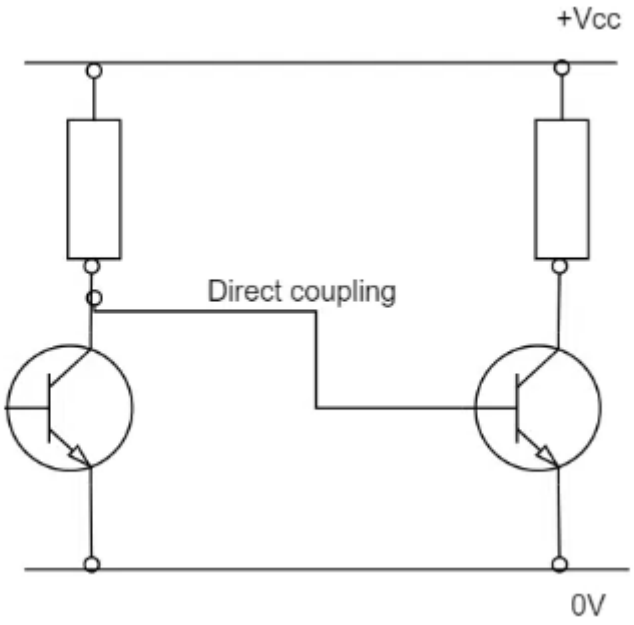
When the amplifiers are connected using a coupling device, it is termed as interstage coupling. The type of coupling decides the classification of the multistage amplifier and those are as follows:

- Direct coupling
- Transformer coupling and
- Capacitor coupling

Direct Coupling (DC)

In a few of the amplifiers, both AC and DC are connected between the amplifier stages. Whereas in the direct coupling, the collector stage output has a direct connection (or through resistance) with the base stage and this does not show any blockage to DC. The direct coupling type permits the amplification of extremely minimal frequency values along with 0Hz. Mostly, wideband amplifiers employ this type so as to remove the usage of capacitors, because capacitors may cause increased frequency instability conditions. With this, there might have changes in the output gain at few frequency levels.

Multistage amplifiers that are coupled through this approach need to have good stability mainly in correspondence with temperature changes.

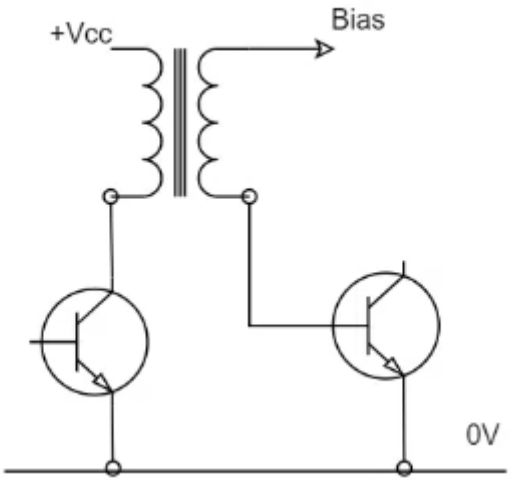


Direct Coupled Multistage Amplifier

Even a minimal variation in the biasing conditions at the transistor base will deliver extremely high changes at the collector. This will generate an error.

Transformer Coupling

In this type of coupling, the current flow at the collector of one stage will stream via the primary winding of the transformer. This stimulates signal voltage to the secondary winding which is connected at the input of the following stage. This signal is connected to the DC biasing at the base end of the following stage.

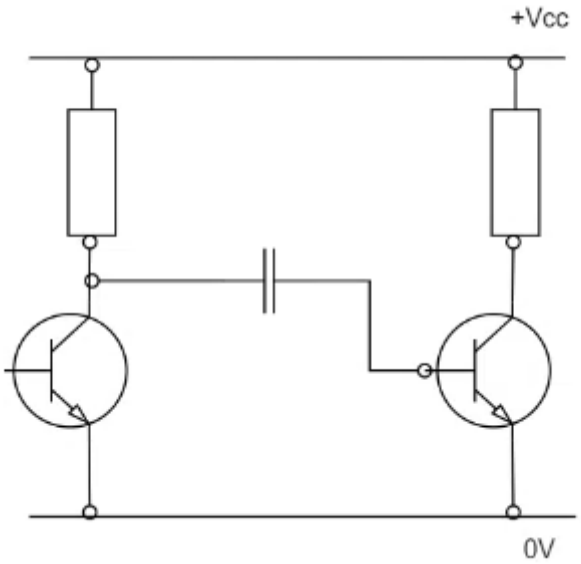


Transformer Coupled Multistage Amplifier

Here, DC is obstructed and the AC signals are cascaded, and the ratio of transformer turns might be even employed to offer impedance matching between the amplifier stages. This coupling type is most appropriate for the RF amplifiers as the reason that the size of the transformer can be maintained so small.

Capacitor Coupling

This type of coupling method offers electrical separation (which means blockage of DC) between the cascaded stages and permits the AC signals. This permits for a various base and the collector voltages on the cascaded stages and minimizes any kind of DC stability complications. Through this approach, the capacitor reactance should be so minimal at the low signal frequency range where this not extensively minimize signal in between the stages.



Capacitor Coupled Multistage Amplifier

Applications:

The multistage amplifier applications can be found in various industries and those are:

- Employed in the conditions when perfect impedance matching is required.
- Used in the applications when correct frequency response is necessary.
- These amplifiers are also used for DC isolation purposes.
- Applications those need enhanced gain, and good flexibility.
- Enhanced bandwidth
- Multistage amplifier cascading is used for high-voltage and high-speed applications.