Contents

1 EXPERIMENT

Design and analysis of 2 stage op amp

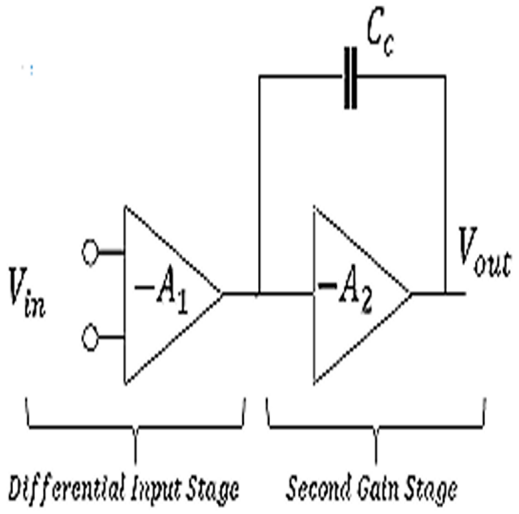
2 DESIGN SPECIFICATIONS

- **Process Technology:** 0.18µm CMOS
- **Power Supply:**
  - $V_{DD} = 1.8V$
  - $V_{SS} = 0V$
- **Load Capacitance:** 1pF
- **Phase Margin:** $\geq 60°$
- **DC Gain:** $\geq$ 1000 V/V (60 dB)
- **Common Mode Gain:** $\leq$ 0.1 V/V (-20 dB)
- **Unity Gain Frequency:** $>$ 100 MHz
- **Slew Rate:** $\geq$ 10 V/µs
- **Output Voltage Swing (Differential Peak-to-Peak):** $\geq 800\,\mathrm{mV_{pp}}$
- **Power Consumption:** Minimum

2.1 PROVIDED

- The source voltage is equal to 1.8 V.
- A bias current of 30 µA is assumed.

3 Theory



- **Two-Stage Operational Amplifier (Op-Amp):** A common configuration used to achieve high gain and good performance.
- **Input Stage (Differential Amplifier):**
  - This is the first stage of the op-amp.
  - Consists of a differential pair of transistors (e.g., MOSFETs or BJTs) that amplify the difference between the two input signals (inverting and non-inverting inputs).
  - Provides high input impedance and common-mode rejection ratio (CMRR).
  - Converts the differential input signal into a single-ended output.
- **Intermediate Stage (Gain Stage):**
  - This is the second stage of the op-amp.
  - Provides additional voltage gain to the signal.
  - Typically implemented using a common-source (for MOSFETs) or common-emitter (for BJTs) amplifier configuration.

  - May include a compensation capacitor (e.g., Miller capacitor) to ensure stability and prevent oscillations.

- **Slew Rate:**
  - Maximum rate of change of output per microsecond, referred to as the slew rate.
  - In differential amplifiers, the maximum output is obtained when the entire tail current flows through one side.
  - The general formula for slew rate is:

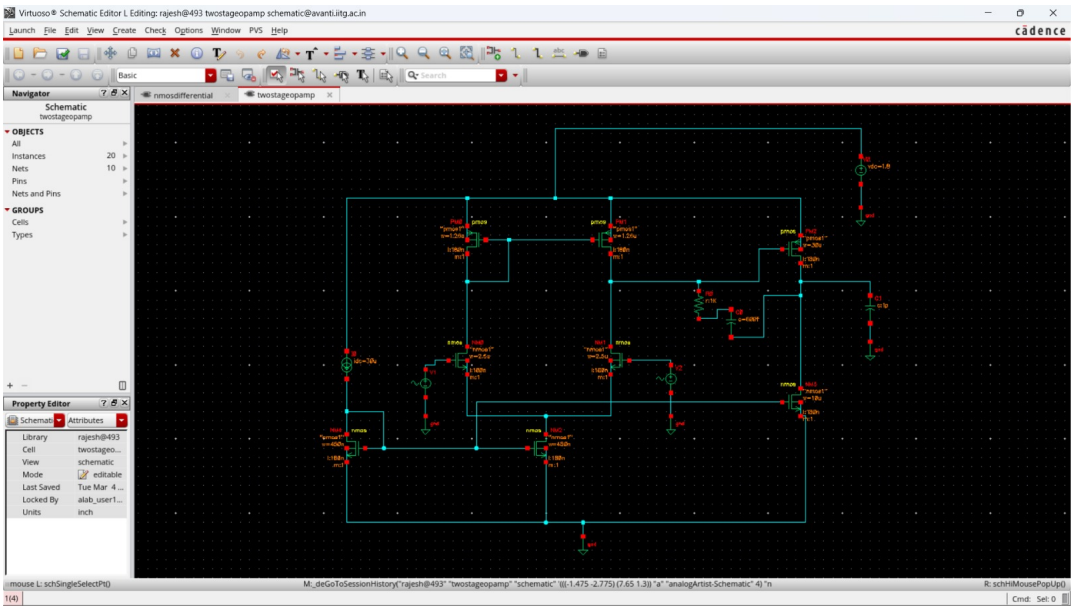
$$\text{Slew Rate} = \left(\frac{dV_{out}}{dt}\right)_{\max}$$

- **ICMR (Input Common Mode Range):**
  - Defined as the range of common-mode input that can be applied to the circuit while keeping all transistors in saturation.
  - Maximum ICMR refers to the highest common-mode input voltage that can be applied without causing transistor operation to exit saturation.

- **GBWP (Gain Bandwidth Product):**
  - The gain-bandwidth product of an amplifier is the product of its open-loop gain and the frequency range at which the amplifier's gain attenuates to 20 dB.

4 Two stage op amp

4.1 Schematic

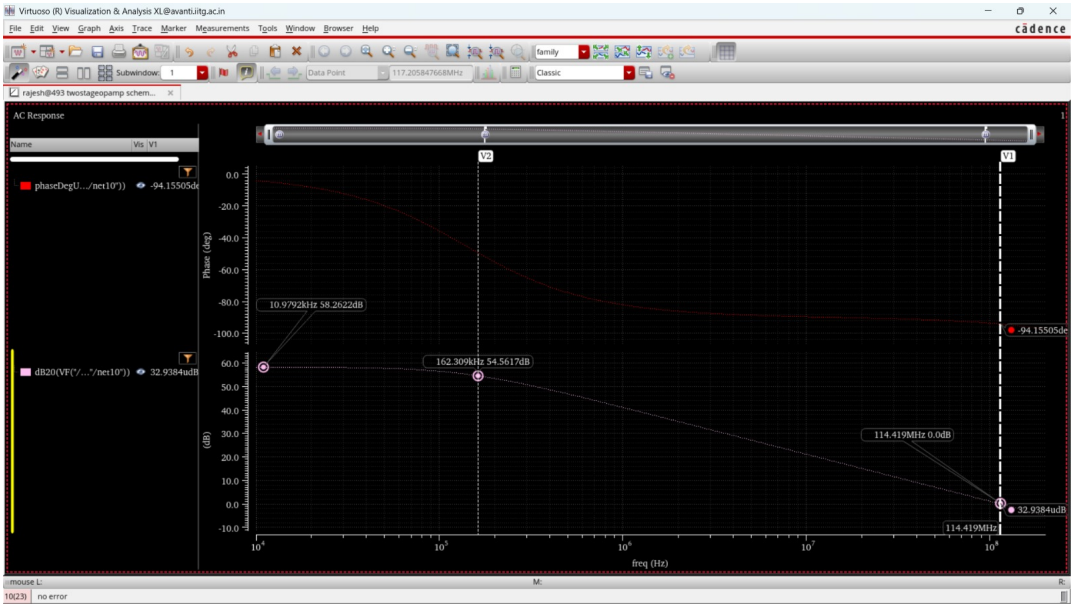


Transistor	Width	Length
M1	2520 nm	180 nm
M2	2520 nm	180 nm
M3	1260 nm	180 nm
M4	1260 nm	180 nm
M5	450 nm	180 nm
M6	3000 nm	180 nm
M7	2500 nm	180 nm
M8	450 nm	180 nm

Table 1: (W/L) of all transistors

- The circuit operates with a voltage of 1.25V(Vg).
- The threshold voltage of mosfet is 0.5V.

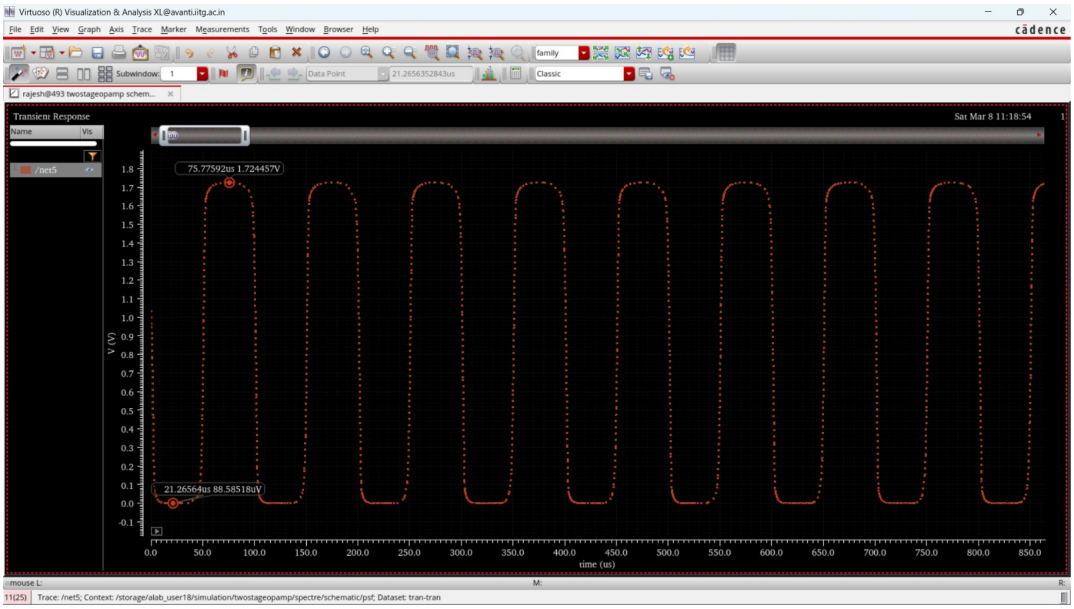
4.2 Gain VS Frequency Plot



- The gain vs. frequency graph is plotted by varying the frequency from 10 kHz to 200 MHz.
- **Intrinsic Gain:** 58.26 dB (The constant or maximum gain in the graph).
- **Cut-off or 3dB Frequency:** 162.57 kHz (The frequency where the gain is 0.707 times of its maximum value).
- **Unity Gain Frequency:** 114.419 MHz (The frequency up to which the MOSFET acts as an amplifier).

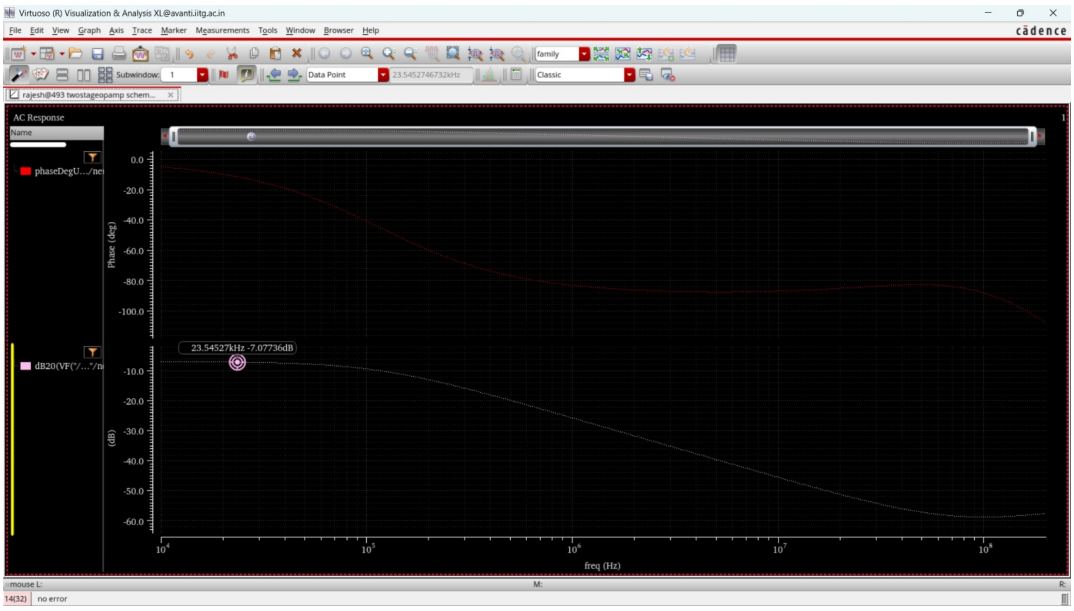
- we obtained the phase margin as 86.92 degrees.

4.3 Output Swing



- The ac input is given 10mv
- we obtained a output swing between 0.08v to 1.72v.

4.4 Common Mode Gain vs frequency



Common Mode Gain (A_{cm}) is the amplification factor of an amplifier when **both inputs** receive the **same signal** (i.e., a common-mode signal).

Mathematically, it is given by:

$$A_{cm} = \frac{V_{\text{out,cm}}}{V_{\text{in,cm}}} \tag{1}$$

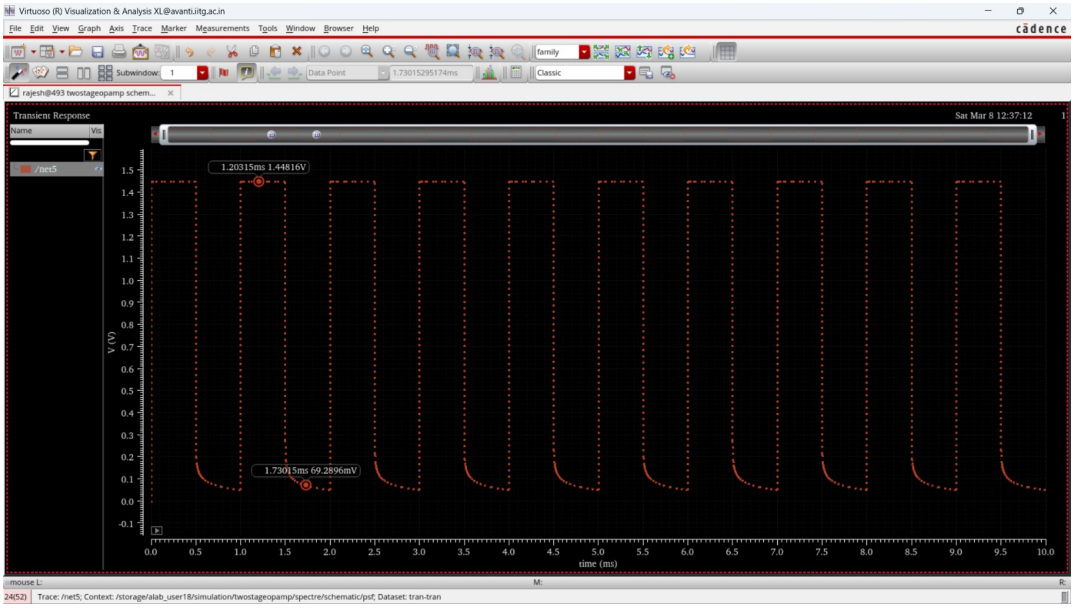
where:

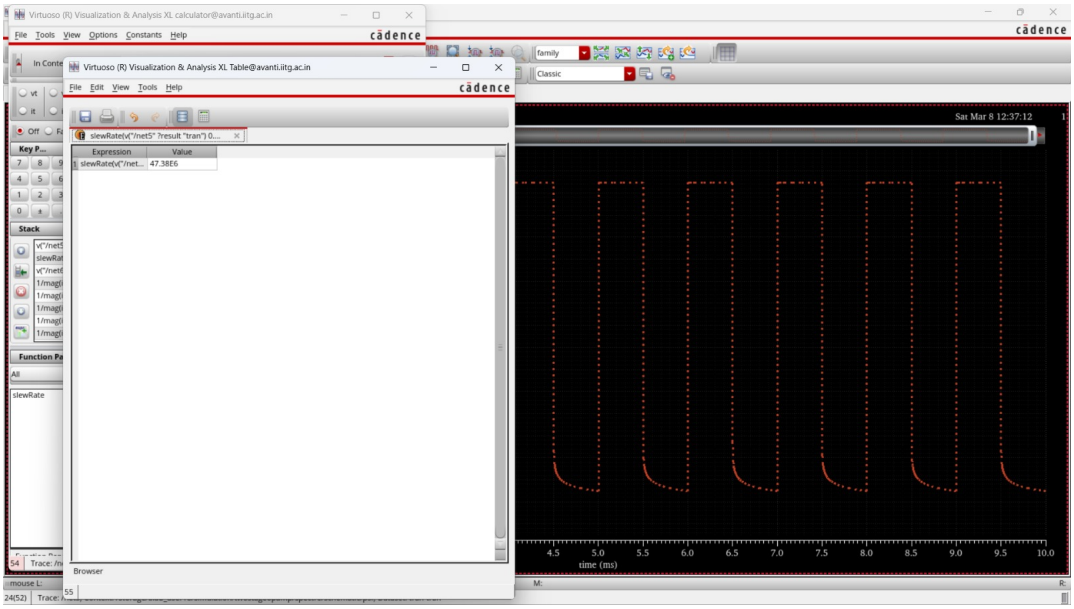
- $V_{\text{out,cm}}$ is the common-mode output voltage.
- $V_{\text{in,cm}}$ is the common-mode input voltage.

An **ideal differential amplifier** should reject common-mode signals, meaning A_{cm} should be as **low as possible** (ideally zero). However, practical amplifiers exhibit some finite common-mode gain, which affects the **Common-Mode Rejection Ratio (CMRR)**.

- we obtained the common mode gain as -7.5db.

4.5 Slew Rate





- we obtained a slew rate of 37.6 volts per microsecond.
- power consupmption is 0.756 milliwatts.

5 CALCULATIONS

- Zero frequency is assumed to be more than ten times the Gain Bandwidth Product. By solving the equations based on this assumption, the condition obtained is:

$$C_c > 0.22 C_L$$

Given that $C_L = 1$ pF, the required Miller capacitance is:

$$C_c > 0.22 \text{ pF}$$

Thus, a value of $C_c = 600$ fF is chosen for implementation.

- The slew rate expression for the circuit is given by:

$$\text{Slew Rate} = \frac{I_5}{C_c}$$

With known values of slew rate and C_L, the current I_5 must satisfy:

$$I_5 \geq 6\mu A$$

For optimal performance, I_5 is taken as 30 μA.

- The transconductance of the first stage can be determined using the relationship:

$$g_{m1} = \text{GBW} \times 2\pi C_c$$

Substituting the values for GBW and C_c, we obtain:

$$g_{m1} = 376.8\mu A$$

From the transconductance equation:

$$g_{m1} = \sqrt{2I_d\mu_n C_{ox}\frac{W}{L}}$$

By substituting the given parameters, the aspect ratio is calculated as:

$$\frac{W}{L}_1 = 14$$

Since symmetry is required for M_1 and M_2, the same aspect ratio is chosen:

$$\frac{W}{L}_1 = \frac{W}{L}_2 = 14$$

- The maximum input common-mode range (ICMR) is specified as 1.6 V. For transistor M_1 to remain in saturation, the condition is:

$$V_{d1} > V_g - V_{th1}$$

which simplifies to:

$$V_g < V_{d1} + V_{th1}$$

Substituting expressions for V_{d1} and considering the potential drop across M_3:

$$V_g < (V_{DD} - V_{sg3}) + V_{th1}$$

$$V_g < (V_{DD} - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} \frac{W}{L}_3}}) + V_{th1})$$

Solving for the required aspect ratio:

$$\frac{W}{L}_3 = 6.25 \quad \text{(approximated as 7)}$$

Since M_3 and M_4 are designed to be symmetric, the same value is used:

$$\frac{W}{L}_3 = \frac{W}{L}_4 = 7$$

- For the minimum ICMR, the transistors must remain in saturation, and the saturation voltage is given by:

$$V_{dsat} = ICMR_{min} - \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L}_1}} - V_{thn}$$

By substituting values:

$$V_{dsat} = 0.22$$

Using this in the current equation results in:

$$\frac{W}{L}_5 = 2.5$$

- Since the zero frequency is assumed to be ten times the GBW, the following condition holds:

$$g_{m6} > 10 \times g_{m1}$$

From earlier calculations:

$$g_{m6} > 3768\mu A$$

Given that M_6 and M_4 form a current mirror, the ratio can be expressed as:

$$\frac{(W/L)_6}{(W/L)_4} = \frac{I_6}{I_4} = \frac{g_{m6}}{g_{m4}}$$

Using known values of $(W/L)_4$ and I_4, and applying the transconductance equation:

$$g_{m4} = 154.91\mu A$$

From the above relation:

$$(W/L)_6 = 194.58$$

The drain current is found to be:

$$I_6 = 364.8\mu A$$

- Since M_6 and M_7 operate in series, their drain currents remain equal. The aspect ratio relation is:

$$\frac{(W/L)_7}{(W/L)_5} = \frac{I_7}{I_5}$$

Thus, solving for $(W/L)_7$:

$$(W/L)_7 = 30.4$$

6 Comparision Of Results

6.1 comparision of theoritical and practical results

parameter	**Theoretical Results**	**Practical Results**
$\|A_v\|$	$60db$	$58.94db$
GBW	100 MHz	114.41 MHz
$phasemargin$	≥ 60 deg	86.92 deg
$slewrate$	≥ 10 v/us	37.6 v/us

Table 2: Comparison of Theoretical and Practical Results

7 CONCLUSION

- The design and implementation of two stage opamp have been completed.
- All the results obtained theoretically and practically matched.