CE218472 - PSoC 6 MCU: Comparing External Voltages Using a Low-Power Comparator

Objective

This example demonstrates the voltage comparison functionality using the LPComp resource in PSoC® 6 MCU, with ModusToolbox™ IDE.

Requirements

Tool: ModusToolbox IDE 1.1

Programming Language: C

Associated Parts: All PSoC 6 MCU parts

Related Hardware: PSoC 6 BLE Pioneer Kit, PSoC 6 WiFi-BT Pioneer Kit, PSoC 6 WiFi-Prototyping Kit

Overview

This code example demonstrates how to configure the low-power comparator (LPComp) resource for comparing internal reference voltage and external voltage input from a GPIO. The LED is used to indicate the comparison result.

Hardware Setup

This example uses the PSoC 6 BLE Pioneer Kit's default configuration. See the kit guide to ensure the kit is configured correctly.

Note: The PSoC 6 BLE Pioneer kit and the PSoC 6 WiFi-BT Pioneer kit ship with KitProg2. ModusToolbox only works with KitProg3. Before using this code example, make sure that the kit is upgraded to KitProg3. See ModusToolbox Help > ModusToolbox IDE Documentation > User Guide; section PSoC 6 MCU KitProg Firmware Loader. If you do not upgrade, you will see an error like "unable to find CMSIS-DAP device" or "KitProg firmware is out of date".

Software Setup

None.

Operation

Follow the instructions that came with your kit to make sure the kit is connected to your PC.

1. Place a potentiometer on P5[6] to change the Vplus input voltage.
2. Import the code example into a new workspace. If you are not familiar with this process, see KBA225201.
3. Program the PSoC 6 MCU device. In the project explorer, select the **mainapp** project. In the Quick Panel, scroll to the **Launches** section and click the **Program (KitProg3)** configuration.
4. Turn the knob of the potentiometer until the Vplus input is higher than Vref.
5. Confirm that KIT_LED2 is OFF.
6. Turn the knob of the potentiometer until the Vplus input is lower than Vref.
7. Confirm that KIT_LED2 is ON.

Debugging

You can debug the example to step through the code. Use the **Debug (KitProg3)** configuration. If you are unfamiliar with how to start a debug session with ModusToolbox IDE, see KBA224621.

Design and Implementation

This code example uses one LPComp resource, one status LED, one GPIO used for the input external input voltage, and one potentiometer. The main function compares the LPComp inputs when an interrupt triggers; it updates the LED state and goes into Deep Sleep to wait for the next interrupt. The status LED shows the voltage comparison result. If the positive terminal input is higher than the negative terminal input, the LED is OFF; otherwise, it is ON.

Note: The internal reference voltage (Vref) can vary; see the device datasheet for the range.

Resources and Settings

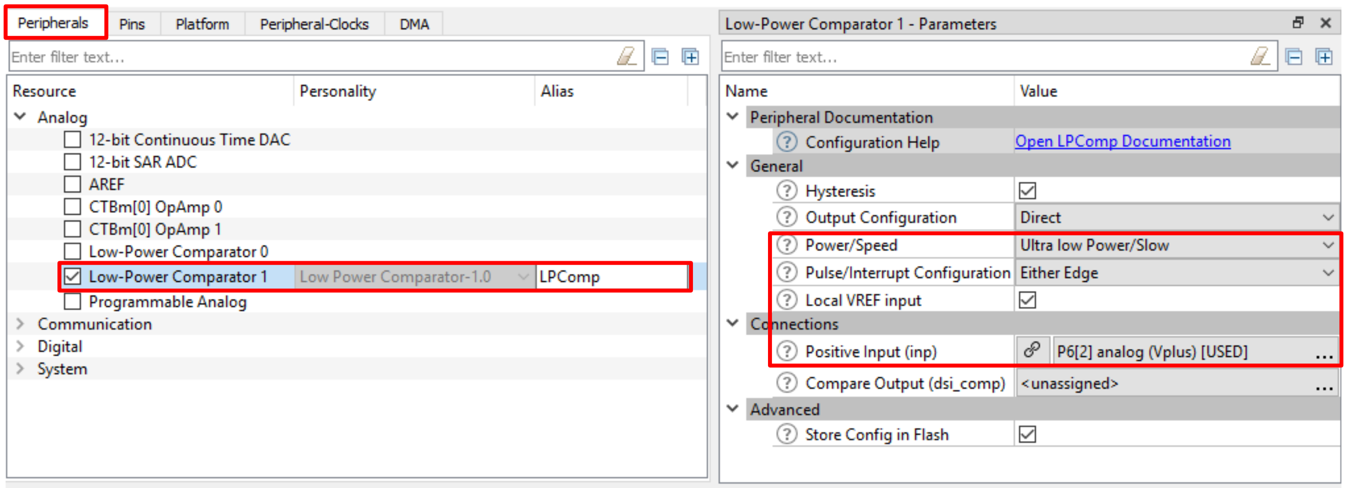
Table 1 lists the ModusToolbox resources used in this example, and how they are used in the design. For pin usage and configuration, open the **Pins** tab of the *design.modus* file.

Table 1. ModusToolbox Resources

Resource	Alias	Purpose
Low-Power Comparator	LPComp	Provide low-power voltage comparison
Digital Output Pin	KIT_LED2	Provide visual feedback
Analog Input Pin	Vplus	Provide user input

Figure 1 to Figure 3 show the non-default configuration settings for the ModusToolbox resources.

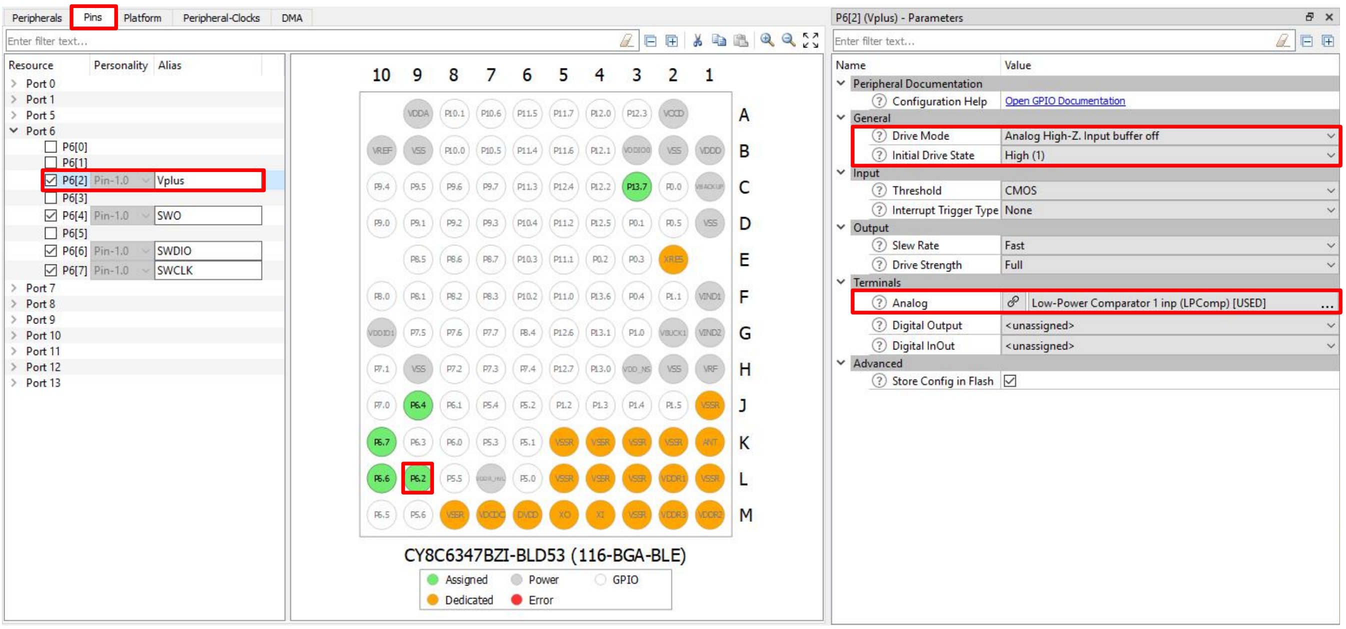
Figure 1. LPComp Configuration



Resource	Personality	Alias
Analog		
□ 12-bit Continuous Time DAC		
□ 12-bit SAR ADC		
□ AREF		
□ CTBm[0] OpAmp 0		
□ CTBm[0] OpAmp 1		
□ Low-Power Comparator 0		
☑ Low-Power Comparator 1	Low Power Comparator-1.0	LPComp
□ Programmable Analog		
Communication		
Digital		
System		

Name	Value
Peripheral Documentation	
Configuration Help	Open LPComp Documentation
General	
Hysteresis	☑
Output Configuration	Direct
Power/Speed	Ultra low Power/Slow
Pulse/Interrupt Configuration	Either Edge
Local VREF input	☑
Connections	
Positive Input (inp)	P6[2] analog (Vplus) [USED]
Compare Output (dsi_comp)	<unassigned>
Advanced	
Store Config in Flash	☑

Figure 2. GPIO Configuration for Non-Inverting Terminal



Resource	Personality	Alias
› Port 0		
› Port 1		
› Port 5		
⌄ Port 6		
□ P6[0]		
□ P6[1]		
☑ P6[2]	Pin-1.0	Vplus
□ P6[3]		
☑ P6[4]	Pin-1.0	SWO
□ P6[5]		
☑ P6[6]	Pin-1.0	SWDIO
☑ P6[7]	Pin-1.0	SWCLK
› Port 7		
› Port 8		
› Port 9		
› Port 10		
› Port 11		
› Port 12		
› Port 13		

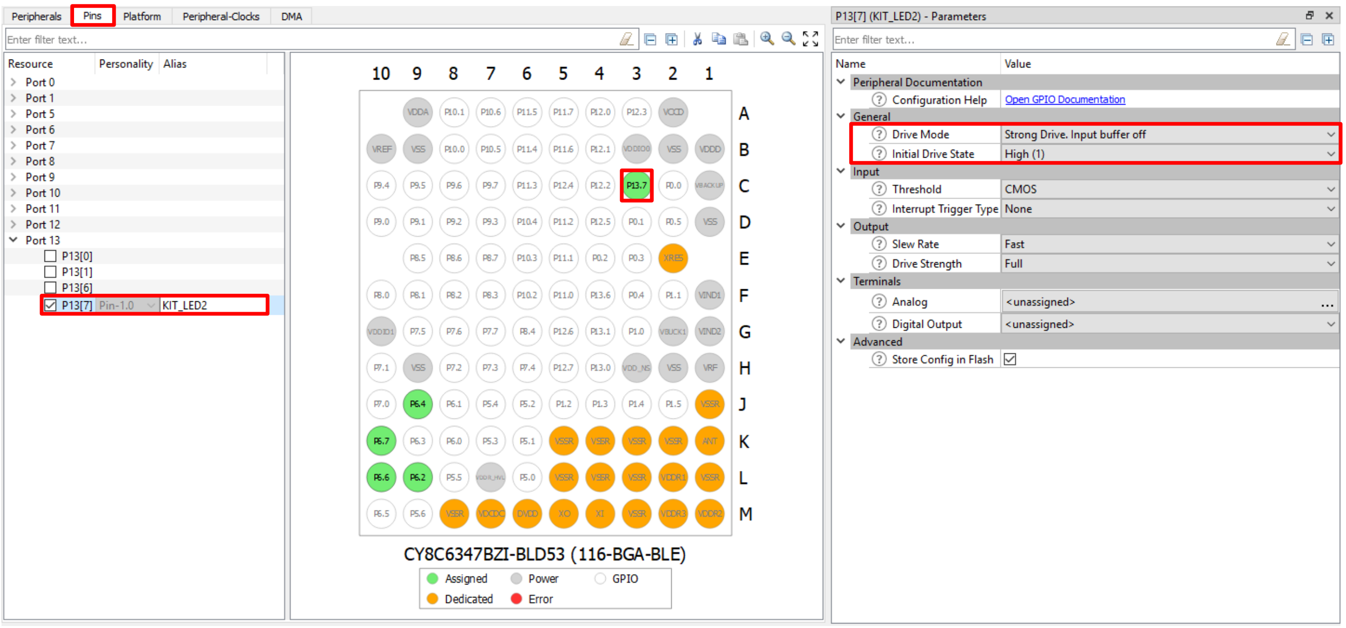
	10	9	8	7	6	5	4	3	2	1
A		VDDA	P10.1	P10.6	P11.5	P11.7	P12.0	P12.3	VCCD	
B	VREF	VSS	P10.0	P10.5	P11.4	P11.6	P12.1	VDDIO0	VSS	VDDD
C	P9.4	P9.5	P9.6	P9.7	P11.3	P12.4	P12.2	P13.7	P0.0	VBACKUP
D	P9.0	P9.1	P9.2	P9.3	P10.4	P11.2	P12.5	P0.1	P0.5	VSS
E		P8.5	P8.6	P8.7	P10.3	P11.1	P0.2	P0.3	XRES	
F	P8.0	P8.1	P8.2	P8.3	P10.2	P11.0	P13.6	P0.4	P1.1	VIND1
G	VDDIO1	P7.5	P7.6	P7.7	P8.4	P12.6	P13.1	P1.0	VBUCK1	VIND2
H	P7.1	VSS	P7.2	P7.3	P7.4	P12.7	P13.0	VDD_NS	VSS	VRF
J	P7.0	P6.4	P6.1	P5.4	P5.2	P1.2	P1.3	P1.4	P1.5	VSSR
K	P6.7	P6.3	P6.0	P5.3	P5.1	VSSR	VSSR	VSSR	VSSR	ANT
L	P6.6	P6.2	P5.5	VDDR_HV	P5.0	VSSR	VSSR	VSSR	VDDR1	VSSR
M	P6.5	P5.6	VSSR	VDCDC	DVDD	XO	XI	VSSR	VDDR3	VDDR2

CY8C6347BZI-BLD53 (116-BGA-BLE)

🟩 Assigned ● Power ○ GPIO
🟧 Dedicated 🟥 Error

Name	Value
⌄ Peripheral Documentation	
Configuration Help	Open GPIO Documentation
⌄ General	
Drive Mode	Analog High-Z. Input buffer off
Initial Drive State	High (1)
⌄ Input	
Threshold	CMOS
Interrupt Trigger Type	None
⌄ Output	
Slew Rate	Fast
Drive Strength	Full
⌄ Terminals	
Analog	Low-Power Comparator 1 inp (LPComp) [USED]
Digital Output	<unassigned>
Digital InOut	<unassigned>
⌄ Advanced	
Store Config in Flash	☑

Figure 3. GPIO Configuration for LED Pin



Resource	Personality	Alias
› Port 0		
› Port 1		
› Port 5		
› Port 6		
› Port 7		
› Port 8		
› Port 9		
› Port 10		
› Port 11		
› Port 12		
⌄ Port 13		
□ P13[0]		
□ P13[1]		
□ P13[6]		
☑ P13[7]	Pin-1.0	KIT_LED2

	10	9	8	7	6	5	4	3	2	1
A		VDDA	P10.1	P10.6	P11.5	P11.7	P12.0	P12.3	VCCD	
B	VREF	VSS	P10.0	P10.5	P11.4	P11.6	P12.1	VDDIO0	VSS	VDDD
C	P9.4	P9.5	P9.6	P9.7	P11.3	P12.4	P12.2	P13.7	P0.0	VBACKUP
D	P9.0	P9.1	P9.2	P9.3	P10.4	P11.2	P12.5	P0.1	P0.5	VSS
E		P8.5	P8.6	P8.7	P10.3	P11.1	P0.2	P0.3	XRES	
F	P8.0	P8.1	P8.2	P8.3	P10.2	P11.0	P13.6	P0.4	P1.1	VIND1
G	VDDIO1	P7.5	P7.6	P7.7	P8.4	P12.6	P13.1	P1.0	VBUCK1	VIND2
H	P7.1	VSS	P7.2	P7.3	P7.4	P12.7	P13.0	VDD_NS	VSS	VRF
J	P7.0	P6.4	P6.1	P5.4	P5.2	P1.2	P1.3	P1.4	P1.5	VSSR
K	P6.7	P6.3	P6.0	P5.3	P5.1	VSSR	VSSR	VSSR	VSSR	ANT
L	P6.6	P6.2	P5.5	VDDR_HV	P5.0	VSSR	VSSR	VSSR	VDDR1	VSSR
M	P6.5	P5.6	VSSR	VDCDC	DVDD	XO	XI	VSSR	VDDR3	VDDR2

CY8C6347BZI-BLD53 (116-BGA-BLE)

🟩 Assigned ● Power ○ GPIO
🟧 Dedicated 🟥 Error

Name	Value
⌄ Peripheral Documentation	
Configuration Help	Open GPIO Documentation
⌄ General	
Drive Mode	Strong Drive. Input buffer off
Initial Drive State	High (1)
⌄ Input	
Threshold	CMOS
Interrupt Trigger Type	None
⌄ Output	
Slew Rate	Fast
Drive Strength	Full
⌄ Terminals	
Analog	<unassigned>
Digital Output	<unassigned>
⌄ Advanced	
Store Config in Flash	☑

Reusing this Example

This example is designed for the supported kits. To port the design to a different PSoC 6 MCU device, right-click an application project and choose **Change Device**. If changing to a different kit, you may need to reassign pins.

Table 2. Device and Pin Mapping Table across PSoC 6 MCU Kits

Kit Name	Device Used	LED	Vplus
CY8CKIT-062-WiFi-BT	CY8C6247BZI-D54	P13[7]	P6[2]
CY8CKIT-062-BLE	CY8C6347BZI-BLD53	P13[7]	P6[2]
CY8CPROTO-062-4343W	CY8C624ABZI-D44	P13[7]	P6[2]

In some cases, a resource used by a code example (for example, an IP block) is not supported on another device. In that case the example will not work. If you build the code targeted at such a device, you will get errors. See the device datasheet for information on what a particular device supports.

Related Documents

For a comprehensive list of PSoC 6 MCU resources, see KBA223067 in the Cypress community.

Application Notes	
AN210781 – Getting Started with PSoC 6 MCU with Bluetooth Low Energy (BLE) Connectivity	Describes PSoC 6 MCU devices with BLE connectivity and how to build your first PSoC Creator™ project
AN221774 – Getting Started with PSoC 6 MCU	Describes PSoC 6 MCU devices and how to build your first PSoC Creator™ project
AN215656 – PSoC 6 MCU: Dual-CPU System Design	Describes the dual-CPU architecture in PSoC 6 MCU devices, and shows how to build a simple dual-CPU design
Code Examples	
CE218129 - PSoC 6 MCU Wake up from Hibernate using a Low-Power Comparator	
Visit the Cypress GitHub site for a comprehensive collection of code examples using ModusToolbox IDE	
Device Documentation	
PSoC 6 MCU: PSoC 63 with BLE Datasheet	PSoC 6 MCU: PSoC 63 with BLE Architecture Technical Reference Manual
Development Kit Documentation	
CY8CKIT-062-BLE PSoC 6 BLE Pioneer Kit	
CY8CKIT-062-WiFi-BT PSoC 6 WiFi-BT Pioneer Kit	
CY8CPROTO-062-4343W PSoC 6 Wi-Fi BT Prototyping Kit	
Tool Documentation	
ModusToolbox	The Cypress IDE for IoT designers

Cypress Resources

Cypress provides a wealth of data at www.cypress.com to help you to select the right device, and quickly and effectively integrate the device into your design.

For the PSoC 6 MCU devices, see KBA223067 in the Cypress community for a comprehensive list of PSoC 6 MCU resources.

Document History

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Document Number: 002-24749

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	6371312	AJYA	11/13/2018	New code example
*A	6489123	AJYA	01/19/2019	Updated code example to ModusToolbox 1.1

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