

EG 211 Computer Architecture Assignment – 1:

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> The program we chose is sorting in ascending order.

> Algorithm in C++ (SELECTION SORT)

```
void selectionSort(int arr[], int n)
{
    int i, j, min_idx;
    for (i = 0; i < n - 1; i++) {
        min_idx = i;
        for (j = i + 1; j < n; j++){
            if (arr[j] < arr[min_idx])
                min_idx = j;
        }
        if (min_idx != i)
            swap(arr[min_idx], arr[i]);
    }
}
```

MARS COMPILER OUTPUT:

```
Enter No. of integers to be taken as input: 8
Enter starting address of inputs(in decimal format): 268501216
Enter starting address of outputs (in decimal format): 268501280
Enter the integer: 12
Enter the integer: 14
Enter the integer: 2
Enter the integer: 7
Enter the integer: 5
Enter the integer: 11
Enter the integer: 4
Enter the integer: 8
2
4
5
7
8
11
12
14

-- program is finished running --
```

- **THIS IS A SCREENSHOT OF THE COMPILATION OF SORTING “EIGHT” INTEGERS INTO ACSENDING ORDER.**

Explanation for sorting algorithm in Mips assembly program language:

1. Copying part:

- \$t4 and \$t5 stores address locations of input and output memory locations from \$t2 and \$t3 respectively.
- Loop2 runs from 0 to n and copies input values from input memory location to output memory location.

2. Sorting part:

- 1. Initialization: - \$s0 is set to 0 to act as an iterator i for the outerloop. \$s1 is set to 1 act as iterator j i.e. iterator for innerloop. \$t7 is set to n - 1, where n is the total number of integers in the array.

\$s5 is initialized to base address of the array \$t3 and is incremented such as to match address pointed by i.

\$t6 is initialized to base address of the array \$s5 and is incremented such as to match address pointed by j.

\$t8 is initialized to base address of the array \$s5 and is incremented such as to match address pointed by min_ind.

- 2. Outer Loop (Mainloop1): - It compares the value in \$s0 (initialized as the index i) with \$t7 (n-1) to determine if the outer loop should continue. - If the condition is met, it proceeds to the inner loop to find the minimum element in the unsorted portion of the array.

- 3. Inner Loop (Loop2): - It uses \$s1 as an iterator (`j`) to traverse the unsorted portion of the array. - Compares the elements at the indices Arr[min_ind] [\$t4] and Arr[j] [\$t5] and updates the index of the minimum element min_ind [\$t9] to [\$s0] if a smaller element is found.
- 4. Cycleloop: - It iterates address from \$t3 to location of new min_ind (by iterating \$t9 number of times) and stores address location in \$s4 ,this locations is later used to in swap.
- 5. Swap: - If a smaller element is found in the inner loop, a swap operation is performed between new Arr[min_ind] “[\$s4]” and Arr[i] “[\$s6]” to put it in the sorted position of the unsorted array.
- 6. Loop Control and Incrementing: - After each iteration of the inner loop, the loop control and index variables (\$t6, \$s1) are updated accordingly. - The program jumps back to outerloop until the entire array is sorted in outerloop [\$t8, \$s0, \$s5] are updated accordingly to maintain addresses of each variable accordingly in the registers.
- 7. sorting_end: - The program exits when the outer loop completes (endouterloop) as all elements are sorted and stored in the memory location started from “\$t3”.

In summary, this MIPS assembly code uses nested loops to implement the Selection Sort algorithm, which repeatedly finds

the minimum element in the unsorted part of the array and swaps with the first unsorted element. This process continues until the entire array is sorted.

Explanation for the Assembler:

1. Defined dictionaries for R-format and I-format and J-format instructions separately. Another dictionary for registers and labels.
2. Implements an assembler that takes an instruction and generates 32-bit machine code for the respective instruction.
3. Reads a MIPS assembly file(mipassembler.asm), processes it and extracts labels and instructions.
4. I stored the labels and their addresses for instructions beq and j instructions. The addresses of those labels are stored in a dictionary register-numbers along with the registers.

Brief overview of how the code works:

- After defining dictionaries there is a function that converts decimal to binary and it converts the decimal input provided into required no of bits in binary.

- For the instructions such as beq and jump the addresses of labels are already stored in the dictionary.
- Now comes the if, elseif conditions that checks the instruction specifically. That is whether it's Addi or beq or j or Subi or slt or etc.... and prints the required 32-bit machine code for each instruction in mipassembler.asm.

```
mipassembler.asm - Visual Studio Code
File Edit Selection View Go Run Terminal Help
PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL PORTS
mannepalli@mannepalli-hp-pavilion-laptop-15-eg2xxx:~/Desktop/computer architecture$ python3 assembler.py
00100000000100000000000000000000
001000010100110000000000000000
001000010110110100000000000000
0001001000001001000000000000110
100011011000111100000000000000
101011011110110100000000000000
0010000110001100000000000000100
0010000110101101000000000000100
0010001000010000000000000000001
000010000001000000000000000011
001000000001000000000000000000
001000000000001000000000000001
000000100100001011110000100010
001000000001101000000000000000
001000010111010100000000000000
000100100000111100000000001101
001000100001000100000000000001
001000101010111000000000000100
001000100001100100000000000000
001000101011100000000000000000
001000010111010000000000000000
100011101011011000000000000000
100011101011000000000000000000
0001001000101001000000000001000
100011011100110100000000000000
0000000110101100100100000101010
00010010010000000000000000010
001000100011100100000000000000
001000011010110000000000000000
001000011100111000000000000100
001000100011000100000000000001
00001000000100000000000001011
001000000001001100000000000000
000100100111100100000000000011
001000101001010000000000000100
```

The bottom most line here and the topmost line in the below screenshot are same

```
0010001010010100000000000000100
0010001001110011000000000000001
0000100000100000000000000010001
000100110011000000000000000011
1000111010010111000000000000000
101011101010100000000000000000
1010111011110101000000000000000
0010001100011000000000000000100
0010001000010000000000000000001
0010001010110101000000000000100
000010000010000000000000001111
mannepalli@mannepalli-hp-pavilion-laptop-15-eg2xxx:~/Desktop/computer architecture$
```

The above pasted screenshots are our assembler's output.

Now we will be pasting the screenshot of running our code in MARS (MIPS Assembler and Runtime Simulator). There will be 45 lines in both of our outputs. But the no of instructions is 44. This is happening due to the split of Subi instruction which is splitted into Addi and sub.

```
0010000000010000000000000000000
0010000101001100000000000000000
0010000101101101000000000000000
0001001000001001000000000000110
1000110110001111000000000000000
1010110110101111000000000000000
0010000110001100000000000000100
0010000110101101000000000000100
0010001000010000000000000000001
000010000010000000000000000011
0010000000100000000000000000000
0010000000000010000000000000001
00000001001000010111100000100010
0010000000011010000000000000000
0010000101110101000000000000000
00010010000111100000000000001101
0010001000010001000000000000001
0010001010101110000000000000100
0010001000011001000000000000000
0010001010111000000000000000000
0010000101110100000000000000000
1000111010101100000000000000000
1000111010101100000000000000000
00010010001010010000000000001000
1000110111001101000000000000000
00000001101011001001000000101010
000100100100000000000000000010
0010001000111001000000000000000
0010000110101100000000000000000
0010000111001110000000000000100
0010001000110001000000000000001
0000100000100000000000000010111
0010000000100110000000000000000
000100100111100100000000000011
0010001010010100000000000000100
0010001001110011000000000000001
00001000001000000000000010001
000100110011000000000000000011
1000111010010111000000000000000
1010111010010110000000000000000
1010111010110111000000000000000
0010001100011000000000000000100
0010001000010000000000000000001
0010001010110101000000000000100
000010000010000000000000001111
~
~
~
~
```