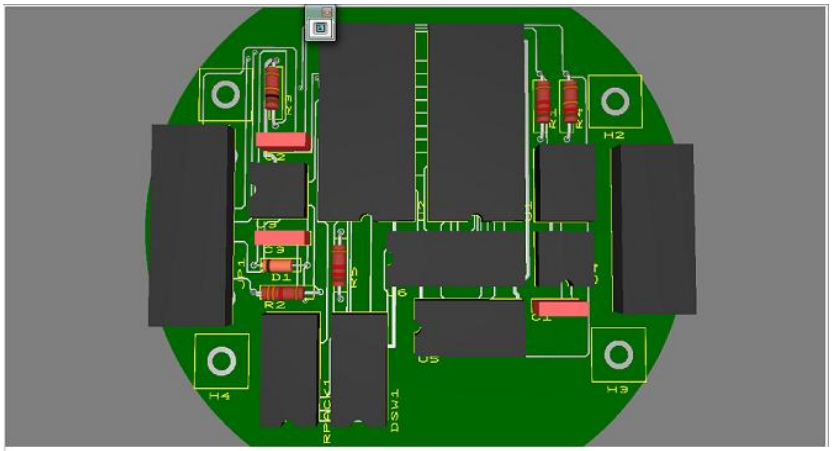

Department of Computer Science

Lab Manual for

Digital Logic & Design: **CEN-201 4(3+1)**

B.S (CS)

Session: Fall 2022

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Table of Content

Student's ID: **Laboratory Exercise No: 1** Student's Name:

Objective: To get familiar with Analog & Digital Training System (M21-7000).

Goal: In this experiment students will develop practical understanding with different functions of Analog & Digital Training System (M21-7000).

Required Tools/Equipment:-

1) Analog & Digital Training System (M21-7000).
2) Connecting Wires (Jumpers).
3) NOT Gates IC (74HC04).

Introduction:-

S.M.I.U Electronic Laboratory equipped with Analog & Digital Training System (M21-7000). This training system has almost all essential functions which are required for both Analog and Digital experiments. Because this training system will be used throughout **Digital Logic and Design** subject's practical work, it need to be examined thoroughly.

This training system has a power switch 

to enable/disable all functions. It contains following main sections:

Solderless Breadboard:

This training system has a breadboard which can be removed from its place if required. This breadboard has 2820 connecting points (holes). It has horizontal, vertical and separation region.

Function Generator:

This trainer has a section of Function Generator. Function Generator is a device which is used to generate different ac voltage wave foam with selected amplitude and frequency. It has 3 connecting holes to connect circuit input. Output and GND are used to connect selected frequency and amplitude output waveform to any circuit input. TTL and GND is used to connect fixed 4V (p-p) TTL mode voltage waveform to any circuit input.

***How to select frequency*:** To select desired frequency, rotate "Frequency Range" knob to select desired frequency multiplier "x1, x10, x100, x1k and x10k" and select suitable "Frequency" by rotating knob from 1 to 10.

Example: To select 2.5 KHz frequency signal from function generator,

Rotate "Frequency Range" multiplier knob to select **x1k** and "Frequency" knob to **2.5**. So frequency will be $2.5 \times 1kHz = 2.5\ kHz$

***How to select amplitude*:** To select desired amplitude of voltage waveform, rotate "Amplitude" knob to suitable position from 0 to 10.

Example: To select amplitude of output waveform to 5 Volts (p-p), rotate "Amplitude" knob to 5.

How to select function of waveform: To select desired function of output waveform, rotate "Function" knob to one of the three given functions (Triangular, Sinusoidal or Square).

Dc Power Supply:

Analog & Digital Training System (M21-7000) has separate DC power supply section which provides both variable and fixed DC voltage levels. It has total 6 connecting terminals. Three terminals +5V, GND and -5V to select +5V/-5V fixed voltage and three terminals 0~+15V, GND and 0~-15V to select variable voltage range from 0 to +15V and 0 to -15V.

***How to select +5 fixed voltage*:** To provide +5V fixed dc voltage, connect one jumper to +5V terminal and second to GND terminal to connect input of any circuit which requires +5V dc voltage**.**

***How to select -5 fixed voltage*:** To provide -5V fixed dc voltage, connect one jumper to -5V terminal and second to GND terminal to connect input of any circuit which requires -5V dc voltage**.**

***How to select any voltage from 0 to +15 volts*:** To select any voltage level from 0 to +15V, connect one jumper to terminal labeled as 0~+15V which will serve as positive terminal of DC supply and connect second jumper to terminal labeled as GND which will serve as ground terminal. Rotate knob which is labeled as +V to select desired voltage level.

***How to select any voltage from 0 to -15 volts*:** To select any voltage level from 0 to -15V, connect one jumper to terminal labeled as 0~-15V which will serve as negative terminal of DC supply and connect second jumper to terminal labeled as GND which will serve as ground terminal. Rotate knob which is labeled as -V to select desired voltage level.

Potentiometer (Variable Resistor):

There are two potentiometers available in this section. One range from 0~100KΩ and second range from 0~1KΩ. Each potentiometer has three terminals and one rotating knob.

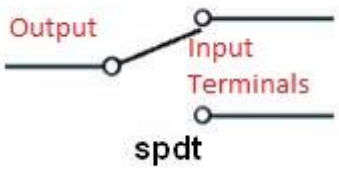
How to select any resistance value from 0 to 100KΩ: Connect three jumpers to terminal 1, 2 and 3 respectively. Conventional current enters in Terminal 1 and leaves from adjustable terminal 2 and 3. When rotating dial at 0, adjustable terminal 2 coincides with the terminal 1, all current passes through terminal 2 hence potentiometer offer 0Ω resistance. When rotating dial at 10, adjustable terminal 2 coincides with the terminal 3, all current passes through terminal 3 hence potentiometer offer 100KΩ resistance. When rotating dial position between 0 and 10, current passes through terminal 2 and 3 hence potentiometer offer resistance R> 0 <100KΩ.

How to select any resistance value from 0 to 1KΩ: Connect three jumpers to terminal 4, 5 and 6 respectively. Conventional current enters in Terminal 4 and leaves from adjustable terminal

5 and fixed terminal 6. When rotating dial at 0, adjustable terminal 5 coincides with the terminal 4, all current passes through terminal 5 hence potentiometer offer 0Ω resistance. When rotating dial at 10, adjustable terminal 5 coincides with the terminal 6, all current passes through terminal 6 hence potentiometer offer 1KΩ resistance. When rotating dial position between 0 and 10, current passes through terminal 5 and 6 hence potentiometer offer resistance R> 0 <1KΩ.

Toggle Switches:

There are 16 toggle switches from SW0 to SW15 and their relevant connecting holes for output terminals. These switches are used to provide Boolean input (0 or 1) to the digital logic components/circuit. There are three terminals of toggle switch. Two terminals are used for inputs and one terminal is used for output. One input terminal is internally connected with positive terminal of DC supply and second terminal is internally connected with ground/very low voltage. When switch position is upward, output terminal is connected with first input terminal and logical 1 appears on the connecting hole/terminal. When switch position is downward, output is connected with second input terminal and logical 0 appears on the connecting hole/terminal.



LED Data Display:

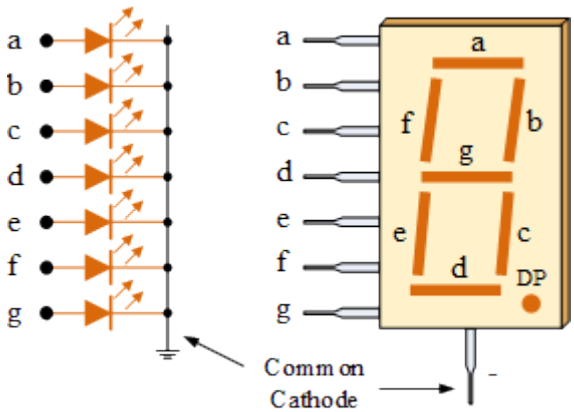
This section contain 16 LED's and their relevant connecting holes from 0 to 15. Anode side of all LED's are connected to their relevant connecting holes and Cathode is internally connected to ground. When no input or logical 0 is provided to the LED input, it becomes reverse biased and remain turned off. When logical 1 is provided to the LED input, it becomes forward biased and turned on.

Pulse Switches:

There are two pulse switches A and B with four output terminals A, $\overline{A}$, B and $\overline{B}$. Two terminals for each pulse switch. When Switch A is pressed, terminal A connecting hole provides logic HIGH output. When Switch A is released, terminal A connecting hole provides logic LOW output. Same applies for Switch B and its output terminals.

BCD Displays:

This section contains two Common Cathode 7 Segment display units and four connecting holes as 4 input terminals for each 7 Segment Display unit. Two 7 Segment Display Decoder driver IC's are internally connected to each display unit.



Following is the output pattern of 7 Segment Display unit's individual LEDs with the relevant BCD inputs.

Decimal Or Function	BCD Inputs D	C	B	A	Outputs a	b	c	d	e	f	g
0	L	L	L	L	H	H	H	H	H	H	L
1	L	L	L	H	L	H	H	L	L	L	L
2	L	L	H	L	H	H	L	H	H	L	H
3	L	L	H	H	H	H	H	H	L	L	H
4	L	H	L	L	L	H	H	L	L	H	H
5	L	H	L	H	H	L	H	H	L	H	H
6	L	H	H	L	L	L	H	H	H	H	H
7	L	H	H	H	H	H	H	L	L	L	L
8	H	L	L	L	H	H	H	H	H	H	H
9	H	L	L	H	H	H	H	L	L	H	H
10	H	L	H	L	L	L	L	H	H	L	H
11	H	L	H	H	L	L	H	H	L	L	H
12	H	H	L	L	L	H	L	L	L	H	H
13	H	H	L	H	H	L	L	H	L	H	H
14	H	H	H	L	L	L	L	H	H	H	H
15	H	H	H	H	L	L	L	L	L	L	L

There are two other sections in M21-7000 which are not covered here.

Answer the following questions:-

Q # 1. Construct any analog or digital circuit and use M21-7000 trainer.

Reference:

[1] http://www.mcpsh.com/M21-7000.html.

Student's ID: **Laboratory Exercise No: 2** Student's Name:

Objective: To familiarize with basic NOT Gate.

Goal: In this experiment students will implement basic Logical NOT gate practically and will observe its function.

Required Tools/Equipment:

1) Analog & Digital Training System (M21-7000).
2) Connecting Wires.
3) I.C (NOT =74HC04).
4) NPN Transistor (BC 548)
5) Resistors (1KΩ and 33KΩ)

Theory:

A logic gate is an electronic circuit which makes different binary decision with respect to binary inputs. A logic gate can have one or multiple inputs but only has single output. Binary 1 is taken as Logic HIGH and binary 0 as Logic LOW. Logic gate activates only for specific input combinations. If same input combination is applied to the inputs of different logic gates, output might be 1 or 0 depends on Logic gate function. Two different logic gates might give same output for same input combinations because there are only two logic levels possible in digital electronics (i-e Logic LOW and Logic HIGH).

Logic gates are implemented through Diodes or Transistors as discrete circuit but they are also implemented directly in the form of integrated circuit (I.C). Logic gates function can also be implemented with switches, electromagnetic relays, solenoid vales, pneumatic relays and mechanical components.

Basic Logic Gates:

1) NOT.
2) AND.
3) OR.

NOT Gate:

NOT gate is the simplest logic gate among all basic logic gates. It is also referred as "Inverting Buffer" or "Digital Inverter" or even sometimes just as "Inverter" when discussing digital circuit/logic. NOT gate is the only Logic gate which requires one logical input. Its function is like a unary operator. When a single binary 0 or Logic LOW is applied to its input, it provides binary 1 or logic HIGH on its output. When a single binary 1 or logic HIGH is applied to its input, it provides binary 0 or logic LOW on its output. Clearly it inverts or complement whatever logic level is applied to its input. If A is input and Z is output then $Z = A'$. (') apostrophe character indicate inverting operation.

Symbol:-

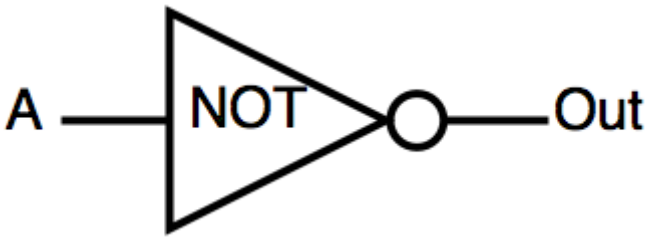
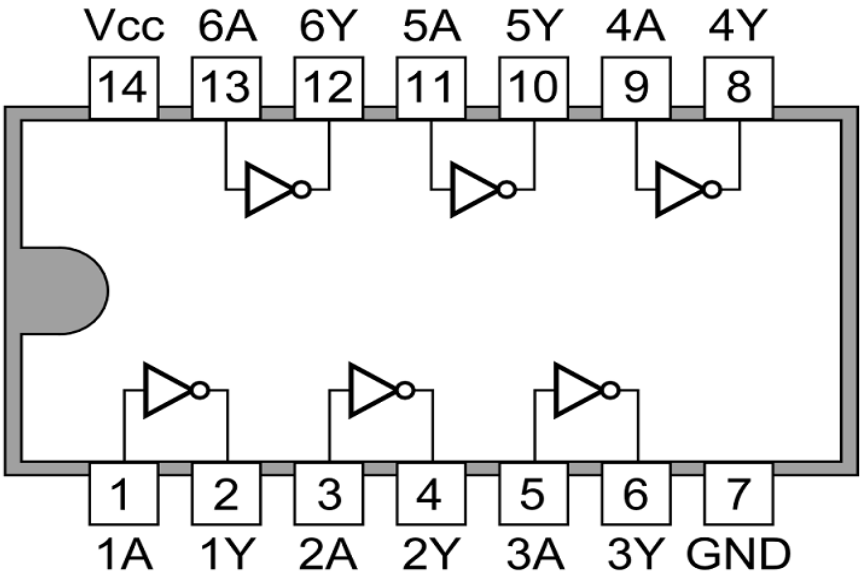


Fig: 2.1

Pin Configuration:-



74HC04 Pin Configuration Fig: 2.2

Procedure:

1) Set 5 volts DC on Analog & Digital Training System (M21-7000) and turn it off.
2) Connect one jumper wire from +V outlet of M21-7000 to Pin No. 14 of Hex inverter IC (74HC04).
3) Connect one jumper wire from GND outlet of M21-7000 to pin No. 7.
4) Connect one jumper from one of toggle switch outlet of M21-7000 to any input of one NOT Gate. Set toggle switch to OFF state (downward). Designate this input as **A.**
5) Connect one jumper from output of specified NOT gate to the input of one LED inlet on M21-7000. Designate this output as **Z.**
6) Turn M21-7000 power on.
7) Use toggle switch to apply logic to input **A** as shown in table 2.1 and note down Output **Z.**

Input (A)	Output (Z)
0 (LOW)	
1 (HIGH)	

Table: 2.1

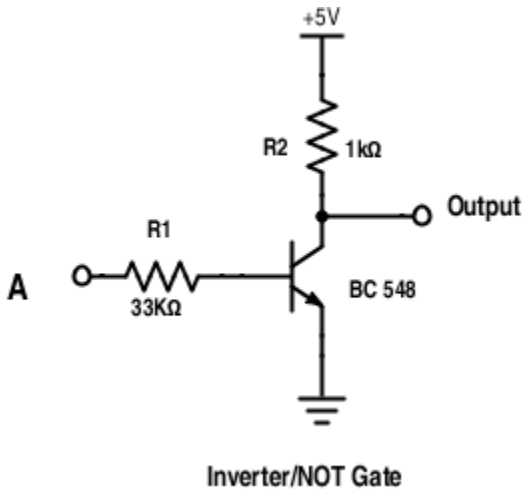


Fig 2.3 NOT Gate with Discrete Components

Answer the following questions:-

Q # 1. Is this possible to apply more than one inputs to NOT gate? Justify your answer.

Answer:

Student's ID: **Laboratory Exercise No: 3** Student's Name:

Objective: To familiarize with basic AND Gate.

Goal: In this experiment students will implement basic Logical AND gate practically and will observe its function.

Required Tools/Equipment:

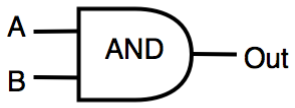
6) Analog & Digital Training System (M21-7000).
7) Connecting Wires.
8) I.C (AND =74HC08).
9) NPN Transistor (BC 548)
10) Resistors (2.2KΩ and 4.7KΩ)

Theory:
AND Gate:

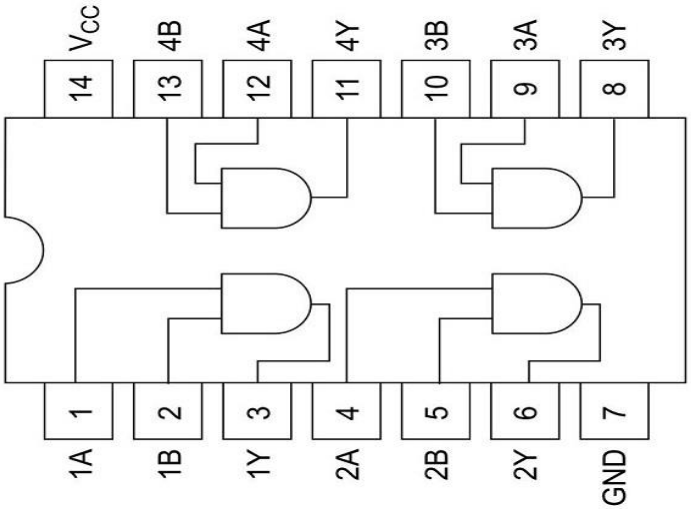
AND Gate provides binary 1 (HIGH) only when binary 1 (HIGH) is applied to all its inputs. In other words AND Gate provides binary 0 (LOW) if binary 0 (LOW) is applied to any of its inputs. If A and B are two inputs to AND Gate and Z is its output then $Z = A.B$

Dot operator is used to indicate AND operation between two or more than two logic inputs. Sometimes dot operator is omitted.

Symbol:-



Pin Configuration:-



Procedure:-

1) Set 5 volts DC on Analog & Digital Training System (M21-7000) and turn it off.
2) Connect one jumper wire from +V outlet of M21-7000 to Pin No. 14 of Quad AND Gate IC (74HC08).
3) Connect one jumper wire from GND outlet of M21-7000 to pin No. 7.
4) Connect one jumper from one of toggle switch outlet of M21-7000 to 1st input of one AND Gate. Set toggle switch to OFF state (downward). Designate this input as **A.**
5) Connect one jumper from one of toggle switch outlet of M21-7000 to 2nd input of AND Gate used in step No. 4. Set relevant toggle switch to OFF state (downward). Designate this input as **B.**
6) Connect one jumper from output of above specified AND gate to the input of one LED inlet on M21-7000.
7) Turn M21-7000 power on.
8) Use toggle switches to apply logics to input **A** and **B** as shown in table 3.1 and note down Output **Z.**

Truth Table:-

Input (A)	Input (B)	Output (Z)
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 3.1

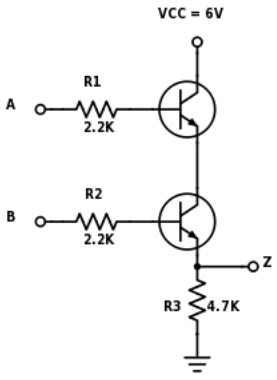


Fig: 3.3 AND Gate with discrete Components

Answer the following questions:-

Q # 1. What do you understand by "&" character mentioned with AND gate symbol?

Answer:

Student's ID: **Laboratory Exercise No: 4** Student's Name:

Objective: To familiarize with basic logic OR gate.

Goal: In this experiment students will implement basic Logic OR Gate practically and will observe its function.

Required Tools/Equipment:-

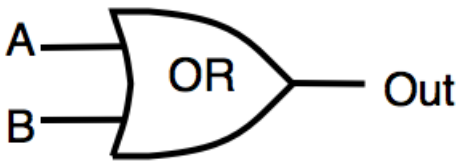
4) Analog & Digital Training System (M21-7000)
5) Connecting Wires (Jumpers)
6) Logic OR Gate IC (74HC32)
7) NPN Transistor (BC 548)
8) Resistors (2.2KΩ and 4.7KΩ)

Theory:-

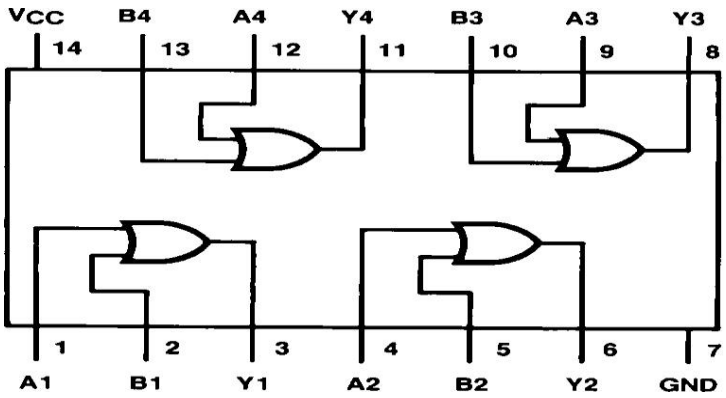
OR Gate:-

OR Gate provides binary 0 (LOW) only when binary 0 (LOW) is applied to all its input. In other words OR Gate provides binary 1 (HIGH) whenever binary 1 (HIGH) is applied to any of its input. If A and B are two inputs to OR Gate and Z is its output then $Z = A + B$. Plus sign '+' is used to indicate OR operation between two or more than two logic inputs. It is **never** omitted.

Symbol:-



Pin Configuration:-



Procedure:-

1) Set 5 volts DC on Analog & Digital Training System (M21-7000) and turn it off.
2) Connect one jumper wire from +V outlet of M21-7000 to Pin No. 14 of Quad OR Gate IC (74HC32).
3) Connect one jumper wire from GND outlet of M21-7000 to pin No. 7.
4) Connect one jumper from one of toggle switch outlet of M21-7000 to 1st input of one OR Gate. Set toggle switch to OFF state (downward). Designate this input as **A.**
5) Connect one jumper from one of toggle switch outlet of M21-7000 to 2nd input of OR Gate used in step No. 4. Set relevant toggle switch to OFF state (downward). Designate this input as **B.**
6) Connect one jumper from output of above specified OR gate to the input of one LED inlet on M21-7000.
7) Turn M21-7000 power on.
8) Use toggle switches to apply logics to input **A** and **B** as shown in table 4.1 and note down Output **Z.**

Input (A)	**Input (B)**	**Output (Z)**
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 4.1

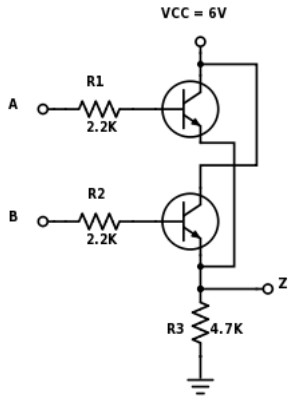


Fig: 4.3 OR Gate with discrete Components

Answer the following questions:-

Q # 1. What do you understand by " ≥1 " character mentioned with OR gate symbol?

Answer:

Student's ID: **Laboratory Exercise No: 5** Student's Name:

Objective: To familiarize with basic logic NOR gate.

Goal: In this experiment students will implement basic Logic NOR Gate practically and will observe its function.

Required Tools/Equipment:-

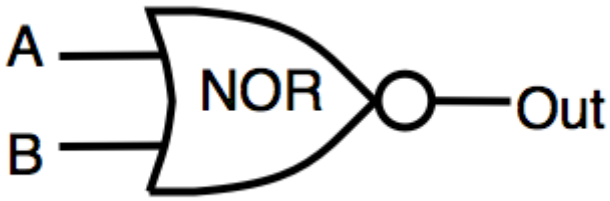
9) Analog & Digital Training System (M21-7000).
10) Connecting Wires (Jumpers).
11) Logic NOR Gate IC (74LS02).
12) NPN Transistor (BC 548)
13) Resistor (2.2KΩ)

Theory:-

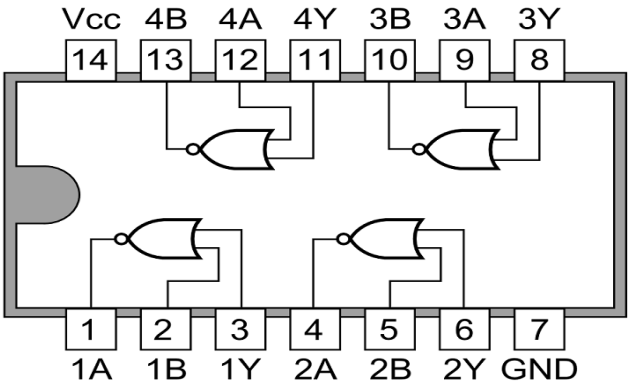
NOR:-

NOR Gate provides binary 1 (HIGH) only when binary 0 (LOW) is applied to all its input. In other words, NOR Gate provides binary 0 (LOW) whenever binary 1 (HIGH) is applied to any of its input. This Logic Gate can also be implemented with OR gate and NOT gate by connecting OR gate output to NOT gate input. In this condition, Inputs will be applied to AND gate input pins and output will be taken at NOT gate output pin. If A and B are two inputs to NOR Gate and Z is its output then $Z = (A + B)'$.

Symbol:-



Pin Configuration:-



Procedure:-

1) Set 5 volts DC on Analog & Digital Training System (M21-7000) and turn it off.
2) Connect one jumper wire from +V outlet of M21-7000 to Pin No. 14 of Quad NOR Gate IC (74LS02).
3) Connect one jumper wire from GND outlet of M21-7000 to pin No. 7.
4) Connect one jumper from one of toggle switch outlet of M21-7000 to 1st input of one NOR Gate. Set toggle switch to OFF state (downward). Designate this input as **A.**
5) Connect one jumper from one of toggle switch outlet of M21-7000 to 2nd input of NOR Gate used in step No. 4. Set relevant toggle switch to OFF state (downward). Designate this input as **B.**
6) Connect one jumper from output of above specified NOR gate to the input of one LED inlet on M21-7000.
7) Turn M21-7000 power on.
8) Use toggle switches to apply logics to input **A** and **B** as shown in table 5.1 and note down Output **Z.**

Input (A)	Input (B)	Output (Z)
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 5.1

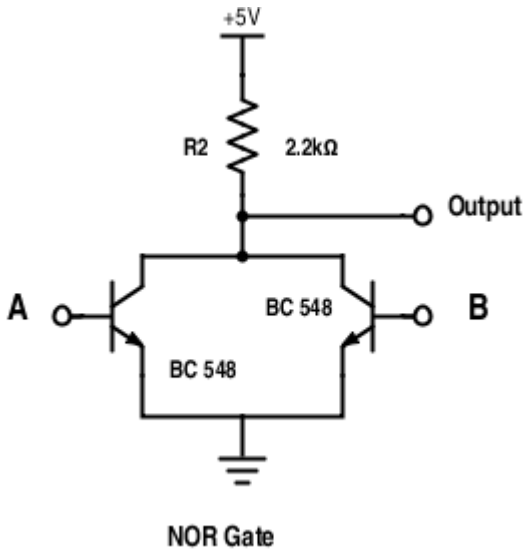


Fig: 5.3 NOR Gate with discrete Components

Answer the following questions:-

Q # 1. Describe working principle of NOR logic gate in words?

Answer:

Student's ID: **Laboratory Exercise No: 6** Student's Name:

Objective: To familiarize with basic logic NAND gate.

Goal: In this experiment students will implement basic Logic NAND Gate practically and will observe its function.

Required Tools/Equipment:-

14) Analog & Digital Training System (M21-7000).
15) Connecting Wires (Jumpers).
16) Logic NAND Gate IC (74HC00).

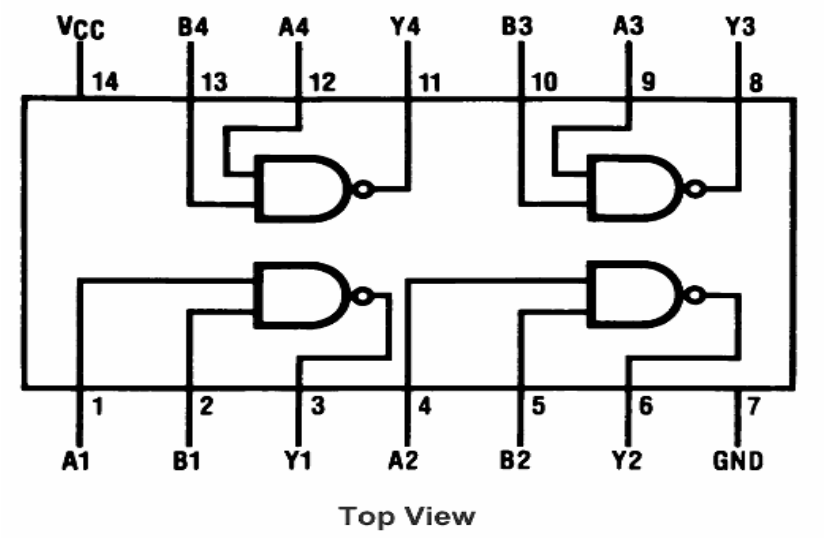
Theory:-

NAND:-

NAND Gate provides binary 0 (LOW) only when binary 1 (HIGH) is applied to all its inputs. In other words NAND Gate provides binary 1 (HIGH) if binary 0 (LOW) is applied to any of its inputs. This Logic Gate can be implemented with AND gate and NOT gate by connecting AND gate output to NOT gate input. In this condition, Inputs will be applied to AND gate input pins and output will be taken at NOT gate output pin. If A and B are two inputs to NAND Gate and Z is its output then $Z = (A.B)'$.

Symbol:-

Pin Configuration:-



Top View

Procedure:-

1) Set 5 volts DC on Analog & Digital Training System (M21-7000) and turn it off.
2) Connect one jumper wire from +V outlet of M21-7000 to Pin No. 14 of Quad NAND Gate IC (74HC00).
3) Connect one jumper wire from GND outlet of M21-7000 to pin No. 7.
4) Connect one jumper from one of toggle switch outlet of M21-7000 to 1st input of one NAND Gate. Set toggle switch to OFF state (downward). Designate this input as **A.**
5) Connect one jumper from one of toggle switch outlet of M21-7000 to 2nd input of NAND Gate used in step No. 4. Set relevant toggle switch to OFF state (downward). Designate this input as **B.**
6) Connect one jumper from output of above specified NAND gate to the input of one LED inlet on M21-7000.
7) Turn M21-7000 power on.
8) Use toggle switches to apply logics to input **A** and **B** as shown in table 6.1 and note down Output **Z.**

Input (A)	Input (B)	Output (Z)
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 6.1

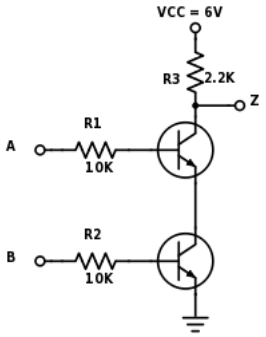


Fig: 6.3 NAND Gate with discrete Components

Answer the following questions:-

Q # 1. How many logic gates are integrated in 74HC00?

Answer:

Student's ID: **Laboratory Exercise No: 7** Student's Name:

Objective: To familiarize with basic logic XOR gate.

Goal: In this experiment students will implement basic Logic XOR Gate practically and will observe its function.

Required Tools/Equipment:-

17) Analog & Digital Training System (M21-7000).
18) Connecting Wires (Jumpers).
19) Logic XOR Gate IC (CD4070).

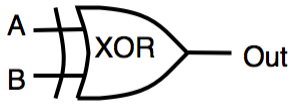
Theory:-

XOR:-

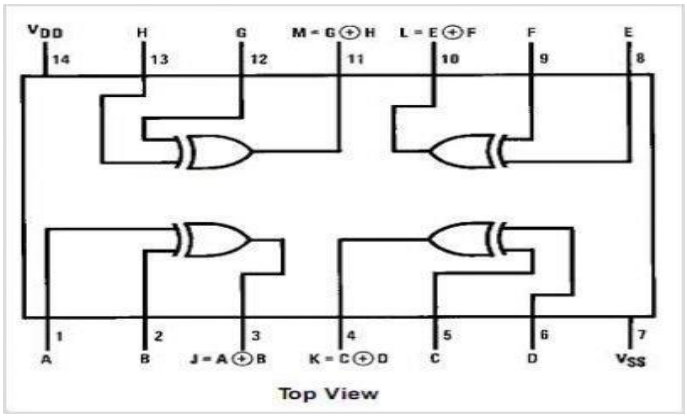
XOR Gate provides binary 1 (HIGH) only when not same logic levels are applied to its input (i-e 0 (LOW) is applied to one input and 1 (HIGH) is applied to second input). In other words, XOR Gate provides binary 0 (LOW) whenever same logic levels are applied to its input (i-e 0 (LOW) or 1 (HIGH) is applied to both inputs). This Logic Gate can also be implemented with one AND, NAND and OR gate by connecting one input pin of OR gate and NAND gate to one common junction, this junction is one input of XOR gate. By connecting second input pin of OR gate and NAND gate to second common junction, this is second input of XOR gate. Connecting these OR gate and NAND outputs to AND gate inputs, Output of this AND gate will provide XOR output. If A and B are two inputs to XOR Gate and Z is its output then $Z = A \oplus B = A'.B + A.B'$.

$\oplus$ Sign express Exclusive OR function between A and B.

Symbol:-



Pin Configuration:-



Procedure:-

1) Set 5 volts DC on Analog & Digital Training System (M21-7000) and turn it off.
2) Connect one jumper wire from +V outlet of M21-7000 to Pin No. 14 of Quad XOR Gate IC (CD4070).
3) Connect one jumper wire from GND outlet of M21-7000 to pin No. 7.
4) Connect one jumper from one of toggle switch outlet of M21-7000 to 1st input of one XOR Gate. Set toggle switch to OFF state (downward). Designate this input as **A.**
5) Connect one jumper from one of toggle switch outlet of M21-7000 to 2nd input of XOR Gate used in step No. 4. Set relevant toggle switch to OFF state (downward). Designate this input as **B.**
6) Connect one jumper from output of above specified XOR gate to the input of one LED inlet on M21-7000.
7) Turn M21-7000 power on.
8) Use toggle switches to apply logics to input **A** and **B** as shown in table 7.1 and note down Output **Z.**

Input (A)	Input (B)	Output (Z)
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 7.1

Answer the following questions:-

Q # 1. How many inputs are available to each gate of XOR I.C?

Answer:

Student's ID: **Laboratory Exercise No: 8** Student's Name:

Objective: To familiarize with basic logic XNOR gate.

Goal: In this experiment students will implement basic Logic XNOR Gate practically and will observe its function.

Required Tools/Equipment:-

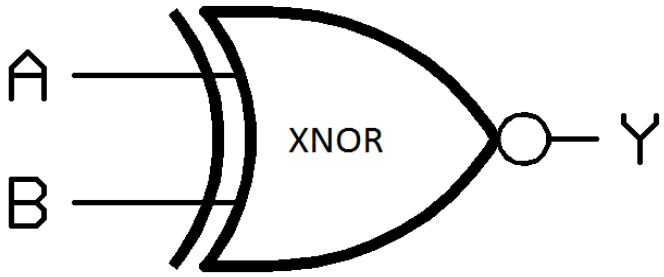
20) Analog & Digital Training System (M21-7000).
21) Connecting Wires (Jumpers).
22) Logic XOR and NOT Gate ICs' (XOR = CD4070, NOT=74HC04).

Theory:-

XNOR:

XNOR Gate provides binary 0 (LOW) only when not same logic levels are applied to its input (i-e 0 (LOW) is applied to one input and 1 (HIGH) is applied to second input). In other words, XNOR Gate provides binary 1 (HIGH) whenever same logic levels are applied to its input (i-e 0 (LOW) or 1 (HIGH) is applied to both inputs). This Logic Gate can be implemented with XOR gate and NOT gate by connecting XOR gate output to NOT gate input. In this condition, Inputs will be applied to XOR gate input pins and output will be taken at NOT gate output pin. If A and B are two inputs to XNOR Gate and Z is its output then $Z = (A \oplus B)' = A.B + A'.B'$.

Symbol:-



Procedure:-

1) Set 5 volts DC on Analog & Digital Training System (M21-7000) and turn it off.
2) Connect one jumper wire from +V outlet of M21-7000 to bread board. Connect second jumper and 3rd jumper from this common point to Pin No. 14 of Quad XOR Gate IC (CD4070) and pin No. 14 of Hex Inverter IC (74HC04).
3) Connect 4th jumper wire from +V outlet of M21-7000 to bread board. Connect 5th jumper and 6th jumper from this common point to Pin No. 7 of Quad XOR Gate IC (CD4070) and pin No. 7 of Hex Inverter IC (74HC04).
4) Connect one jumper from one of toggle switch outlet of M21-7000 to 1st input of one XOR Gate. Set toggle switch to OFF state (downward). Designate this input as **A.**

5) Connect one jumper from one of toggle switch outlet of M21-7000 to 2nd input of XOR Gate used in step No. 4. Set relevant toggle switch to OFF state (downward). Designate this input as **B.**
6) Connect one jumper from output of above specified XOR gate to the input of one NOT gate and one jumper from output of this NOT gate to LED inlet on M21-7000.
7) Turn M21-7000 power on.
8) Use toggle switches to apply logics to input **A** and **B** as shown in table 8.1 and note down Output **Z.**

Input (A)	**Input (B)**	**Output (Z)**
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 8.1

Student's ID: **Laboratory Exercise No: 9** Student's Name:

Objective: To construct XOR gate using discrete components.

Goal: In this experiment students will implement XOR Logic Gate practically using discrete components and will observe its function.

Required Tools/Equipment:-

23) Analog & Digital Training System (M21-7000).
24) Connecting Wires (Jumpers).
25) PNP Transistor
26) Resistors (10KΩ and 4.7KΩ)

Theory:-

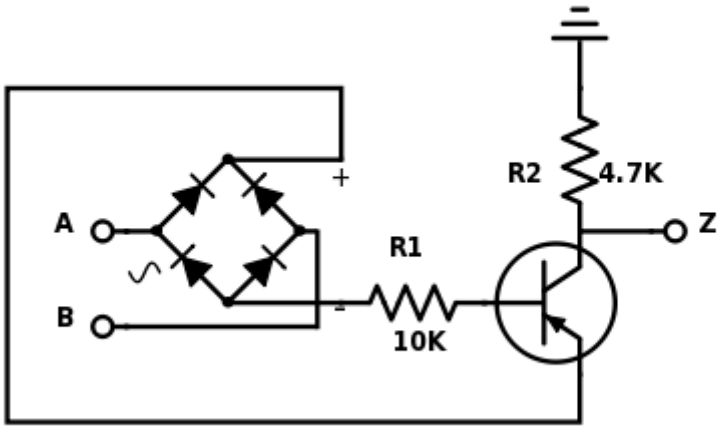


Fig: 9.1 XOR Gate with discrete Components

When the voltages at terminals A and B are at opposite logic states forward biases the Emitter-Base junction and turns ON the transistor. Thus an approximate Logic HIGH voltage VH−0.6V−VCE is available at output terminal Z. The Logic LOW voltage is approximately 0V but the sink current limited by the collector resistance 10K ohm.

As the Logic HIGH input current for TTL is approximately 0.4mA, which is the transistors emitter current and would generate a voltage drop of approximately 4V across 10K ohm resistor. But the problem is the 10K ohm resistor cannot provide the required sink current 0.4mA when the output Z is at Logic ZERO. Thus this XOR configuration seems to be suitable only for CMOS or TTL inputs at A and B and capable of driving only CMOS at output Y.

Procedure:-

9) Construct circuit as shown in Fig 9.1.
10) Use toggle switches to apply logics to input **A** and **B** as shown in table 9.1 and note down Output **Z.**

Input (A)	**Input (B)**	**Output (Z)**
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 9.1

Answer the following questions:-

Q # 1. What are TTL and CMOS voltage level?

Answer:

Student's ID: **Laboratory Exercise No: 10** Student's Name:

Objective: To construct XNOR gate using discrete components.

Goal: In this experiment students will implement XNOR Logic Gate practically using discrete components and will observe its function.

Required Tools/Equipment:-

27) Analog & Digital Training System (M21-7000).
28) Connecting Wires (Jumpers).
29) NPN Transistor (BC 548)
30) Resistors (10KΩ and 4.7KΩ)

Theory:-

XNOR:

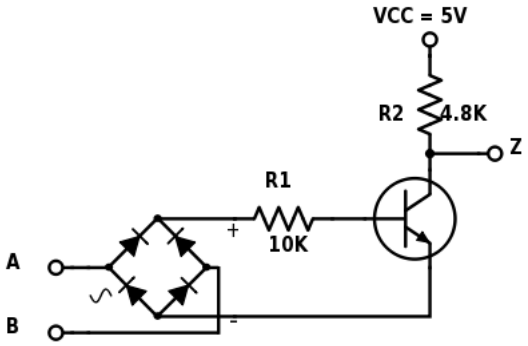


Fig: 10.1 XNOR Gate with discrete

When the voltage at A and B terminals are at opposite logic state, a voltage of higher voltage minus lower voltage minus 1.2V (voltage drop between two diodes) forward bias the Emitter-Base junction of the Transistor. This turns ON the transistor and the Logic LOW voltage available at the collector of the transistor is approximately equal to 0.6+VL+VCE, where VL is the Logic LOW input and VCE is the Collector to Emitter voltage of the transistor. When the both inputs A and B are at the same Logic Levels, the Emitter to Base junction of the transistor cannot be forward biased, thus the transistor is in OFF state and the output Y is at supply voltage.

Procedure:-

9) Construct circuit according to Fig 10.1
10) Use toggle switches to apply logics to input **A** and **B** as shown in table 10.1 and note down Output **Z.**

Input (A)	**Input (B)**	**Output (Z)**
0 (LOW)	0 (LOW)	
0 (LOW)	1 (HIGH)	
1 (HIGH)	0 (LOW)	
1 (HIGH)	1 (HIGH)	

Table: 10.1

Student's ID: **Laboratory Exercise No: 11** Student's Name:

Objective: To verify De Morgan's Laws practically using logic gates.

Goal: In this experiment students will implement digital circuit according to De Morgan's Laws and will verify its validity practically.

Required Tools/Equipment:-

31) Analog & Digital Training System (M21-7000).
32) Connecting Wires (Jumpers).
33) Basic Logic Gates ICs (NOT =74HC04, AND =74HC08, OR = 74HC32).

Theory:-

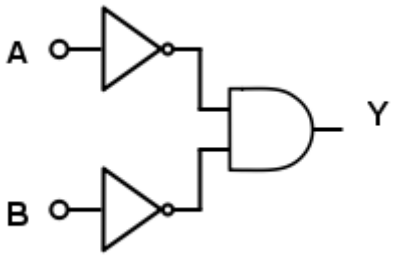
According to De Morgan's Laws:

$$\overline{(A + B)} = \overline{A} \cdot \overline{B} \text{ ---------- (i)}$$
$$\overline{(A \cdot B)} = \overline{A} + \overline{B} \text{ ---------- (ii)}$$

Procedure:

Verification of Eq. i

Circuit Equivalent to LHS of Eq. i Fig.11.1



Circuit Equivalent to RHS of Eq. i Fig.11.2

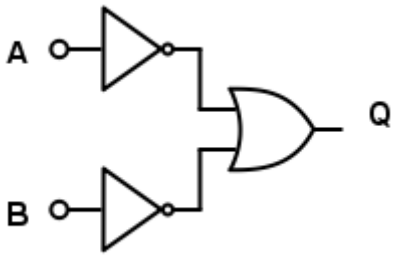
1. Construct circuit according to Fig. 11.1 and 11.2.
2. Apply inputs according to truth table 11.1.
3. Same output of X and Y will prove validity of De Morgan's Law's equation i

Input (A)	Input (B)	Output (X)	Output (Y)
0 (LOW)	0 (LOW)		
0 (LOW)	1 (HIGH)		
1 (HIGH)	0 (LOW)		
1 (HIGH)	1 (HIGH)		

Table 11.1

Verification of Eq. ii

Circuit Equivalent to LHS of Eq. ii Fig.11.3



Circuit Equivalent to RHS of Eq. ii Fig.11.4

1. Construct circuit according to Fig. 11.3 and 11.4.
2. Apply inputs according to truth table 11.2.
3. Same output of Z and Q will prove validity of De Morgan's Law's equation ii.

Input (A)	Input (B)	Output (Z)	Output (Q)
0 (LOW)	0 (LOW)		
0 (LOW)	1 (HIGH)		
1 (HIGH)	0 (LOW)		
1 (HIGH)	1 (HIGH)		

Table 11.2

Answer the following questions:-

Q # 1. Describe De Morgan's Laws in your own words.

Answer:

Student's ID: **Laboratory Exercise No: 12** Student's Name:

Objective: To verify Karnaugh Map Validation Using SOP.

Goal: In this experiment students will reduce a logic expression using K-map and will verify their simplification practically.

Required Tools/Equipment:-

34) Analog & Digital Training System (M21-7000).
35) Connecting Wires (Jumpers).
36) Basic Logic Gates ICs (NOT =74HC04, AND =74HC08, OR = 74HC32).

Theory:-

A Karnaugh map provides a systematic method for simplifying Boolean expressions, if properly used, will produce the simplest SOP or POS expression possible, known as the minimum expression. [1]

A Karnaugh map is similar to a truth table because it represents all of the possible values of input variables and the resulting output of each value. Instead of being organized into columns and rows like a truth table, the Karnaugh map is an array of cells, in which each cell represents a binary value of the input variables.[2]

Procedure:

Consider a SOP expression:

$$\overline{A}\overline{B}\overline{C} + A\overline{B}\overline{C} + \overline{A}B\overline{C} + AB\overline{C} = X$$

This expression yield following truth table:

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

This Truth Table will produce K map as shown:

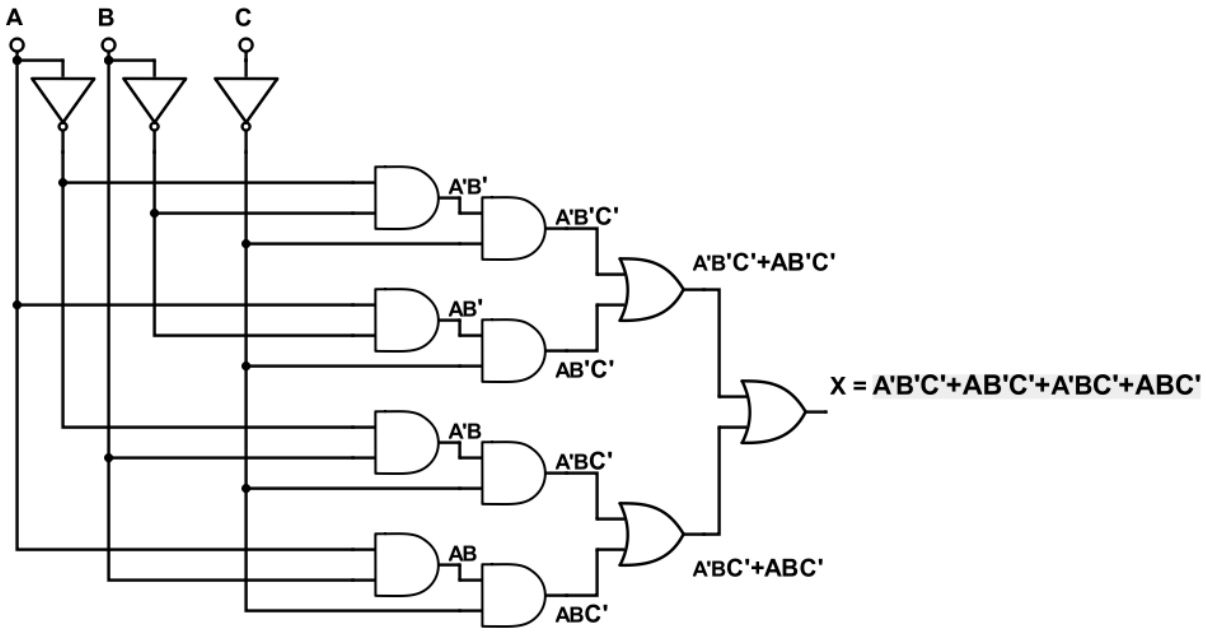
AB \ C	$\overline{C}$	C
$\overline{A}\,\overline{B}$	1	0
$\overline{A}\,B$	1	0
$A\,B$	1	0
$A\,\overline{B}$	1	0

Carefully following K-Map rules, expression will be reduced as shown:

AB \ C	$\overline{C}$	C
$\overline{A}\,\overline{B}$	1	0
$\overline{A}\,B$	1	0
$A\,B$	1	0
$A\,\overline{B}$	1	0

Reduced equation will be: X = $\overline{C}$

1. Construct digital circuit of above mentioned SOP expression as:



2. Apply input to this circuit according to table below and completely fill it.

A	B	C	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{ABC}$	$A\overline{BC}$	$\overline{A}B\overline{C}$	$AB\overline{C}$	$\overline{ABC} + A\overline{BC} + \overline{A}B\overline{C} + AB\overline{C} = X$	$\overline{C}$
0	0	0	1	1	1						
0	0	1	1	1	0						
0	1	0	1	0	1						
0	1	1	1	0	0						
1	0	0	0	1	1						
1	0	1	0	1	0						
1	1	0	0	0	1						
1	1	1	0	0	0						

3. If X = $\overline{C}$ for same set of inputs then it is proved that K-Map simplification is done successfully.

Answer the following questions:-

Q # 1. Reduce following POS expression using K-Map

$$(A + B + C) \cdot (\overline{A} + B + C) \cdot ($$

Answer:

_____

_____

_____

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_____

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_____

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_____

Reference:

Digital Fundamentals By Floyd. 9th edition. Chapter No. 4.

Student's ID: **Laboratory Exercise No: 13** Student's Name:

Objective: To verify Karnaugh Map Validation Using POS.

Goal: In this experiment students will reduce a logic expression using K-map and will verify their simplification practically.

Required Tools/Equipment:-

37) Analog & Digital Training System (M21-7000).
38) Connecting Wires (Jumpers).
39) Basic Logic Gates ICs (NOT =74HC04, AND =74HC08, OR = 74HC32).

Theory:-

A Karnaugh map provides a systematic method for simplifying Boolean expressions, if properly used, will produce the simplest SOP or POS expression possible, known as the minimum expression. [1]

A Karnaugh map is similar to a truth table because it represents all of the possible values of input variables and the resulting output of each value. Instead of being organized into columns and rows like a truth table, the Karnaugh map is an array of cells, in which each cell represents a binary value of the input variables.[2]

Procedure:

Consider a POS expression:

$$(A + B + C)\ (A + B + \bar{C})\ (A + \bar{B} + C)\ (A + \bar{B} + \bar{C})\ (\bar{A} + \bar{B} + C) = X$$

The process for minimizing a POS expression is same as SOP expression except that we have to group zeros (0s) to produce minimum sum terms instead of grouping 1s to produce minimum product terms.

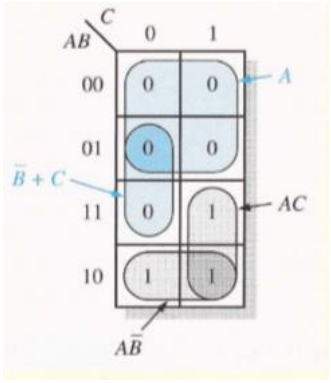
Thus combination of binary values of expression are

$$(0 + 0 + 0)(0 + 0 + 1)(0 + 1 + 0)(0 + 1 + 1)(1 + 1 + 0)$$

This expression yield following truth table:

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

This Truth Table will produce K map as shown:

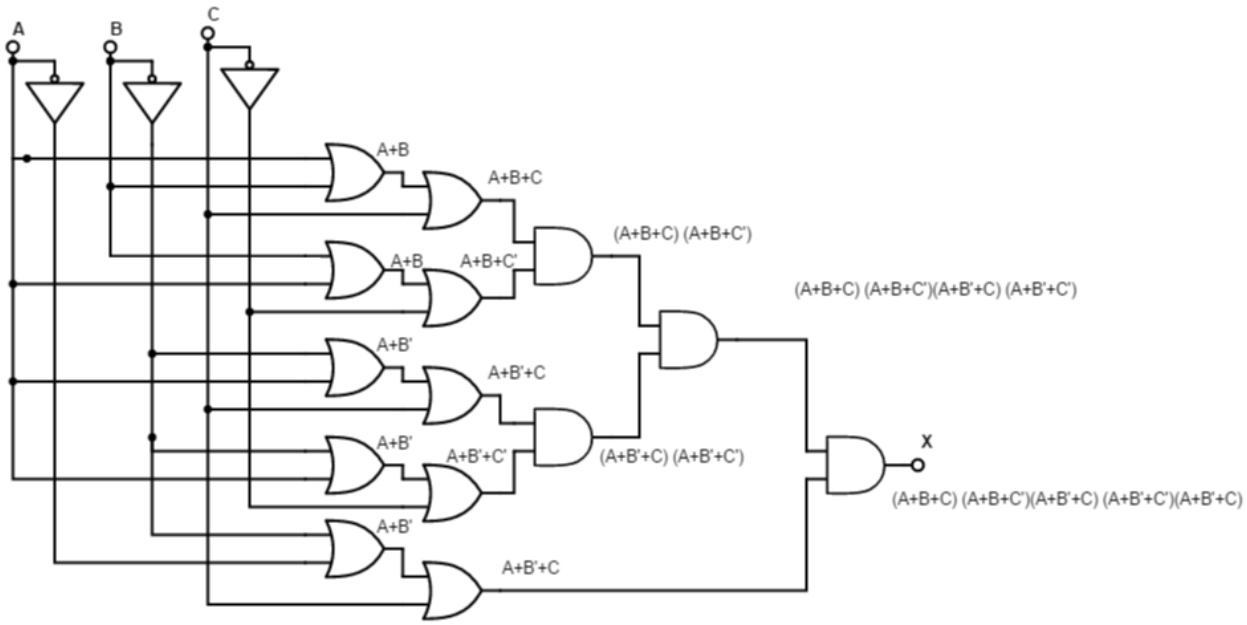


Carefully following K-Map rules, grouping zeros to produce minimum expression will be reduced as shown:

$$(A).(\bar{B}+C)$$

Reduced equation will be: X = $A \cdot (\bar{B}+C)$

4. Construct digital circuit of above mentioned POS expression as:



5. Apply input to this circuit according to table below and completely fill it.

A	B	C	$\overline{A}$	$\overline{B}$	$\overline{C}$	A+B+C	A+B+$\bar{C}$	$A+\bar{B}+C$	A+$\bar{B}+\bar{C}$	$\bar{A}+\bar{B}+C$	X	$A(\bar{B}+C)$
0	0	0	1	1	1							
0	0	1	1	1	0							
0	1	0	1	0	1							
0	1	1	1	0	0							
1	0	0	0	1	1							
1	0	1	0	1	0							
1	1	0	0	0	1							
1	1	1	0	0	0							

6. If X = $A \cdot (\bar{B} + C)$ for same set of inputs then it is proved that K-Map simplification is done successfully.

Answer the following questions:-

Q # 1. Reduce following POS expression using K-Map

$$(A + B + C) \cdot (\overline{A} + B + C) \cdot ($$

Answer:

Reference:

Digital Fundamentals By Floyd. 9th edition. Chapter No. 4.