

National School of Nanoscience and Nanotechnology (NSNN)

Nano and Microelectronics

Analog Electronics Lab Report 1

Experiment: Diode and Transistor Characteristics

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Abstract

This document reports the work done in the first laboratory session of the Analog Electronics course. The focus is in the application of the semiconductor devices like diode and transistors in switching circuits. Theoretical studies were followed by practical experiments to put the concepts into tests, then simulations finalized the work. The lab session was very enriching carrying very important concepts in the fields of CMOS and VLSI design.

1. Theory and Pre-Lab Calculations

1.1 Diodes

1.1.1 7-seg display

For the common anode 7 segment display, the anode pin is connected to the 5 V power supply and then the switch is connected between each segment pin resistor and the ground, as shown in the figure 1.

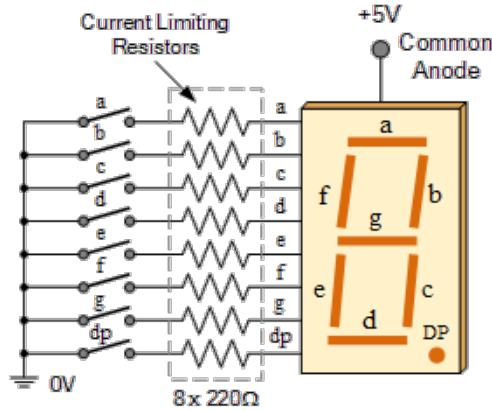


Figure 1: Common anode 7-seg display circuit

A part of the datasheet of the 7-seg display used (5101AS) is shown in the figure 2, the data will be used to calculate the required resistor value to limit the current through each segment led.

We know that:

$$V_{CC} = I_F R + V_F$$

$$R = \frac{V_{CC} - V_F}{I_F}$$

$$R = \frac{5\text{ V} - 1.8\text{ V}}{10\text{ mA}} = 320\Omega$$

Adjusting for E12 series, we choose a resistor of 330Ω for each segment.

Forward Voltage	VF	1.8	V	IF=10mA
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Figure 2: Extracted from 5101AS datasheet

1.1.2 Diode in circuit

We used the datasheet extraction of the 1N4007 as shown in the figure 3 to identify the characteristics of the diode in forward mode.

PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	1.0 A
V_{RRM}	50 V, 100 V, 200 V, 400 V, 600 V, 800 V, 1000 V
I_{FSM} (8.3 ms sine-wave)	30 A
I_{FSM} (square wave $t_p = 1$ ms)	45 A
V_F	1.1 V

Figure 3: Extraction of the 1N4007 model

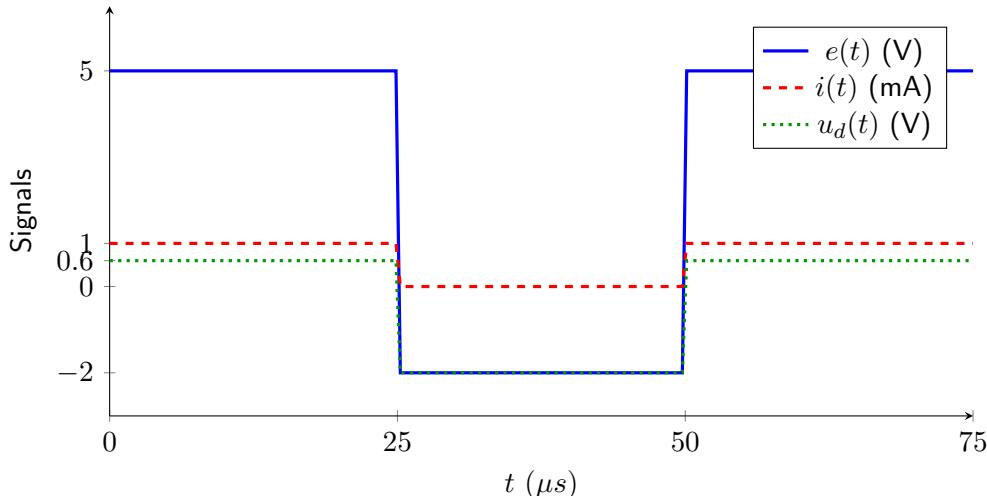
Also the dynamic resistance was found using the I-V curve provided in the datasheet.

$$V_F = 0.6 \text{ V}, \quad r_d \approx 4.36 \Omega$$

For 1 mA current;

$$R_{\text{theoretical}} = \frac{5 - V_F}{1 \text{ mA}} = \frac{5 - 1.1}{1 \times 10^{-3}} \approx 4.4 \text{ k}\Omega$$

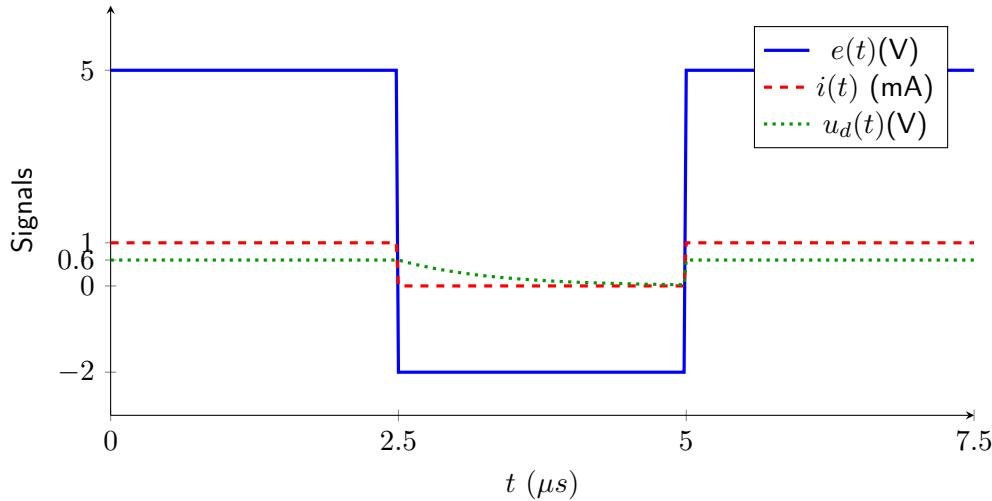
For the wave form, it is shown in the figure below.



The blocking of a diode, stored charge phenomenon, the blocking ability recovery: Applying a negative voltage on the pn junction increases the voltage polarity that already exist in the junction causing its depletion region to widen from the repulsion of like-wise charge carriers, causing the current to be nearly zero (but leakage current exists). When applying a strong enough positive voltage so that charges can jump of the depletion region, the two junctions start storing carriers of the opposite side, which is called the stored charge phenomenon, this will contribute to the lag of the diode switching behaviour at high frequencies. Only when the charges are removed that the depletion region get back to its normal state and the current drops once again to leakage levels.

Why t_{on} isn't instantaneous? When a semiconductor device, like a diode put to a sudden change in its state i.e: the square wave changing it from forward to reverse bias, this will cause the diode to change from a conductor to insulator. But the charge carriers that need to be removed from the p-junctions take more time than when moving them inside the junction. For this reason, the switching of the diode to off state will lag at high frequencies.

As we talked earlier, we can suppose that the wave from at 200 kHz is more lagging than the 20 kHz, due to the very small amount of time left for the junction to remove its charges, this can be described by the following graph.



1.1.3 Diode I-V curve

The I-V curve can be obtained automatically using two methods.

One is to use a special port for the oscilloscope that will measure the current going through the diode, and then using X-Y mode plotting the I-V characteristics curve.

The second method is using a $1\ \Omega$ in series with the diode as shown in the figure 4, and then plotting both voltages in the X-Y mode. The voltage across the $1\ \Omega$ resistor is equal to the current.

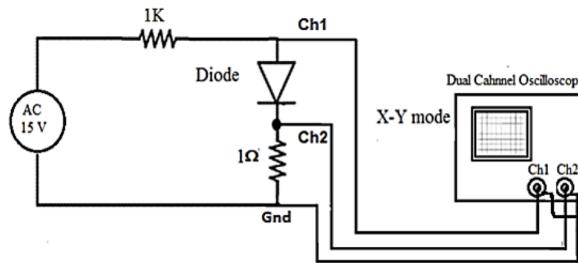


Figure 4: Circuit for plotting the I-V curve in oscilloscope

1.2 Transistors

For this part, we are going to use the 2N222 npn BJT transistor.

1.2.1 Transistor in a circuit

For determining the values of R_C and R_B , we extracted some important informations from the datasheet of the component, as shown in the figures 5 and 6.

ON CHARACTERISTICS		h_{FE}			
DC Current Gain ($I_C = 0.1 \text{ mA}dc, V_{CE} = 10 \text{ Vdc}$) ($I_C = 1.0 \text{ mA}dc, V_{CE} = 10 \text{ Vdc}$) ($I_C = 10 \text{ mA}dc, V_{CE} = 10 \text{ Vdc}$) ($I_C = 10 \text{ mA}dc, V_{CE} = 10 \text{ Vdc}, T_A = -55^\circ\text{C}$) ($I_C = 150 \text{ mA}dc, V_{CE} = 10 \text{ Vdc}$) (Note 1) ($I_C = 150 \text{ mA}dc, V_{CE} = 1.0 \text{ Vdc}$) (Note 1) ($I_C = 500 \text{ mA}dc, V_{CE} = 10 \text{ Vdc}$) (Note 1)		35 50 75 35 100 50 40	- - - - 300 - -		
Collector – Emitter Saturation Voltage (Note 1) ($I_C = 150 \text{ mA}dc, I_B = 15 \text{ mA}dc$) ($I_C = 500 \text{ mA}dc, I_B = 50 \text{ mA}dc$)	$V_{CE(sat)}$	- -	0.3 1.0		Vdc
Base – Emitter Saturation Voltage (Note 1) ($I_C = 150 \text{ mA}dc, I_B = 15 \text{ mA}dc$) ($I_C = 500 \text{ mA}dc, I_B = 50 \text{ mA}dc$)	$V_{BE(sat)}$	0.6 -	1.2 2.0		Vdc

Figure 5: On characteristics of the 2N2222 transistor

OFF CHARACTERISTICS		$V_{(BR)CEO}$	40	-	Vdc
Collector – Emitter Breakdown Voltage ($I_C = 10 \text{ mA}dc, I_B = 0$)					

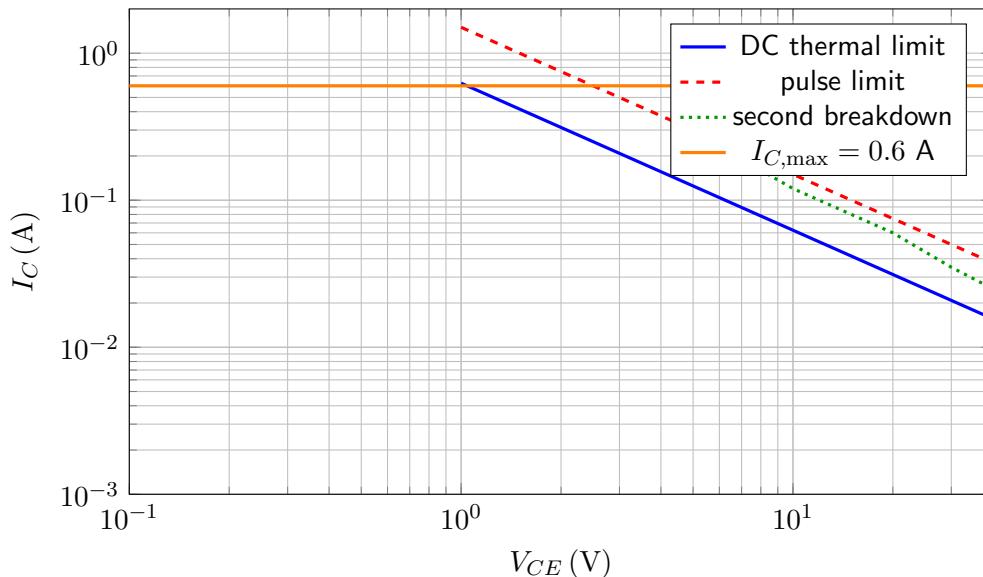
Figure 6: V_{CE} breakdown voltage of the 2N2222 transistor

From the datasheet, we establish the table 1 for the values we will use in our calculations.

Parameter	Value
β	40
$V_{CE(sat)}$	0.2 V
V_{CE0}	40 V
$V_{BE(sat)}$	0.6 V

Table 1: Extracted parameters for 2N2222 transistor

For industrial applications, the Safe Operating Area (SOA) of the transistors is very important for reliable operation at high scale integration. Based on the data extracted from the datasheet, we can establish an approximate SOA curve for the 2N2222 transistor, as shown below.



$$I_{C,DC} = \frac{0.625}{V_{CE}}, \quad I_{C,pulse} = \frac{1.5}{V_{CE}}, \quad I_{C,max} = 0.6, \quad I_{C,SB} = k V_{CE}^{-n}$$

Using the data from the table 1, we can calculate the values of R_C and R_B needed for the switching circuit. Given

Limit	Equation	Origin
$I_{C,\max}$	$I_C \leq 0.6 \text{ A}$	Continuous collector current rating
DC thermal	$I_C \leq \frac{0.625}{V_{CE}}$	$P_D = 625 \text{ mW} @ T_A = 25^\circ\text{C}$
Pulse / case dissipation	$I_C \leq \frac{1.5}{V_{CE}}$	$P_D = 1.5 \text{ W} @ T_C = 25^\circ\text{C}$
Second breakdown	$I_C \leq kV_{CE}^{-n}$	Hot spots, current crowding, avalanche

Given

$$V_{CC} = 10 \text{ V}, \quad V_{BB} = 5 \text{ V}, \quad I_C^{\text{sat}} = 20 \text{ mA}, \quad \beta = 40, \quad V_{CE(\text{sat})} = 0.2 \text{ V}, \quad V_{BE(\text{sat})} = 0.6 \text{ V}.$$

$$R_C^{\text{theoretical}} = \frac{V_{CC} - V_{CE(\text{sat})}}{I_C^{\text{sat}}} = \frac{10 - 0.2}{20 \times 10^{-3}} = 490 \Omega.$$

$$R_{C,\text{normalized}} \approx 510 \Omega \text{ (série E12).}$$

$$I_B^{\text{theoretical}} = \frac{I_C^{\text{sat}}}{\beta} = \frac{20 \times 10^{-3}}{40} = 0.5 \times 10^{-3} \text{ A} = 0.5 \text{ mA.}$$

$$R_B = \frac{V_{BB} - V_{BE(\text{sat})}}{I_B^{\text{theoretical}}} = \frac{5 - 0.6}{0.5 \times 10^{-3}} = 8.8 \times 10^3 \Omega = 8.8 \text{ k}\Omega.$$

The choice of the static value of the gain $\beta = 40$ is because that the transistor needs to be in saturation biasing before moving to small signal amplification, or switching mode where the dynamic values of the transistor will be put in use.

The previous calculations are way too ideal, in the experiment this will cause the transistor to function in an undesired way. For higher accuracy, the value of the gain will be divided by a factor of 4. This will keep the transistor in the active region, while increasing the chance of saturation when needed. Higher-accuracy rule:

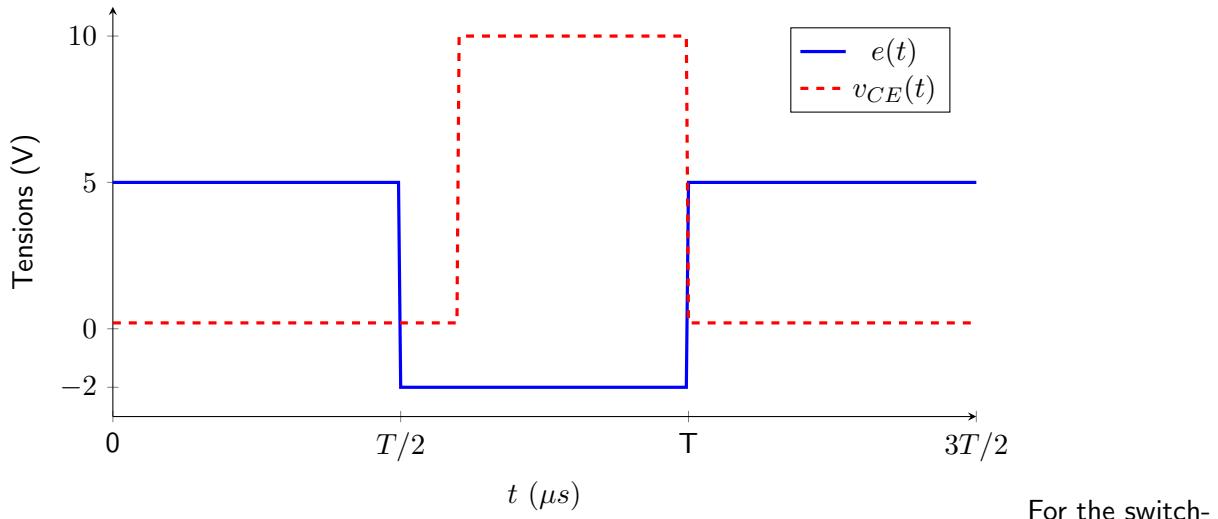
$$\beta_{\text{forced}} = \frac{\beta}{4} = \frac{40}{4} = 10.$$

$$I_B = \frac{I_C^{\text{sat}}}{\beta_{\text{forced}}} = \frac{20 \text{ mA}}{10} = 2 \text{ mA.}$$

$$R_B = \frac{V_{BB} - V_{BE(\text{sat})}}{I_B} = \frac{5 - 0.6}{2 \times 10^{-3}} = 2.2 \text{ k}\Omega.$$

Due to the fact that the BJT transistor have two n junctions and one p junction, it can be approximated to two diodes connected in series. inherently, the transistor will have similar switching behavior as the diode, i.e there will be a lag when switching to an off state at high frequencies. This lag can be presented in the figure below.

Transistor switching waveforms with stored charge effect



Delay Time	$(V_{CC} = 30 \text{ Vdc}, V_{BE(off)} = -2.0 \text{ Vdc}, I_C = 150 \text{ mA}, I_{B1} = 15 \text{ mA})$ (Figure 1)	t_d	-	10	ns
Rise Time		t_r	-	25	ns
Storage Time	$(V_{CC} = 30 \text{ Vdc}, I_C = 150 \text{ mA}, I_{B1} = I_{B2} = 15 \text{ mA})$ (Figure 2)	t_s	-	225	ns
Fall Time		t_f	-	60	ns

Figure 7: Switching characteristics of the 2N2222 transistor

The storage time is mainly due to the stored charge phenomenon, which is 225 ns in this model.

Inductive Charge without DRL

We suppose that $t = 0$ with

$$i_c(0) = I_{C \max}, \quad \frac{di_c}{dt} = -a,$$

And the current becomes zero after $10 \mu\text{s}$.

$$i_c(t) = I_{C \max} - a t, \quad 0 \leq t \leq 10 \mu\text{s},$$

So

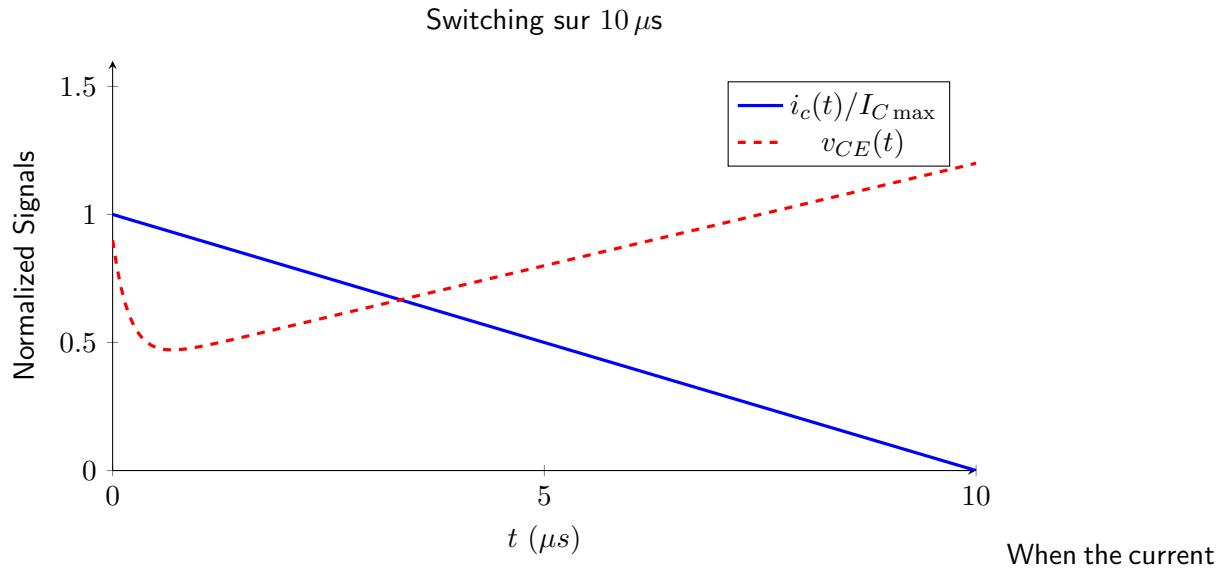
$$a = \frac{I_{C \max}}{10 \mu\text{s}}.$$

$$v_L(t) = L \frac{di_c}{dt} = -L a$$

Applying Kirchhoff's voltage law:

$$v_{CE}(t) = V_{CC} + L a.$$

When the transistor changes its state, the current spikes rapidly causing the voltage across the inductor to overshoot uncontrollably.



1.2.2 Transistor with an active load and DRL

When adding a reversed diode across the inductive load, the voltage across the transistor will be limited to the value of the breakdown voltage of the diode. This is a great solution for protecting the transistor from high voltage spikes.

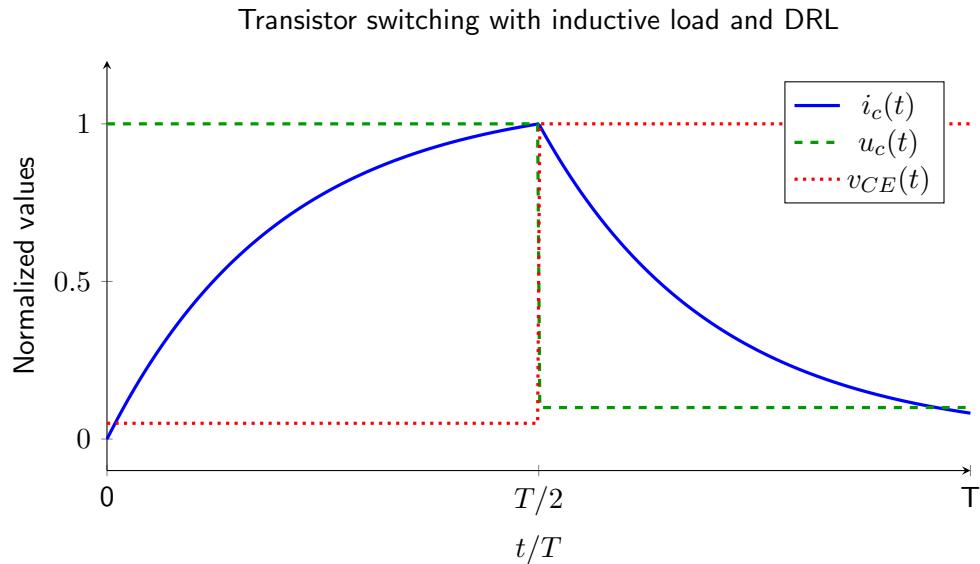
Using the diode current equation, we can build an approximate model for the circuit behaviour.

$$\tau = \frac{L}{R_L}$$

$$i_c(t) = \begin{cases} I_{c,\min} e^{-t/\tau} + \frac{V_{CC}}{R_L} (1 - e^{-t/\tau}), & 0 \leq t \leq DT, \\ I_{c,\max} e^{-(t-DT)/\tau}, & DT \leq t \leq T, \end{cases}$$

$$u_c(t) = L \frac{di_c(t)}{dt} + R_L i_c(t)$$

$$v_{CE}(t) = \begin{cases} 0, & 0 \leq t \leq DT, \\ V_{CC}, & DT \leq t \leq T. \end{cases}$$



1.2.3 Switching mode

My first suggestion when dealing with switch circuits, is to use MOSFETs instead of BJTs, MOSFETs have way less power consumption and faster switching speeds, since it is voltage controlled. Another solution is to use digital solutions instead of purely analog ones, NE555 timer ICs can be a great alternative.

But sticking with the BJT choice, I used my favorite book on electronics to find a solution to the stored charge phenomenon, Art of Electronics by Paul Horowitz and Winfield Hill, 3rd edition. The book offer more than one solution to the problem, one of them is to use a speed-up capacitor across the base-collector junction or the base resistor, to help in removing the charges when passing to a blocked state, as it's shown in the figure 8.

I quote, "A small "speed-up" capacitor – typically just a few picofarads – is often connected across the base resistor to improve high-speed performance." - Chapter 2, Bipolar Transistors.

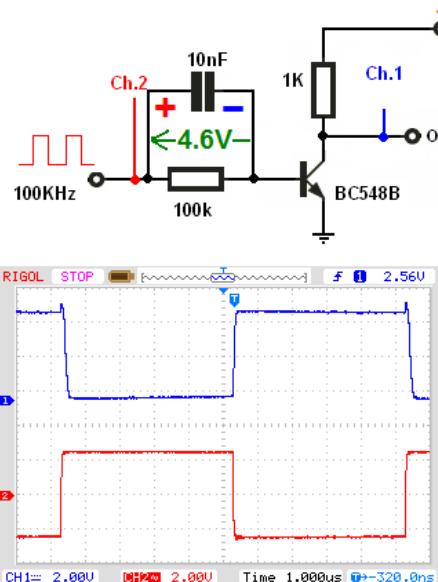


Figure 8: Solution to the stored charge phenomenon: Speed-up capacitor

Also another book proposed "Baker Clamp" circuit with two diodes in the base-collector junction to help in removing the stored charges, as shown in the figure 9.

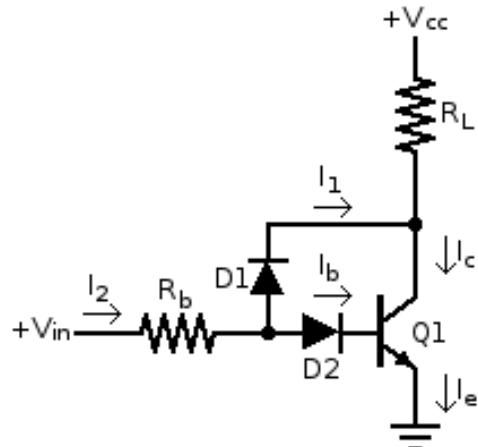


Figure 9: Solution to the stored charge phenomenon: Baker Clamp circuit

2. Laboratory Work

2.1 Diodes

2.1.1 7-segment display testing

After connecting the common anode 7 segment display, we tested each segment by connecting it to a $330\ \Omega$ and the ground as in the figure 10. noted the pins for each segment to compare with the datasheet.

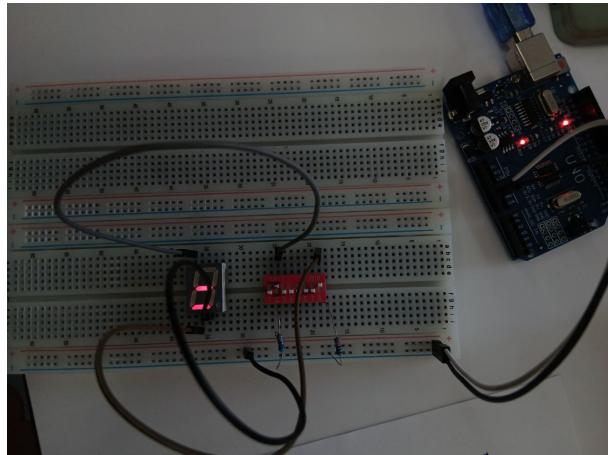


Figure 10: Testing of the 7-seg display

2.1.2 Switching in diodes

After connecting the diode in the proper circuit for testing its switching behavior, we applied a $e(t)$ signal as was required. We observed the output voltage across the diode (Blue), and $e(t)$ as the supply voltage (Yellow), as shown in the figure 11. A lag between the two signal was recorded, due to the stored charge phenomenon explained earlier. The time of the lag is $10\ \mu s$, which is about 20 % of the period at 20 kHz.



Figure 11: Output signal across the diode at 20 kHz

After recording the data with a signal $e(t)$ of a frequency of 20 kHz, we increased the frequency gradually until reaching 50 kHz where it marks the limit of the diode switching behavior, the figure 12 shows that the blue signal of the diode spends almost no time on the low state. For higher frequencies the output signal will not set on the off state properly.



Figure 12: Output signal of the diode at 50 kHz, marks the limit of switching behavior

We continued on the increasing of the frequency to 200 kHz, the point that marks the failure of the diode switching behaviour. The state now is almost totally in the on state, as shown in the figure 13.



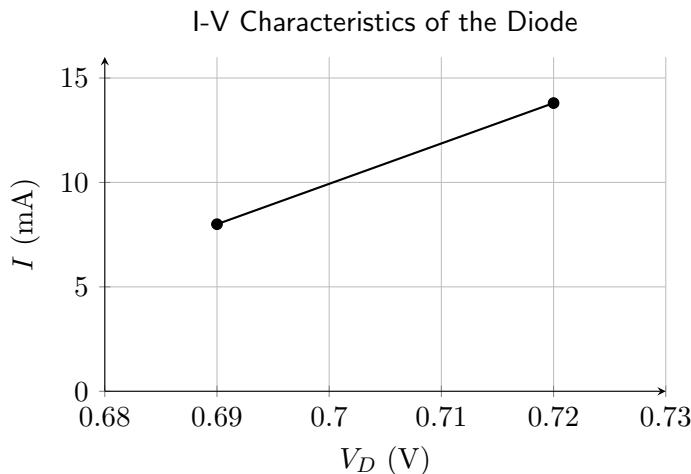
Figure 13: Output signal of the diode at 200 kHz, marks the failure of switching behavior

2.1.3 I-V Characteristics of the Diode

Due to limit access to the materials required for this part, we used an approximated method to calculate the dynamic resistance of the diode. We measured the voltage at two different values.

V_{CC} (V)	R (Ω)	V_D (V)	V_R (V)	I (mA)
5.2	325.8	0.72	4.40	13.8
3.3	325.8	0.69	2.602	8.0

$$r_d \approx 5.2 \Omega$$



After 5 days of the lab session, we were able to get the equipment required for characterizing a *Led Diode*. The circuit required two signal representation of voltages in the oscilloscope, one across the diode, and the other of a $1\ \Omega$ resistor in series with it, as it is shown in the figure 14.

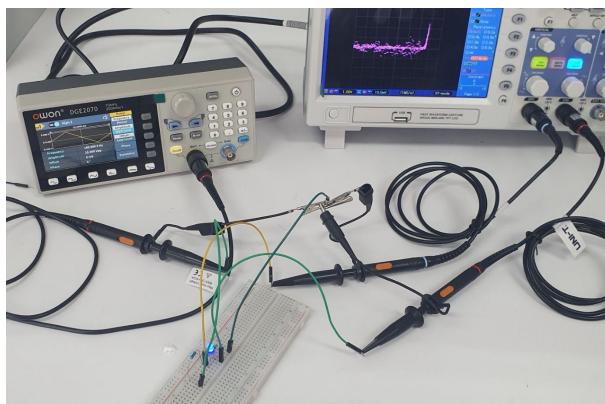


Figure 14: Circuit used for plotting the I-V curve of the led diode

Using the X-Y mode in the oscilloscope, we were able to plot the current versus its voltage, and that only after applying a triangular signal on the circuit. The resulting plot is presented in the figure 15.

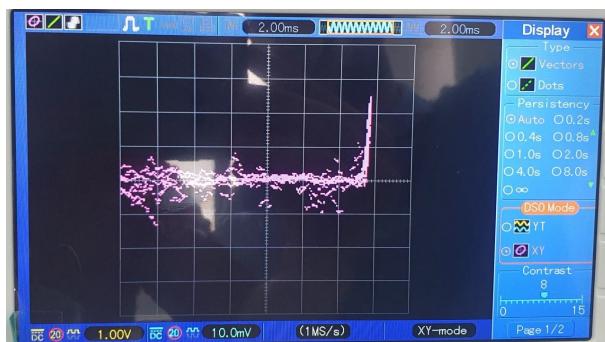


Figure 15: I-V curve for a led diode

Using the multimeter, it was possible to measure the forward voltage of the led diode, that was 2.5 V, supporting the results obtained from the oscilloscope with respect to error caused by the $1\ \Omega$ resistor and other sources.

2.2 Transistors

Following our pre-lab calculations, we used the 2N222 BJT transistor with the values of $R_c = 470 \Omega$ and $R_b = 2200 \Omega$ we found earlier.

2.2.1 Switching behavior

We applied $V_{cc} = 10 \text{ V}$, $e(t)$ on the base and set the frequency to 50 kHz, we observed the voltage across the collector and The emmiter of the BJT, and compared it to the input signal $e(t)$, as shown in the figure 16

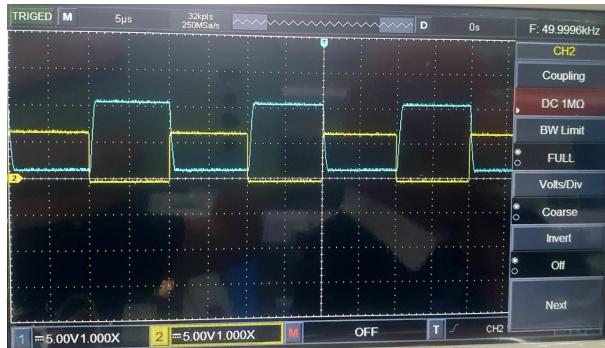


Figure 16: V_{CE} (Blue) and $e(t)$ (Yellow) at 50 kHz

At 50 kHz, the transistor is able to switch properly between the on and off states, with an approximately $0.5 \mu\text{s}$ delay in both transitions.

2.2.2 Switching on inductive load

When adding an inductor in the collector circuit, we observed that v_{CE} signal now have a spike when switching from off to on state, with oscillations along the on state. This is well expected as we learned when we prepared the laboratory work.

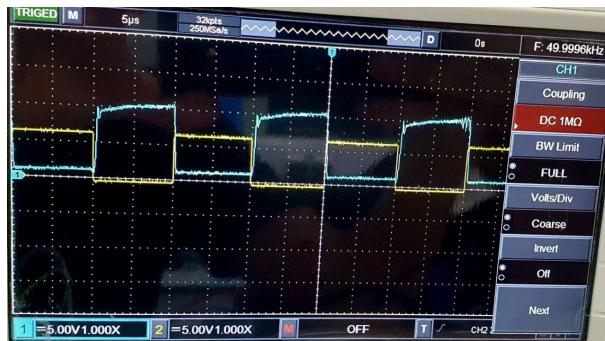


Figure 17: V_{CE} (Blue) and $e(t)$ (Yellow) at 50 kHz with inductive load

After adding the fly-back diode, in reversed baising across the inductor, the spike disappeared due to the effect of the reverse volatge of the diode. This observation shows that the assumptions that were made in the preparation were correct, and the diode in fact can protect the transistors from high voltage inputs.



Figure 18: The flyback diode effect on the voltage across the BJT at 50 kHz

Effects of the fly-back diode When the transistor changes its state, the inductor will try to keep the current through it constant for that the stored energy inside it will cause voltage spikes.

By adding the fly-back diode, the voltage across the transistor will be limited and controlled by the reverse voltage of the DRL.

The voltage v_{CE} will get clamped to a higher value, causing the current in both terminals, base and collector currents to decrease and become more stable.

Power dissipation in the circuit will be reduced also, since the voltages are more in control now. As we explained earlier, the phenomenon of stored charges can be reduced if we apply a negative voltage on the base, speeding up the movement of charge carriers in the pn junction to their supposed place. For this reason, i.e we haven't observed any long lags in the transistor switching like in the figure 16, even though that we are at 50 kHz frequency.

3. Simulation Studies (LTspice / Simulink)

For the simulation part, we used LTspice to develop our understanding of the lab experiments. The 50 year old software provided highly accurate data for the 2N222, and 1N4007 components.

3.1 LTspice for Diode switching

After building the circuit, we tested out different values for the frequency of the input signal.

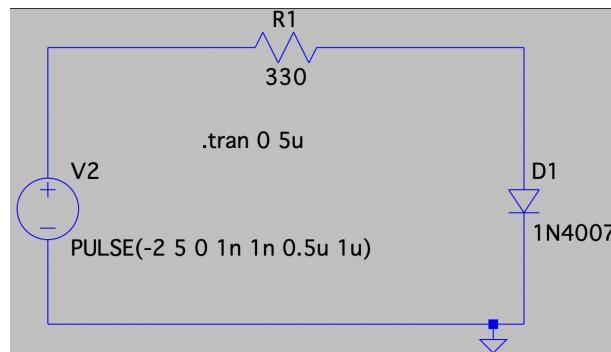


Figure 19: Diode switching in LTspice

LTspice netlist for the diode switching circuit is shown below:

```

R1 N002 N001 330
V2 N001 0 PULSE(-2 5 0 1n 1n 0.5u 1u)
D1 N002 0 1N4007
.model D D
.lib /Users/sid/Library/Application Support/LTspice/lib/cmp/standard.dio
.tran 0 5u
.backanno
.end

```

The outputs for different frequencies are shown below:

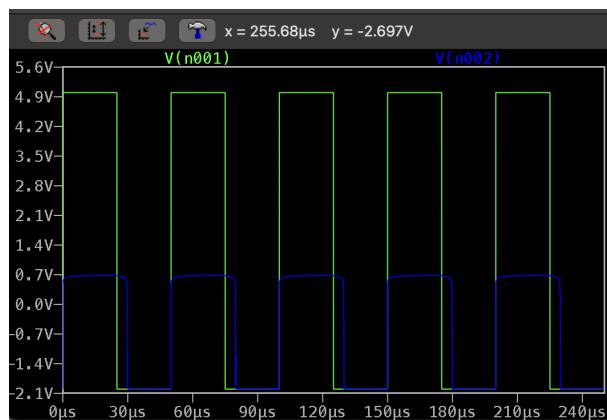


Figure 20: At 20 kHz, The lag between the input and output is visible 10 % of the period

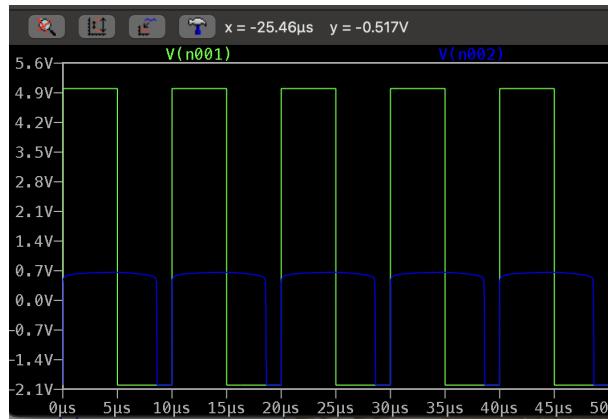


Figure 21: At 100 kHz, The lag between the input and output is visible 25 % of the period

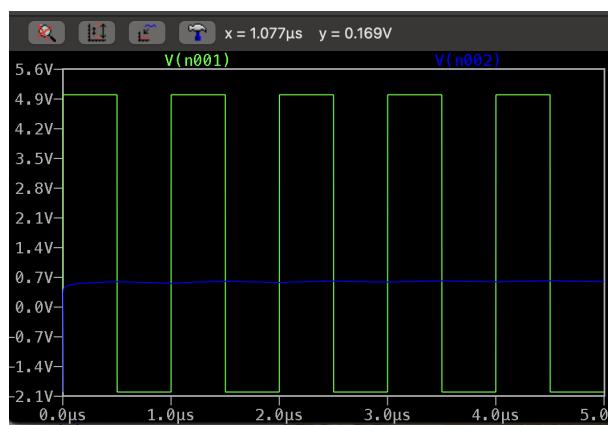


Figure 22: At 1 MHz, The state of the diode is almost always ON

The included figures support our earlier observations, and the experimental results found in the diode switching circuit.

3.2 LTspice for BJT switching

Following the same methodology, we built the BJT switching circuit in LTspice.

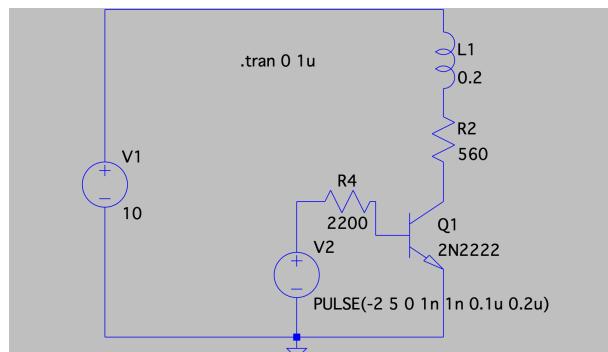


Figure 23: BJT switching with inductive load in LTspice

We provide the netlist for the BJT switching circuit below:

```

V1 N001 0 10
V2 N004 0 PULSE(-2 5 0 1n 1n 0.1u 0.2u)
R2 N002 N003 560
L1 N001 N002 10e-3 Rser=10
R4 N005 N004 2200
Q1 N003 N005 0 0 2N2222
D1 N003 N001 1N4007
.model D D
.lib /Users/sid/Library/Application Support/LTspice/lib/cmp/standard.dio
.model NPN NPN
.model PNP PNP
.lib /Users/sid/Library/Application Support/LTspice/lib/cmp/standard.bjt
.tran 0 1u
.backanno
.end

```

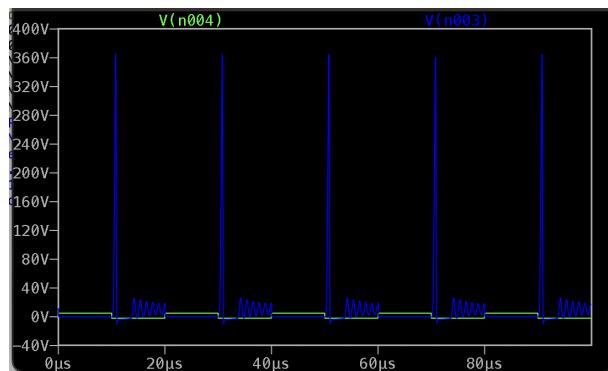


Figure 24: Response of the simulated BJT switching circuit at 50 kHz

Indeed the simulation results shows a very high spick in the v_{CE} voltage when switching to ON state, with oscillations along the period.

Now moving to the last part, a diode in reverse position was added in the circuit presented in the figure 25.

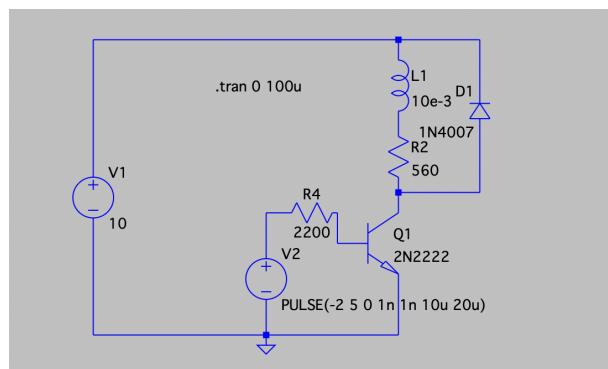


Figure 25: BJT switching with inductive load and DRL in LTspice

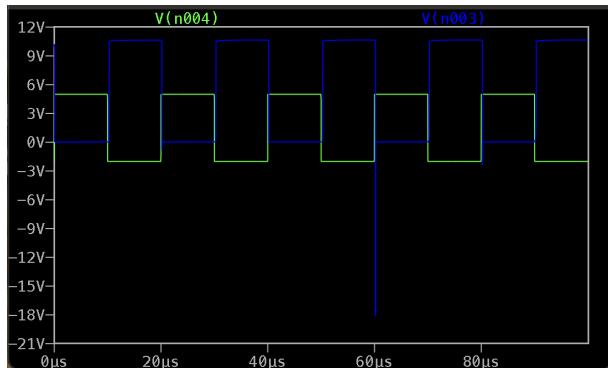


Figure 26: Response of the simulated BJT switching with inductive load and DRL

At last, the simulations show that the fly-back diode is very effective at limiting the voltage across the collector load, as we can see in the figure 26, the spikes are almost completely gone.

4. Conclusion

The laboratory session contained a lot of new concepts in the semiconductor devices field. First, the diode switching behavior was studied, using the stored energy phenomenon and other related theories. A study on the I-V characteristics of the diode was also established, with totally new methods.

Then, the BJT transistor was put under scope to study the effects of the negative voltage supply, inductive loads, and fly-back diodes on the switching speed of the device. With strong theoretical work, such as in the research of the effective ways to support the switching circuit, the lab work had a positive impact on the creative mind more than the lab itself.

Simulations were also conducted to support the outcomes of the laboratory work, and indeed it matched the theory, and the lab results.

As a consequence, the concepts developed on the first laboratory sessions are now on a concrete basis, and will be used in future sessions to develop the intuition on semiconductors furthermore.

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