Analog IC Design lab (EC1061)
Experiment No.: 05

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***Abstract*—Simulation of CMOS inverter.**

I. Brief Description of the Work

a) Construct CMOS inverter.

b) Plot its VTC and estimate noise margin(NM) and power consumption.

c) Determine rise time τ_{rise}, fall time τ_{fall} and propagation delay τ_{pd}.

II. Simulation Steps and results

A. CMOS inverter to determine VTC, NM and power

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1) A CMOS inverter circuit is designed as shown in Fig.1.

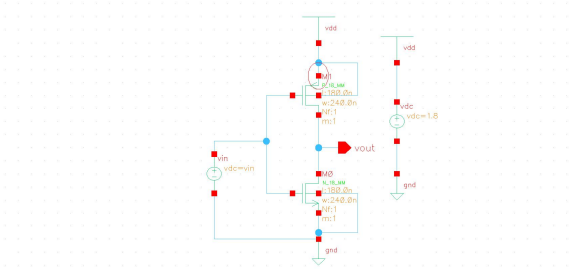

Fig. 1. CMOS inverter with DC input

2) The input and output nodes is labeled as V_{in} & V_{out} respectively.

3) The value of V_{in} is set to 1.8 V in the ADE.

4) In DC analysis varying V_{in} from 0 to $1.8V$.

5) Plot VTC, V_{OUT} vs V_{in} is shown in Fig 2.

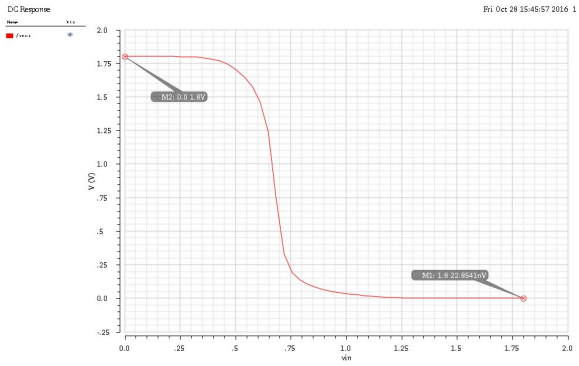

Fig. 2. V_{OUT} vs V_{in}

6) To find the mid voltage V_m, intersection point of the plot as shown in Fig 3.

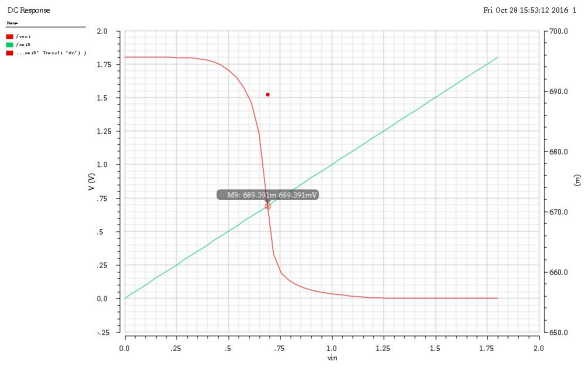

Fig. 3. V_{OUT} vs V_{in} and V_m

7) Plot the dV_{OUT}/dV_{in} shown in Fig 4.

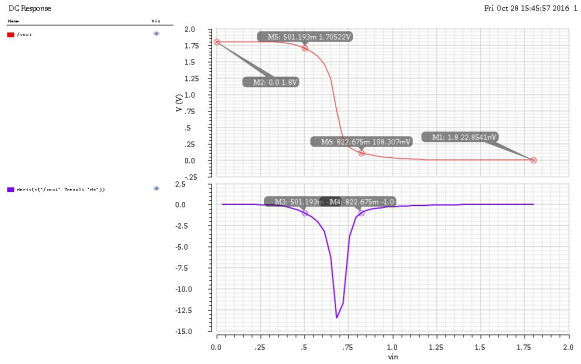

Fig. 4. V_{OUT} vs V_{in} Noise Margin

8) By use marker $dV_{OUT}/dV_{in} = -1$.

9) Determine V_{OH},V_{OL},V_{IH},V_{IL}.

10) Calculate the value of noise margin(NM).

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

11) Power plot is shown in Fig 5.

$$power(\mu W) = 1.8V * I_D(\mu A)$$

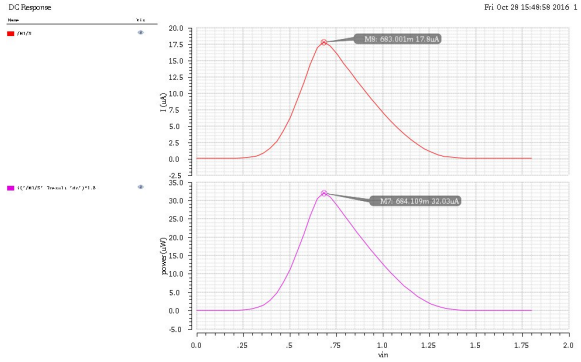

Fig. 5. Power plot

12) Power maximum is at mid voltage V_m.

B. CMOS inverter to determine τ_{rise}, τ_{fall}&τ_{delay}

1) The schematic diagram to calculate rise time τ_{rise}, fall time τ_{fall} & propagation delayτ_{pd} is shown in Fig 6.

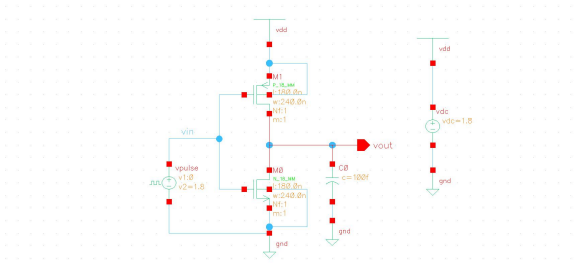

Fig. 6. Schematic diagram CMOS inverter

2) At the input side V_{pulse} is applied which has period $100ns$ and pulse width 50 ns.

3) Place a capacitance $100fF$ at the V_{OUT}.

4) Calculation of rise time τ_{rise}, fall time τ_{fall} & propagation delayτ_{pd}

5) Transient analysis of signal V_{OUT} from 10% to 90% is called Rise time τ_{rise}.

6) Transient analysis of signal V_{OUT} from 90% to 10% is called Fall time τ_{fall}.

7) Difference of Transient analysis of signal V_{OUT} and V_{pulse} from 50% rise is called propagation delay low to high τ_{PLH} .

8)Difference of Transient analysis of signal V_{OUT} and V_{pulse} to 50% fall is called propagation delay high to low τ_{PHL} .

9) Average of propagation delay from low to high and high to low is called propagation delay τ_{pd}.

$$\tau_{pd} = (\tau_{PHL} + \tau PLH)/2$$

$$V_{10\%} = V_{min} + 10/100(V_{max} - V_{min})$$

$$V_{90\%} = V_{min} + 90/100(V_{max} - V_{min})$$

$$V_{50\%} = V_{min} + 50/100(V_{max} - V_{min})$$

10) transient analysis of V_{OUT} is shown in Fig 7.

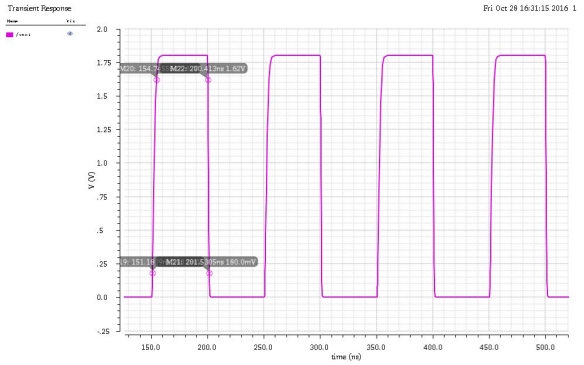

Fig. 7. Transient analysis of V_{OUT}

11) Calculate rise time τ_{rise}, fall time τ_{fall} from the Fig 7.

12) Transient analysis of V_{OUT} and V_{pulse} shown in Fig 8.

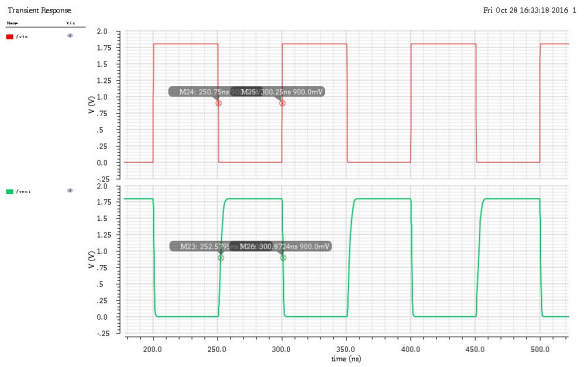

Fig. 8. Transient analysis of V_{OUT} and V_{pulse}

13) Calculate the propagation delayτpd from the Fig 8.

III. Observations & Conclusions

The values obtained are tabulated in TABLE I and II.

TABLE I
NOISE MARGINS OF THE CMOS INVERTER

V_{OH}	V_{OL}	V_{IH}	V_{IL}	NM_H	NM_L
1.8 V	0.02285 mV	822.675 mV	501.193 mV	0.9773 V	0.50117 V

Power consumed = 32.03 μW

TABLE II
VALUES OF τ_{rise}, τ_{fall} AND τ_D

τ_{rise}	τ_{fall}	τ_{PHL}	τ_{PLH}	τ_D
3.5646 nS	1.1175 nS	0.6224 nS	1.8295 nS	1.22595 nS

Acknowledgment