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LAB 2: AutoChip

This report documents the results of running four Verilog design examples using the AutoChip Colab framework. Each experiment is described in terms of setup, iteration logs, simulation outcomes, and final observations. A summary table is also included for quick comparison.

Summary Table

Example	Specification	Iterations / Candidates	Simulation Results	Final Outcome
Example 1 7420 NAND Chip	Two 4-input NAND gates (7420 IC)	1 iteration, 5 candidates	All passed, 0 mismatches (239 samples)	Correct in first pass
Example 2 Arbiter FSM	FSM-based arbiter with 3 request lines (priority r1 > r2 > r3)	1 iteration, multiple candidates	Simulation passed, correct grants	Correct FSM generated
Example 3 Rule 90 Automaton	512-cell sequential cellular automaton (Rule 90 update)	Multiple iterations, 5 candidates each	2 correct (0 mismatches / 7121 samples), others failed	Converged to correct solution
Example 4 PWM Generator	Parameterizable PWM with duty, period, sync reset	1 iteration, 5 candidates	3 correct (0 mismatches / 2403 samples), minor errors in others	Stable and functional PWM

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Detailed Results

Example 1: 7420 NAND Chip

- Specification: Implement a Verilog model for the 7420 IC with two 4-input NAND gates.
- Setup: Prompt (7420.sv), Testbench (7420_tb.sv), Model: gpt-4o-mini, Iterations: 1, Candidates: 5
- Iteration Log: All 5 candidates compiled and simulated correctly with 0 mismatches (239 samples).
- Final Result: Correct implementation on first attempt.
- Observation:Example 1 was simple combinational logic and AutoChip solved it perfectly.

Example 2: Arbiter FSM

- Specification: FSM-based arbiter with priority among 3 requesters (r1 > r2 > r3).
- Setup: Prompt (FSM.sv), Testbench (FSM_tb.sv), Model: gpt-4o-mini, Iterations: 1, Candidates: multiple
- Iteration Log: Iteration 0 produced valid FSM code. Best candidate passed simulation with correct grants.
- Final Result: Correct FSM implementation achieved.
- Observation: Sequential FSM logic was handled well, confirming priority rules correctly.

Example 3: Rule 90 Cellular Automaton

- Specification: 512-cell register updated each clock cycle with Rule 90.
- Setup: Prompt (Rule90.sv), Testbench (Rule90_tb.sv), Model: gpt-4o-mini, Iterations: multiple, Candidates: 5 each
- Iteration Log: Iteration 0: 3 failed compilation, 1 produced 7058 mismatches, 1 passed (0 mismatches). Iteration 1: similar results with consistent passing candidate.
- Final Result: Correct automaton synthesized; 2 candidates achieved perfect results.
- Observation: Sequential design was harder. AutoChip converged using ranking and simulation feedback.

Example 4: PWM Generator

- Specification: Parameterizable PWM generator with duty, period, synchronous reset.
- Setup: Prompt (pwm.sv), Testbench (pwm_tb.sv), Model: gpt-4o-mini, Iterations: 1, Candidates: 5
- Iteration Log: Iteration 0: 3 candidates passed with 0 mismatches (2403 samples). 2 candidates showed minor mismatches (1–4 errors).
- Final Result: Stable and functional PWM design.
- Observation: PWM was more complex, but AutoChip still generated multiple correct solutions; simulation feedback ensured correctness.

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Overall Conclusion

Across four experiments, AutoChip consistently generated synthesizable Verilog designs. Simple examples converged in one pass, while more complex sequential cases required candidate ranking. Simulation feedback was critical in filtering incorrect designs and confirming correctness.