THE UNIVERSITY OF TEXAS AT DALLAS

Department Of Electrical Engineering

EECT 6326 ANALOG IC DESIGN

Design of Analog Multiplier based on 2 stage Op-Amp design.

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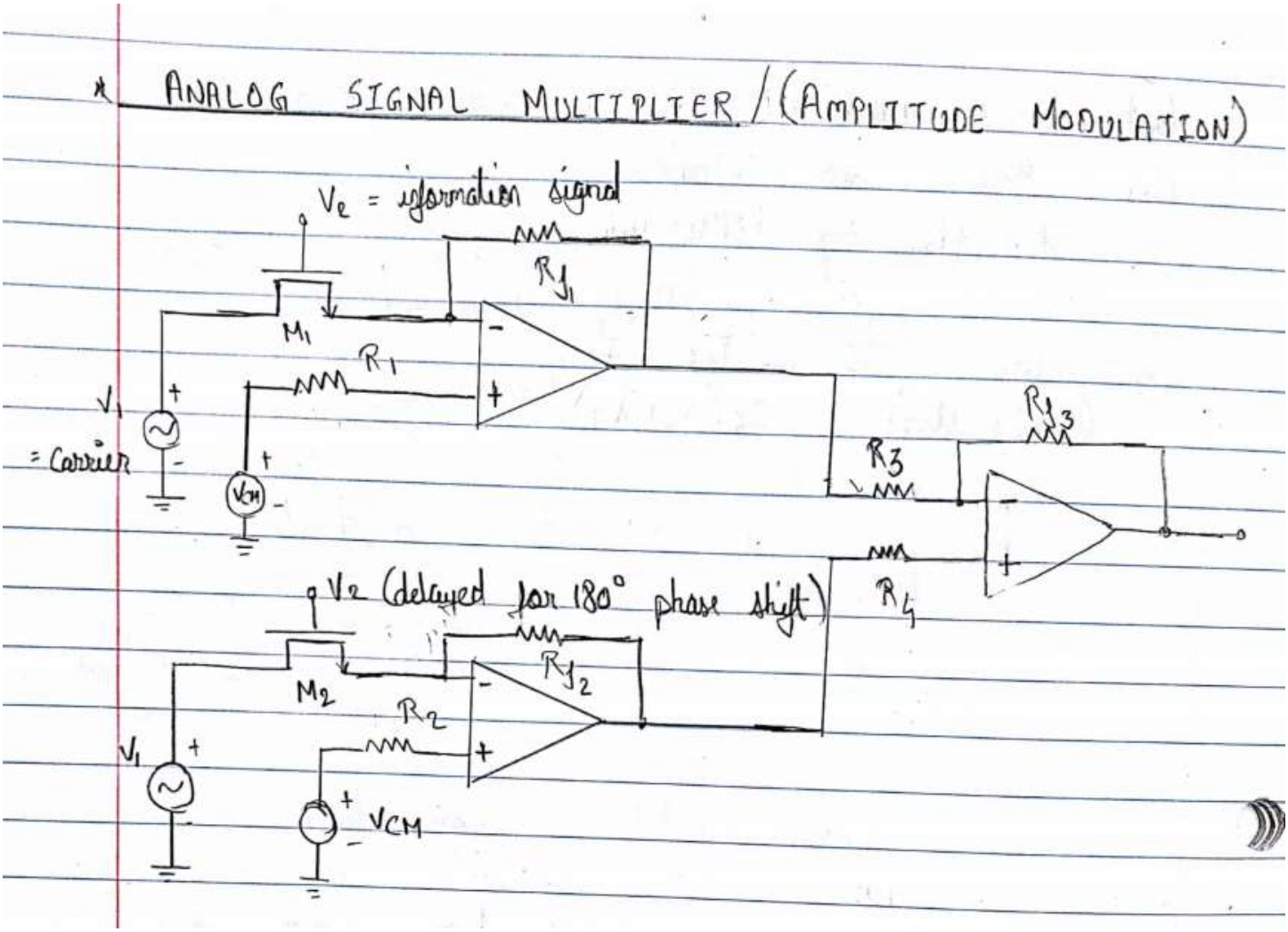
Problem Statement:

The project is aimed at designing an analog signal multiplier/AM-modulator using a OP-AMP designed for a gain of 60 dB. The multiplication is achieved by using a a MOSFET in Triode region whose resistance varies with the input information signal. Thus it provides for a basic multiplier with a simple topology and low power dissipation. The Op-amp needs to have a high CMRR to achieve a good multiplication of the signals.



Design Specifiaction of Op-amp:

Differential voltage gain: Avd ≥ 60dB.

Output voltage swing range: OVSR = Vo(max) - Vo(min) ≥ 2V.

Slew rate: SR ≥ 20 V/µS into 2 pF.

Input common mode max: 3.0V

Input common mode min: 1.2V

Common mode rejection ratio: CMRR ≥ 60 dB.

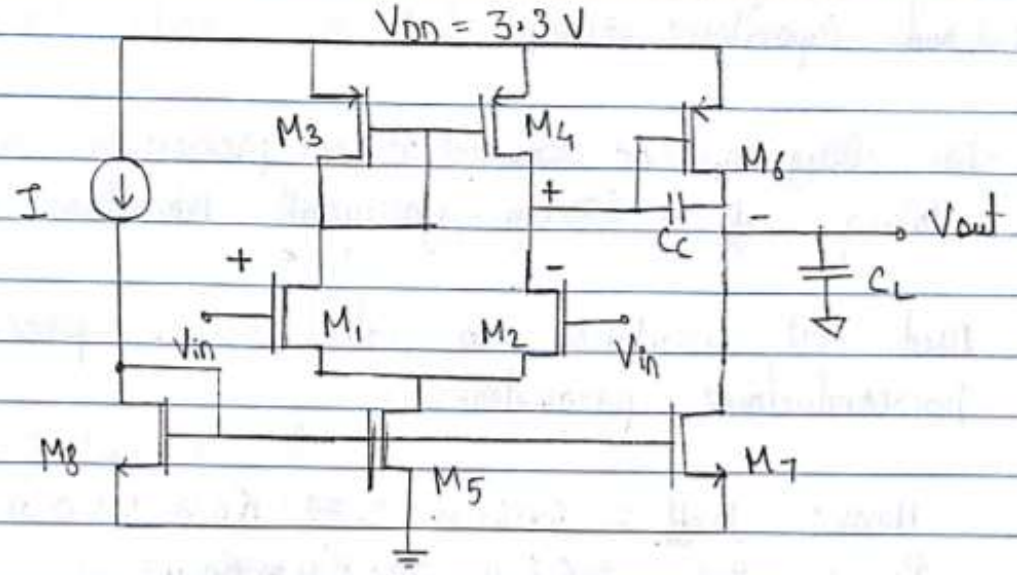
Unity Gain-bandwidth: GB ≥ 30 MHz with a 2 pF load capacitance.

Phase Margin: f(GB) ≥ 60° with a 2 pF load capacitance.

Power dissipation: Pdiss ≤ 1mW.

Op-amp Design procedure:

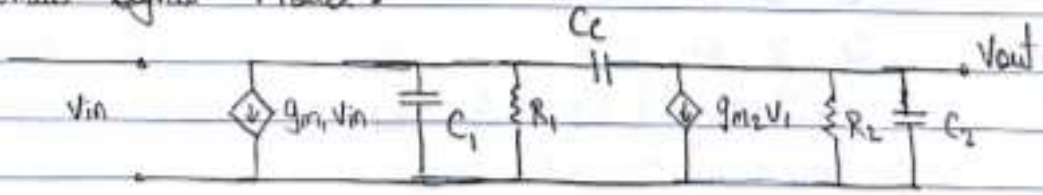
OP-AMP DESIGN :



Let $R_1 = r_{o4} \parallel r_{o2}$ $\quad C_1 = C_{gs6} + C_{DS4} + C_{DS2}$

$R_2 = r_{o6} \parallel r_{o7}$ $\quad C_2 \approx C_L$

Small signal Model :



* OP-AMP target specifications :

i) DC gain $\geq$ 60 dB
ii) Gain bandwidth product GBW $\geq$ 30 MHz
iii) Phase Margin $\geq$ 60°
iv) Slew Rate $\geq$ 20 V/μs

v) $V_{DD} = 3.3\,V$

vi) Power dissipation $\leq 1mW$

vii) Load capacitance $= 2pF$

viii) ICMR Max $= 3.0\,V$

ix) ICMR Min $= 1.2\,V$

→ For Designing we use 350 nm process
taking Leff = 500 nm for all transistors

- used Test simulation to calculate the process transconductance parameters

- Nmos: $\beta_{eff} = 2.161\,m \Rightarrow K'_n \approx 220\,u$
- Pmos: $\beta_{eff} = 566.6\,u \Rightarrow K'_p \approx 60\,u$

→ Now first we choose a value for Compensation capacitor for a phase margin $\geq 60°$

$\therefore C_c \geq 0.22 \times C_L$

$C_c \geq 0.22 \times 2$

$C_c \geq 0.44\,pF$

$\therefore$ choose $\boxed{C_c = 0.8\,pF}$

→ Next we find the tail current I_5 for the differential input stage from the Slew Rate condition

$\therefore SR = \frac{I_5}{C_c}$

$\therefore I_5 = SR \times C_c$

$\therefore I_5 = 120 \times 10^6 \times 0.8 \times 10^{-12}$

$I_5 = 16 \times 10^{-6}$ A

$\therefore$ we choose a tail current $\boxed{I_5 = 20\,\mu A}$

To get (W/L) of input transistors M_1 and M_2 we use the gain bandwidth product specification

$$\therefore GBW = \frac{g_{m1}}{C_c}$$

$$\therefore GBW(\text{in Hz}) = \frac{g_{m1}}{C_c \times 2\pi}$$

$$\therefore g_{m1} = GBW \times C_c \times 2\pi$$

$g_{m1} = 30 \times 10^6 \times 0.8 \times 10^{-12} \times 2\pi = 150\,\mu S$

$\therefore$ we set a target $\boxed{g_{m1} \approx 160\,\mu S}$

Now we know that $I_{D1} = \frac{I_{D5}}{2} = \frac{20\mu}{2} = 10\,\mu A$

also $g_m = \sqrt{2\beta I_{D1}}$

$160\mu = \sqrt{2 \times \beta \times I_{D1}}$

$\therefore (160)^2 \times 10^{-12} = 2 \times K'_n (W/L)_1 \times 10 \times 10^{-6}$

$$\therefore \left(\frac{W}{L}\right)_{1,2} = \frac{160^2 \times 10^{-12}}{2 \times 220 \times 10^{-6} \times 10 \times 10^{-6}}$$

$= 5.81 \sim$

$$\boxed{\left(\frac{W}{L}\right)_{1,2} \approx 6}$$

Next we utilize the ICMR max range of 3.0V to get the $(W/L)_{3,4}$

$$I_{CMR\ max} = 3.0V$$

$$\therefore V_{DD} - V_{SG3} + V_{TH_1} = 3.0$$

$$V_{SG3} = \sqrt{\frac{2I_{D3}}{\beta_P}} + |V_{THP}|_{max}$$

$$\therefore V_{DD} - \sqrt{\frac{2I_{D3}}{\beta_P}} - |V_{THP}|_{max} + V_{TH_1}{}_{max} = 3.0$$

$$V_{DD} - 3.0 - |V_{THP}|_{max} + V_{TH_1} = \sqrt{\frac{2I_{D3}}{\beta_P}}$$

$$(3.3 - 3.0 - |V_{THP}|_{max} + V_{TH_1})^2_{max} = \frac{2I_{D3}}{K'_P (W/L)_3}$$

$$\therefore (W/L)_3 = \frac{2I_{D3}}{K'_P (0.3 - |V_{THP}| + V_{TH_1})^2}$$

from Test simulation we get

$|V_{THP}|_{max} = 720mV$

and $V_{TH_1\ max} = 600mV$

$$\therefore (W/L)_{3,4} = \frac{2 \times 10 \times 10^{-6}}{60 \times 10^{-6} (0.3 - 0.72 + 0.6)^2}$$

$$= 10.28$$

$$\boxed{(W/L)_{3,4} \approx 11}$$

Similarly we can use ICMR min to get the $(W/L)_5$

$\therefore$ ICMR min = 1.2 V

$\therefore$ ICMR min $= V_{OVE} + V_{GS1}$

$$= \left[\sqrt{\frac{2I_{D1}}{\beta_1}} + V_{TH1}\right] + V_{Dsat5}$$

$$= \sqrt{\frac{2I_{D1}}{\beta_1}} + V_{TH1} + V_{Dsat5}$$

$$\therefore V_{Dsat5} = \text{ICMR min} - \sqrt{\frac{2I_{D1}}{\beta_1}} - V_{TH1}$$

$$= 1.2 - \sqrt{\frac{2\times10}{220\times6}} - V_{TH1}$$

$$= 1.2 - 0.13 - 0.91$$

$$= 0.167 \text{ V}$$

$V_{Dsat5} \approx 0.17$ V

$$\therefore I_{D5} = \frac{\beta}{2}(V_{Dsat5})^2$$

$$20 = \frac{K'_n}{2}(W/L)_5 (V_{Dsat5})^2$$

$$40 = 220 \times (0.17)^2 (W/L)_5$$

$$\therefore \left(\frac{W}{L}\right)_5 = 7$$

Design of M6

→ for 60° phase margin

$g_{m6} \geq 10 g_{m1}$

$g_{m6} \geq 10 \times 160 \times 10^{-6}$

$g_{m6} \geq 1600\ \mu S$

→ for proper mirroring we want

$V_{DSM3} = V_{DS4} \approx V_{DSM6}$

$V_{GSM3} = V_{GSM4} \approx V_{GSM6}$

$$I_{D6} = \frac{\mu_p C_{ox}}{2}\left(\frac{W}{L}\right)(V_{GS} - |V_{THP}|)^2$$

$$\therefore \frac{(W/L)_6}{(W/L)_4} = \frac{I_{D6}}{I_{D4}} = \frac{g_{m6}}{g_{m4}}$$

$$\therefore g_{m4} = \sqrt{2\beta I_{D4}}$$

$$= \sqrt{2 \times \mu_p C_{ox} \times 11 \times 10 \times 10^{-6}}$$

$g_{m4} = 114.89\ \mu S$

$\boxed{g_{m4} \approx 115\ \mu S}$

$$(W/L)_6 = \frac{g_{m6}}{g_{m4}} \times (W/L)_4$$

$$= \frac{1600 \times 10^{-6}}{115 \times 10^{-6}} \times 11$$

$= 153.04$

$\boxed{(W/L)_6 \approx 154}$

Now,

$$\frac{I_6}{I_4} = \frac{(W/L)_6}{(W/L)_4}$$

$$\therefore I_{D7} = I_{D6} = \frac{(W/L)_6 \times I_{D4}}{(W/L)_4}$$

$$= \frac{154 \times 10 \times 10^{-6}}{11}$$

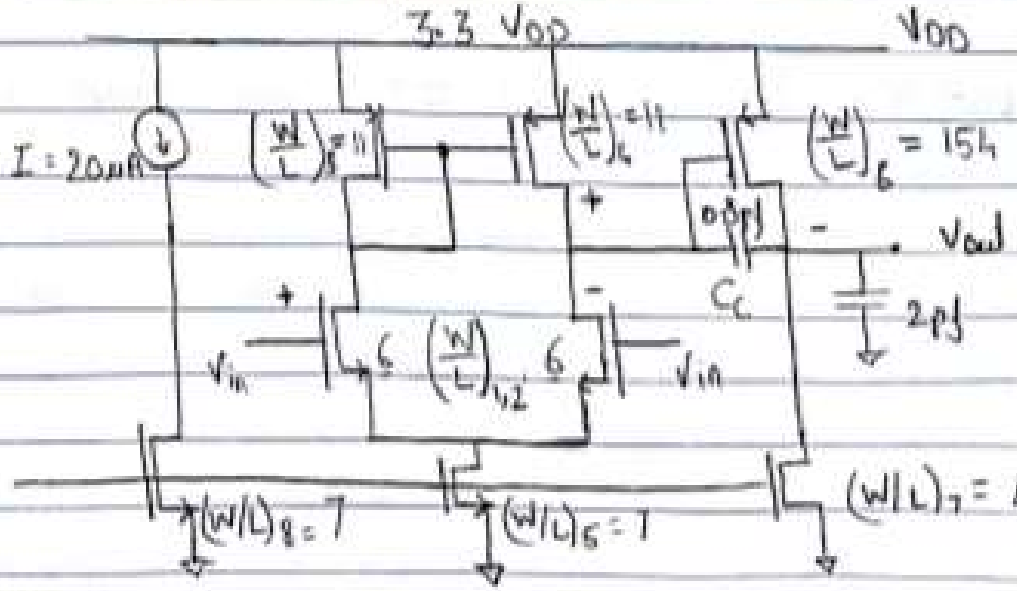
$$\boxed{I_{D6} = 140\ \mu A}$$

also $$\frac{I_7}{I_5} = \frac{(W/L)_7}{(W/L)_5}$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_{D7} \times (W/L)_5}{I_{D5}}$$

$$= \frac{140 \times 7}{20}$$

$$\boxed{(W/L)_7 = 49}$$



- Power dissipation $= V_{DD} \times I_{Total}$

  $= V_{DD} \times (20\mu + 20\mu + 140\mu)$

  $= 3.3 \times 200\mu$

  $= 660\mu W$

  Power dissipation $= 0.6\ mW$

* Poles and zeros

- $P_1 = \dfrac{1}{g_{m6} \cdot (r_{o2} \| r_{o4})(r_{o6} \| r_{o7}) \times C_c} = \dfrac{-1}{1600\mu \times 277k \times 20.42k \times 1.5}$

  $P_1 = 104.55\ kHz$

- $P_2 = \dfrac{g_{m6}}{C_L} = \dfrac{1600\mu}{2p} = 800\ MHz$

- R.H.P zero $= \dfrac{g_{m6}}{C_c} = \dfrac{1600 \times 10^{-6}}{1.5 \times 10^{-12}}$

  $= 1.066\ GHz$

* Gain of stage 1:

- $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$ $\quad \lambda_n = 0.11$, $\lambda_p = 0.25$

$= \frac{2 g_{m1}}{I_5(\lambda_2 + \lambda_4)}$

$= \frac{2 \times 160\,\mu}{20\,\mu(0.25 + 0.11)}$

$A_{v1} = 44.44$

- $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}}$

$= \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$

$= \frac{1600}{140(0.25 + 0.11)}$

$A_{v2} = 31.74$

∴ Total open loop gain $A_{v(o)} = A_{v1} \cdot A_{v2}$

$= 44.44 \times 31.74$

$\therefore A_{v(o)} = 1410.79$

$A_{v(o)} = 20 \log (1410.79)$

$= 62.98$ dB

$\boxed{A_{v(o)} \approx 63 \text{ dB}}$

* OUTPUT VOLTAGE SWING:

$V_{out\,min} = V_{OV7}$

$= V_{Dsat\,7}$

$= \sqrt{\frac{2I_{D7}}{\beta}}$

$= \sqrt{\frac{2 \times 140}{220 \times 49}}$

$\boxed{V_{out\,min} = 161\ mV}$

$V_{out\,max} = V_{DD} - V_{Dsat\,6}$

$V_{Dsat\,6} = \frac{2I_D}{g_m}$

$= \frac{2 \times 140}{1600} = 175\ mV$

$\boxed{V_{out\,max} = 3.3 - 0.175 = 3.125\ V}$

∴ Total output voltage swing = $V_{out\,max} - V_{out\,min}$

$= 3.125 - 0.161$

$\boxed{\text{Total output voltage swing} = 2.964\ V}$

* CMRR :

- Common mode gain
- Using Half circuit analysis

we get $A_{CM} = \dfrac{r_{o4}/2}{\dfrac{1}{2g_{m2}} + r_{o5}}$

- From Cadence test simulation we get

$\lambda_2 = 0.20 \quad \lambda_4 = 0.24 \quad \lambda_5 = 0.11$

$\lambda_6 = 0.25 \quad \lambda_7 = 0.11$

$$\therefore A_{CM} = \frac{1}{\dfrac{2\lambda_4 I_{D4}}{2g_{m2}} + \dfrac{1}{\lambda_5 I_{D5}}} = \frac{1}{\dfrac{2 \times 0.24 \times 10 \times 10^{-6}}{2 \times 160 \times 10^{-6}} + \dfrac{1}{0.11 \times 20 \times 10^{-6}}}$$

$A_{CM} = 0.155$

$\therefore A_{CM} = 20 \log (0.155)$

$\boxed{A_{CM} = -6.83 \text{ dB}}$

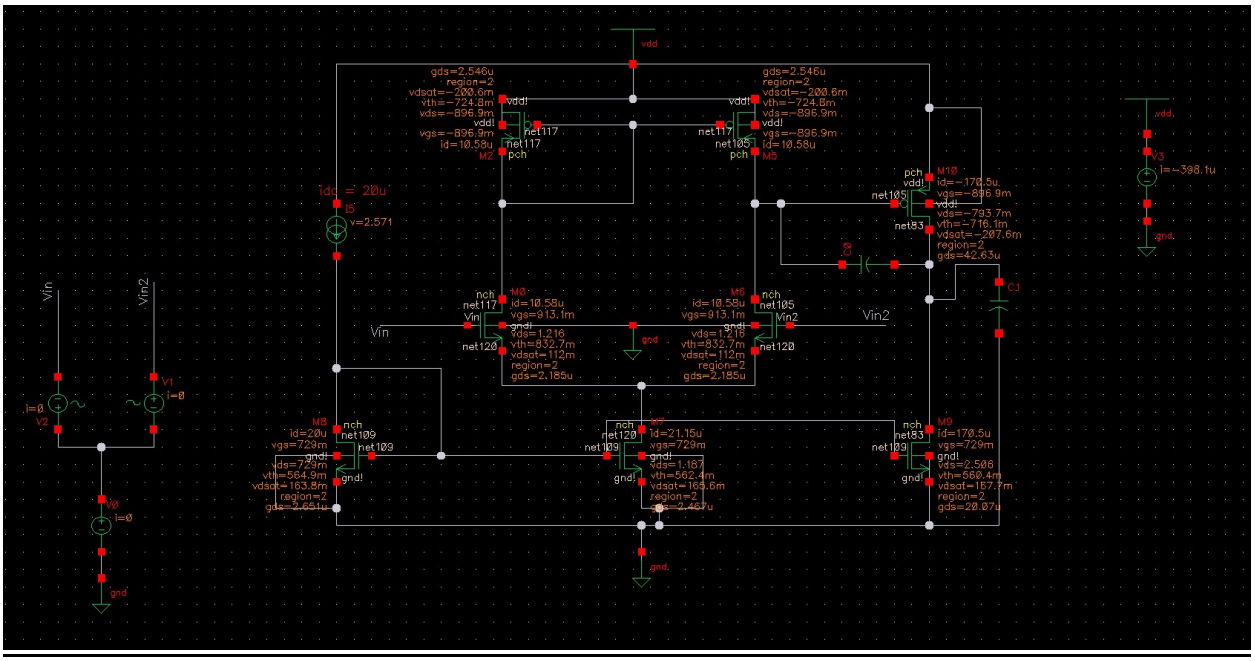
$\therefore CMRR = \text{gain (dB)} - A_{CM}\text{(dB)}$

$= 63 + 6.83$

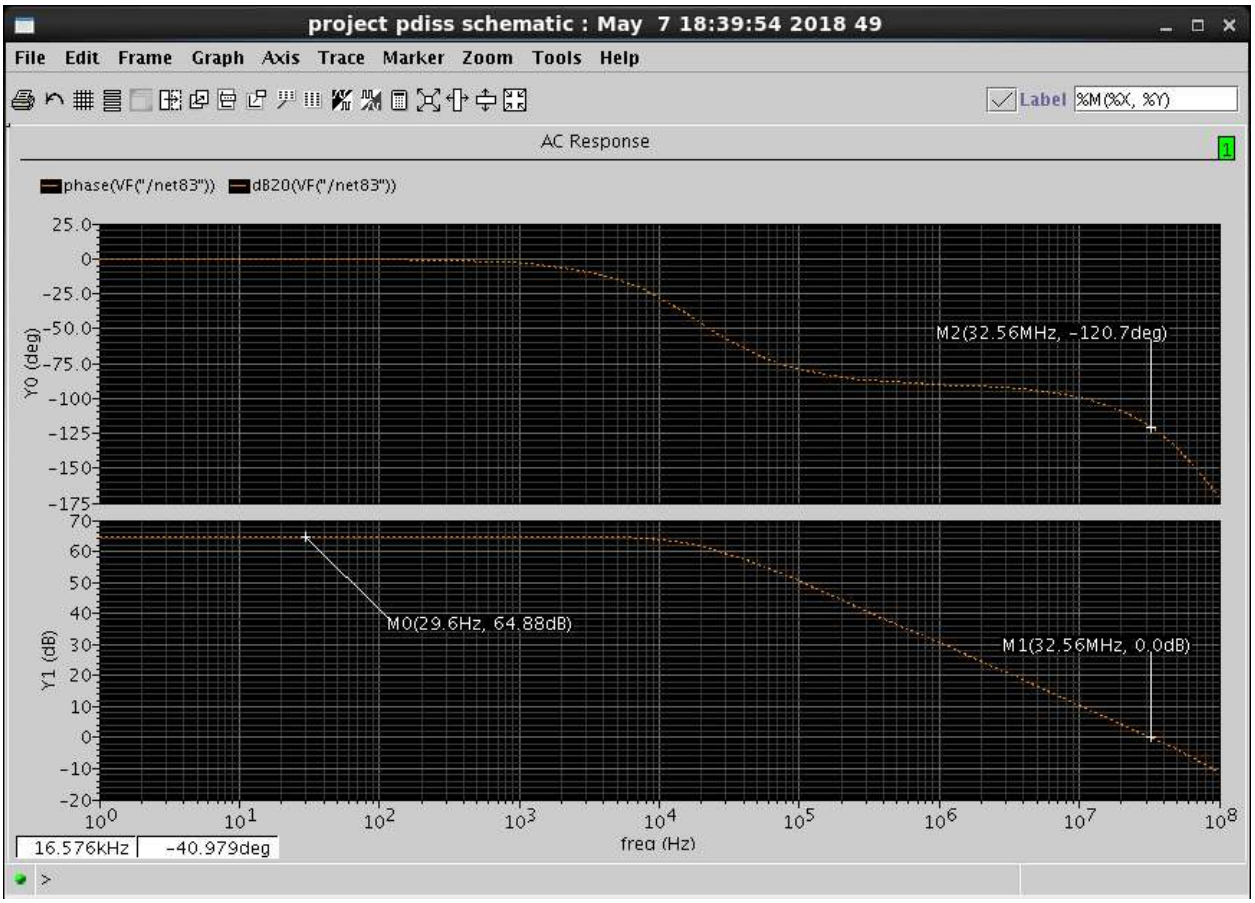
$\boxed{CMRR = 69.83 \text{ dB}}$

Op-amp SIMULATIONS:

Schematic



Frequency response, Phase Margin, Gain Bandwidth



From the Above plots we see the differential gain **Adm=64.88 dB, GBW=32.56 MHz,**

Phase Margin= -180-(-120.7)=59.3 degree

Slew Rate:

* Positive Slew Rate from simulation:

Lower pulse voltage = 1.2 V
upper pulse voltage = 3.0 V

10% of lower pulse = 1.2 + 0.12
= 1.32 V

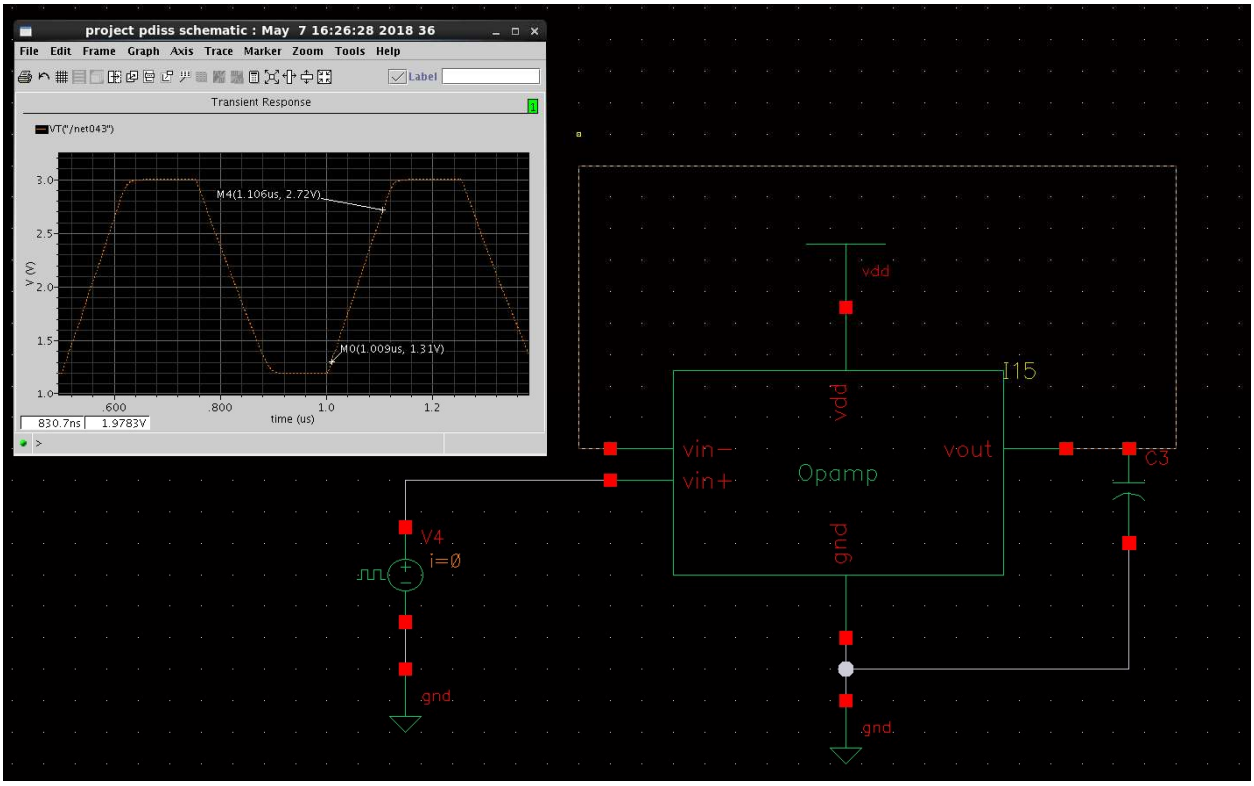
10% of upper pulse voltage = 3.0 - 0.3
= 2.7

∴ Positive slew rate = $\frac{2.7 - 1.32}{1.106u - 1.009u}$
= 14.22 V/us

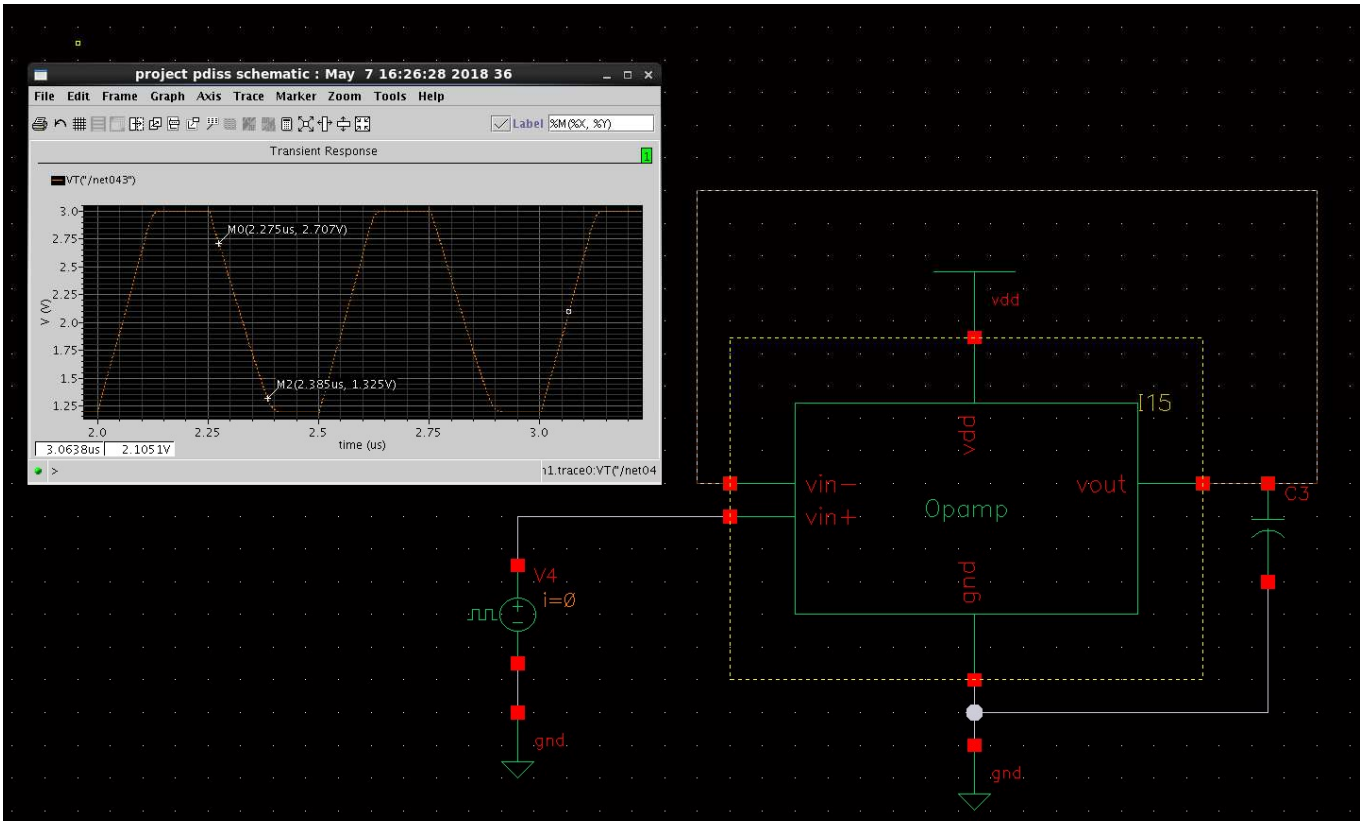
Negative slew rate = $\frac{2.7 - 1.32}{2.275 - 2.385}$
= 12.54 V/us

Total Slew Rate = 13.38 V/us

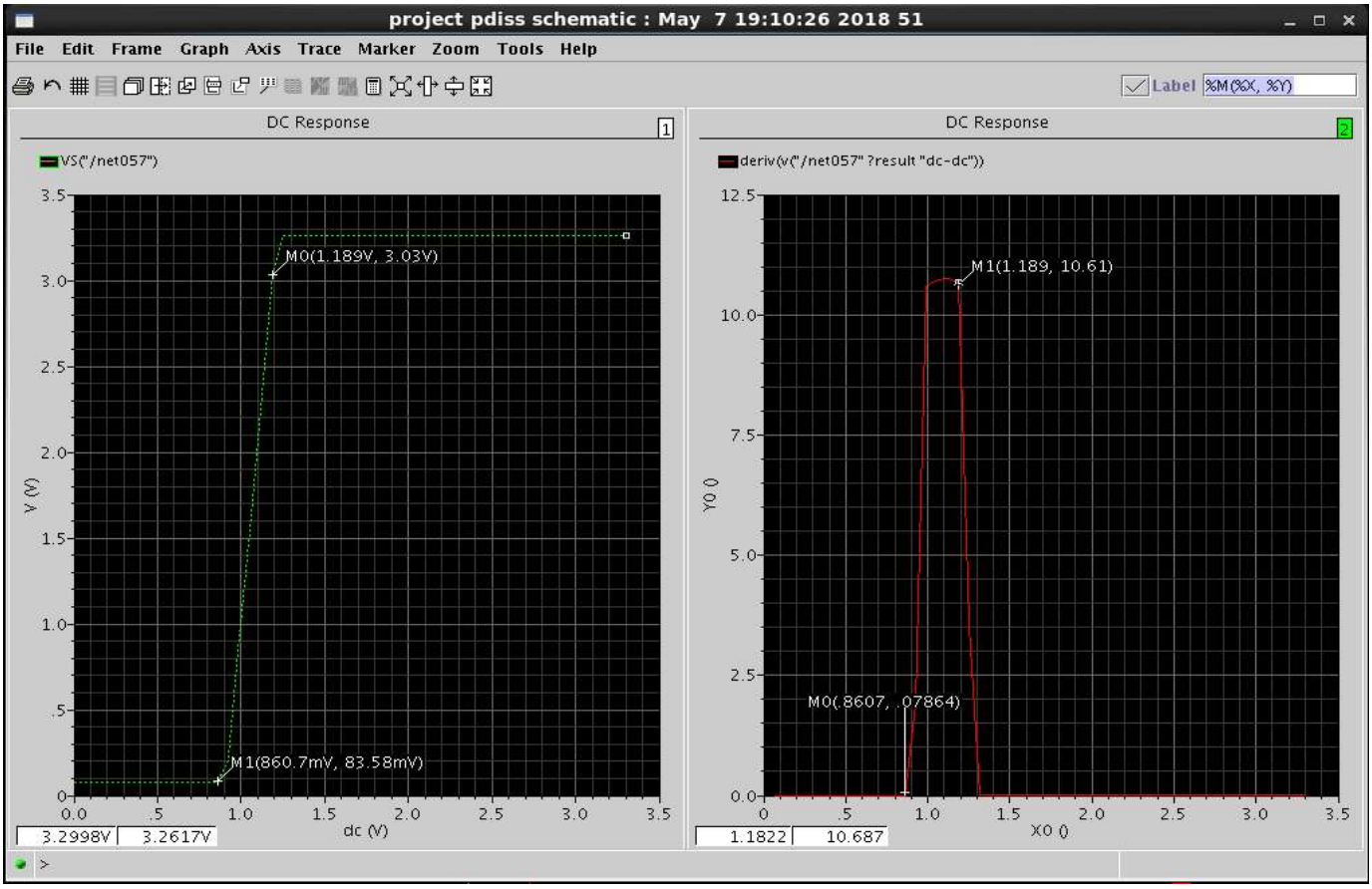
Positive Slew rate: 14.22 V/us



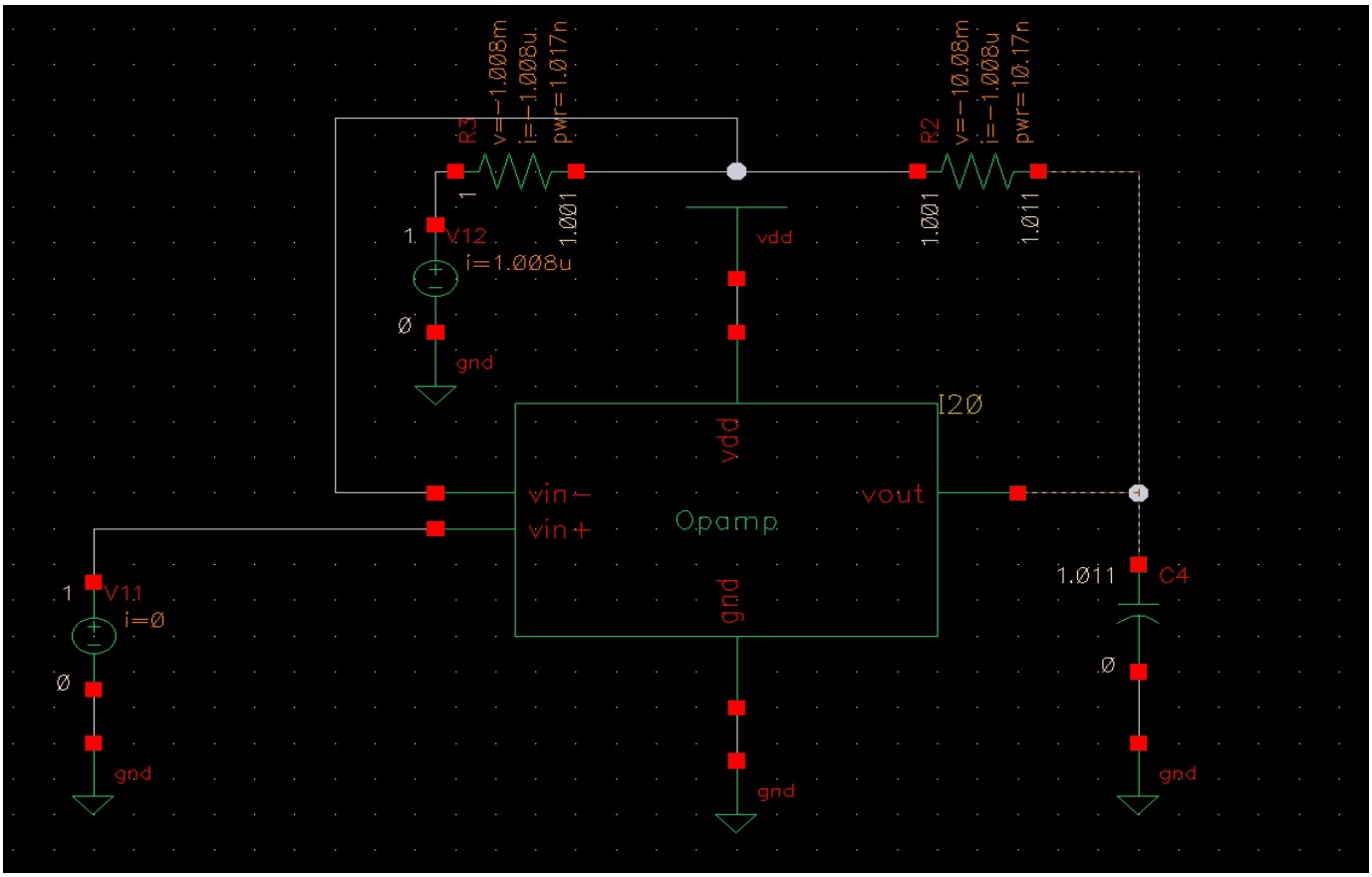
Negative Slew Rate: 13.38 V/us



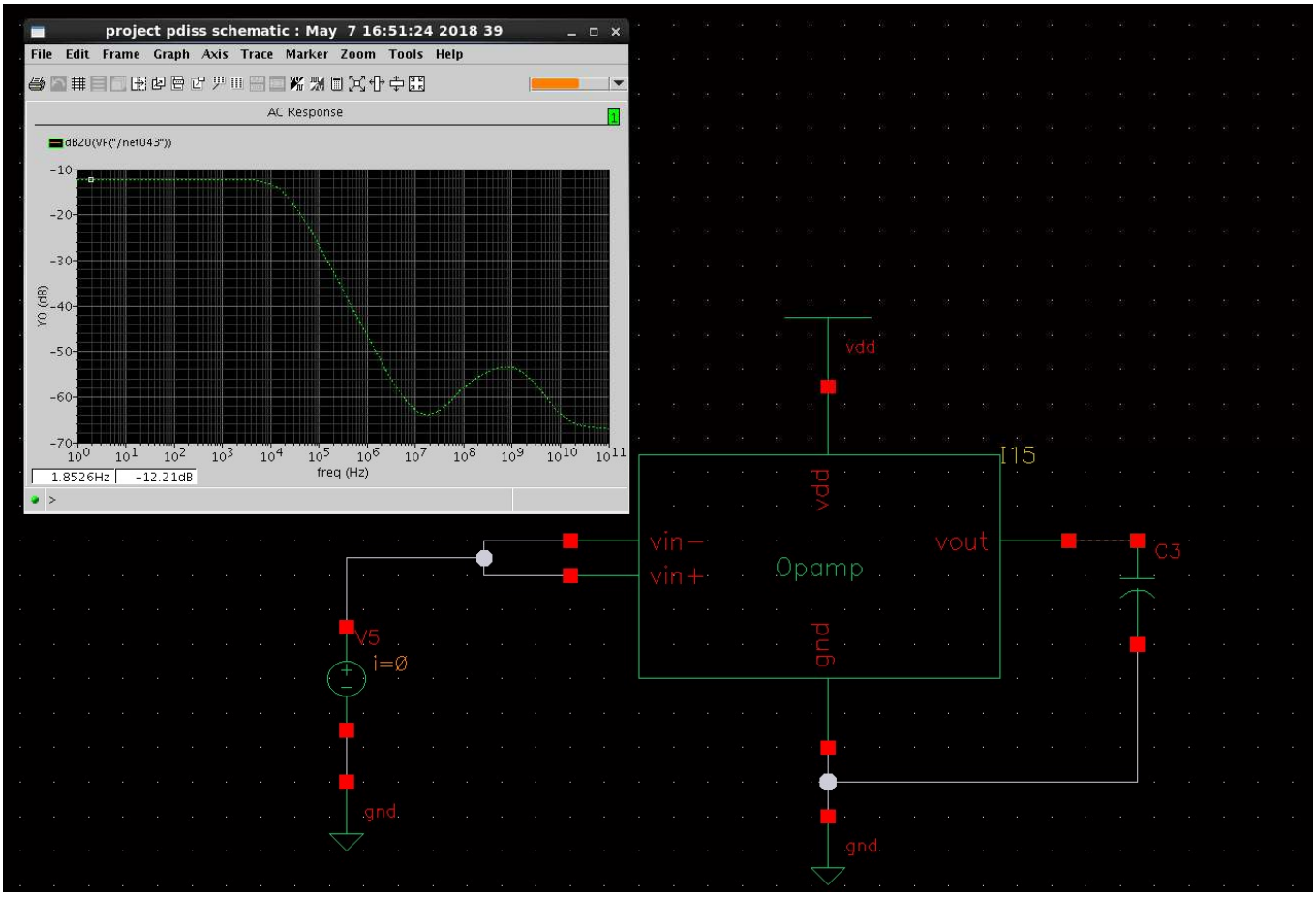
Output Voltage Swing:



We see that the output voltage Vomax is 3.03V and Vomin is 0.0835V. Total OVSR=2.9465 V



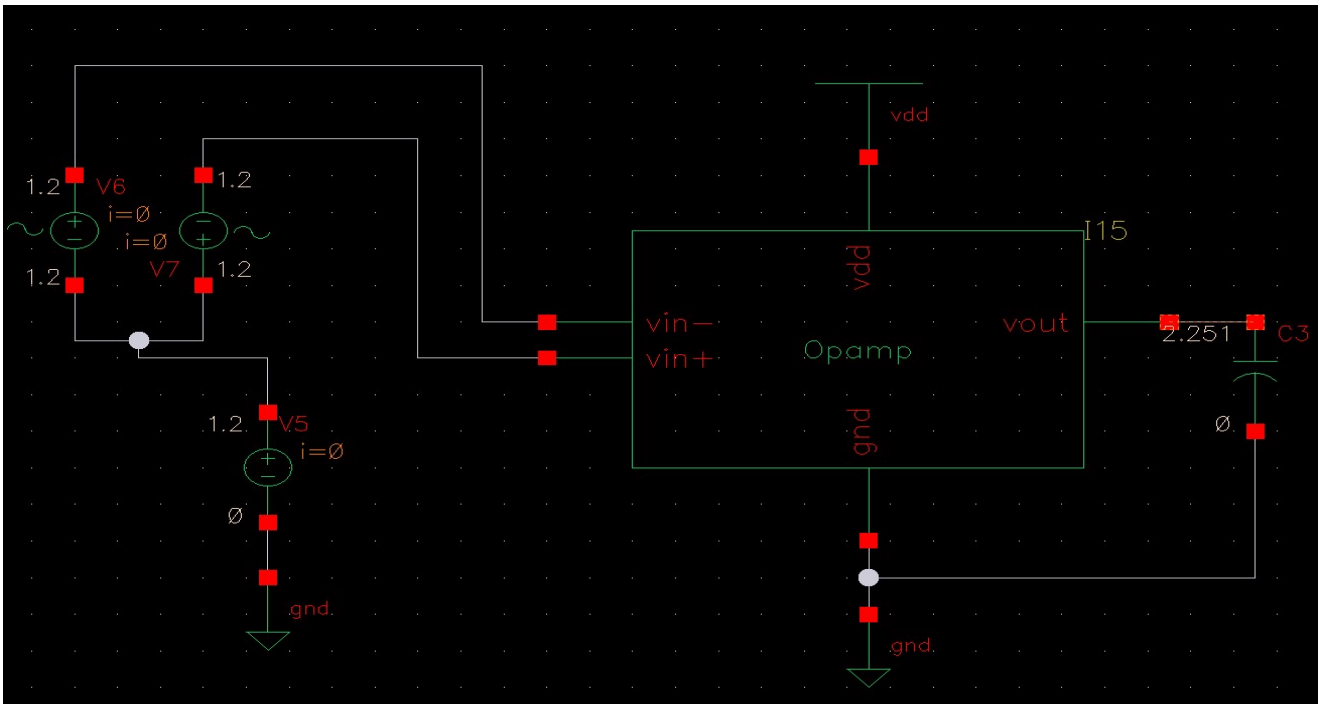
Common Mode Gain:

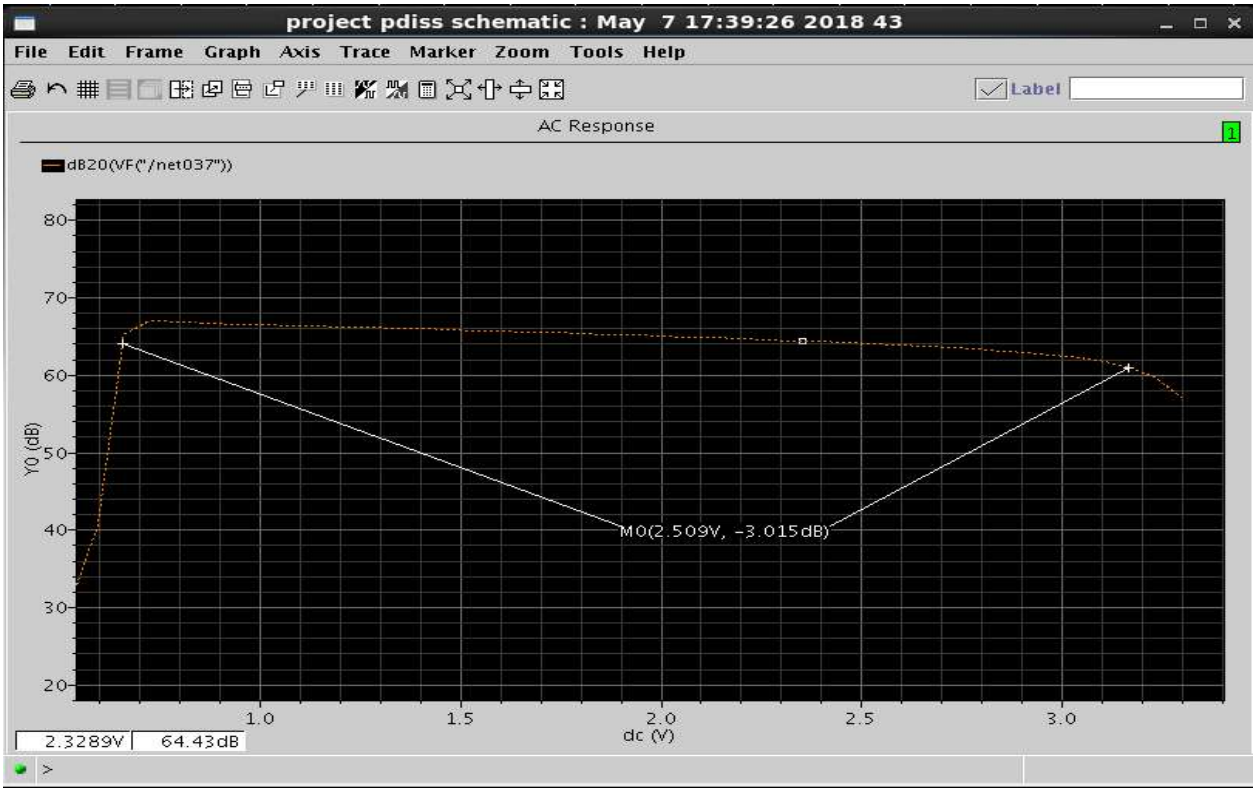


We get a **common mode gain of -12.21 dB** from simulations.

CMRR=64.88-(-12.21)=77.09 dB

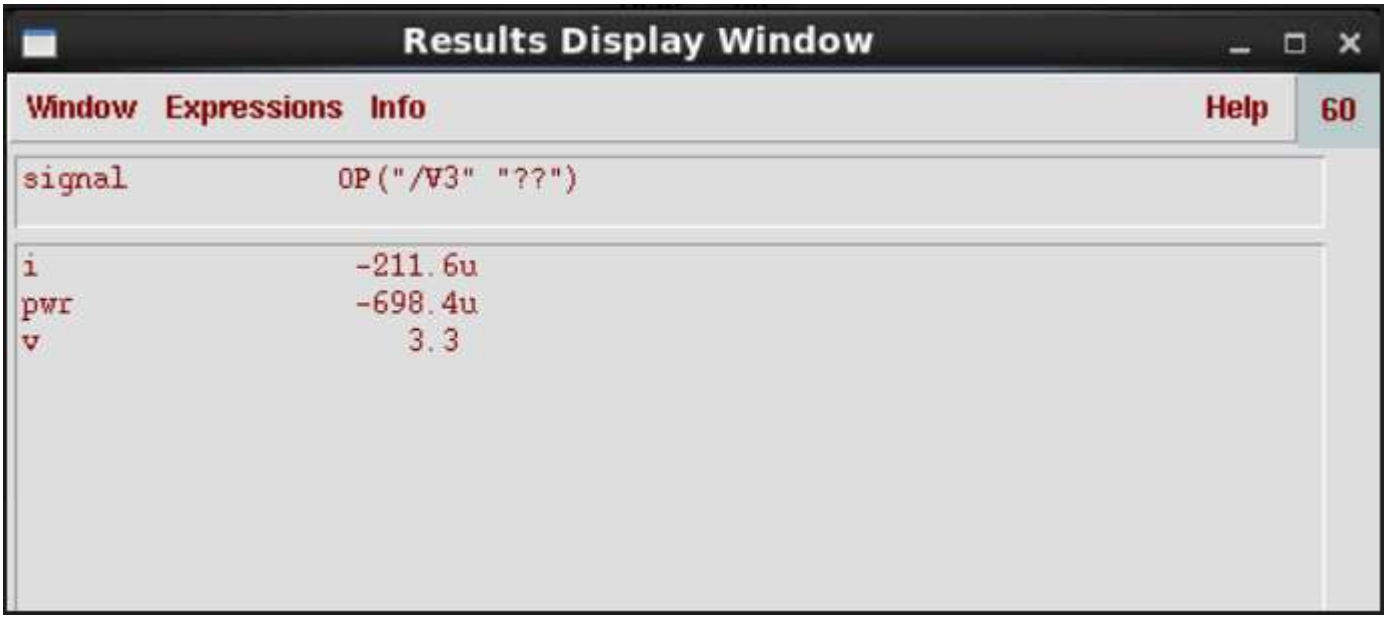
Input Common Mode Range ICMR:





We see a minimum **ICMR of 2.509V** for which the gain stays in the 3 dB range of its value where **Avdm=64.88 dB**

Power Dissipation:



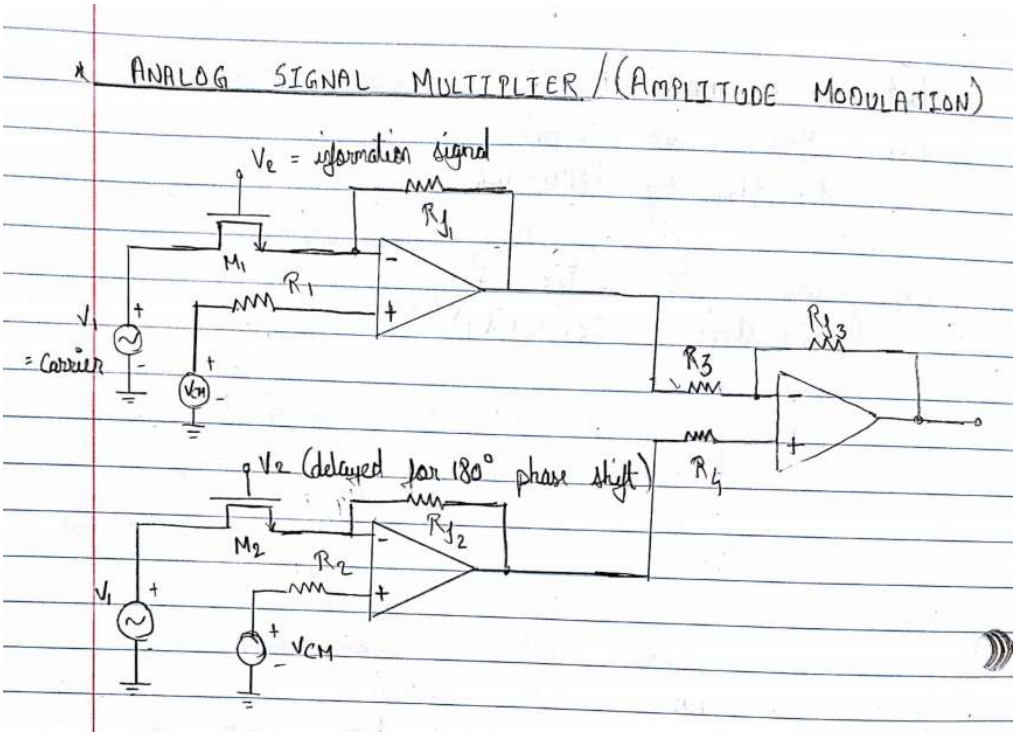
Correlation of Simulation and Hand Calculation:

Parameter	Hand-Calculation	Simulation
Differential voltage gain	63 dB	64.88 dB
Output voltage swing range	Vomin: 0.161V Vomax: 3.125V OVSR: 2.964V	Vomin: 0.083V Vomax: 3.03V OVSR: 2.947V
Phase Margin: f(GB)	60°	59.3°
Unity Gain-bandwidth: GB	30 MHz	32.56 MHz
Slew rate:	20 V/us	13.3 V/us
Input common mode max	3.0 V	3.15 V
Input common mode min	1.2 V	0.7 V
Common mode rejection ratio: CMRR	69.83 dB	77.09 dB
Power dissipation	0.69 mW	0.692 mW

Parameters Tweaked after Simulation:

1. Initial gain achieved was 55 dB → Increased the size of input transistors to increase gm1 and thus the gain.
2. Phase Margin achieved was 60° → increased the Compensation capacitor Cc to 1.5 pF to get a better phase margin at the cost of Slew rate.
3. Slew rate is less then target value as the Compensation capacitor Cc was increased.

Multiplier Theory Of Operation:



The multiplication is achieved by transistors M1 and M2 operating in the Triode region. The Drawback of the circuit is that multiplication for signals less than 1mV in amplitude with a carrier of amplitude less than 1mV cannot give a efficient output waveform. For uV level signal multiplication we need to design a more sensitive Op-amp.

The frequency ratio is also important here and the multiplier works for signals with frequency ratio f1/f2 less than 1/100.

The gain of the Op-amp of which is greater than 1000 limits the upper value of amplitude that can be multiplied to a few mV

The amplitude of the carrier has to be always greater than the amplitude of information signal.

The resistors $Rf_{(1,2)}R_{(1,2)}$ are chosen such that the ratio is $Rf_{(1,2)}/R_{(1,2)}$ =1/100

The size of M1 and M2 is chosen to be large as they are the input stage for the Op-amp and have to provide a larger range of operation.

$(W/L)_{1,2}$ = 200

The resistors in the Difference amplifier stage are chosen to cancel out this ratio in the final output signal. i.e $Rf_{(3)}/R_{(3,4)}$=100.

Here we have taken

Carrier: v1=a1.cos($2\pi f1t$), where f1=100 kHz, a1= 10mV

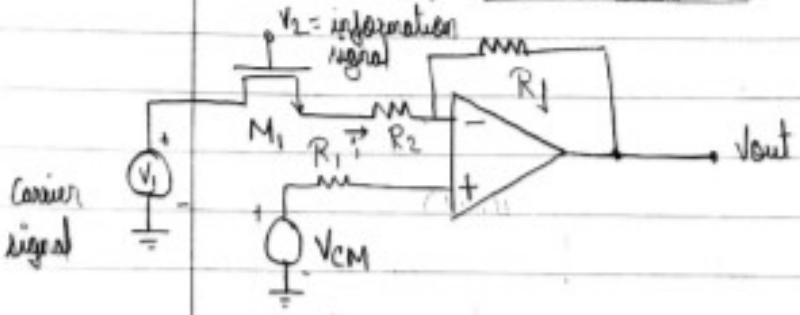
Modualting Signal: v2=a2.cos($2\pi f2t$), where f2=1kHz, a2= 5mV

V_{CM}=2.1V, V_{Th}=0.573V

Thus we Select VG0 such that we can eliminate the common mode term from the output signal.

$V_{G0}=V_{CM}+V_{Th}$=2.1+0.573=2.573V

* ANALOG MULTIPLIER :



- FOR operation of the circuit as a Multiplier we have to maintain the transistor M_1 in triode region
- To get Multiplication operation we have to change this resistance with respect to the information signal

$$i = \frac{\beta}{2}\left[2(V_G - V_{DS} - V_T)V_{DS} - V_{DS}^2\right]$$

Let $V_1 = A_1 \cos(\omega_1 t)$ where $f_1 = 100 \times 10^3$ Hz
$V_1 = A_1 \cos \omega_1 t$ i.e carrier frequency
and $V_2 = A_2 \cos \omega_2 t$ $f_2 = 1 \times 10^3$ Hz
i.e information signal frequency

$$I_{D_1} \simeq \frac{\beta}{2}\left\{\left[2(V_{GS} - V_T - |V_{DS}|)\right]|V_{DS}| - |V_{DS}|^2\right\}$$

Now, $V_{GS} = V_2 + V_{GO} = A_2 \cos(\omega_2 t) + V_{GO}$
where V_{GO} is the DC voltage such that M_1 is

in linear region of operation and the V_{CM} of V_1 is such that it satisfies the DC voltage requirement of the OP-AMP.

$|V_{D,S}| = V_1 = A_1 \cos \omega_1 t$

$$\therefore I_{D_1} = \frac{\beta}{2}\left[2(V_2 + V_{GD} - V_1 - V_{CM} - V_T)\right]V_1 - \frac{\beta V_1^2}{2}$$

$$= \beta\left[\{(V_{GD} - V_{CM} - V_T) + (V_2 - V_1)\}\right]V_1 - \frac{\beta V_1^2}{2}$$

$$= \beta(V_{GD} - V_{CM} - V_T)V_1 + \beta V_2 V_1 - V_1^2 - \frac{\beta}{2}V_1^2$$

$$I_{D_1} = \beta(V_{GD} - V_{CM} - V_T)V_1 + \beta V_2 V_1 - \frac{3\beta}{2}V_1^2$$

$$V_{out_1} = \left[\beta(V_{GD} - V_{CM} - V_T)V_1 + \beta V_2 V_1 - \frac{3\beta}{2}V_1^2\right].R_d$$

- Now to eliminate the $\beta(V_{GD} - V_{CM} - V_T)V_1$ term we set the DC voltage at gate of M_1 such that $V_{GD} = V_{CM} + V_{TH_1}$

- To eliminate the $-\frac{3}{2}\beta V_1^2$ term from V_{out_1} expression we apply a 180° phase shifted information signal

$\therefore V_2 = A_2 \cos(\omega_2 t + 180°)$

$V_2 = -A_2 \cos \omega_2 t$

Now, now

$$I_{D_2} = \beta(V_{GD} - V_{CM} - V_T)V_1 - \beta V_2 V_1 - \frac{3}{2}\beta V_1^2$$

$$V_{out2} = \left[\beta(V_{GO} - V_{CM} - V_T)V_1 - \beta V_2 V_1 - \frac{3\beta V_1^2}{2}\right] \cdot R_f$$

Therefore the signals V_{out1} and V_{out2} have

by setting $V_{GO} = V_{CM} + V_T$

we Let $\beta(V_{GO} - V_{CM} - V_T)V_1 \longrightarrow 0$

$$\therefore V_{out1} = \left[\beta V_1 V_2 - \frac{3}{2}\beta V_1^2\right] \cdot R_f$$

$$V_{out2} = \left[-\beta V_1 V_2 - \frac{3}{2}\beta V_1^2\right] \cdot R_f$$

Therefore by passing the signals through a difference amplifier configuration of op-amp we

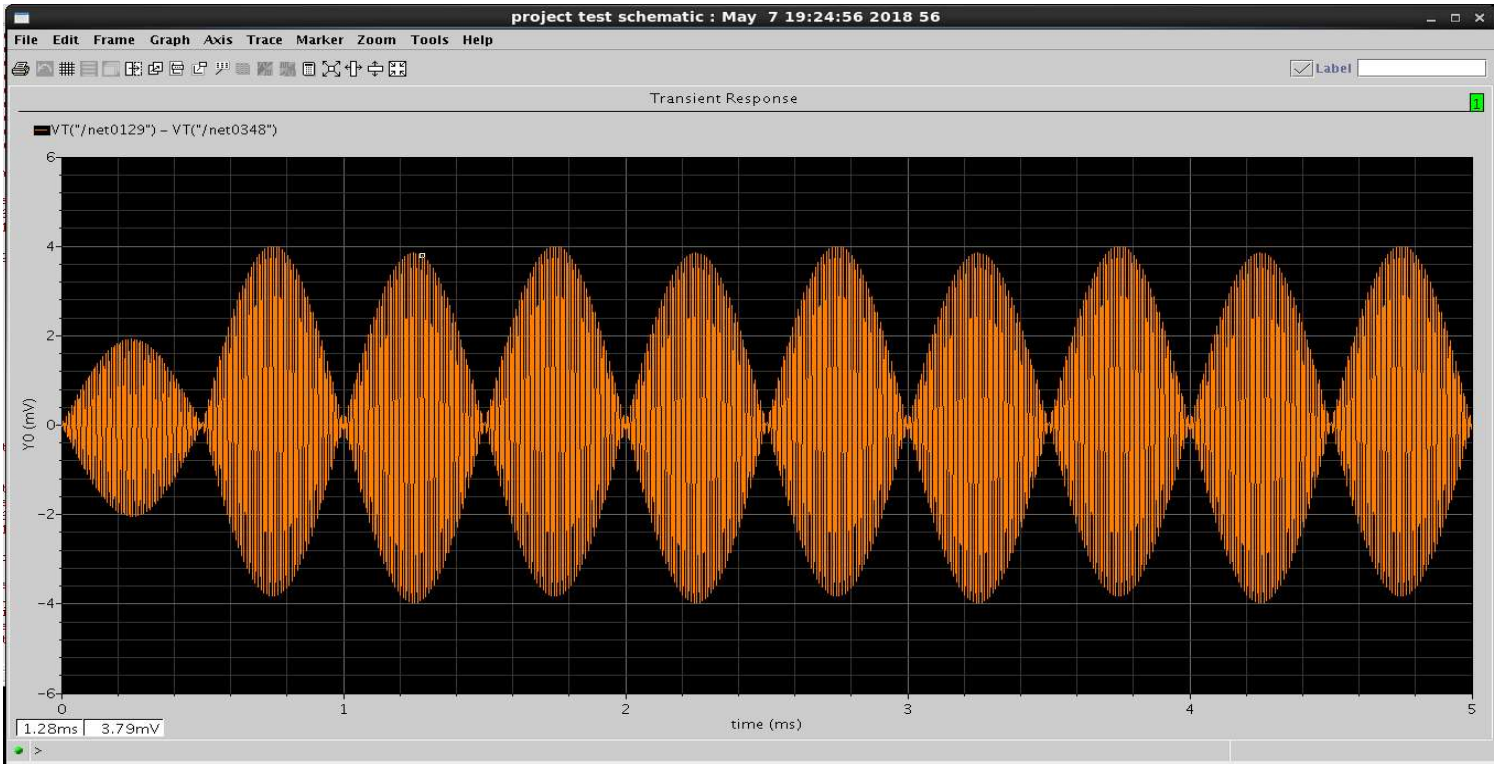
eliminate the Common mode term $-\frac{3}{2}\beta V_1^2$

and the product terms are differential with equal amplitude but opposite phase.

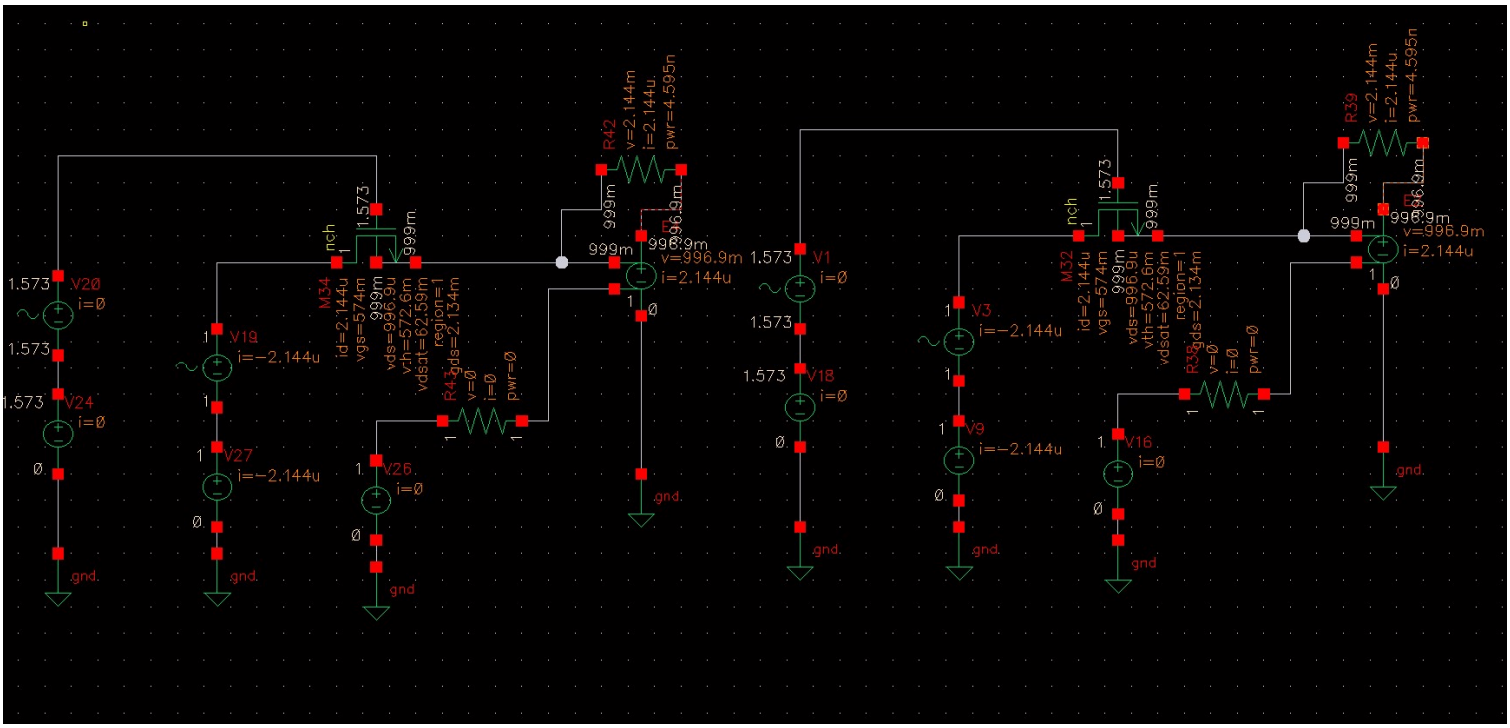
Hence at the output of the difference amplifier we get a $\boxed{V_{out} = -\beta V_1 V_2 \cdot \frac{R_{f2}}{R_f}}$

Multiplier Macro model: VCVS gain = -1000

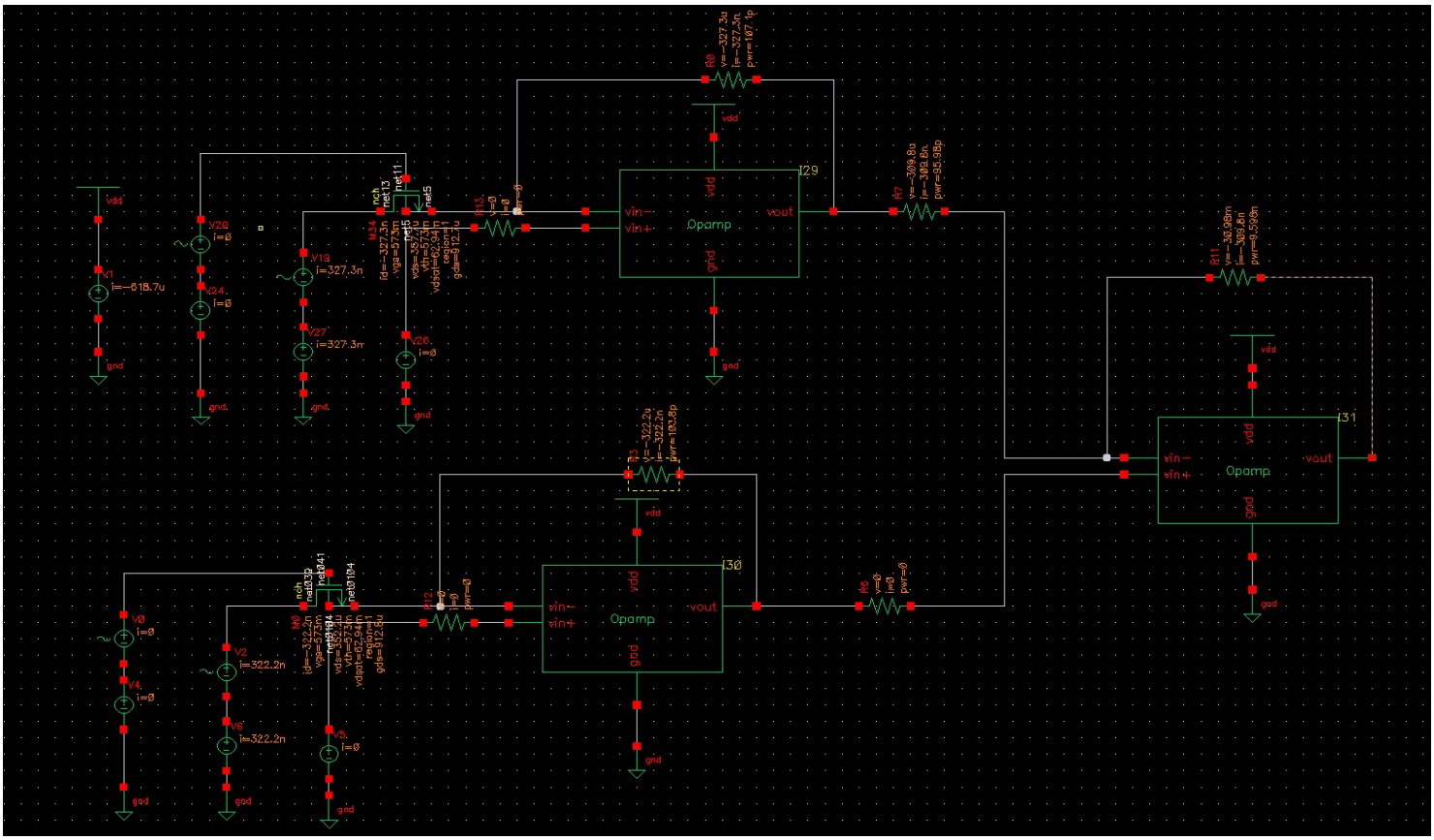
Output:(Ideal)



Schematic of Macro Model

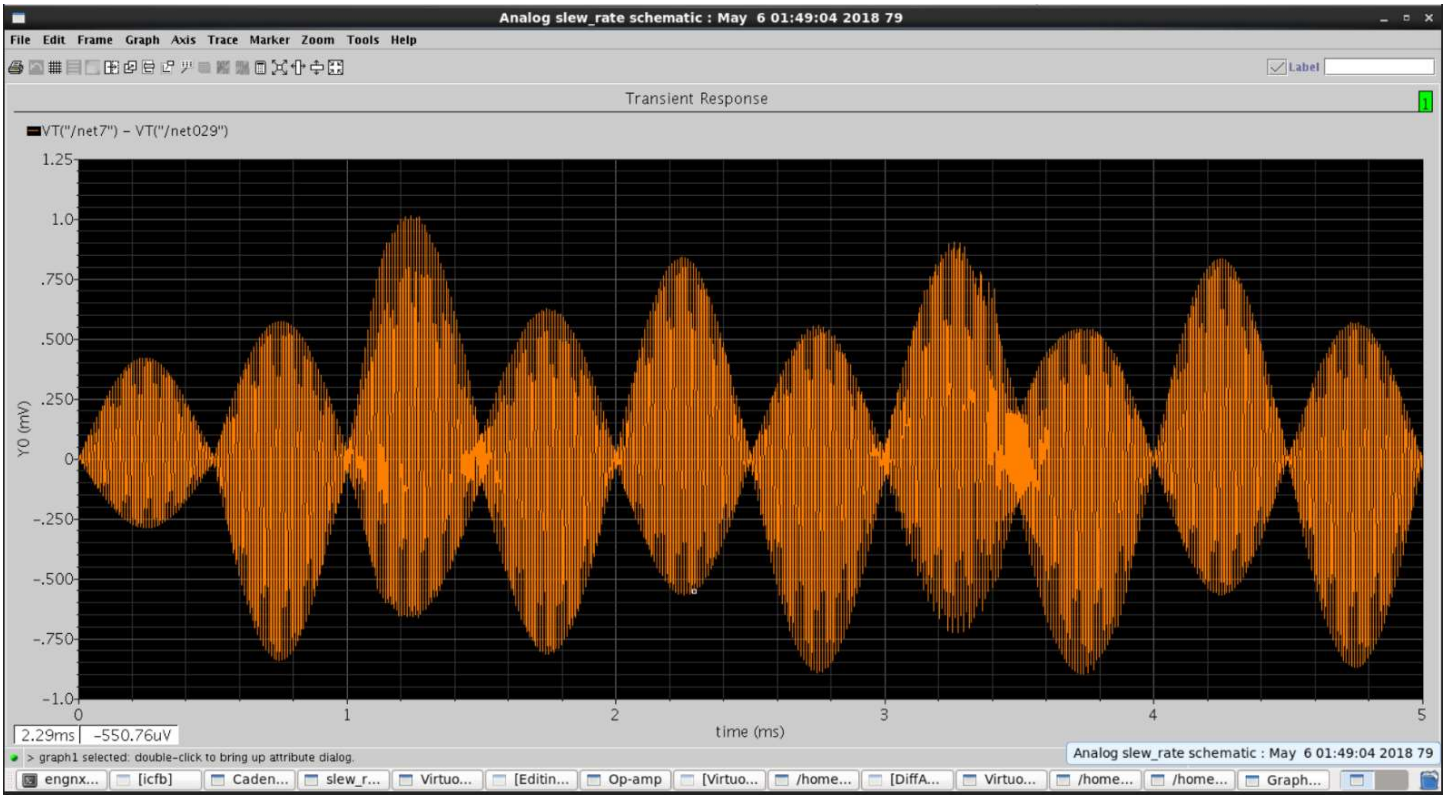


Multiplier Schematic:

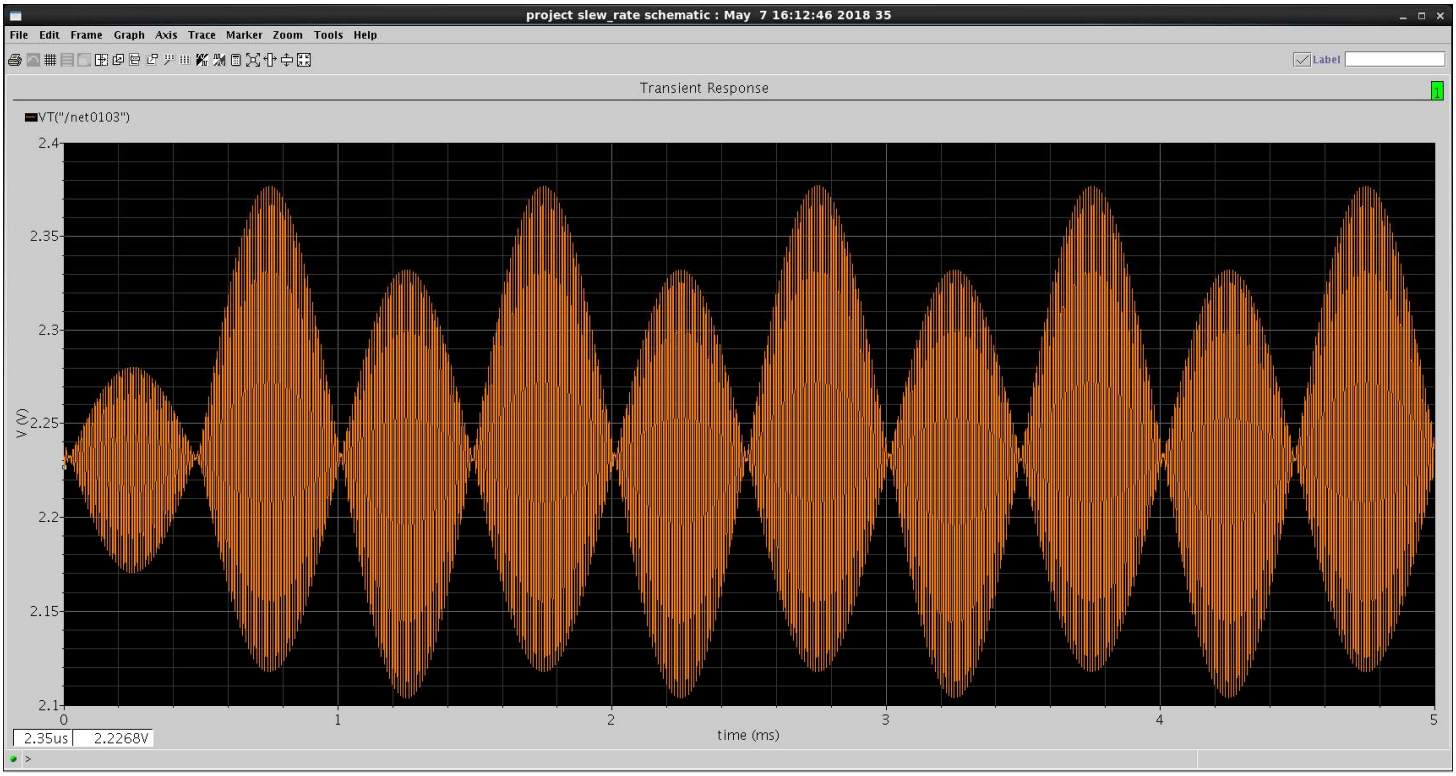


Multiplier Output: using the designed Op-amp.

For a Vcm closer to the ICMR min range of OP-amp i.e Vcm=1V



VCM set at half of ICMR of Op-amp i.e 2.1V gives a more balanced modulated output waveform.



Conclusion:

Thus, we have Successfully designed a multiplier and a 2-stage miller compensated Op-amp with parameters that meet the target specs and also has Low power dissipation. The multiplier is also able to provide stable performance for a wide range of signal amplitudes and frequencies and due to the Op-amps high CMRR we are able to eliminate the Common mode signals generated as byproduct of the quadratic multiplication operation. The Multiplier can be further improved by designing an OP-amp with higher CMRR and a larger range of operating frequency.