THE UNIVERSITY OF TEXAS AT DALLAS
Department of Electrical Engineering

EECT 7326 ADVANCED ANALOG IC DESIGN

HOMEWORK-1 Layout

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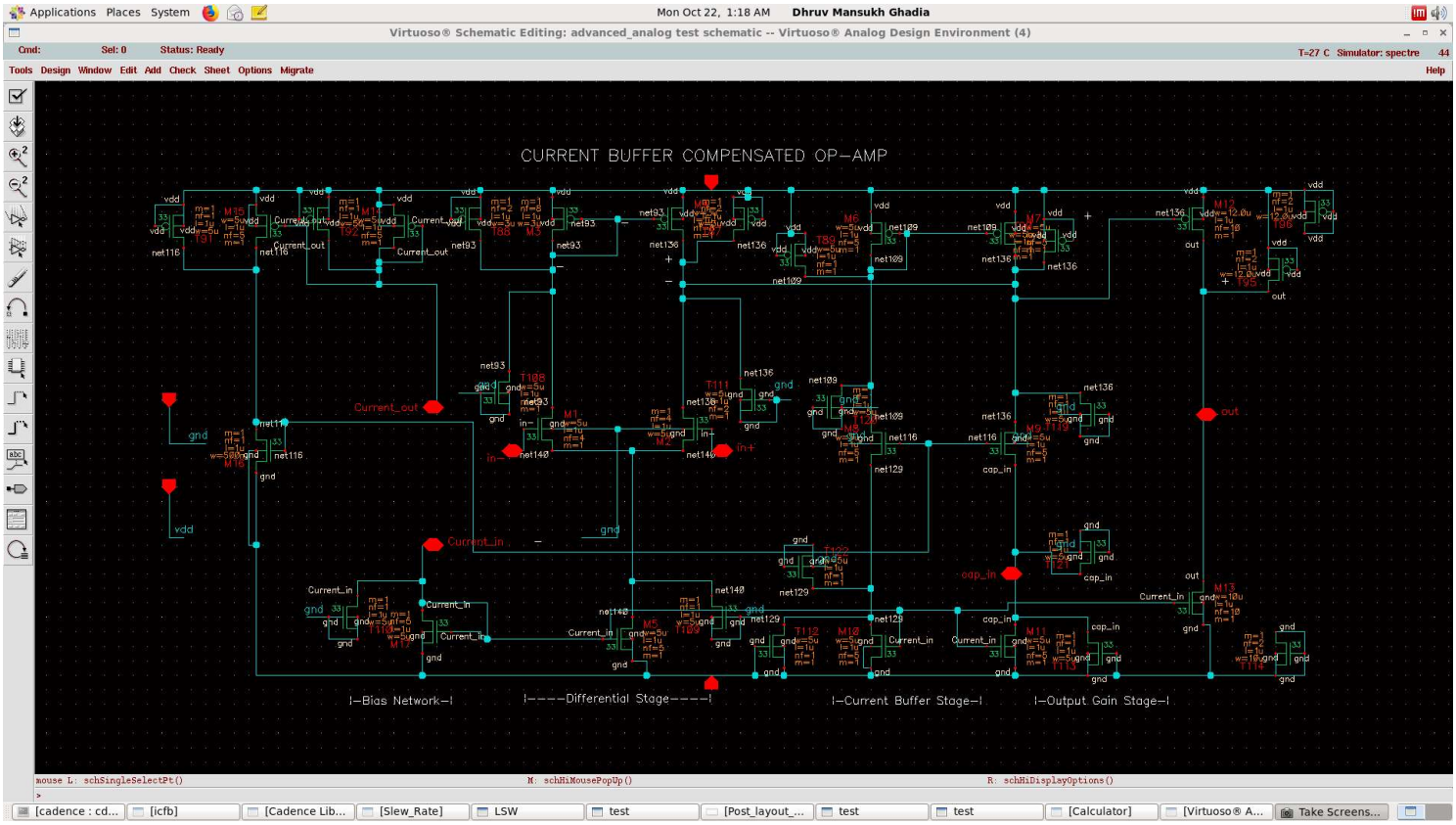
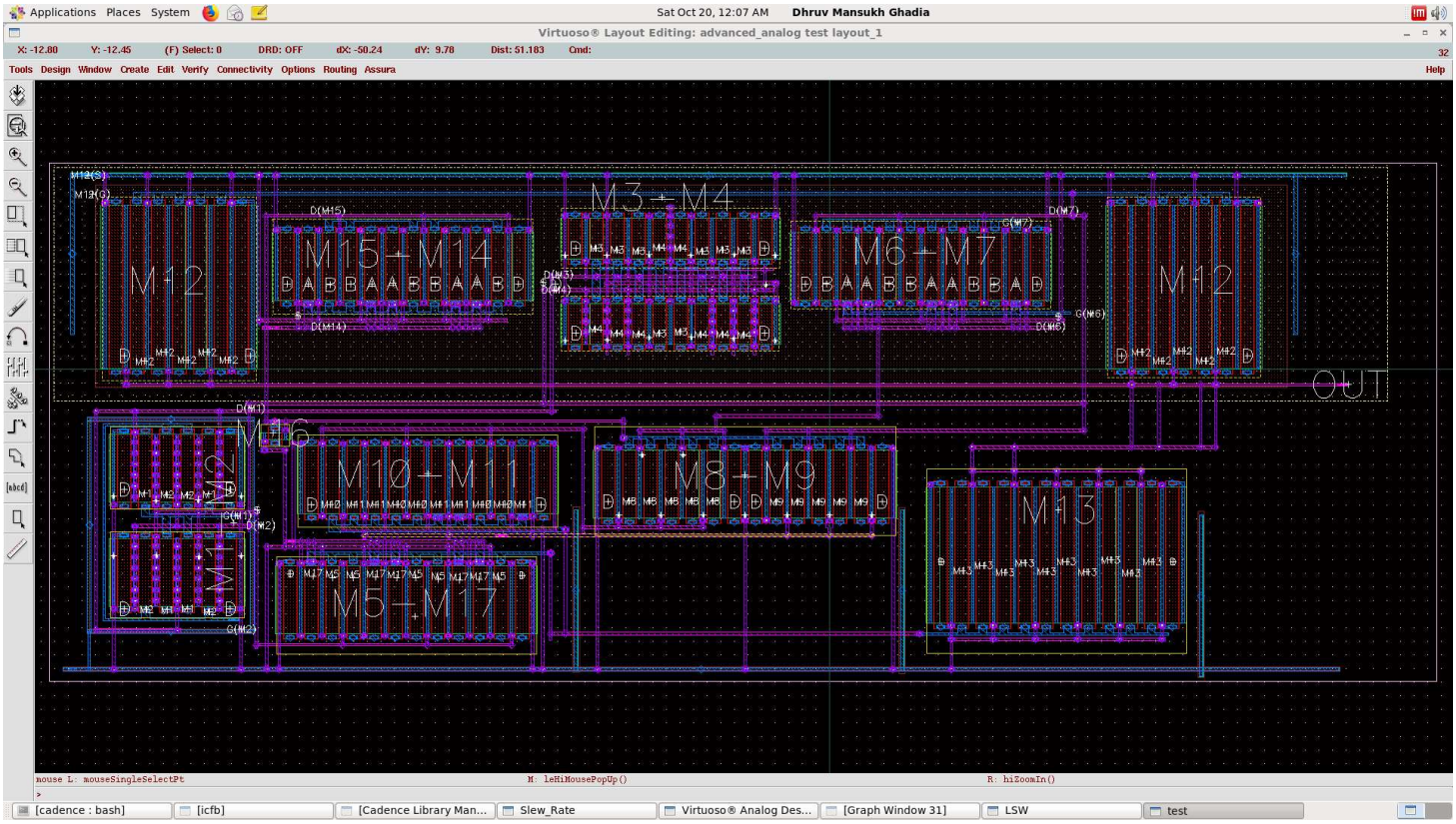
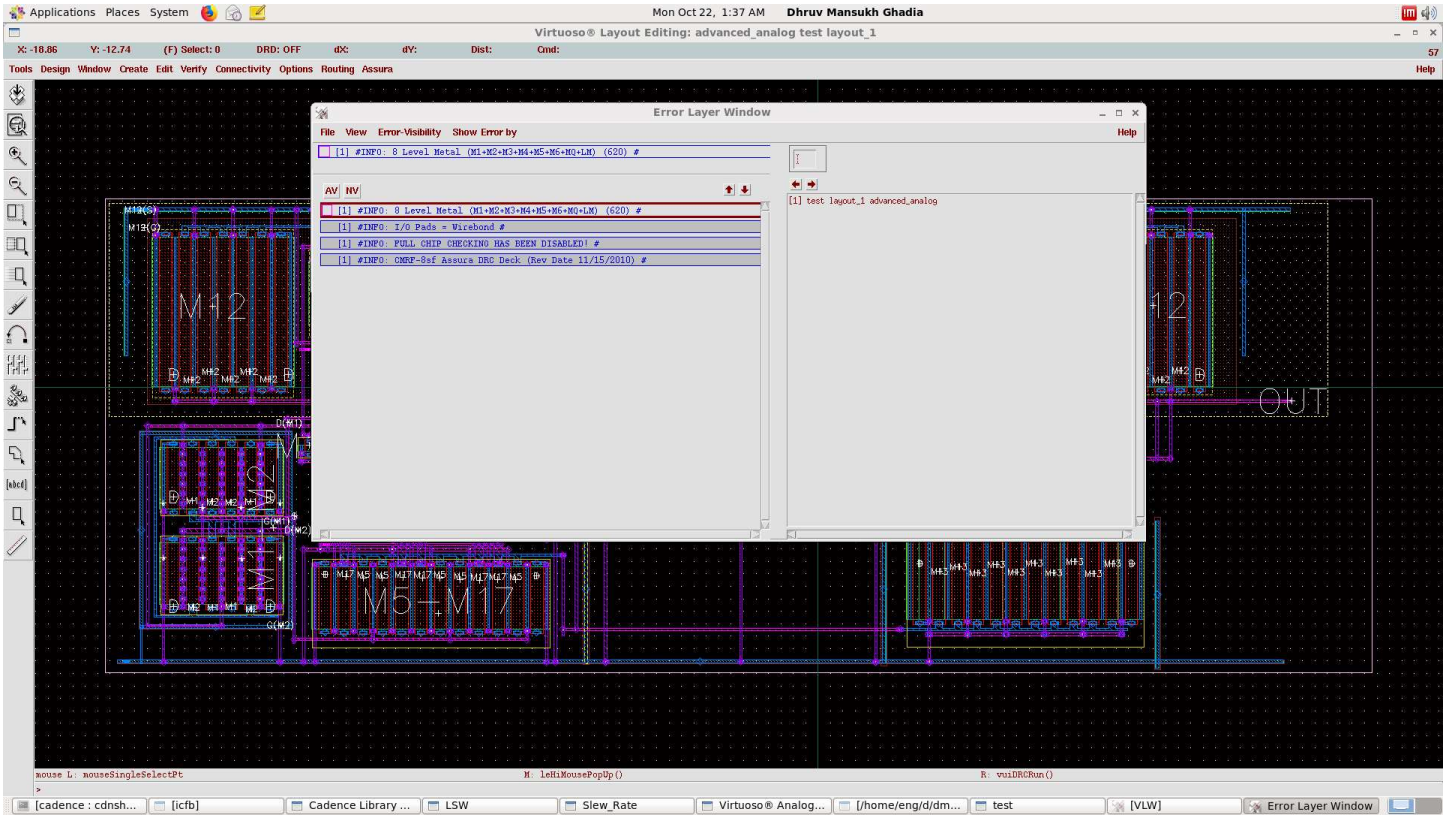
OP-Amp Schematic:



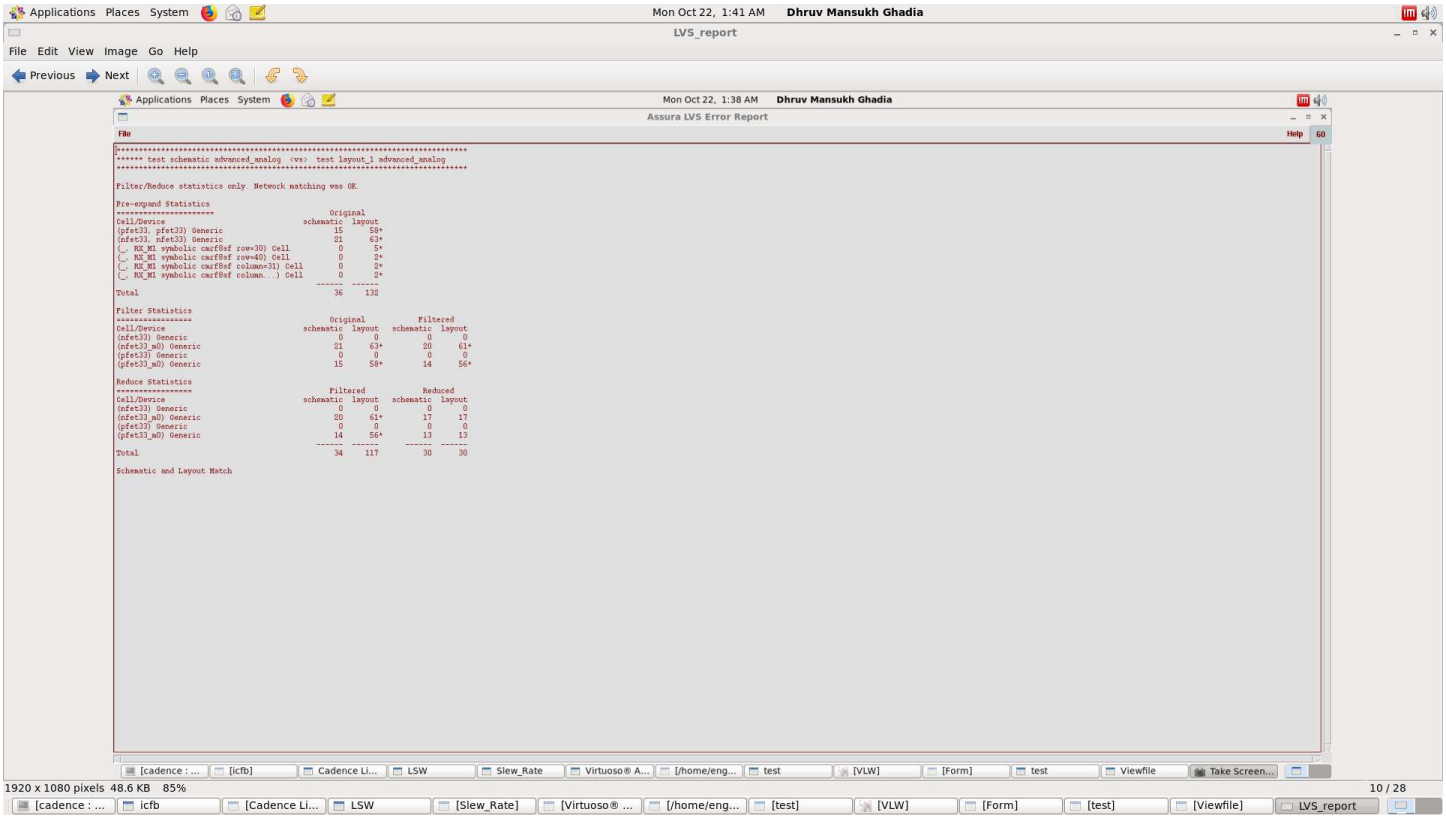
OP-AMP Layout:



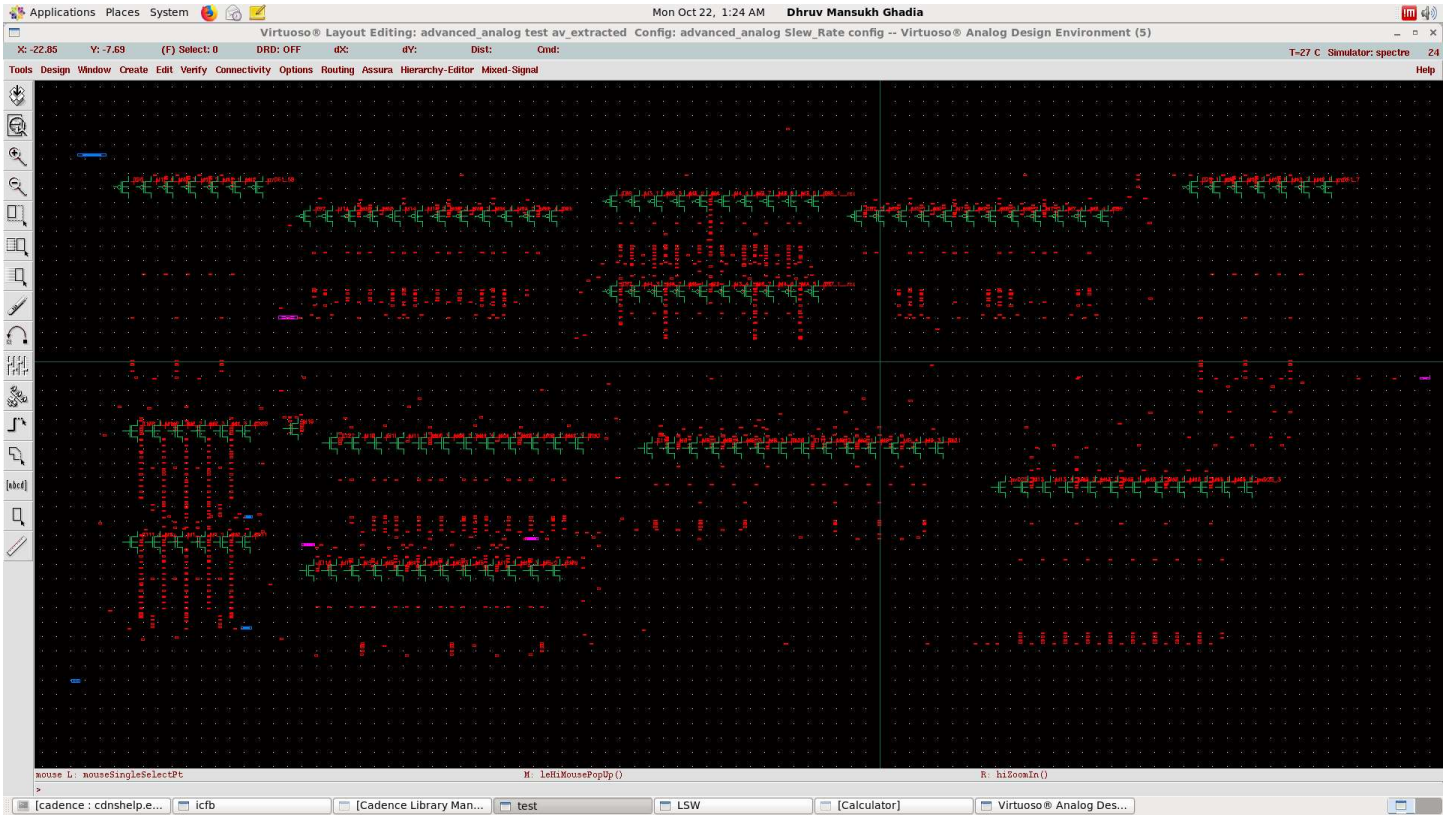
DRC Report:



LVS Report:



Extracted View:

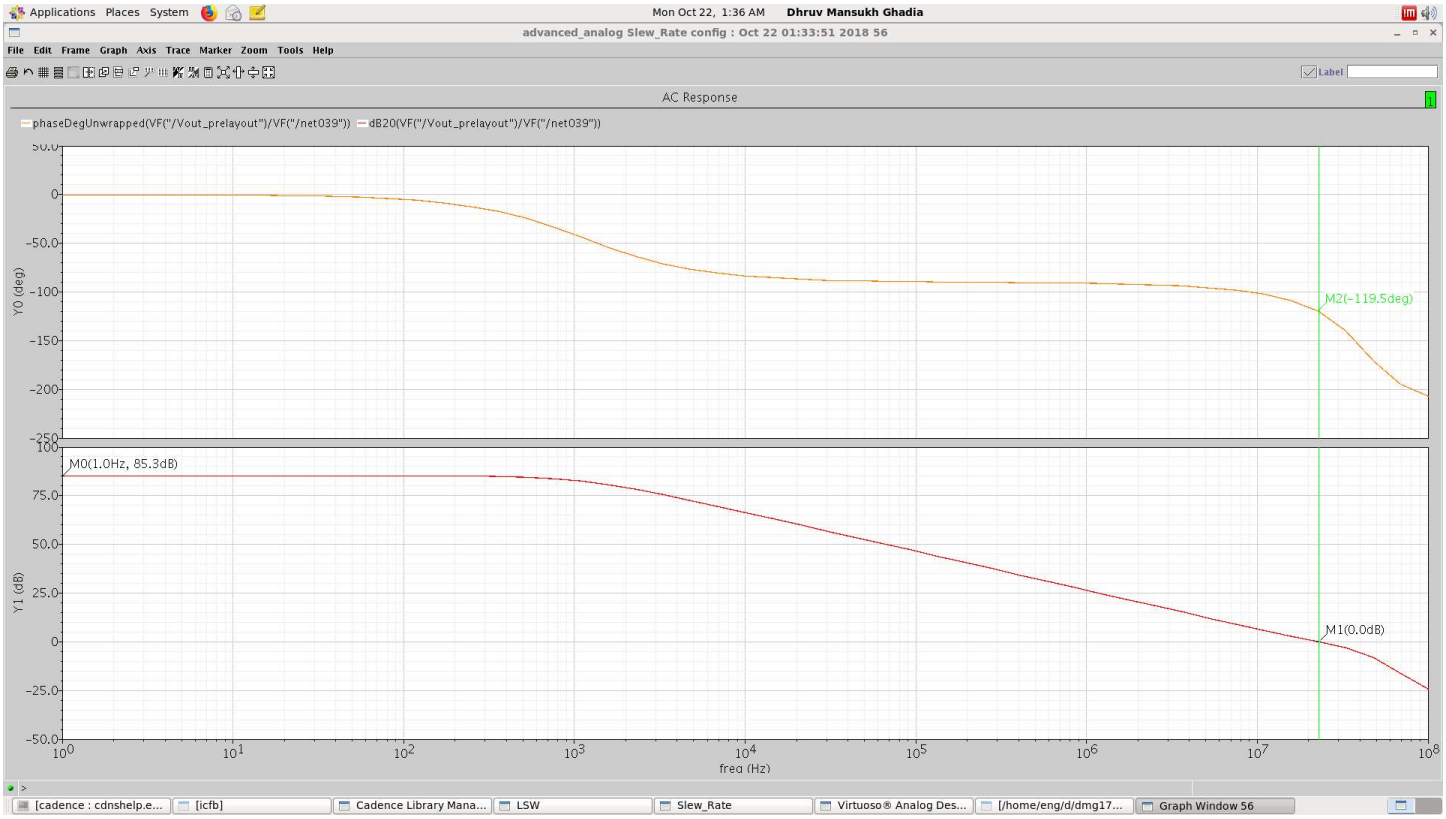


POST LAYOUT SIMUALTION:

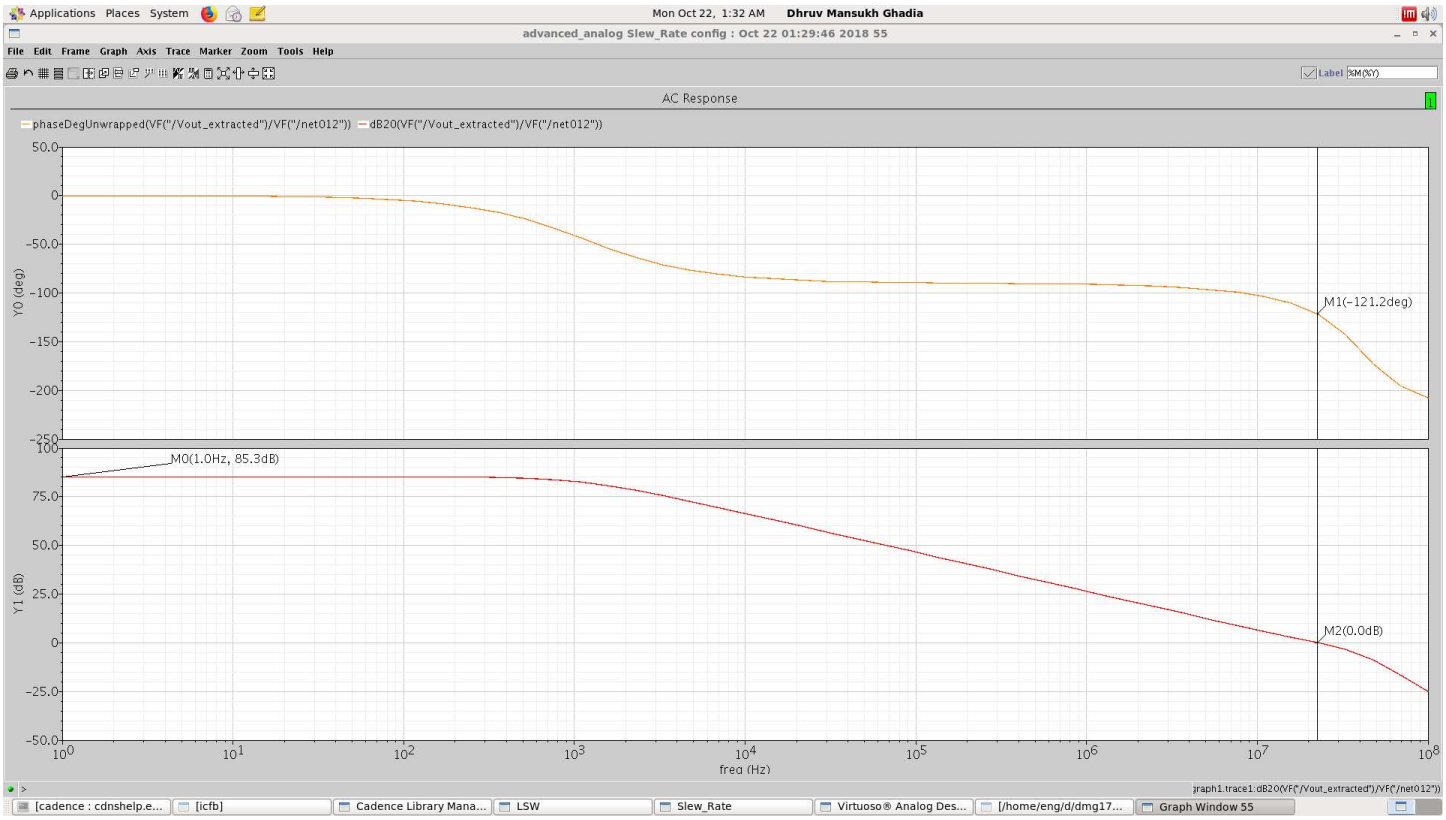
Pre-layout:

Post layout:

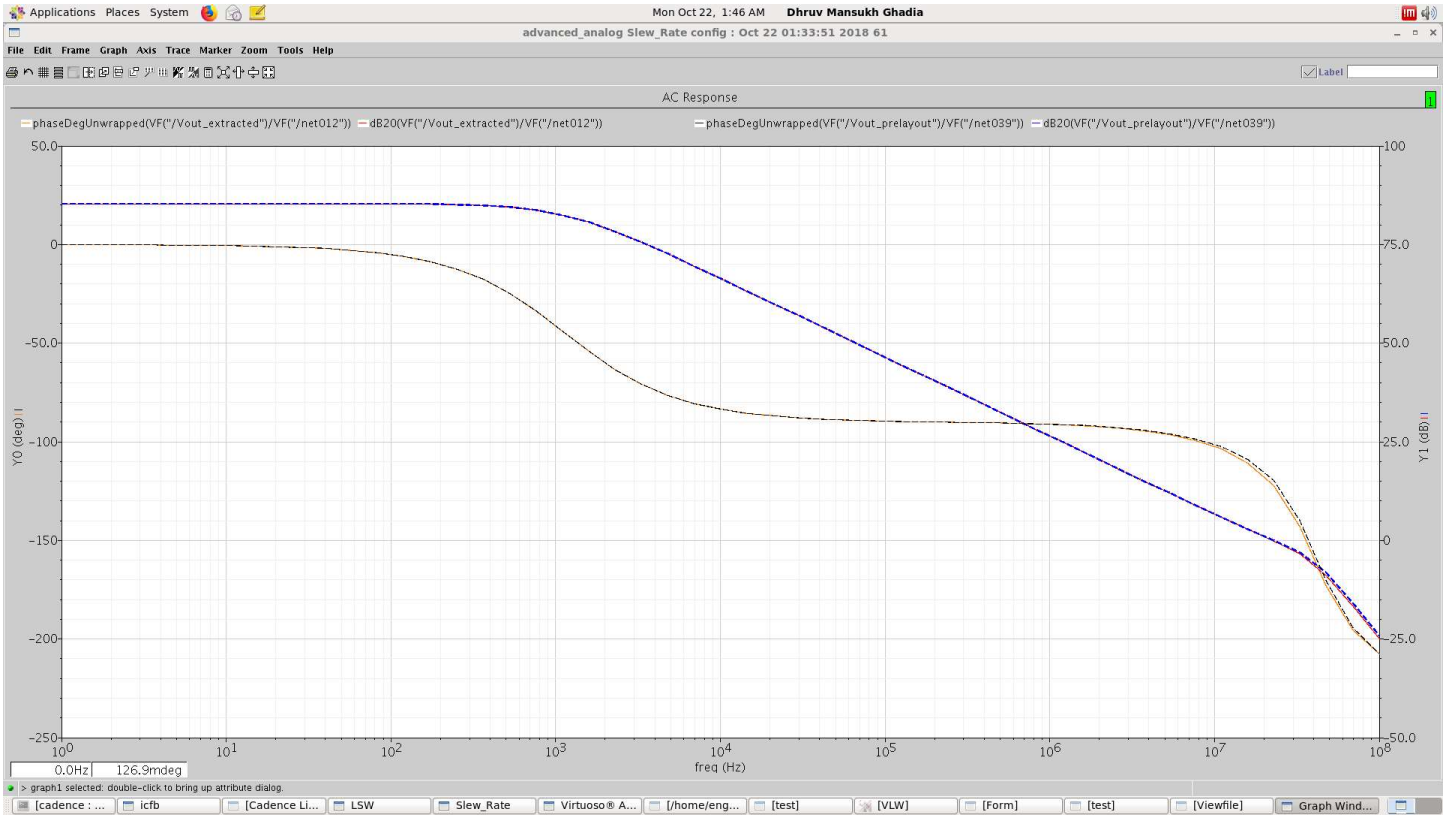
Pre-layout gain and phase:



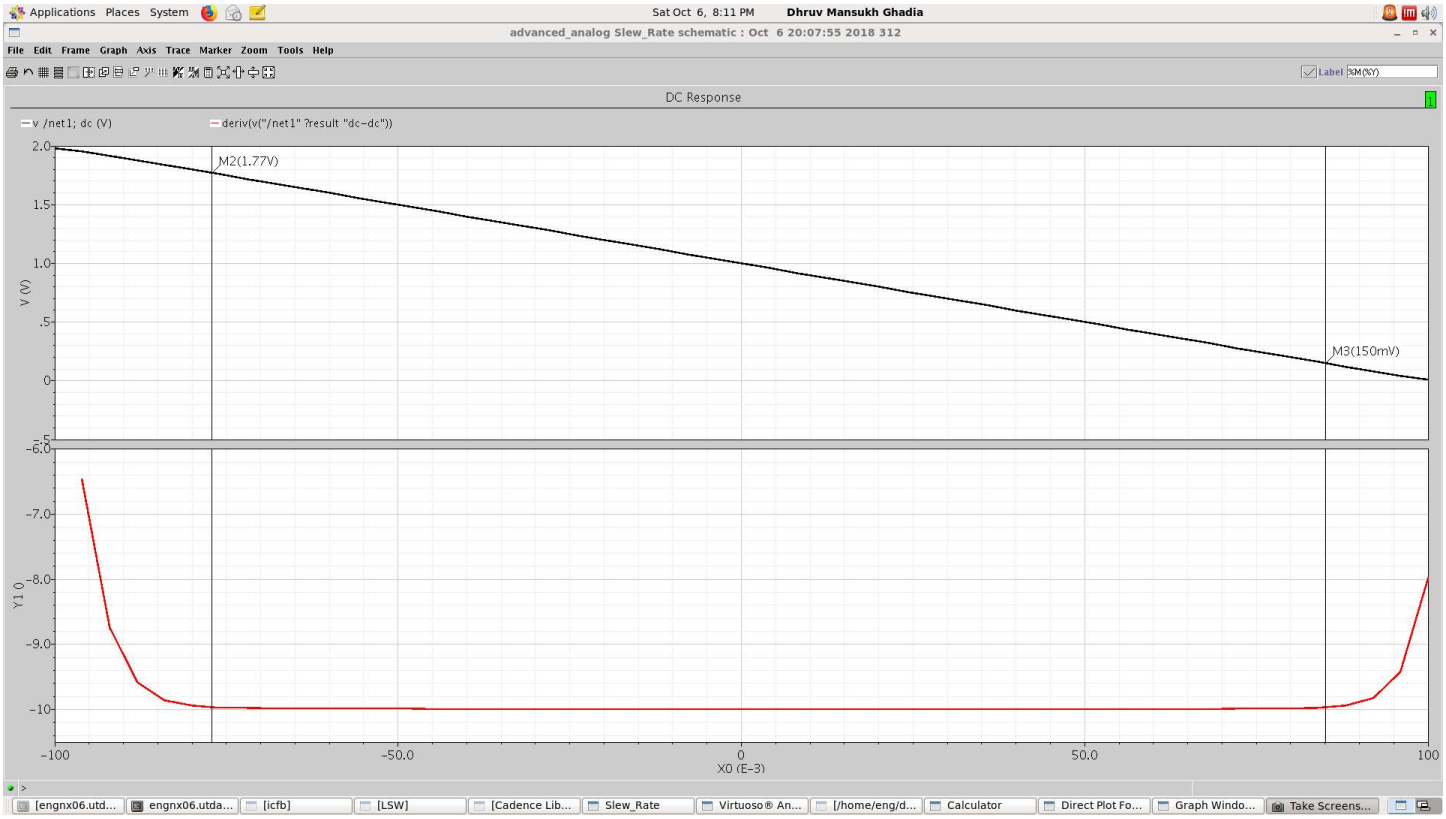
Post layout gain and phase:



Difference:



OVSR Post Simulation:



Parameter	**Pre Layout Simulation**	**Post Layout SImulation**
Dc Voltage Gain	85.3dB	85.3 dB
Output voltage swing range	Vomin: 0.15V Vomax: 1.75V	Vomin: 0.15 V Vomax: 1.75 V
Phase Margin: f(GB)	58.51°	60.8°
Unity Gain-bandwidth: GBW	21.19 MHz	22.39 MHz
Slew rate:	15.19V/ μs	20.87 V/μs
Power dissipation	197.3 μW	197.3 μW

We see some degradation in Phase Margin, Gain Bandwidth and Slew rate as these factors depend on capacitance in circuits and due to presence of various parasitic capacitances these factors get degraded, while the DC conditions remain the same.