EEL2020 Digital Design

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Title: Lab 1
AIM:

1. Create a Half-Adder. Write its test bench and simulate
2. Use Half Adder to create Full Adder
3. Use Full Adder to create 4 Bitt-Adder. Write its test bench and simulate

Task 1: Half Adder

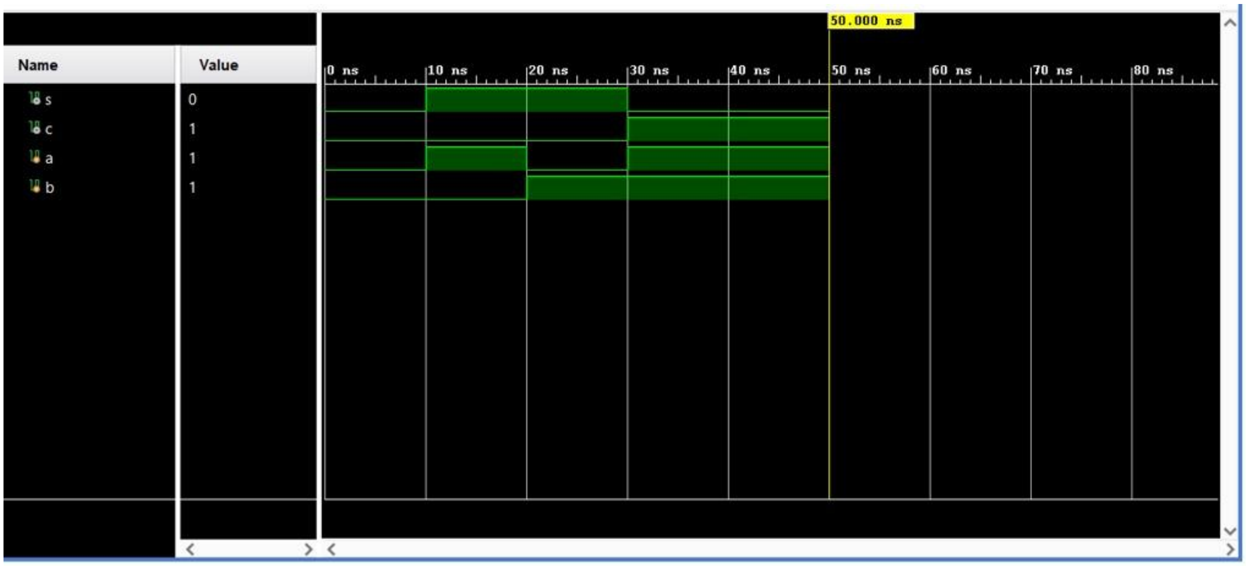
- **Code**

```
`timescale 1ns / 1ps
module Test_Half_Adder();
wire s,c;
reg a,b;
Half_Adder H(a,b,s,c);
initial
    begin
        a=1'b0;b=1'b0;
        #10 a=1'b1;
        #10 b=1'b1; a=1'b0;
        #10 a=1'b1;
     end
initial #50 $finish;
endmodule
```

- **Test Bench**

```
`timescale 1ns / 1ps
module Test_Half_Adder();
wire s,c;
reg a,b;
Half_Adder H(a,b,s,c);
initial
    begin
        a=1'b0;b=1'b0;
        #10 a=1'b1;
        #10 b=1'b1; a=1'b0;
        #10 a=1'b1;
    end
initial #50 $finish;
endmodule
```

- **Wave Form**



Name	Value
s	0
c	1
a	1
b	1

Task 2:Full Adder

- **Code**

```
`timescale 1ns / 1ps
module Full_Adder(a,b,c,sum,carry);
   input a,b,c;
   output sum,carry;
   wire sum1,carry1,carry2;
   Half_Adder H1(b,c,sum1,carry1);
   Half_Adder H2(a,sum1,sum,carry2);
   assign carry=carry1|carry2;
endmodule
```

Task 3: Four-Bit Adder

- **Code**

```
`timescale 1ns / 1ps
module
FourBitAdder(a0,b0,a1,b1,a2,b2,a3,b3,SumFirst,SumSecond,SumThird,SumFourth,Carr
y);
    input a0,b0,a1,b1,a2,b2,a3,b3;
    output SumFirst,SumSecond,SumThird,SumFourth,Carry;
    wire Carry1,Carry2,Carry3;
    Full_Adder f1(a0,b0,0,SumFirst,Carry1);
    Full_Adder f2(a1,b1,Carry1,SumSecond,Carry2);
    Full_Adder f3(a2,b2,Carry2,SumThird,Carry3);
    Full_Adder f4(a3,b3,Carry3,SumFourth,Carry);
endmodule
```

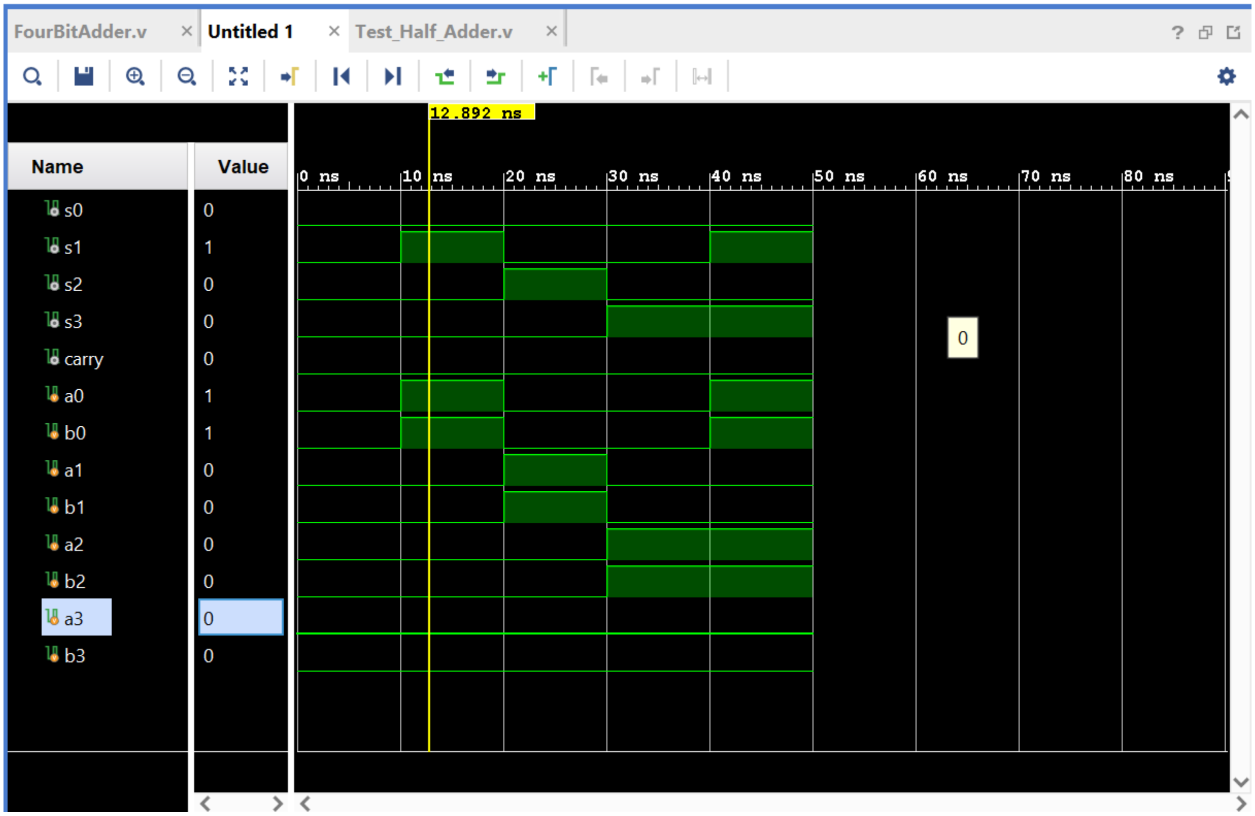
- **Test Bench**

```
`timescale 1ns / 1ps
module TestFourBitAdder();
    wire s0, s1, s2, s3, carry;
    reg a0, b0, a1, b1, a2, b2, a3, b3;
    FourBitAdder Fb(a0, b0, a1, b1, a2, b2, a3, b3, s0, s1, s2, s3, carry);
    initial
        begin
        a0 = 1'b0;  a1 = 1'b0;a2 = 1'b0;a3 = 1'b0;
        b0 = 1'b0; b1 = 1'b0;  b2 = 1'b0;  b3 = 1'b0;
        #10 a0 = 1'b1; b0 = 1'b1;
        #10 a0 = 1'b0; b0 = 1'b0; a1 = 1'b1; b1 = 1'b1;
        #10 a0 = 1'b0; b0 = 1'b0; a1 = 1'b0; b1 = 1'b0;a2 = 1'b1; b2 = 1'b1;
        #10 a0 = 1'b1; b0 = 1'b1;a2 = 1'b1; b2 = 1'b1;
        #10 a0 = 1'b0; b0 = 1'b0; a1 = 1'b1; b1 = 1'b1;a2 = 1'b1; b2 = 1'b1;
        end
initial #50 $finish;
Endmodule
```

- **Truth Table**

A3	A2	A1	A0		B3	B2	B1	B0		S3	S2	S1	S0		C
0	0	0	0		0	0	0	0		0	0	0	0		0
0	0	0	1		0	0	0	1		0	0	1	0		0
0	0	1	0		0	0	1	0		0	1	0	0		0
0	0	1	1		0	0	1	1		0	1	1	0		0
0	1	0	0		0	1	0	0		1	0	0	0		0
0	1	1	0		0	1	1	0		1	1	0	0		0

- **Wave Form**



Name	Value
s0	0
s1	1
s2	0
s3	0
carry	0
a0	1
b0	1
a1	0
b1	0
a2	0
b2	0
a3	0
b3	0