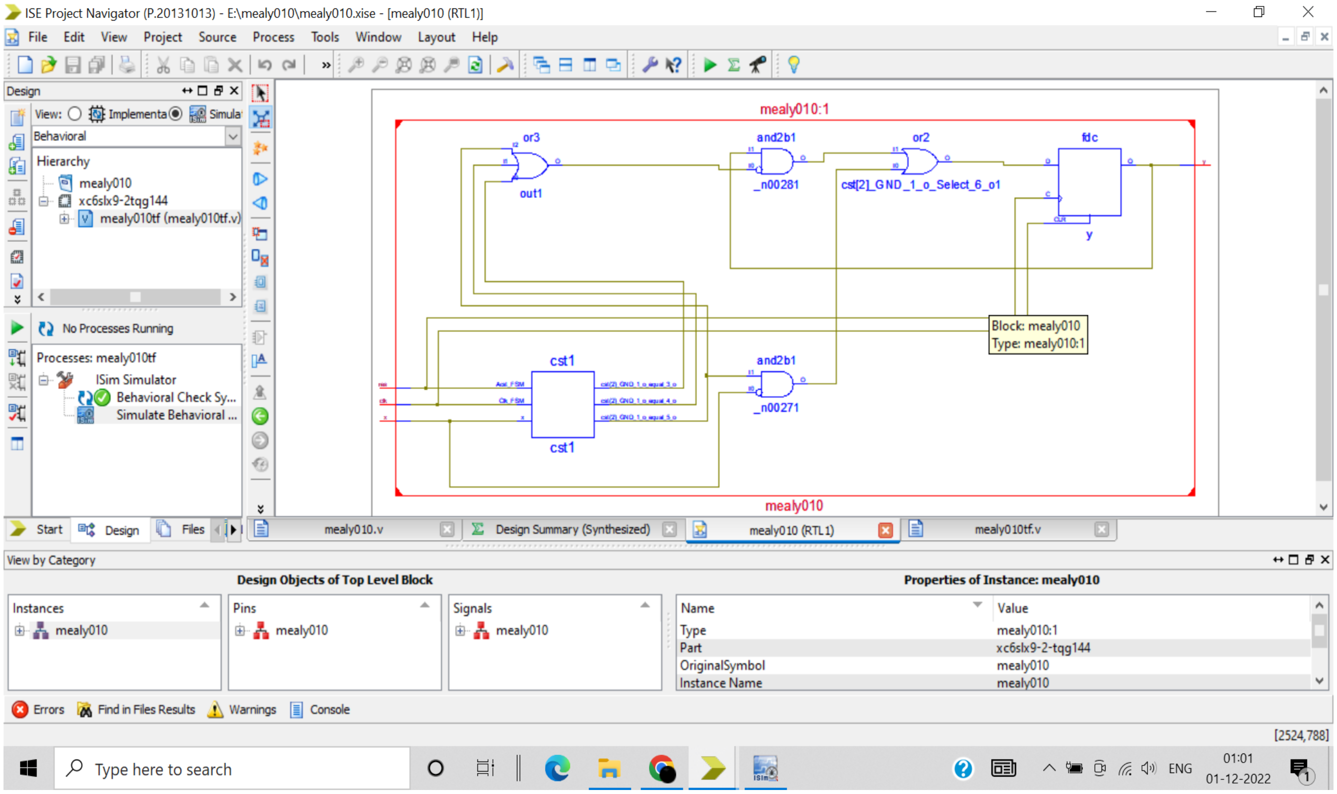
Experiment 20

Code:

```
       module mealy010( input x,clk,res,
                                output reg Y );
         reg [2:0] cst; parameter s0=2'b00, s1=2’b01,s2=2'b10;
         always@(posedge clk or posedge res) begin
         if(res) begin
         y<=0;
         cst<=s0;
         end
         else begin
          case(cst)
           s0: begin
            if(~x) begin
                    y<=0;
                    cst<=s1;
                   end
                   else begin
                    y<=0;
                    cst<=s0;
                   end
           end
           s1: begin
            if(x) begin
                    y<=0;
                    cst<=s2;
                   end
                   else begin
                    y<=0;
                    cst<=s1;
                   end
           end
           s2: begin
            if(~x) begin
                    y<=1;
                    cst<=s0;
                    end
                   else begin
                   y<=0;
                  cst<=s0;
                 end
               end
           default: cst<=s0;
          endcase
         end
 end
Endmodule
```

RTL SCHEMATIC:



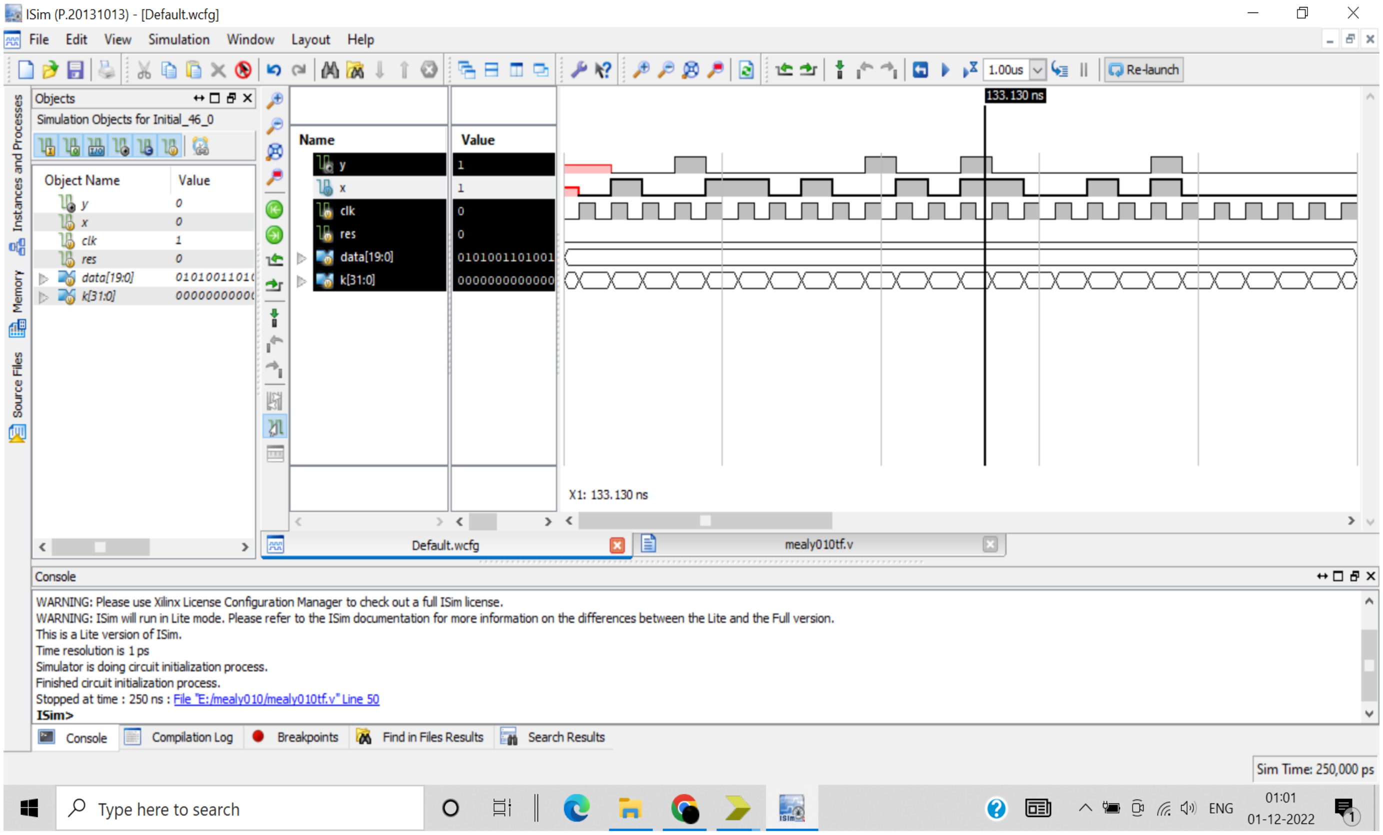
Design Objects of Top Level Block

Instances	Pins	Signals
mealy010	mealy010	mealy010

Properties of Instance: mealy010

Name	Value
Type	mealy010:1
Part	xc6slx9-2-tqg144
OriginalSymbol	mealy010
Instance Name	mealy010

WAVEFORM :



Simulation Objects for Initial_46_0

Object Name	Value
y	0
x	0
clk	1
res	0
data[19:0]	01010011010
k[31:0]	0000000000

Name	Value
y	1
x	1
clk	0
res	0
data[19:0]	0101001101001
k[31:0]	000000000000

```
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Stopped at time : 250 ns : File "E:/mealy010/mealy010tf.v" Line 50
ISim>
```

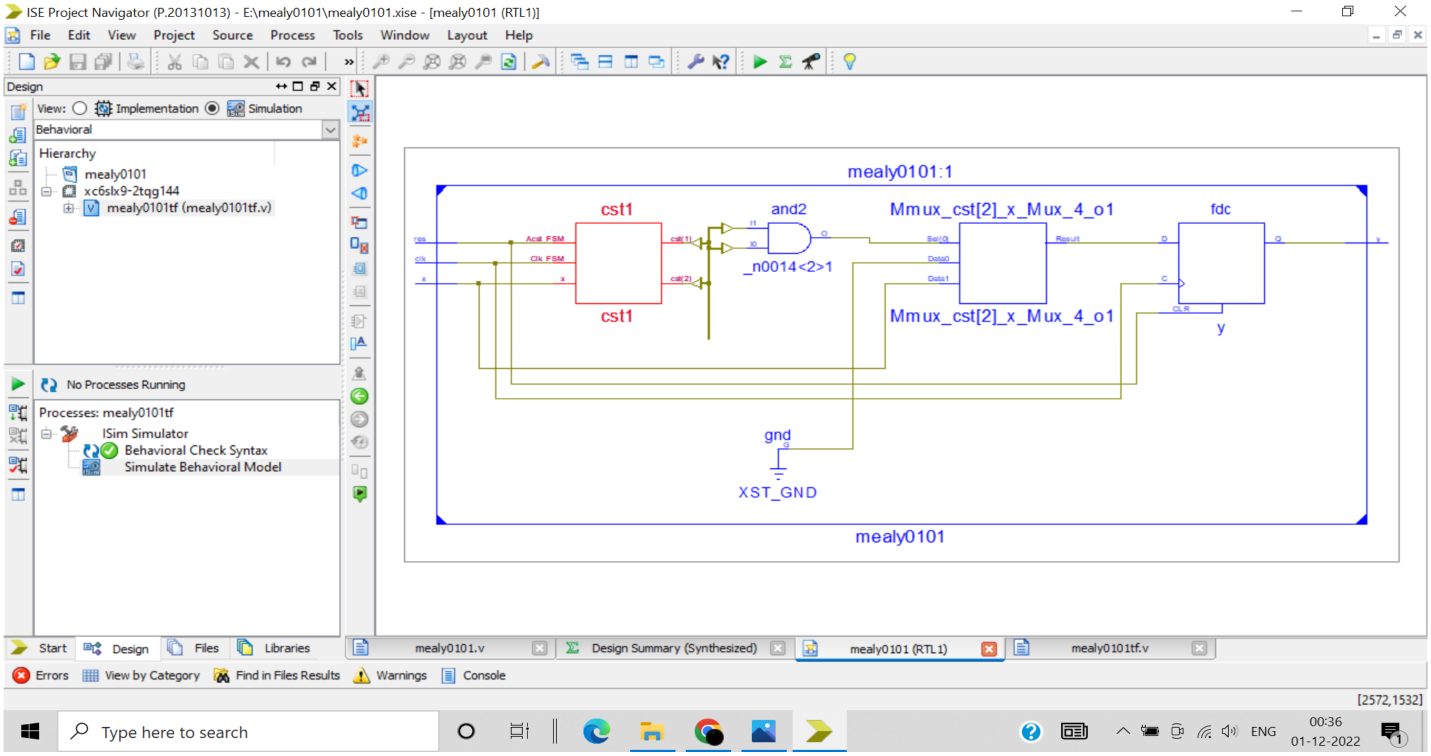
Experiment - 21

Code:

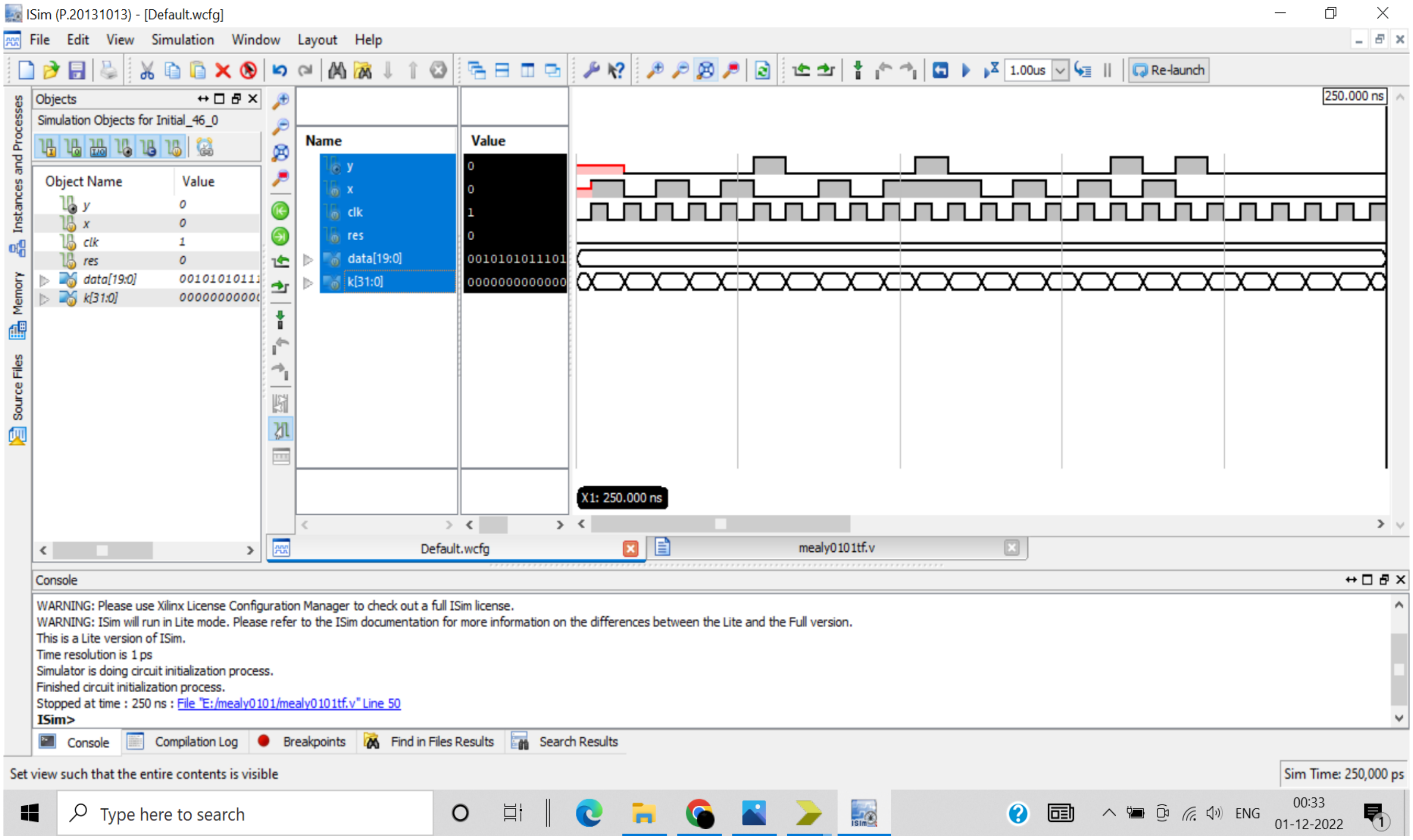
```
module mealy0101(
    input x,clk,res,
            output reg y
    );
            reg [2:1] cst;
            parameter s0=2'b00,s1=2'b01,
                      s2=2'b10,s3=2'b11;
           always@(posedge clk or posedge res) begin
           if(res) begin
           y<=0;
           cst<=s0;
           end
           else begin
            case(cst)
             s0: begin
              if(~x) begin
                      y<=0;
                      cst<=s1;
                      end
                      else begin
      y<=0;
      cst<=s0;
      end
     end
     s1: begin
      if(x) begin
       y<=0;
       cst<=s2;
       end
      else begin
       y<=0;
       cst<=s1;
      end
     end
     s2: begin
      if(~x) begin
```

```
       y<=0;
       cst<=s3;
      end
      else begin
       y<=0;
       cst<=s0;
      end
              end
                      s3: begin
                       if(x) begin
                        y<=1;
                        cst<=s2;
                       end
                       else begin
                        y<=0;
                        cst<=s1;
                       end
                      end
                      default: cst<=s0;
     endcase
    end
   end
endmodule
```

RTL SCHEMATIC:



WAVEFORM:



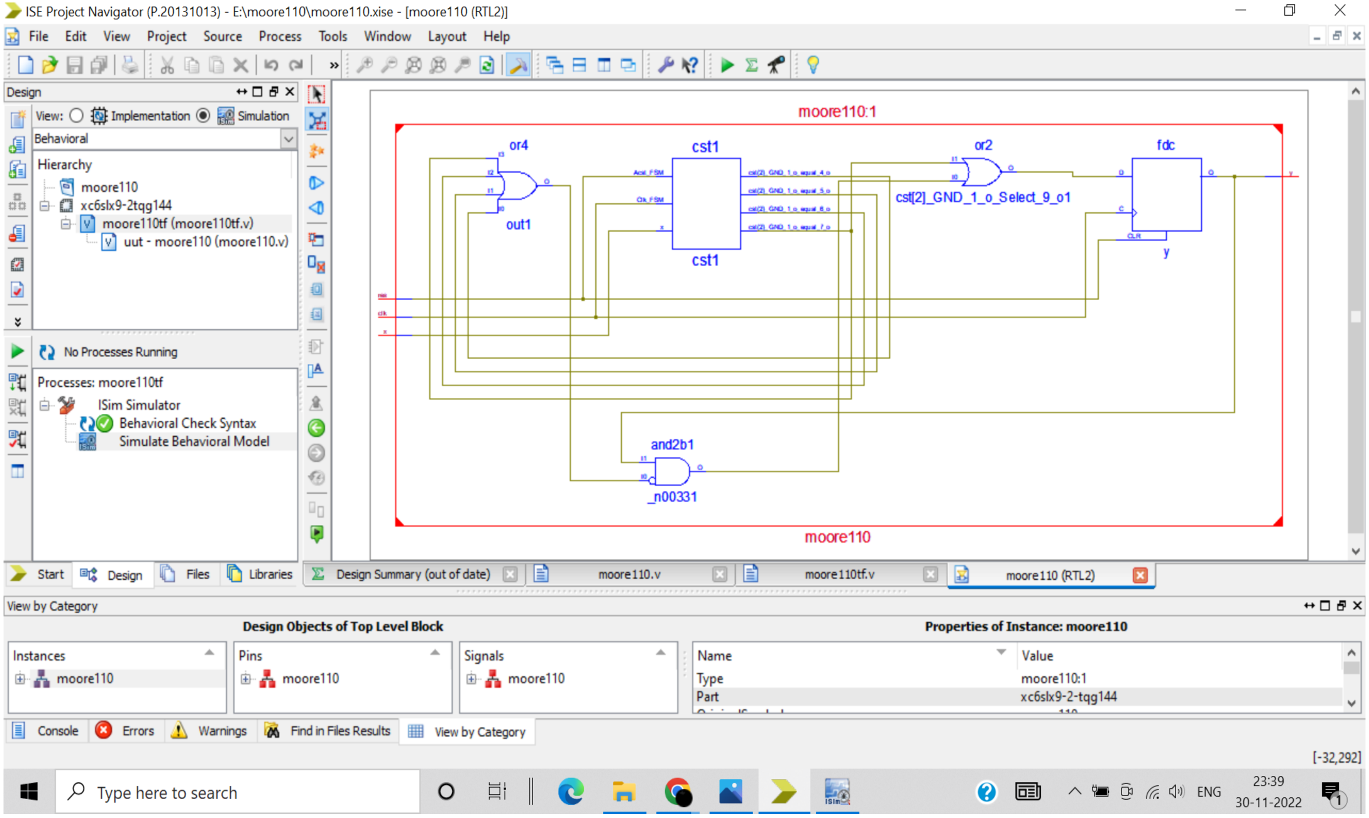
```
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Stopped at time : 250 ns : File "E:/mealy0101/mealy0101tf.v" Line 50
ISim>
```

EXPERIMENT - 22

Code:

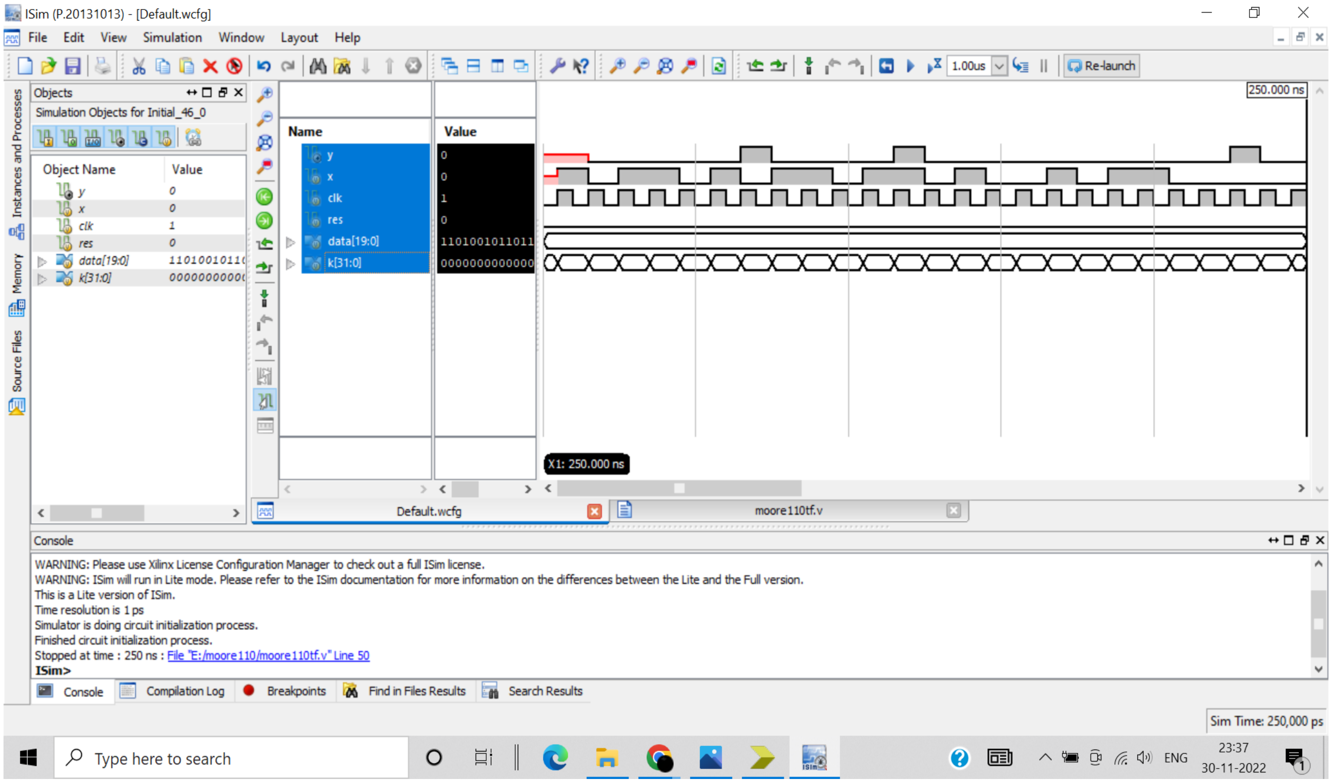
```
module moore110(input x,clk,res,
                      output reg y );
          reg [2:0] cst;
          parameter s0=2'b00,s1=2'b01,
                       s2=2'b10, s3=2'b11;
         always@(posedge clk or posedge res) begin
         if(res) begin
         y<=0;
         cst<=0;
         end
         else begin
          case(cst)
           s0: begin
                   y<=0;
                         if(x)
                          cst<=s1;
                         end
                s1: begin
                   y<=0;
                         if(x)
                          cst<=s2;
                         else
                          cst<=s0;
                         end
          s2: begin
             y<=0;
                        if(~x)
                         cst<=s3;
                        else
                         cst<=s1;
                        end
                s3: begin
                   y<=1;
                         cst<=s0;
                         end
                default: cst<=s0;
          endcase
         end
        end
endmodule
```

RTL SCHEMATIC:



Name	Value
Type	moore110:1
Part	xc6slx9-2-tqg144

WAVEFORM:



Object Name	Value
y	0
x	0
clk	1
res	0
data[19:0]	1101001011(
k[31:0]	0000000000(

```
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Stopped at time : 250 ns : File "E:/moore110/moore110tf.v" Line 50
ISim>
```

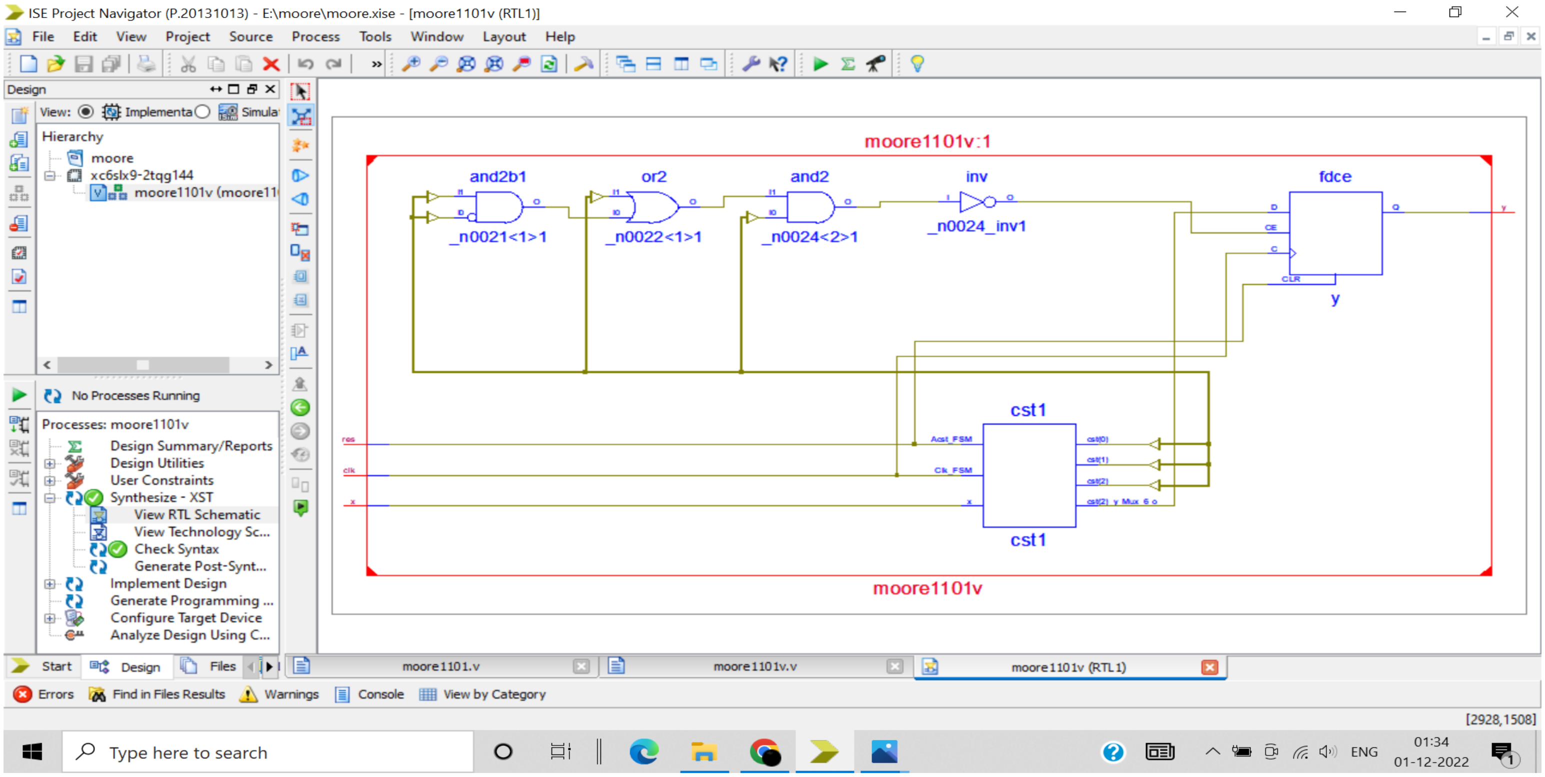
EXPERIMENT - 23

Code:

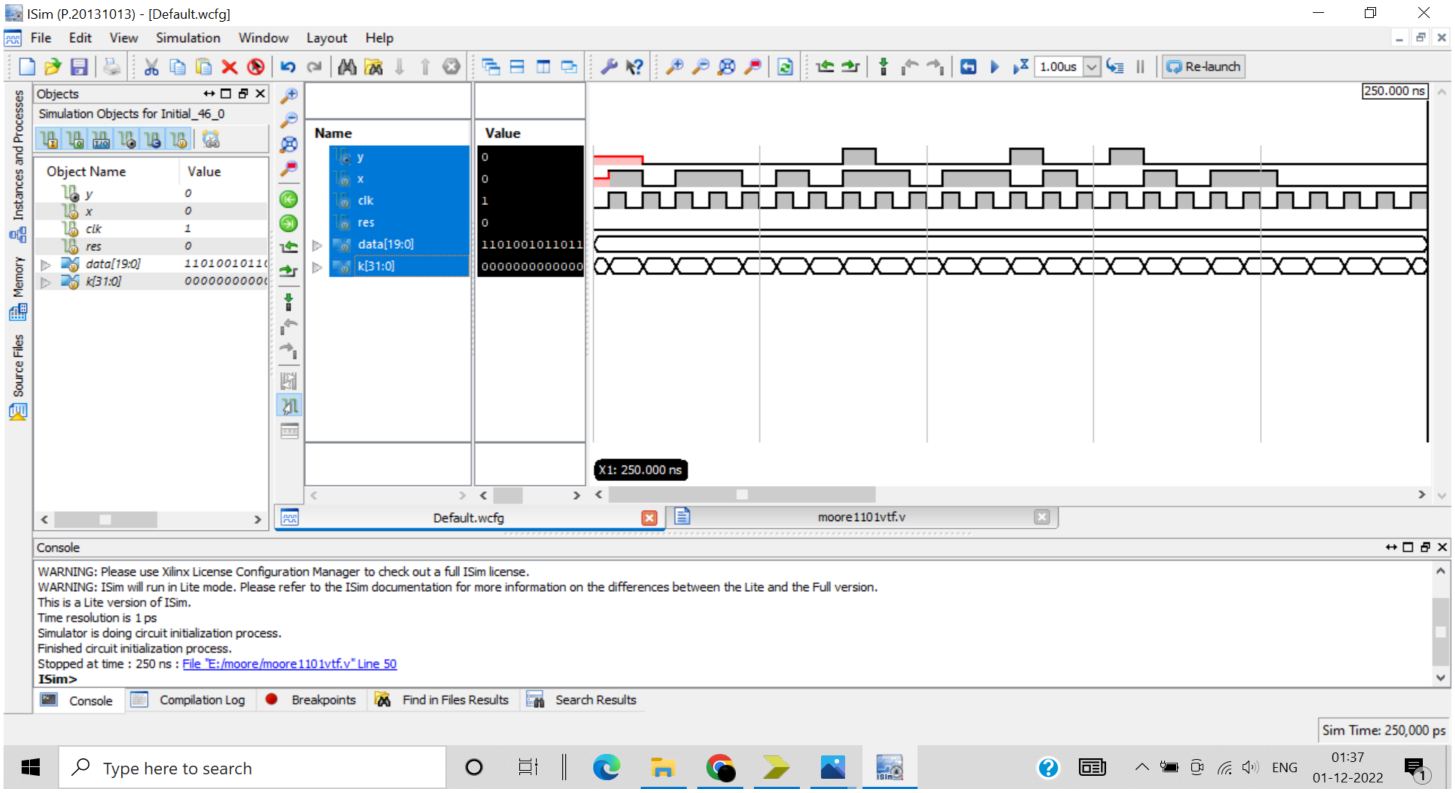
```
module moore1101v(
        input x,clk,res,
         output reg Y);
         reg [2:0] cst;
         parameter s0=3'b000,s1=3'b001,
                s2=3'b010,s3=3'b011,s4=3'b100;
        always@(posedge clk or posedge res) begin
        if(res) begin
        y<=0;
        cst<=s0;
        end
        else begin
         case(cst)
          s0: begin
           y<=0;
           if(x)
                 cst<=s1;
                 else
    cst<=s0;
   end
   s1: begin
           y<=0;
    if(x)
     cst<=s2;
    else
     cst<=s0;
   end
   s2: begin
           y<=0;
    if(~x)
     cst<=s3;
    else
     cst<=s2;
           end
                 s3: begin
                  y<=0;
                  if(x)
```

```
                         cst<=s4;
                        else
                         cst<=s0;
                       end
                       s4: begin
                        y<=1;
                        if(x)
                         cst<=s2;
                        else
                         cst<=s0;
                        end
                       default: cst<=s0;
     endcase
    end
   end
endmodule
```

RTL SCHEMATIC:



WAVEFORM:



Console

```
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Stopped at time : 250 ns : File "E:/moore/moore1101vtf.v" Line 50
ISim>
```