Enrolment Number: _____

P P SAVANI UNIVERSITY
P P SAVANI SCHOOL OF ENGINEERING
4th Semester of B.Tech Examination (1st Internal Exam)

Subject: Computer Organization (SECE2040)
Branches: CE/IT

[Date: 11/02/2019, Monday] [Time: 10.15 A.M. to 11.15 A.M.] [Total Marks: 30]

Instructions:

- Figures to the right indicate full marks.
- Q 1 is compulsory.
- Draw neat and clean drawings & Assume suitable data if necessary.

Q.1 Answer the following Questions.(Any five): **(05)**

1. _____ is concerned with the way the hardware components operate to form computer system.
   a. Computer Design
   b. Computer Architecture
   c. Computer Implementation
   d. Computer Organization
2. The number 43 in 2's complement representation is _____.
3. The register that keeps track of the instruction in the program stored in memory is:
   a. Control Register
   b. Program Counter
   c. Status Register
   d. Direct Register
4. HLT is _____ type of instruction.
5. _____table is generated at the end of first pass of the assembler.
6. What will be the size of program counter (PC) if we have memory unit with 128k words of 32 bits each.

Q.2.A Convert the following numbers to the bases indicated. (Any Three). **(06)**

a. $(7562)_{10}$ to binary
b. $(1938)_8$ to hexadecimal
c. $(1001.1010)_2$ to decimal
d. $(3A)_{16}$ to decimal

Q.2.B Explain Stored Program Organization with one processor register and an instruction code format with two parts. **(04)**

OR

Q.2.A Perform the arithmetic operations in binary using signed-2's complement representation for negative numbers: (+42) + (-13) and (-42) - (-13) **(06)**

Q.2.B Demonstrate Direct and Indirect addressing with example. **(04)**

Q.3.A List out all basic computer registers with its functionality. Explain number of bits each register has with proper justification. **(05)**

Q.3.B Write an assembly language program to add two numbers. **(05)**

OR

Q.3.A Explain all three instruction code format of basic computer with example. **(05)**

Q.3.B Write an assembly language program to subtract two numbers. **(05)**

Q.4 List out the tables used during second pass of assembler. Draw flowchart to explain second pass of assembler. **(05)**

Q.3.A The memory unit of a computer has 128K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of 10 addressing modes, a register address field to specify one of 30 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word. (05)

Q.3.B An instruction is stored at location 300 with its address field at location 301.The address field has the value 400.A processor register R1 contains the number 200.Evaluate the effective address if the addressing mode of the instruction is a) Direct b) Immediate c) Relative d) Register indirect e) Index with R1 as the index register. (05)

OR

Q.3.A Convert the following numerical arithmetic expression into reverse polish notation (postfix) and show the stack operations for evaluating the numeric result. (05)
(300 + 23) * (43-21) / (84 + 7)

Q.3.B Design a bus organized CPU having seven registers, two multiplexers (MUX), an ALU and a destination decoder. Using that specify the control word for micro-operation R1← R3 ⊕ R4. (OPR selection for XOR = 01100). (05)

Q.4 Explain the Three-Address and Two-Address instructions with expression (A+B)*C. (05)