Enrolment Number: 17

P P SAVANI UNIVERSITY
P P SAVANI SCHOOL OF ENGINEERING
4th Semester of B.Tech Examination (2nd Internal Exam)
Subject: Computer Organization (SECE2040)
Branches: CE/IT

[Date: 18/03/2019, Monday] [Time: 10.15 A.M. to 11.15 A.M.] [Total Marks: 30]

Instructions:

- Figures to the right indicate full marks.
- Q 1 is compulsory.
- Draw neat and clean drawings & Assume suitable data if necessary.

Q.1 Answer the following Questions.(Any five): **(05)**

1. What will be the value of SC(Sequence Counter) during multiplication of 45 * 10
   a. 010 b. 011
   c. 100 d. 110
2. Perform Arithmetic Shift Right on following binary number$(110110011)_2$
3. In the process of multiplication of unsigned numbers, the sign of result is decided by
   a. Qs ⊕ Bs b. As ⊕ Qs
   c. Bs ⊕ As d. None of Above
4. Which of following co-ordinates various operations using timing signals?
   a. Control Unit b. Memory Unit
   c. Input/Output Unit d. ALU
5. The most efficient method for translating arithmetic expressions into machine language instructions is using
   a. Prefix notation b. Postfix Notation
   c. Infix Notation d. None of Above
6. Zero Address instruction format is used for
   a. RISC b. CISC
   c. Von-Neumann d. Stack Organized

Q.2.A Show the contents of registers E, A, Q and SC during the process of binary multiplication of two numbers, 14(multiplicand) and 10(multiplier).The signs are not included. **(05)**

Q.2.B Design a Flowchart for addition and subtraction of two binary numbers A and B. Assume that the numbers are stored in signed-magnitude representation. **(05)**

OR

Q.2.A Show the step-by-step multiplication process using Booth algorithm when the following numbers are multiplied, +14(multiplicand) and -10(multiplier). Assume 5-bit registers that hold signed numbers. **(05)**

Q.2.B Show the contents of register E, A, Q and SC during the process of division of 10010011 by 1011.(Use a dividend of eight bits). **(05)**