Date:

EXPERIMENT NO. 4

AIM: Implement arithmetic and logic unit circuits in Logisim.

OBJECTIVES:

i. Implement 1-bit, 2-bit, 4-bit and 8-bit arithmetic unit circuits

ii. Implement 1-bit, 2-bit, 4-bit and 8-bit logical unit circuits for four logical functions

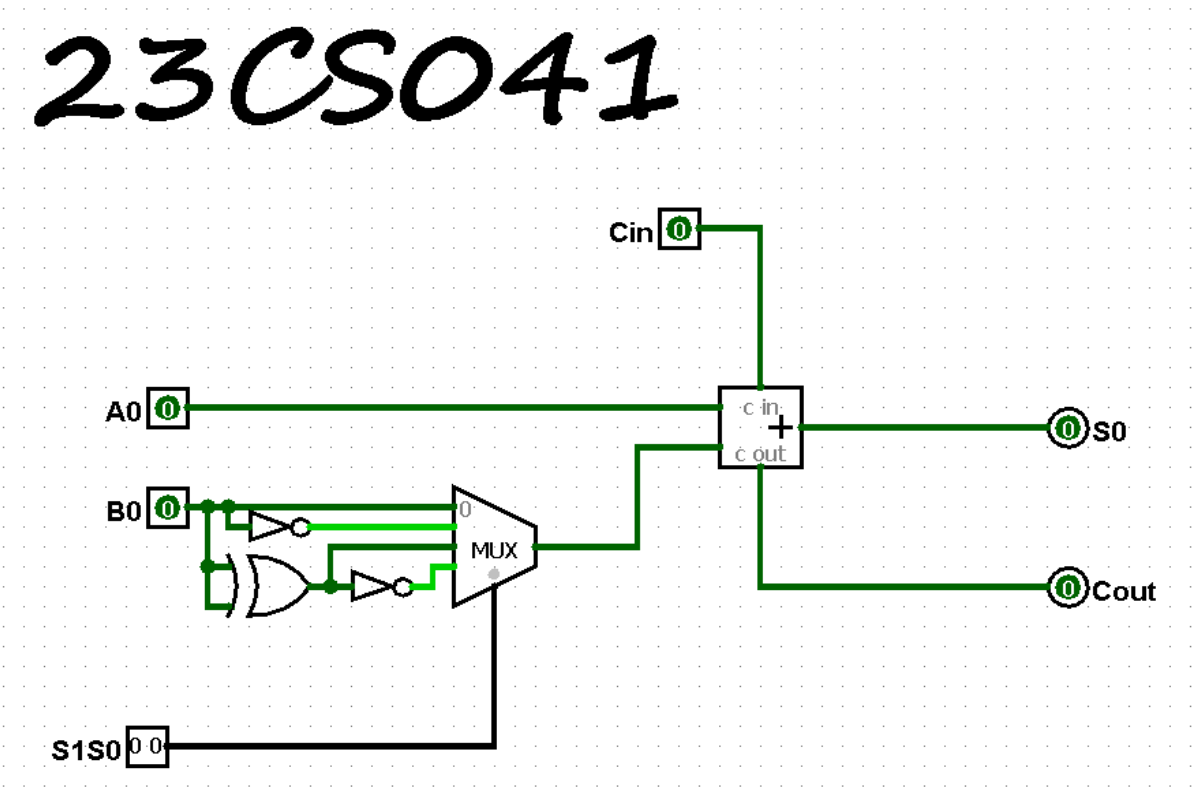
iii. Implement 1-bit and 2-bit logical unit circuits for sixteen logical functions

iv. Implement 2-bit, 4-bit and 8-bit bidirectional shifter

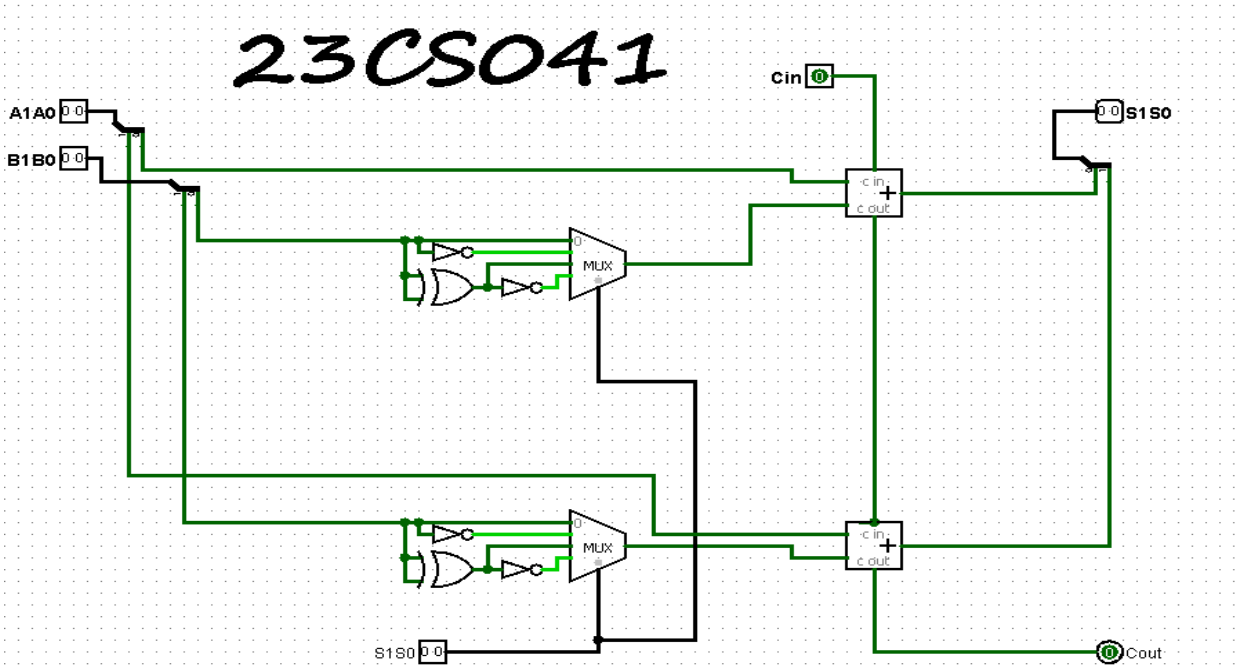
v. Implement 1-bit, 2-bit, 4-bit and 8-bit ALU

CIRCUITS:

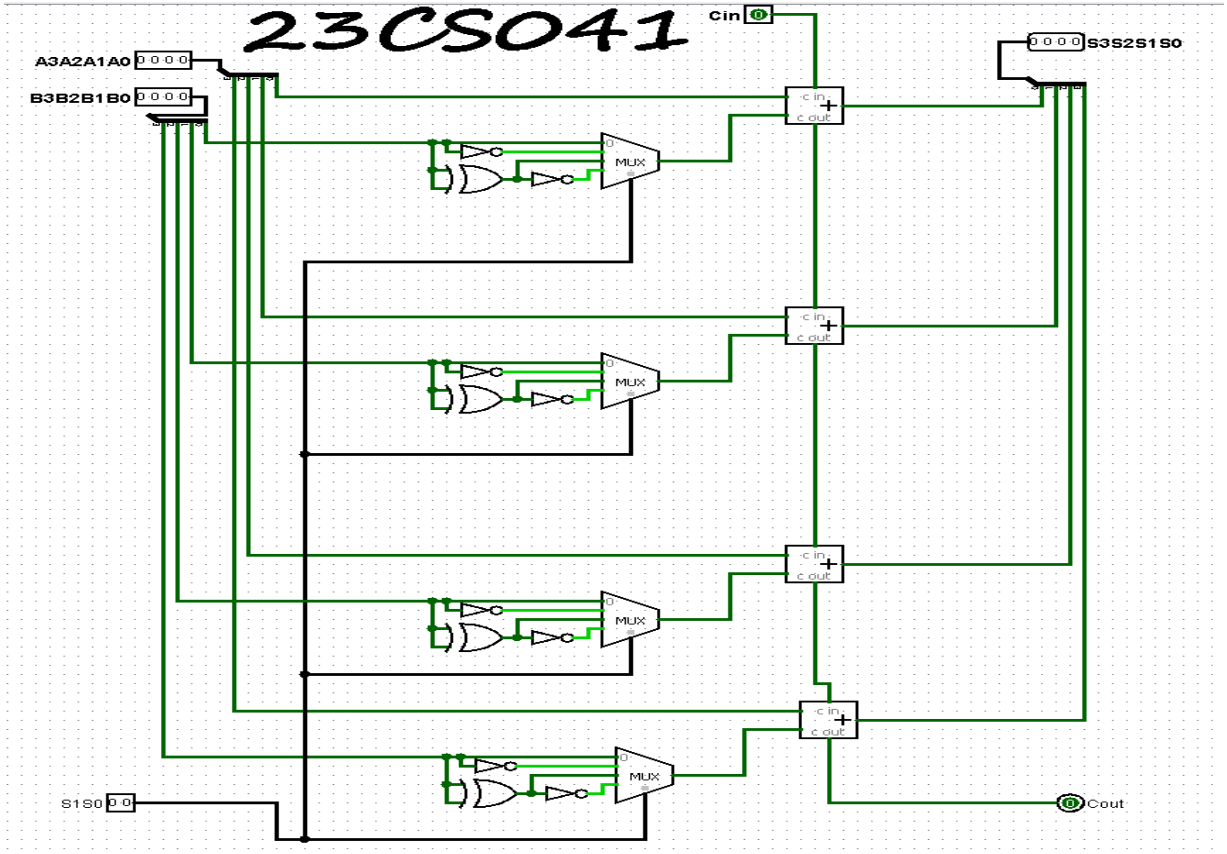
i. 1) 1-bit arithmetic



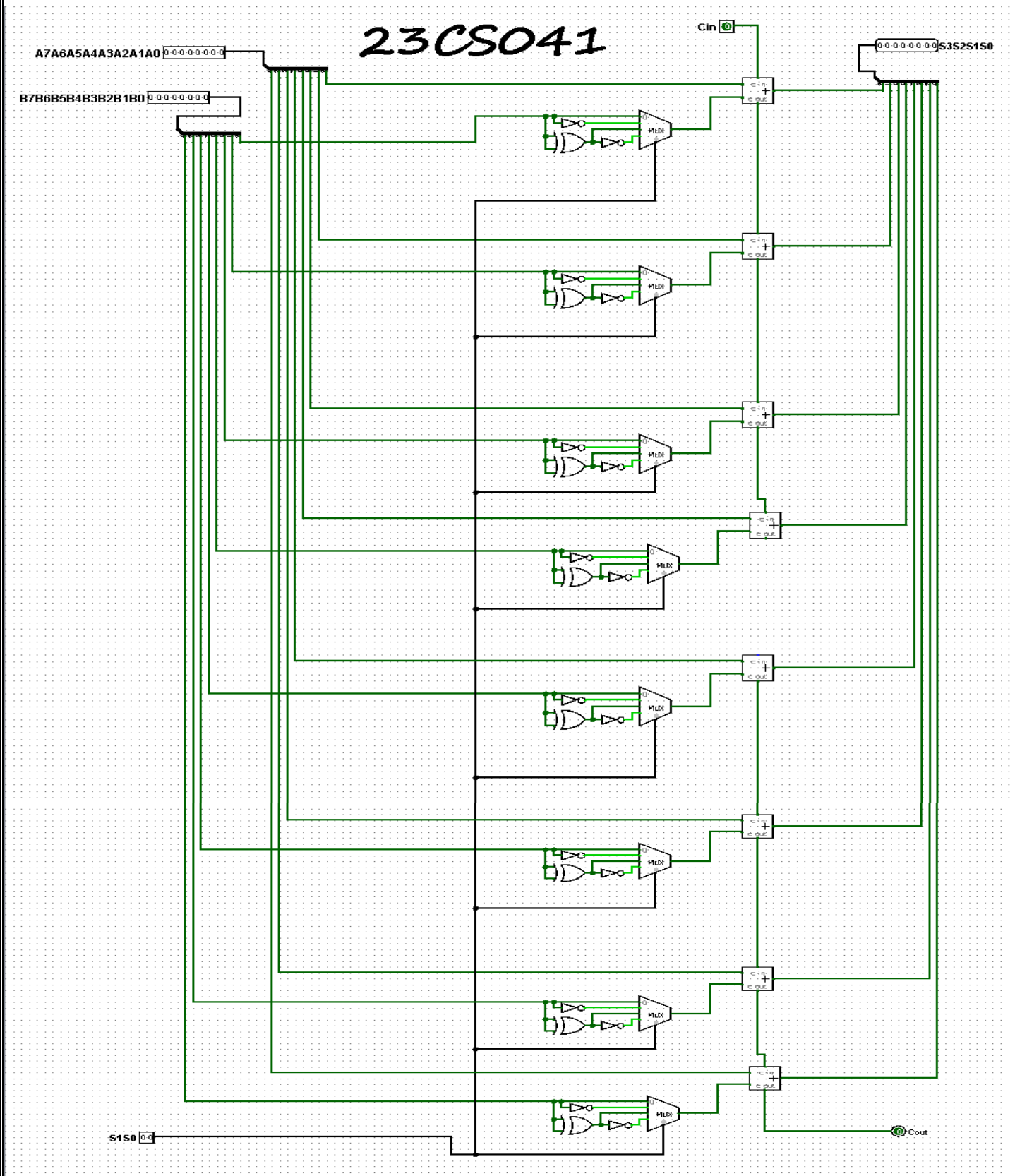
2) 2-bit arithmetic



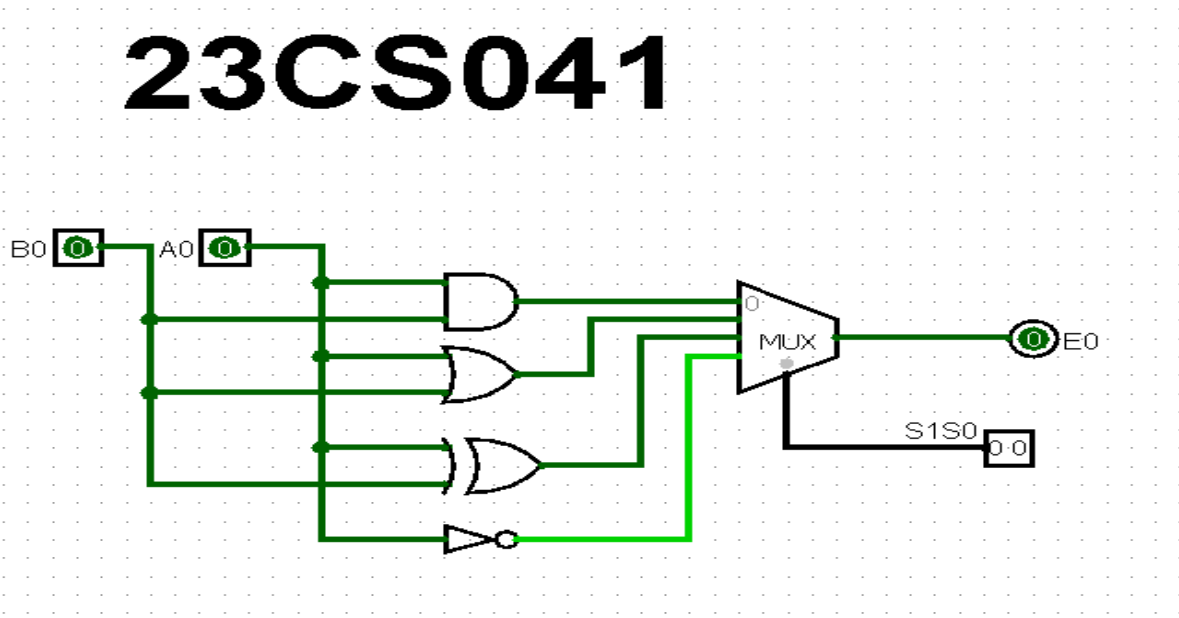
3) 4-bit arithmetic



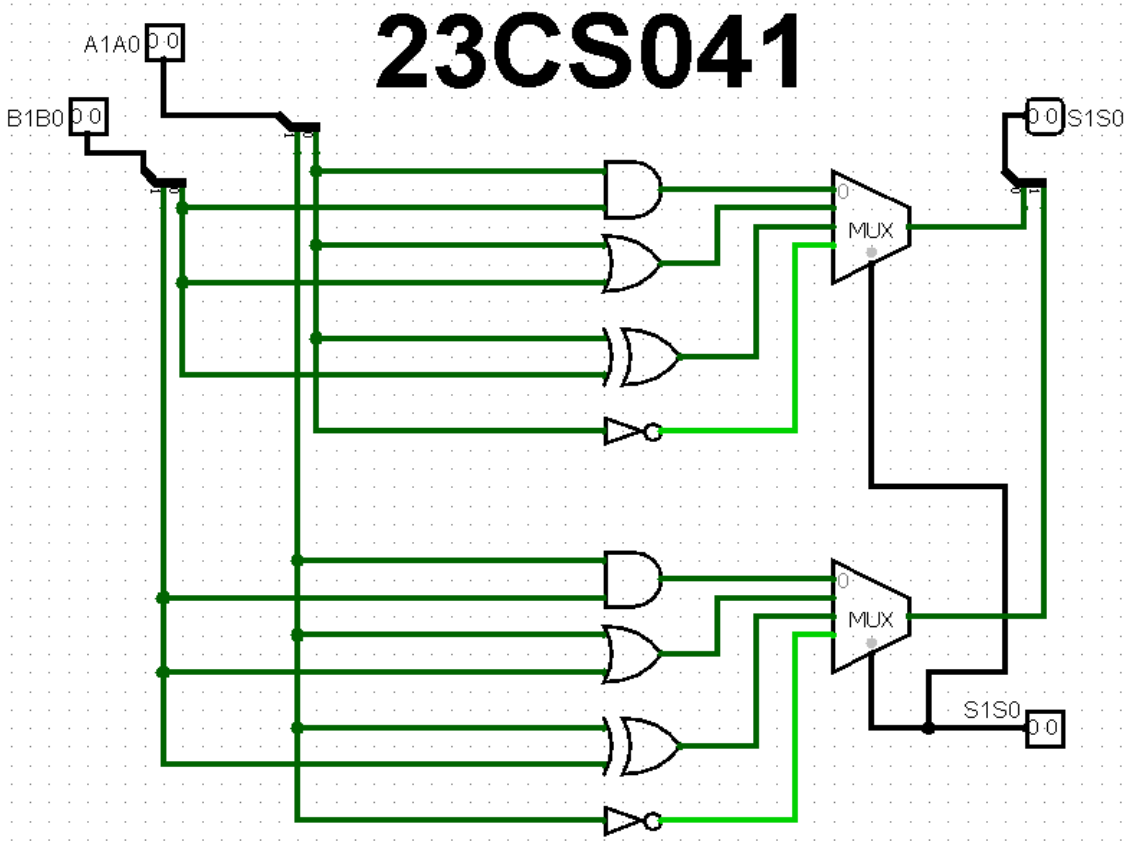
4) 8-bit arithmetic



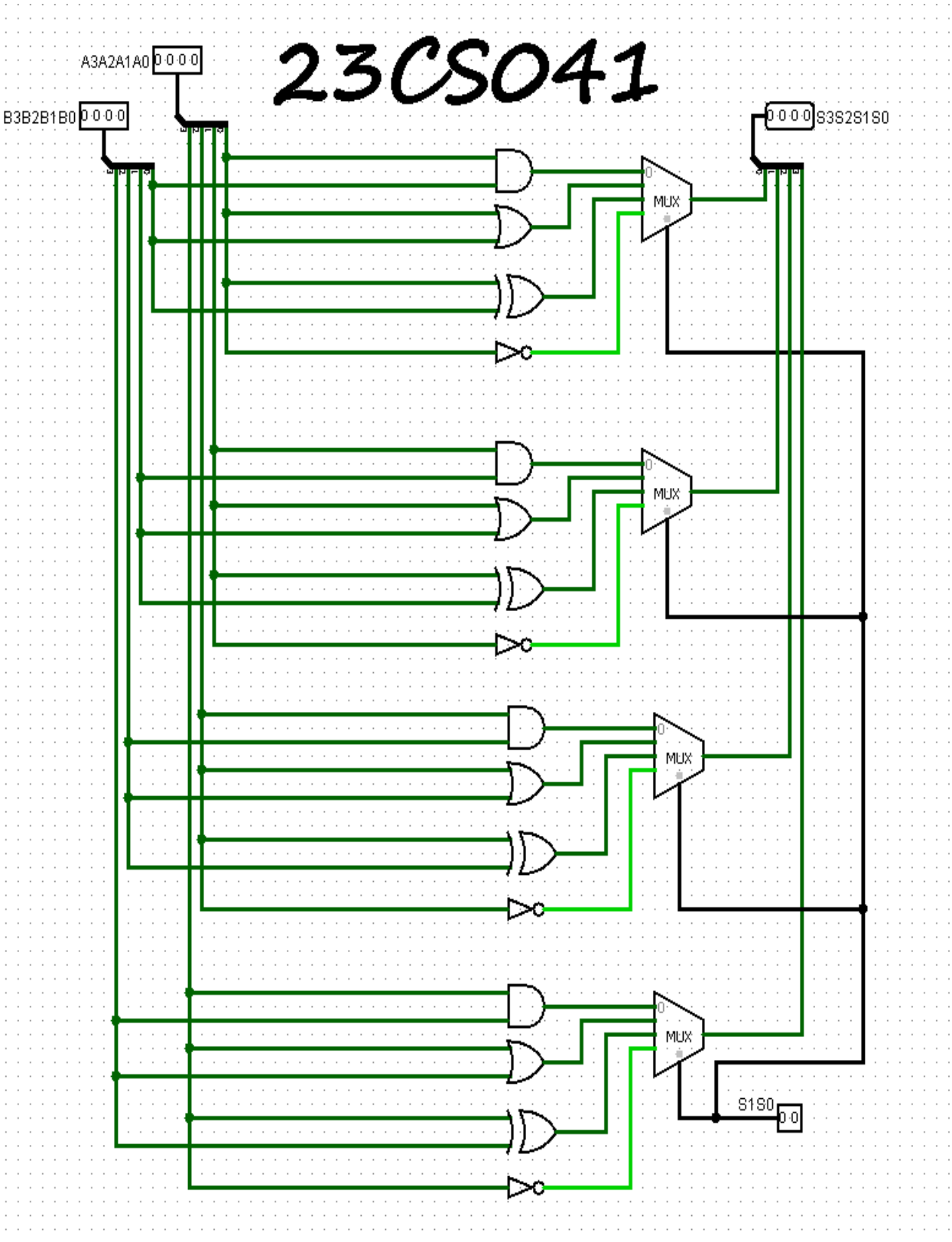
ii. 1) 1-bit logical



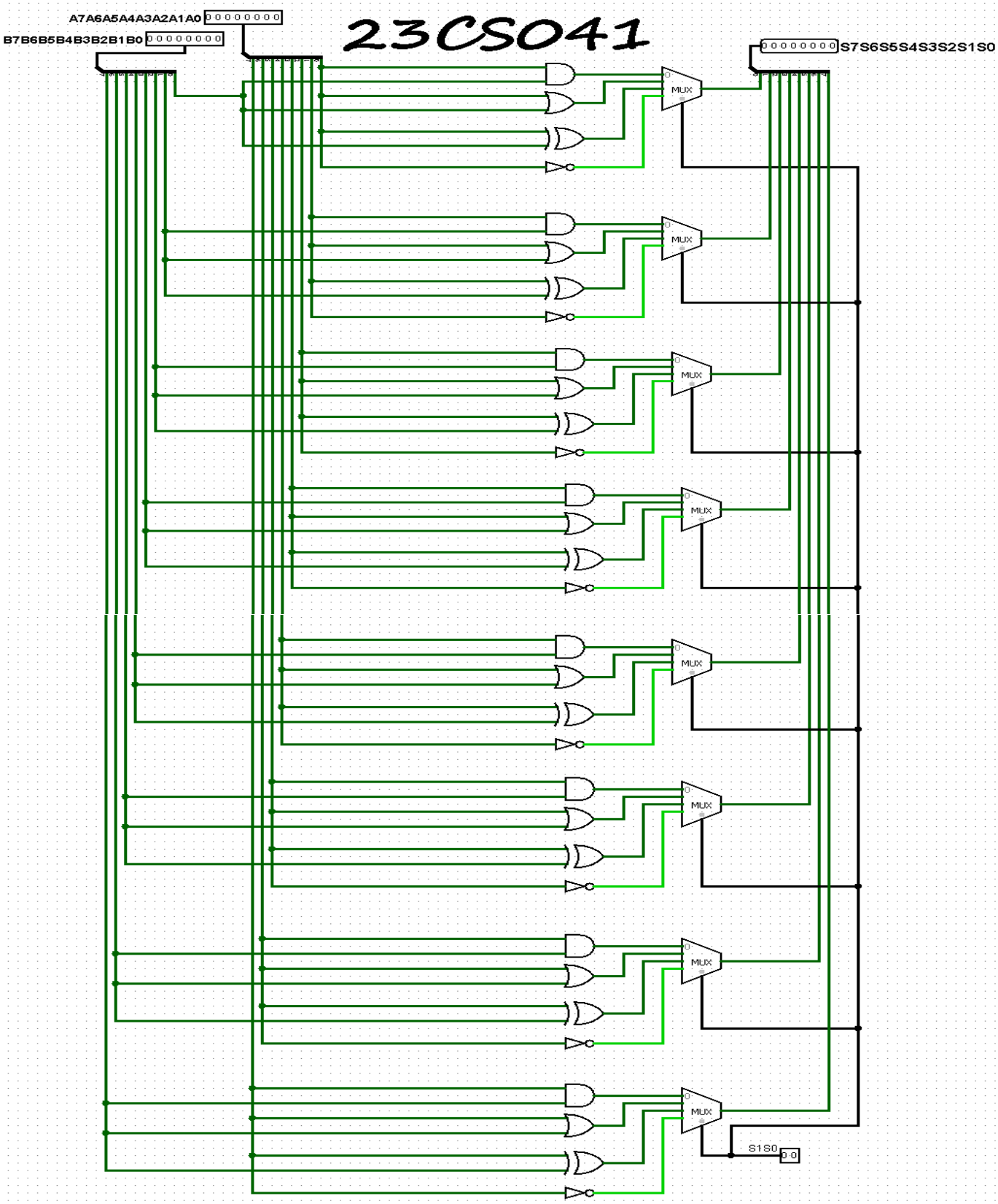
2) 2-bit logical



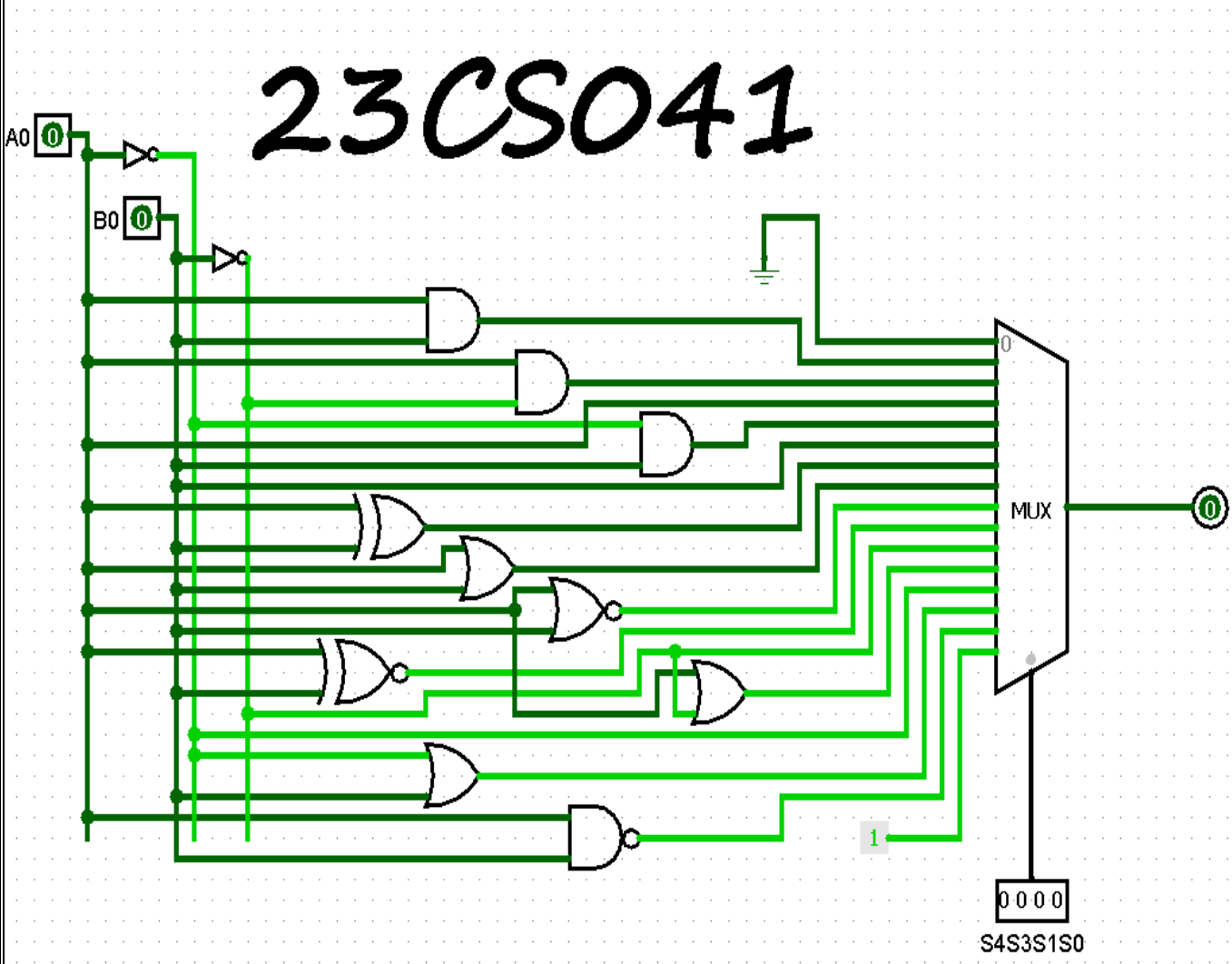
3) 4-bit logical



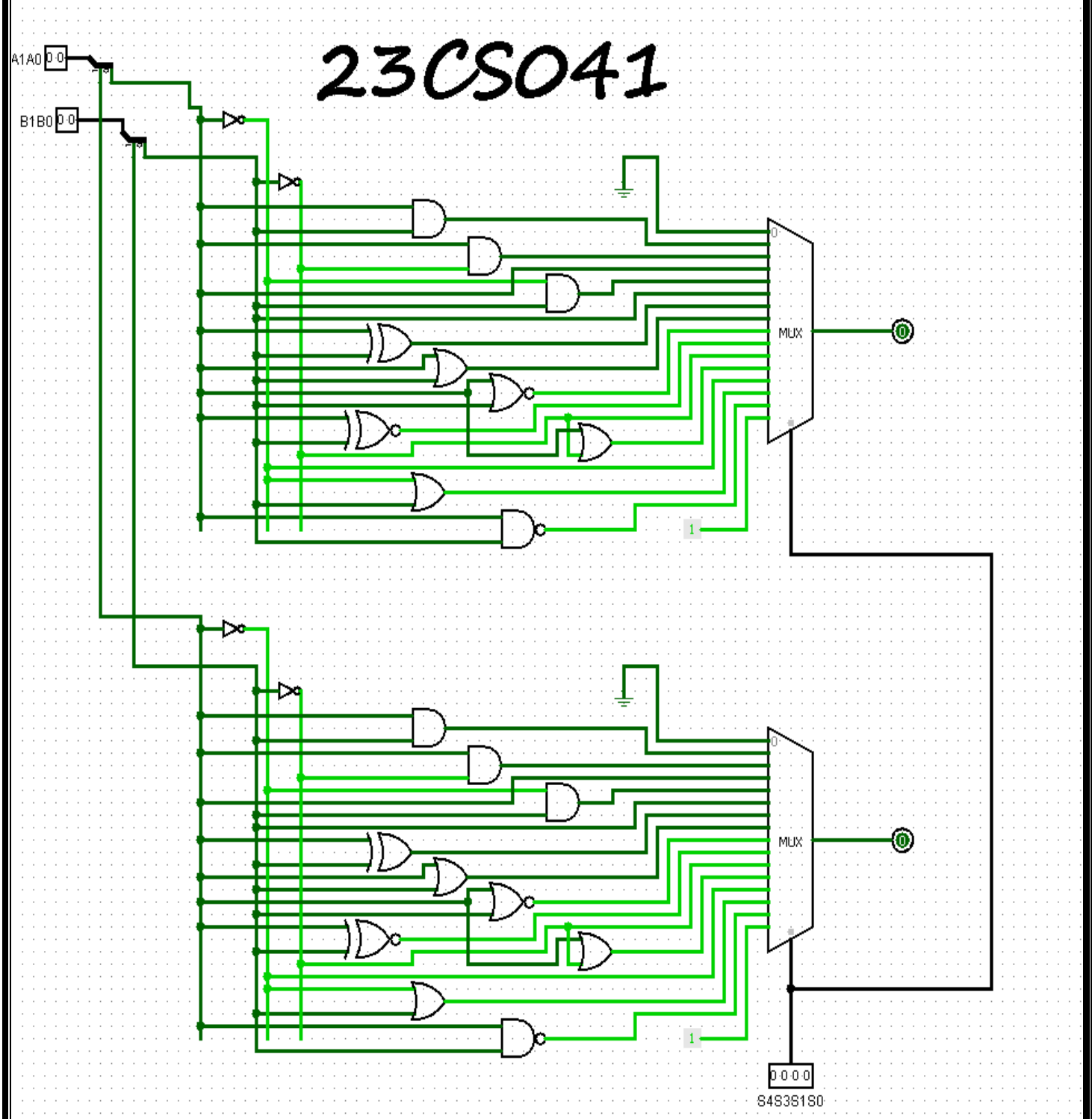
4) 8-bit logical



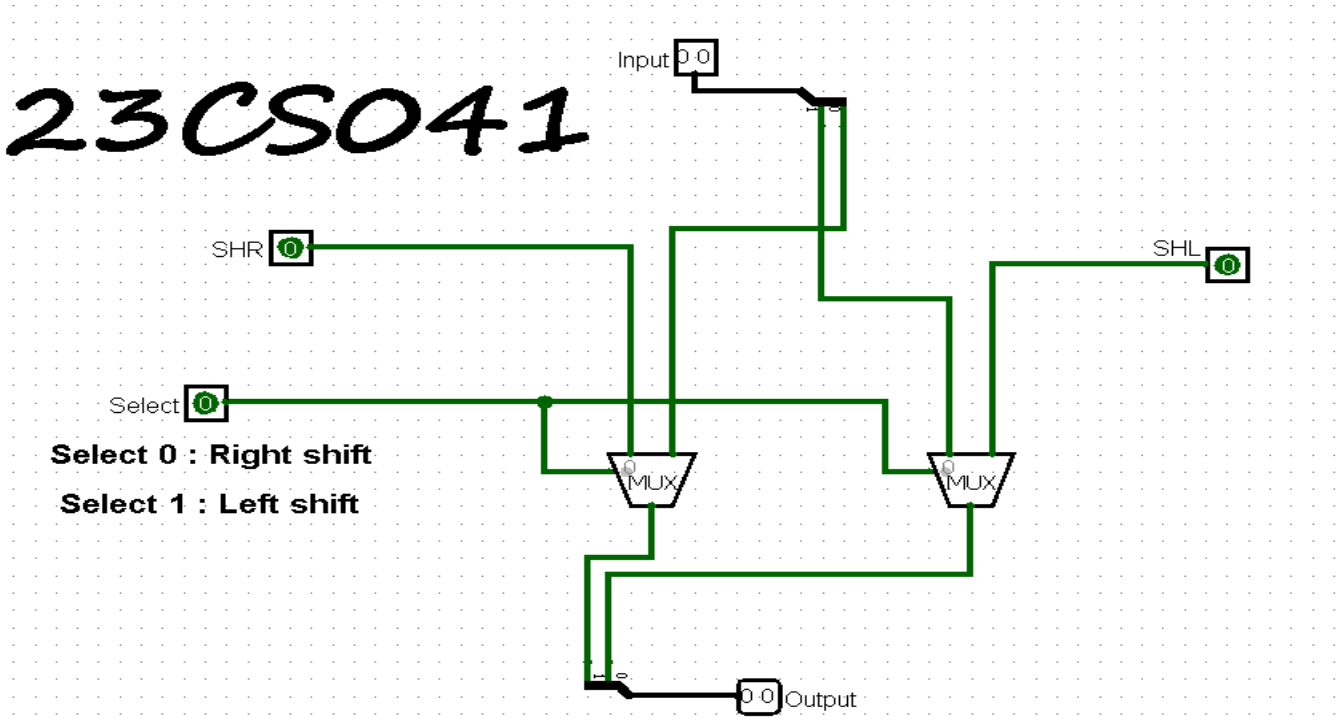
iii. 1) 1-bit logical circuits for sixteen logical functions



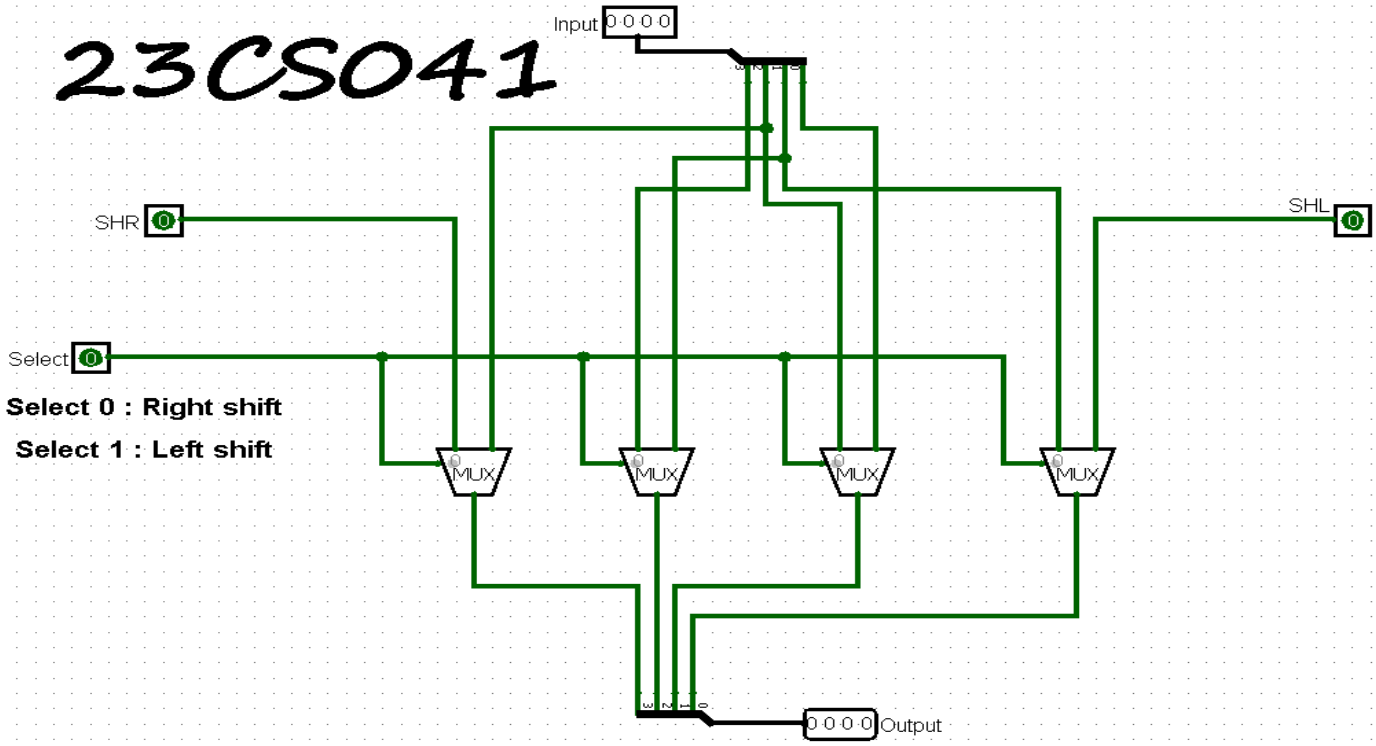
2) 2-bit logical circuits for sixteen logical functions



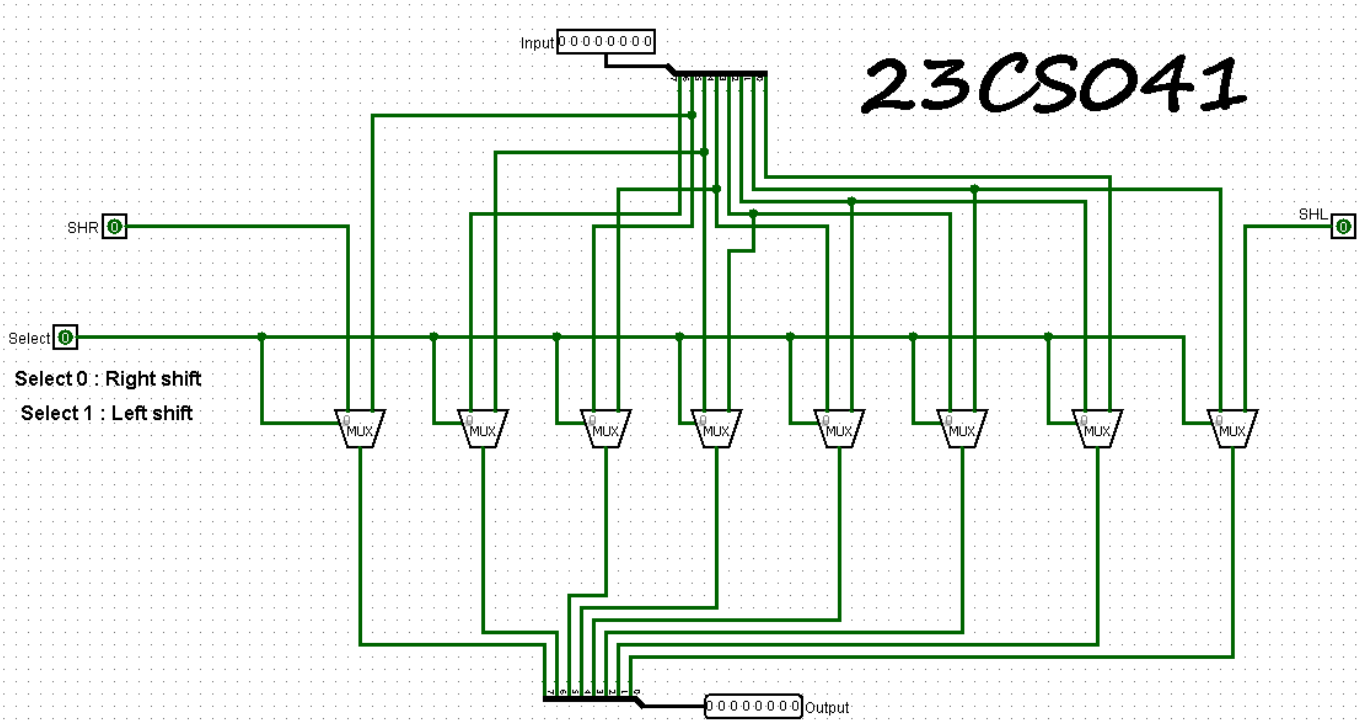
iv. 1) 2-bit bidirectional shifter



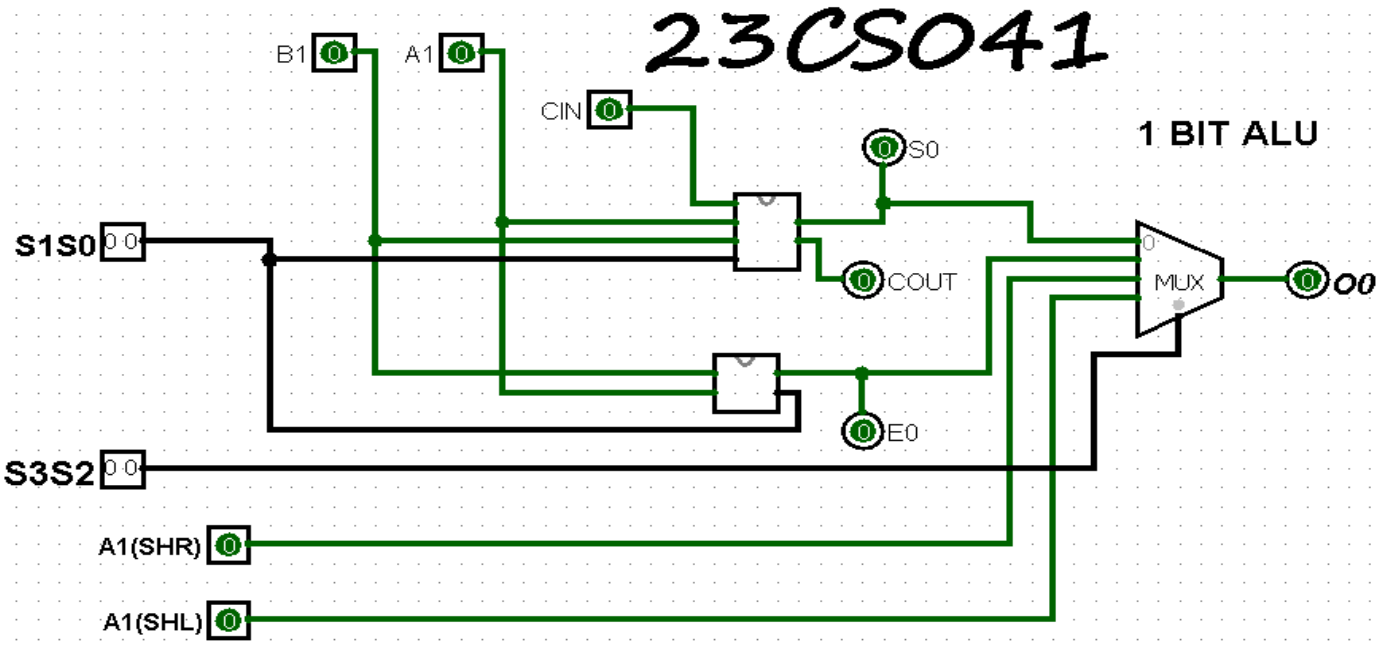
2) 4-bit bidirectional shifter



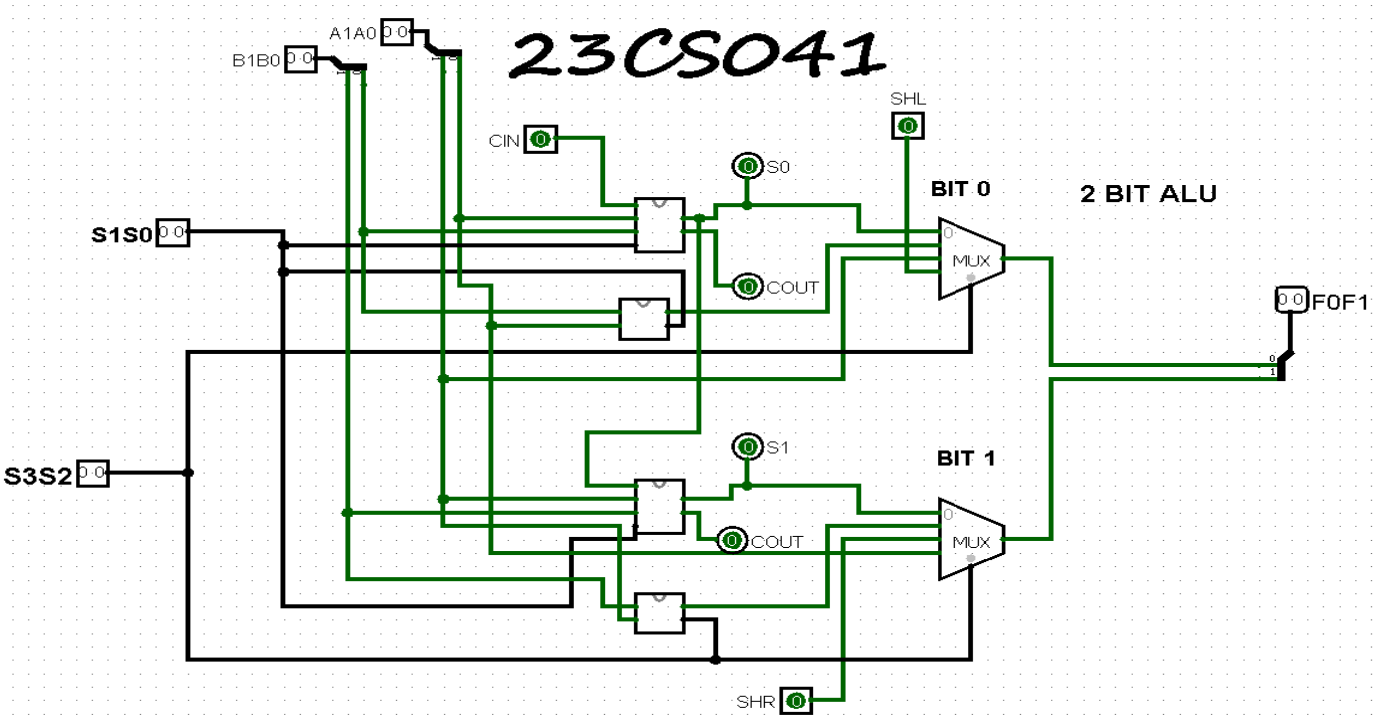
3) 8-bit bidirectional shifter



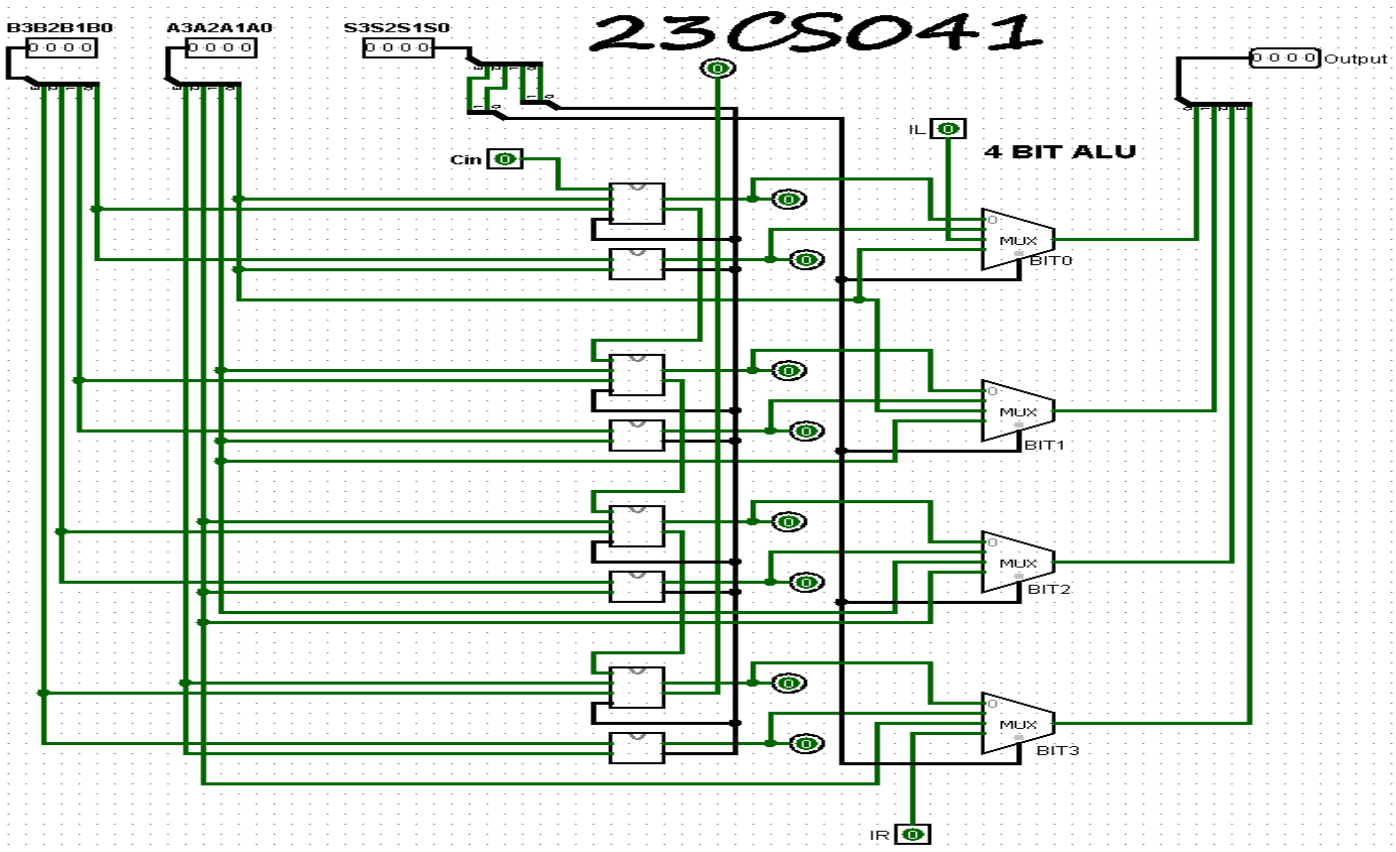
v. 1) 1-bit ALU



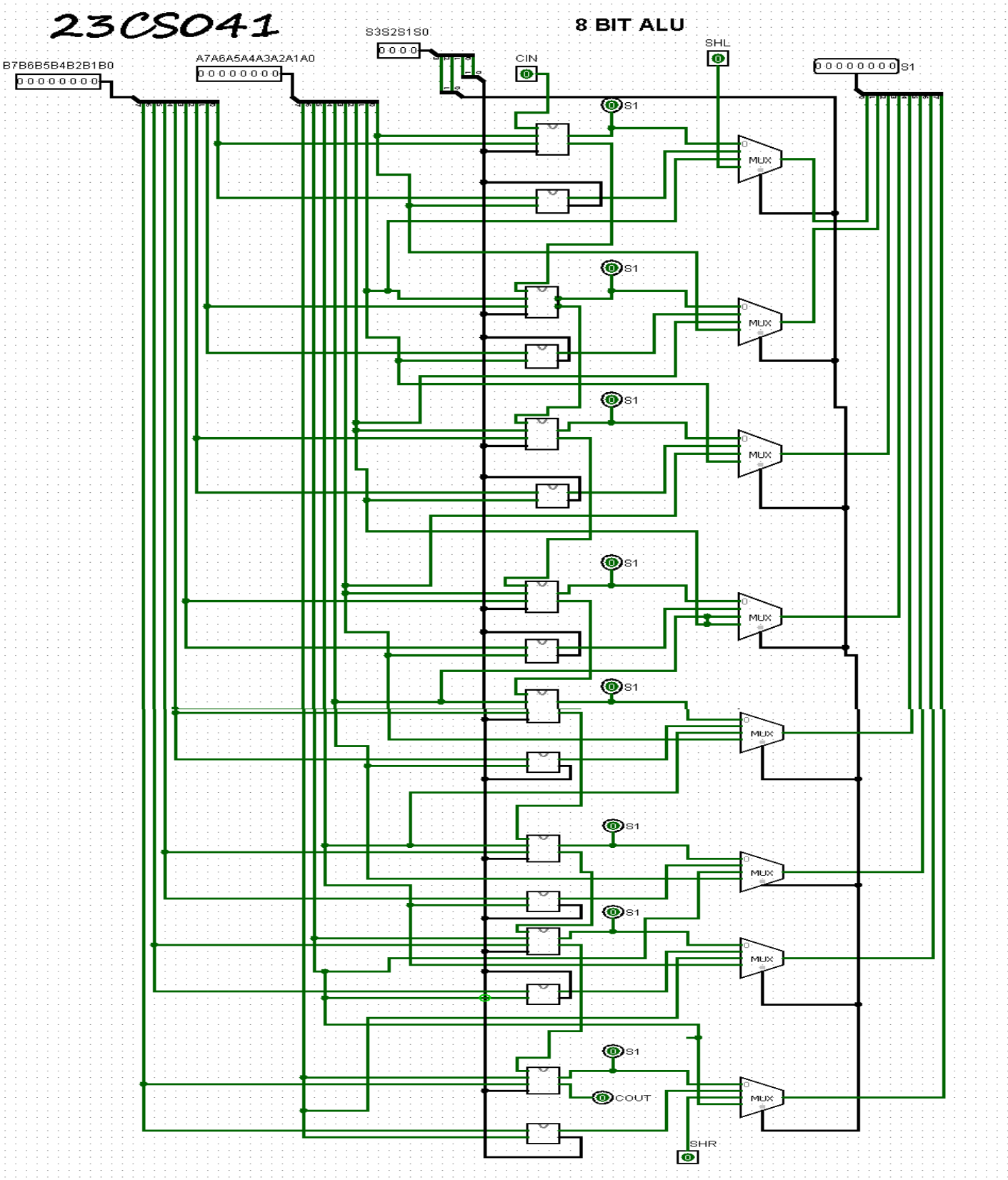
2) 2-bit ALU



3) 4-bit ALU

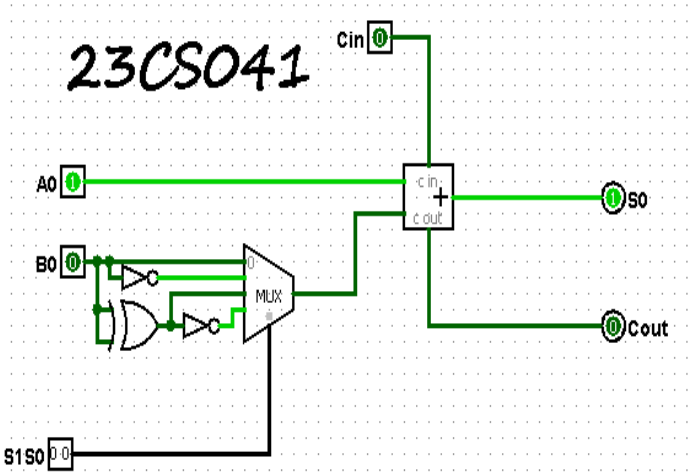


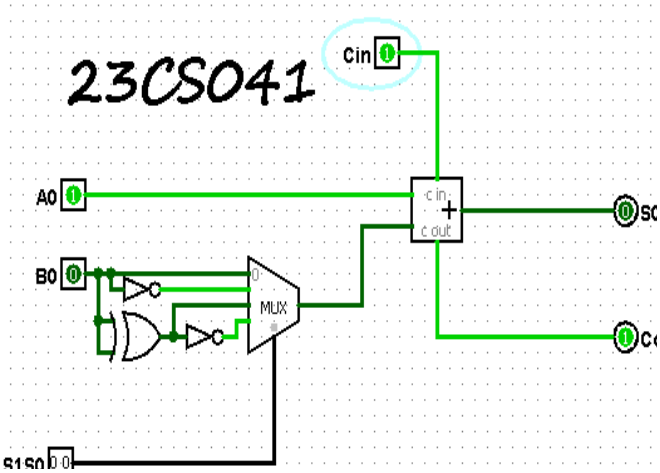
4) 8-bit ALU

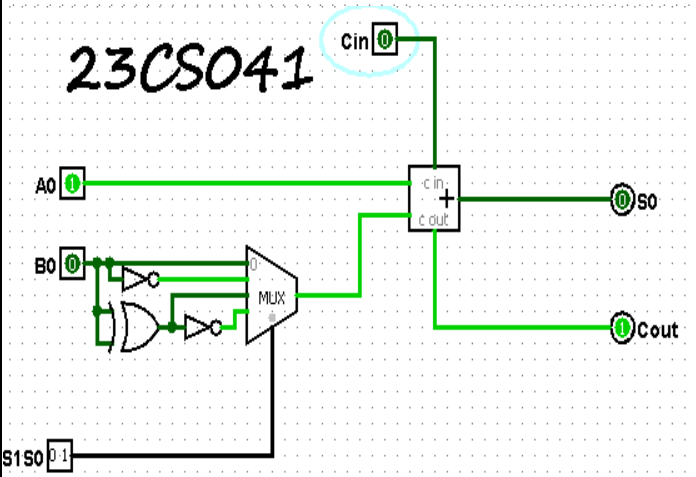

23CS041
8 BIT ALU
B7B6B5B4B2B1B0
A7A6A5A4A3A2A1A0
S3S2S1S0
CIN
SHL
S1
MUX
COUT
SHR

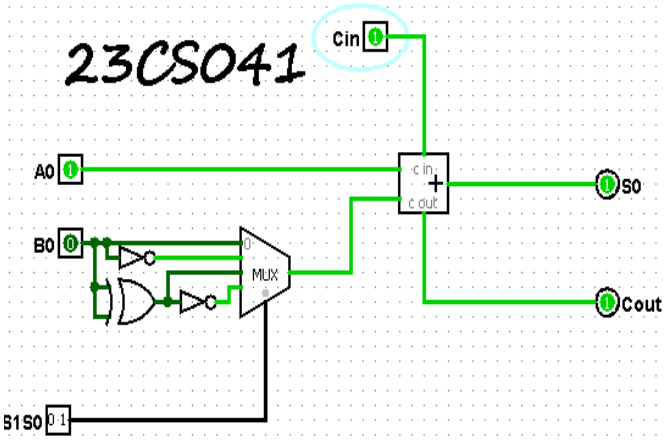
OUTPUTS:

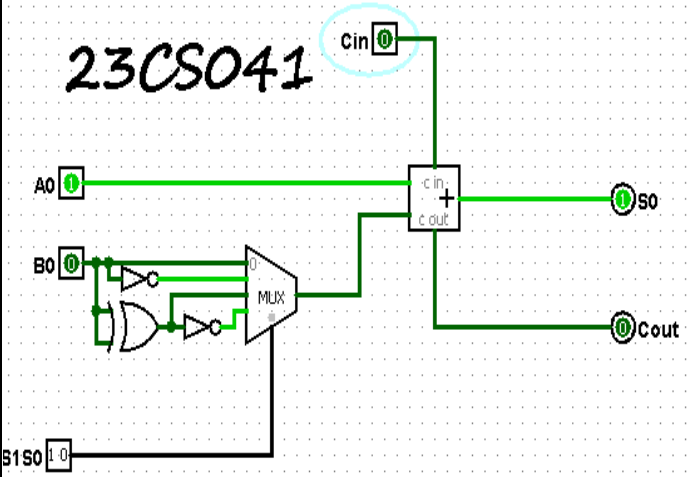
i. 1) 1 bit arithmetic

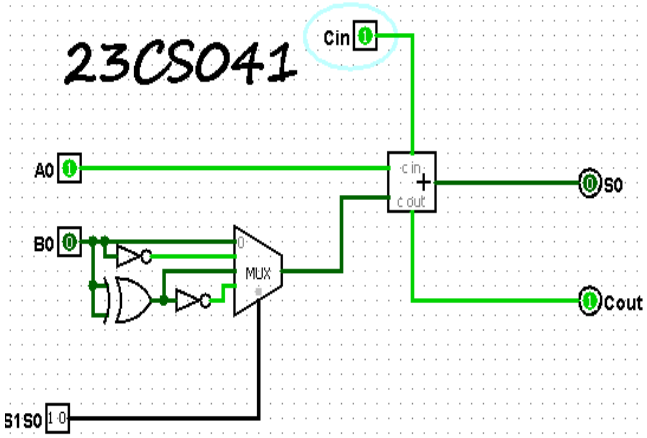


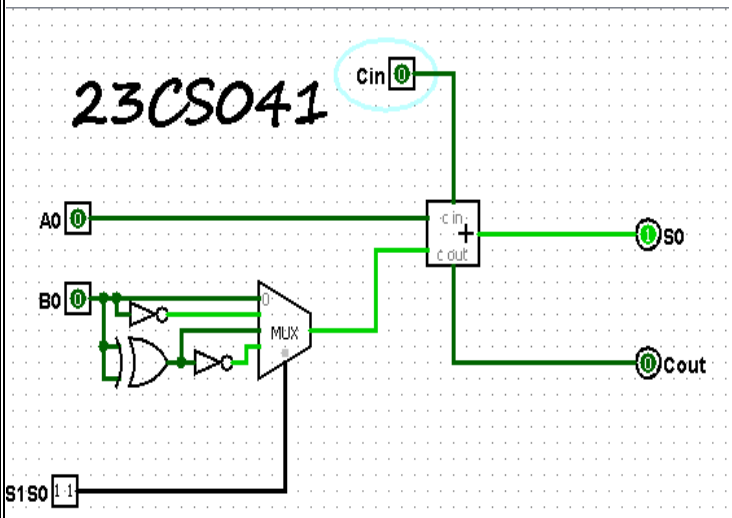


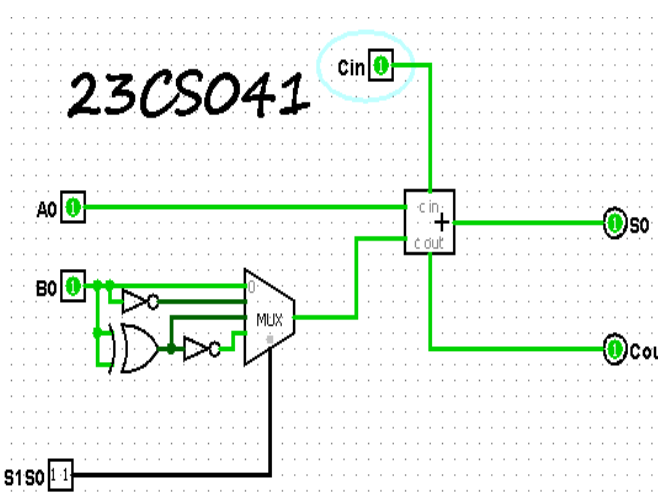




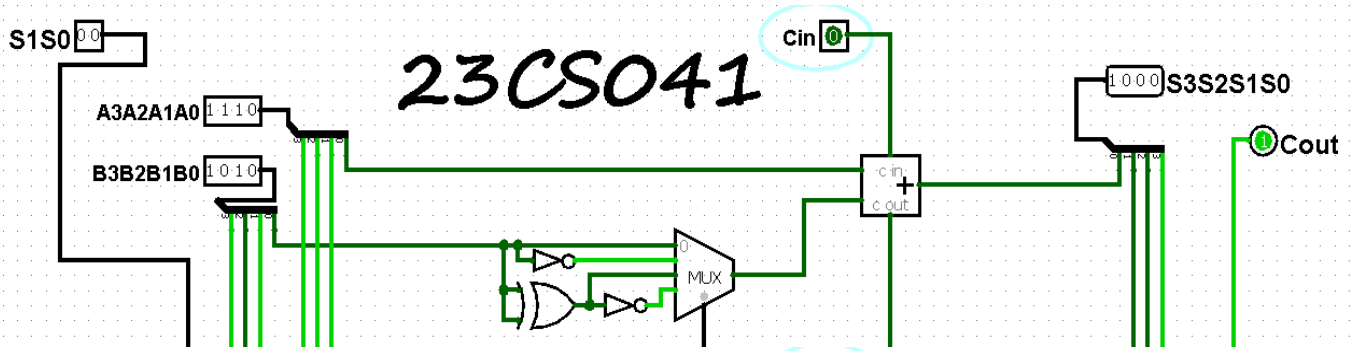


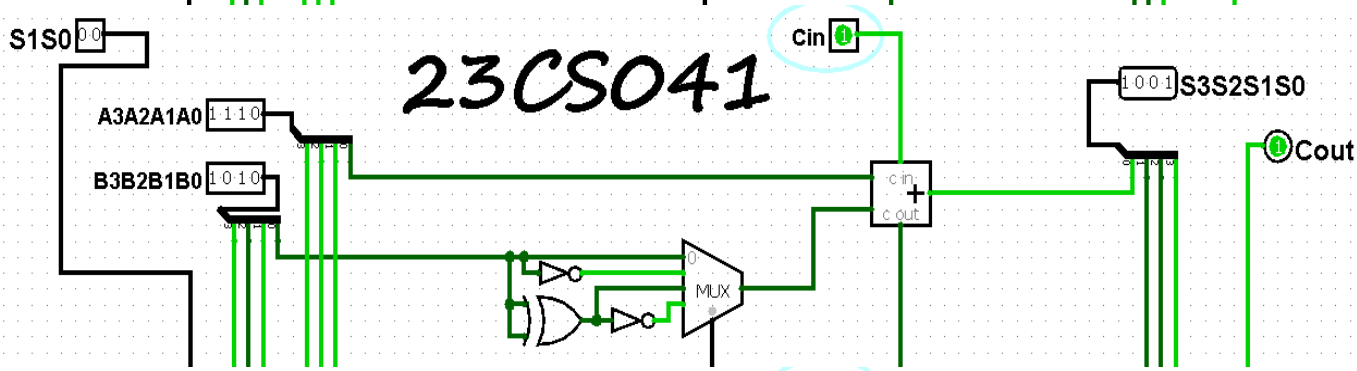


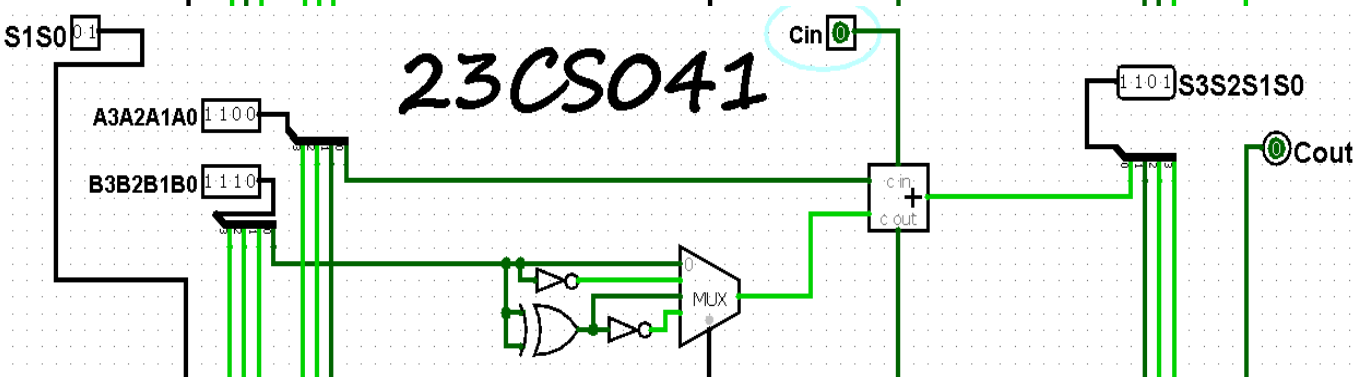


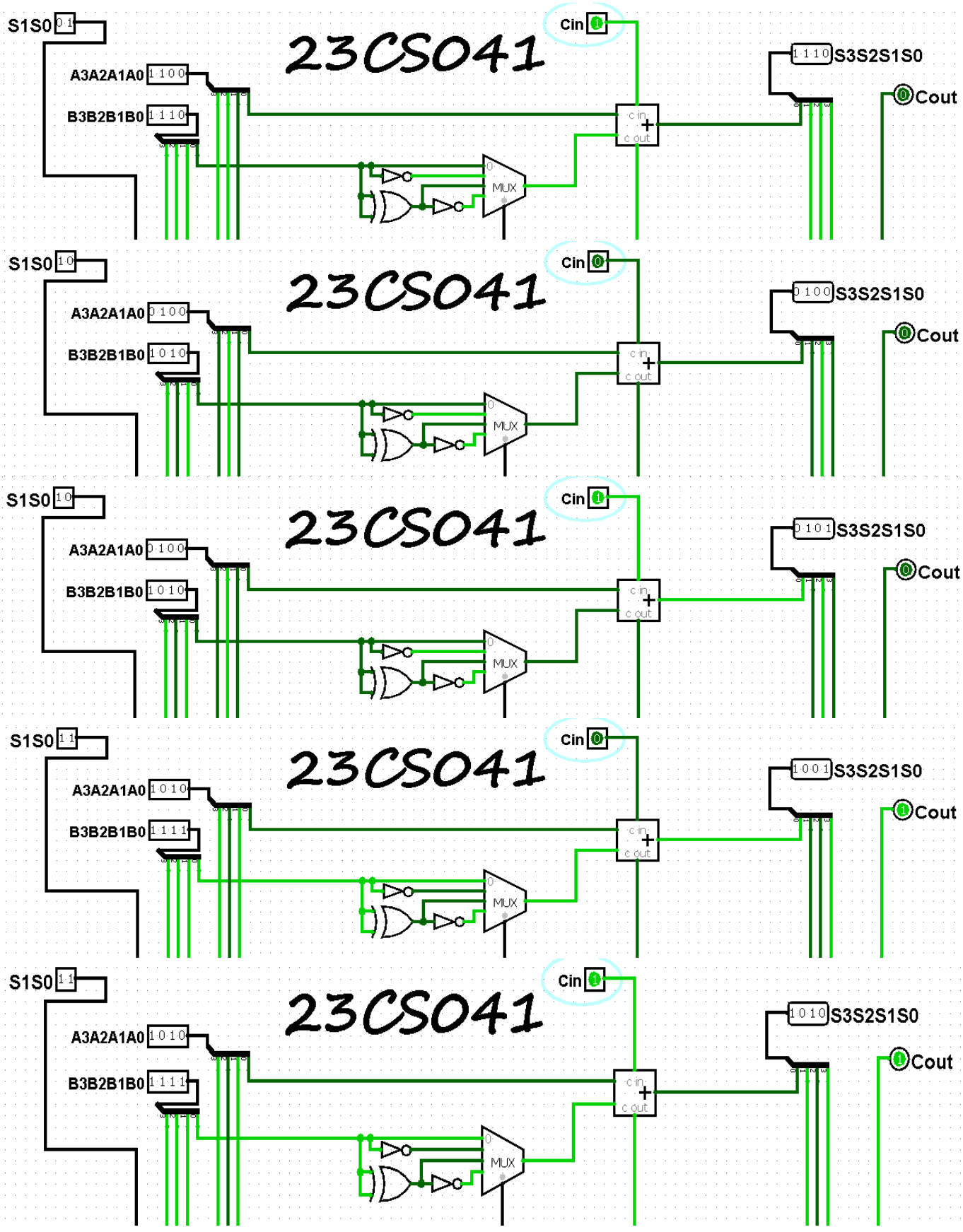


2) 4 bit arithmetic

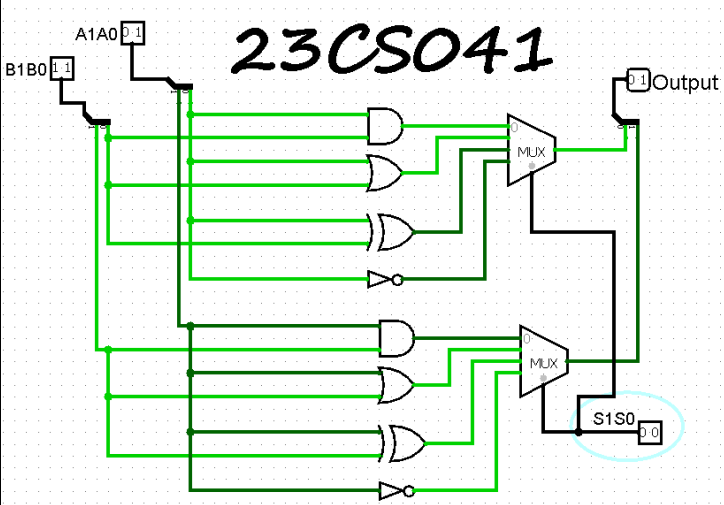


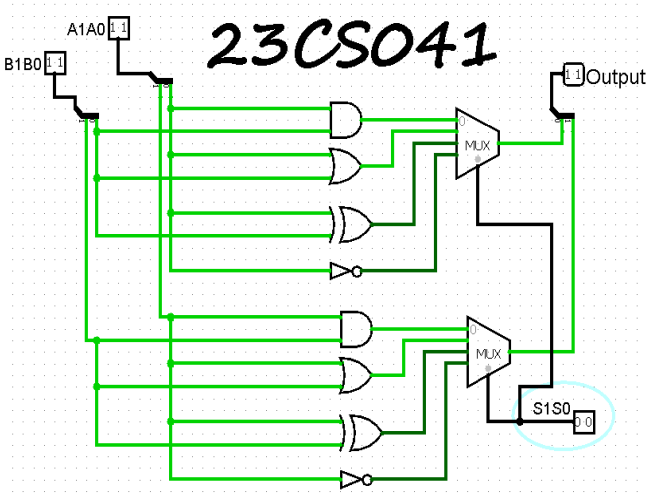


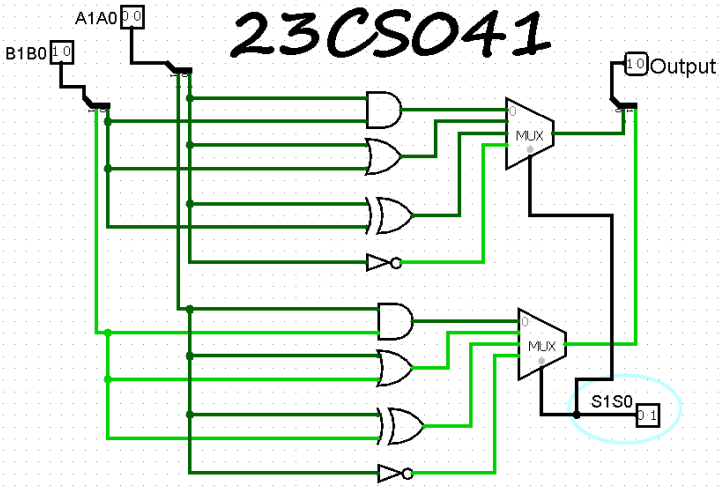


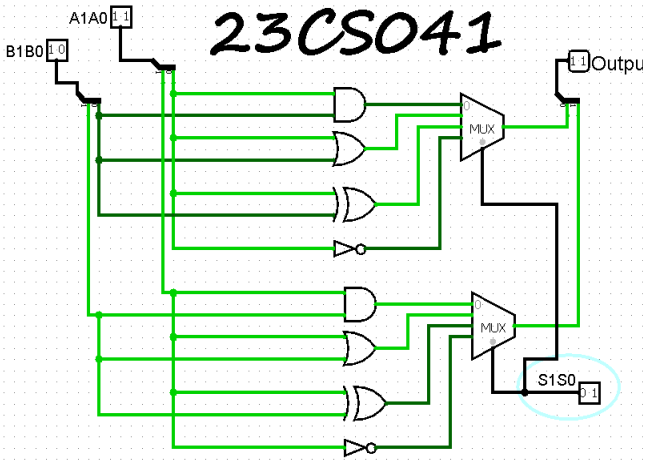

S1S0 01
A3A2A1A0 1100
B3B2B1B0 1110
23CS041
Cin 1
1110 S3S2S1S0
0 Cout
S1S0 10
A3A2A1A0 0100
B3B2B1B0 1010
23CS041
Cin 0
0100 S3S2S1S0
0 Cout
S1S0 10
A3A2A1A0 0100
B3B2B1B0 1010
23CS041
Cin 1
0101 S3S2S1S0
0 Cout
S1S0 11
A3A2A1A0 1010
B3B2B1B0 1111
23CS041
Cin 0
1001 S3S2S1S0
1 Cout
S1S0 11
A3A2A1A0 1010
B3B2B1B0 1111
23CS041
Cin 1
1010 S3S2S1S0
1 Cout
MUX
c in
c out

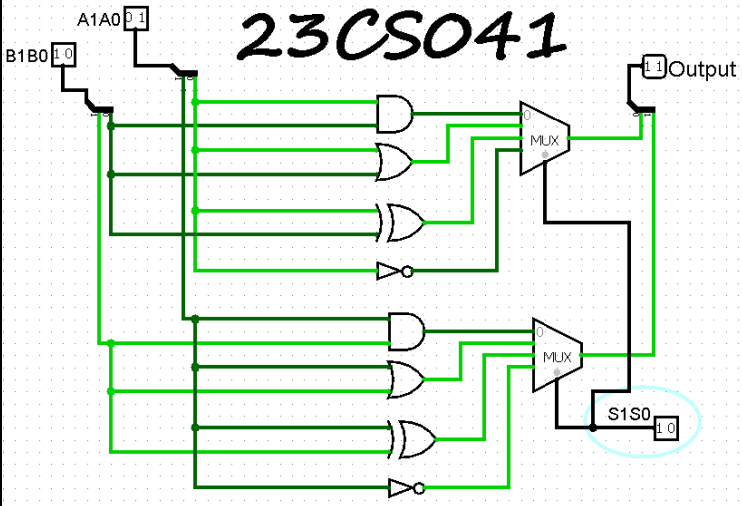
ii. 1) 2 bit logical

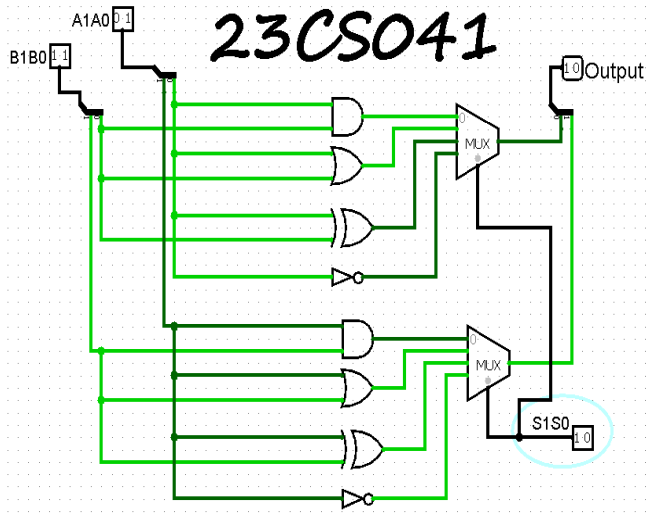


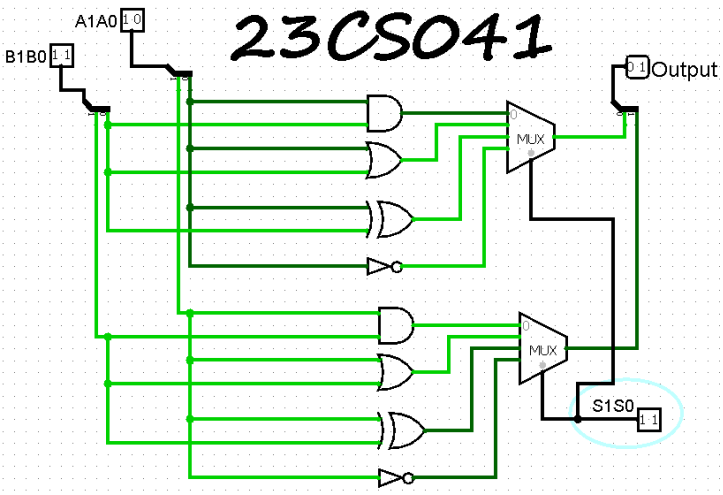


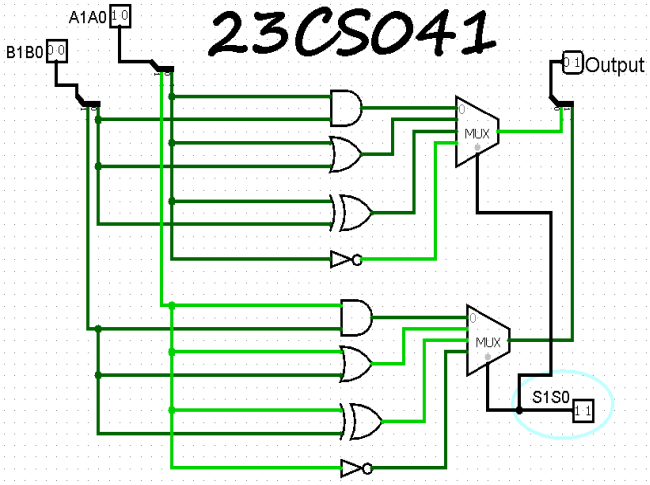




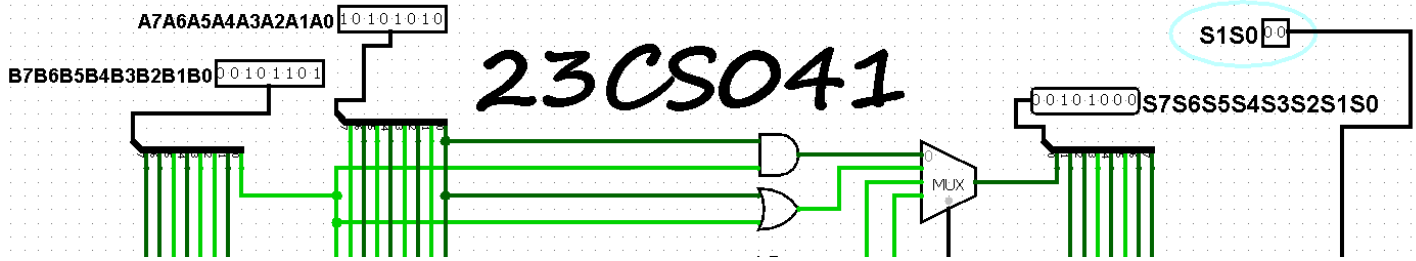


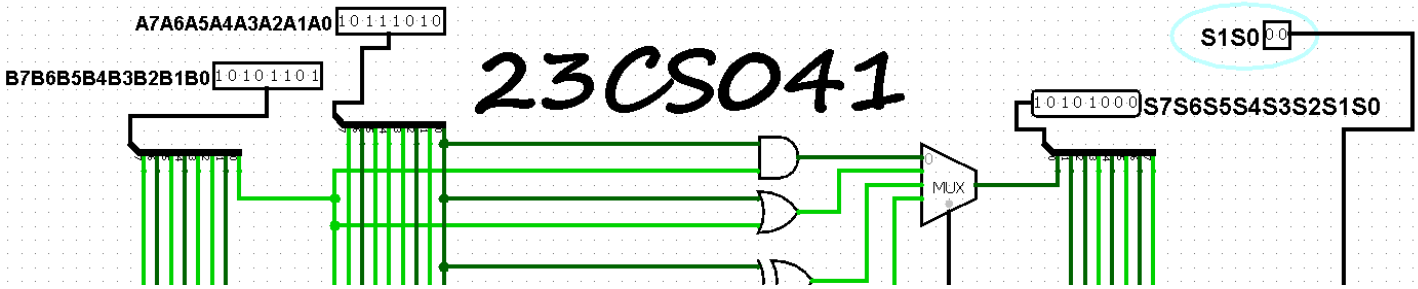


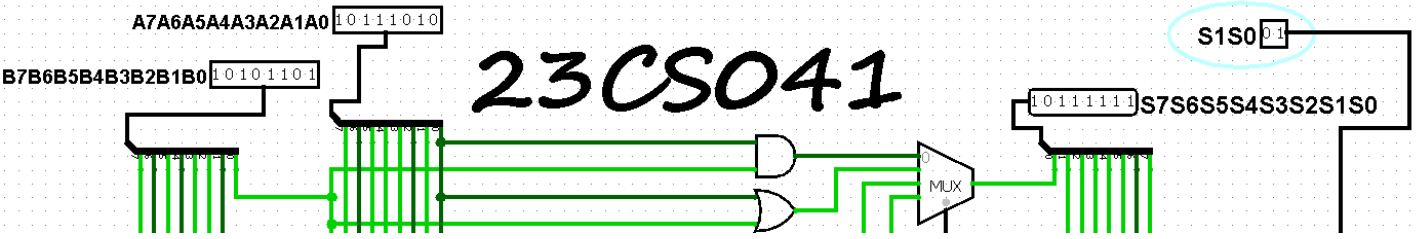


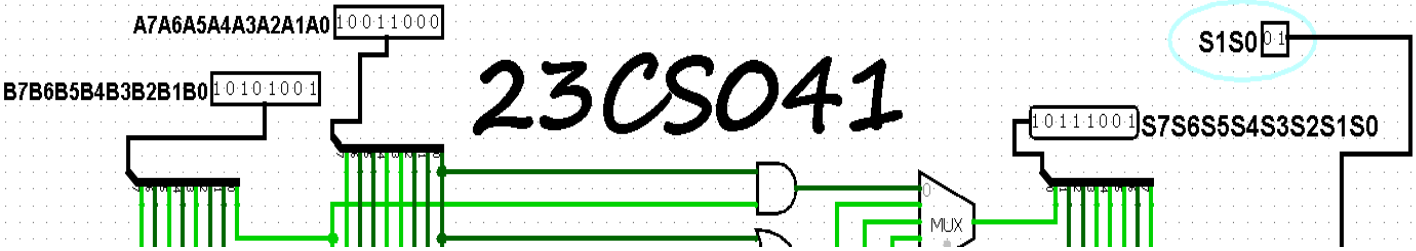


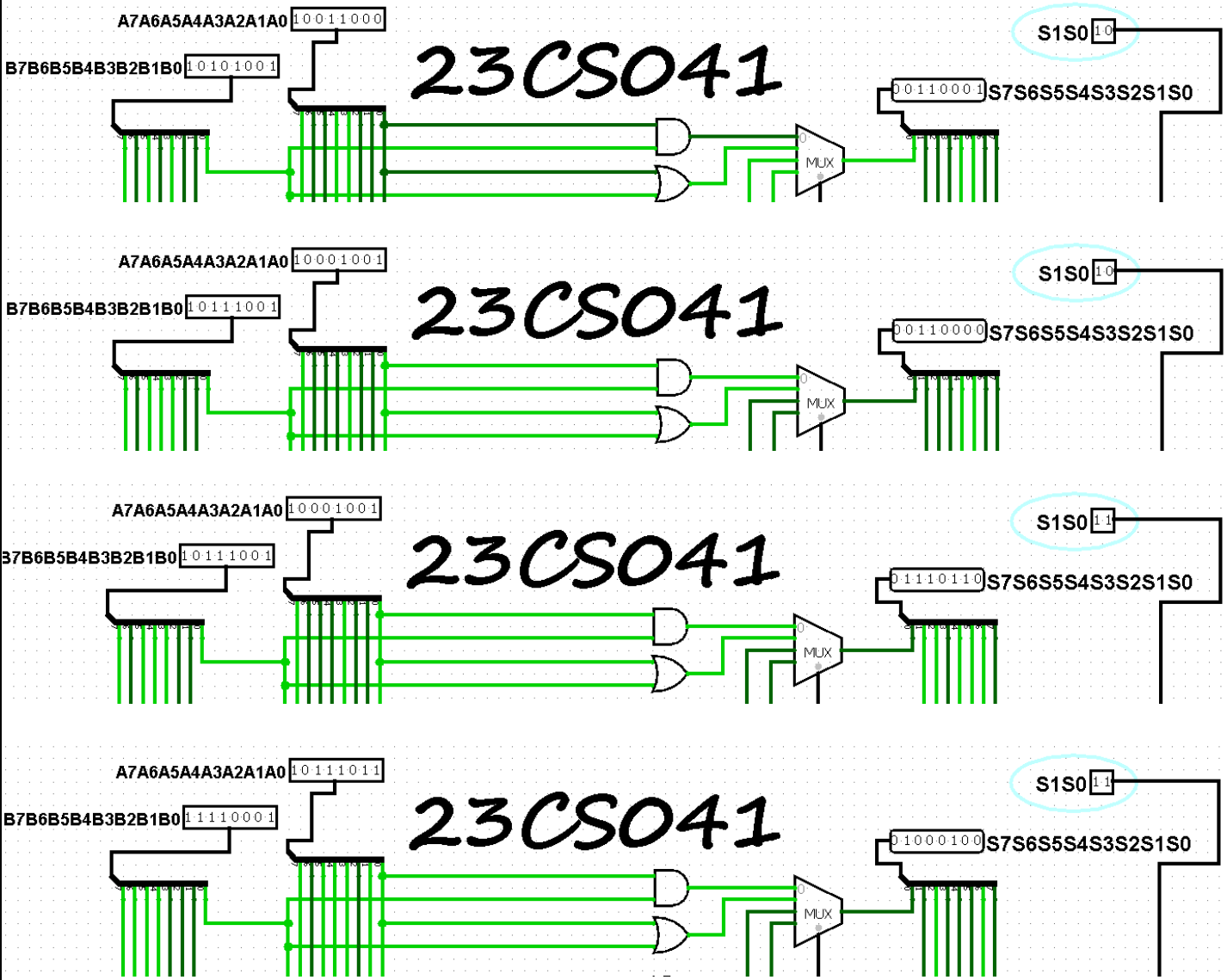
2) 8 bit logical



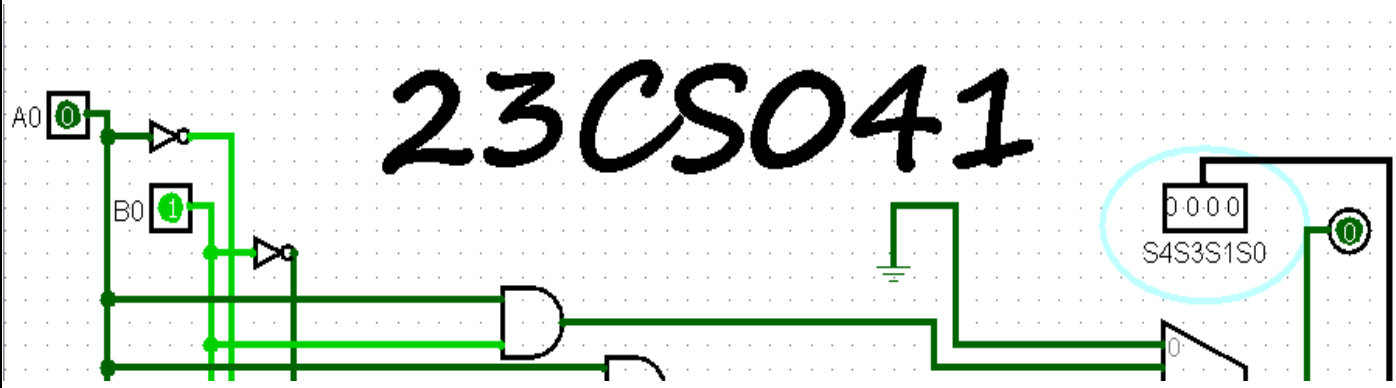


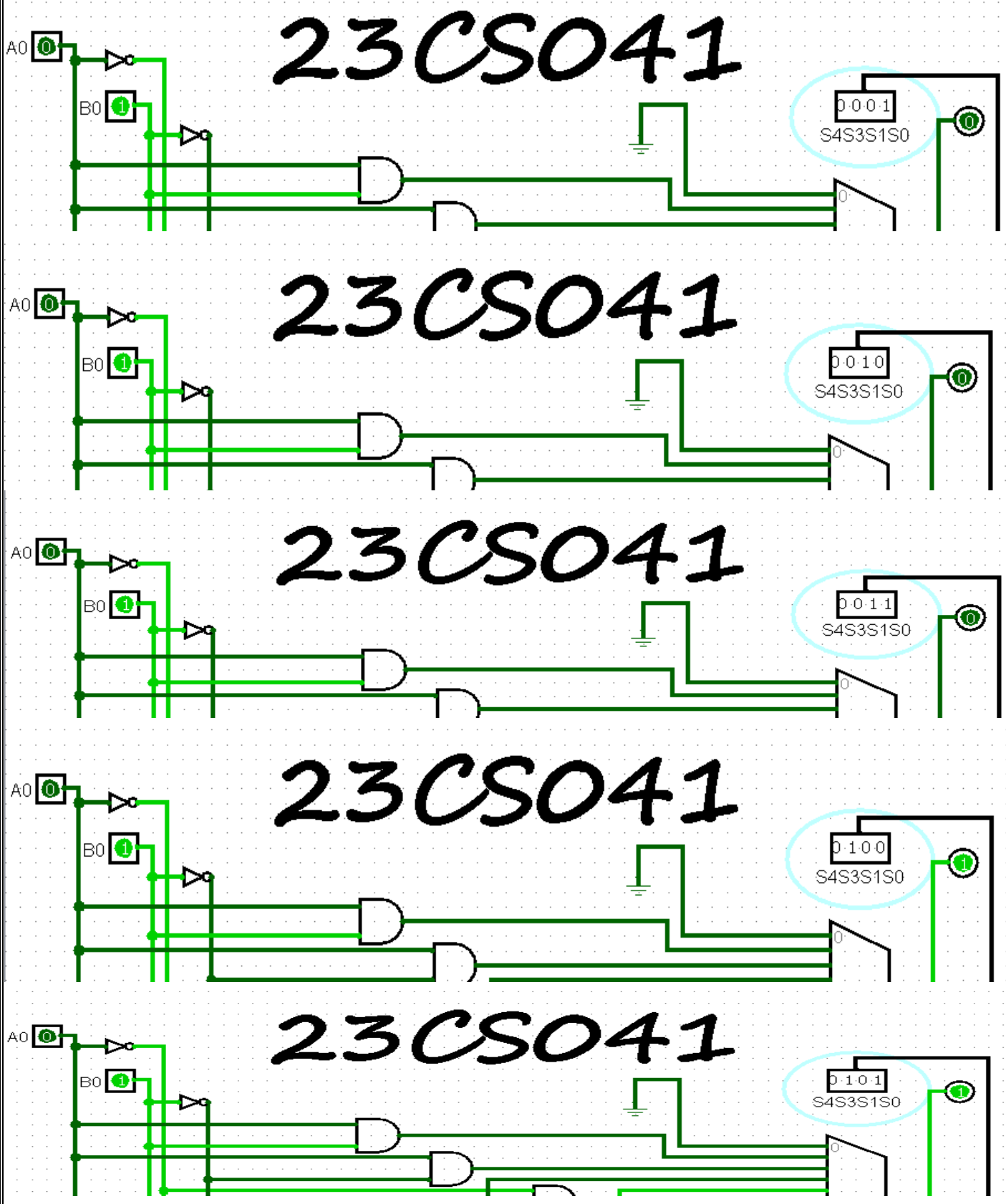


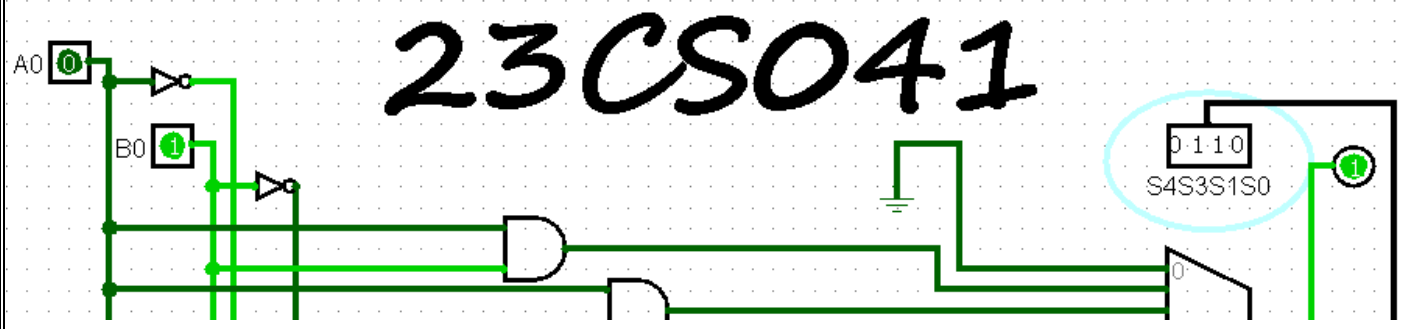


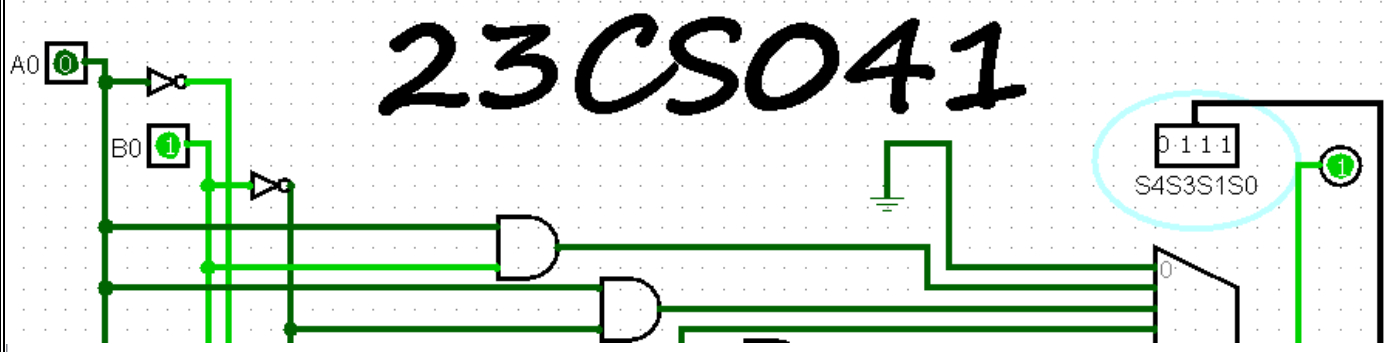


iii. 1) 1-bit 16 logical functions




23CS041
A0
B0
0 0 0 1
S4S3S1S0
23CS041
A0
B0
0 0 1 0
S4S3S1S0
23CS041
A0
B0
0 0 1 1
S4S3S1S0
23CS041
A0
B0
0 1 0 0
S4S3S1S0
23CS041
A0
B0
0 1 0 1
S4S3S1S0


23CS041
A0
B0
0 1 1 0
S4S3S1S0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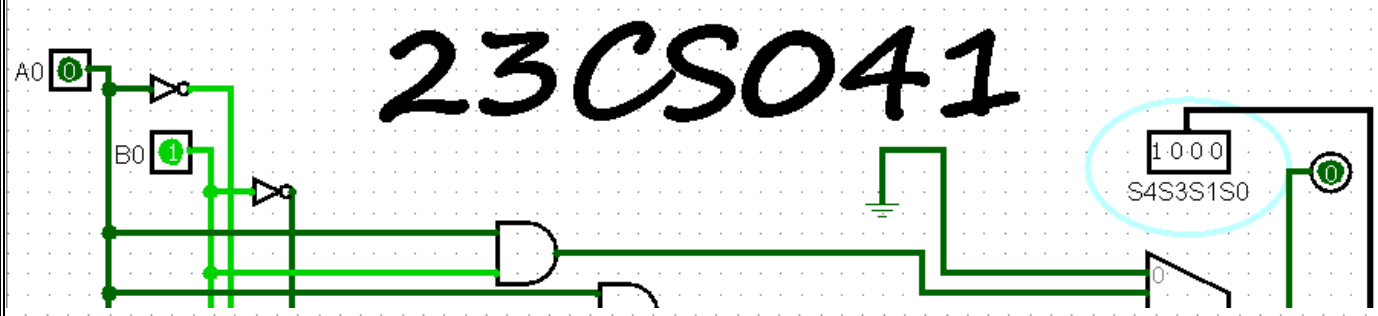
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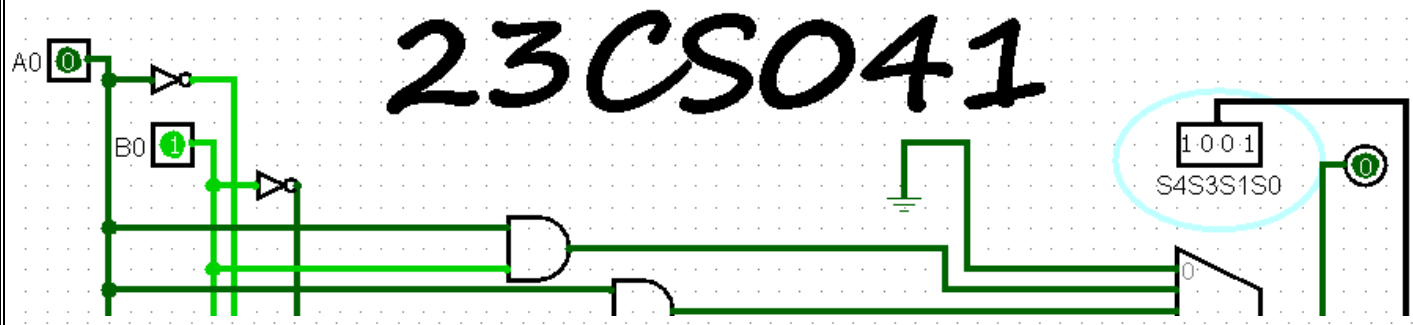
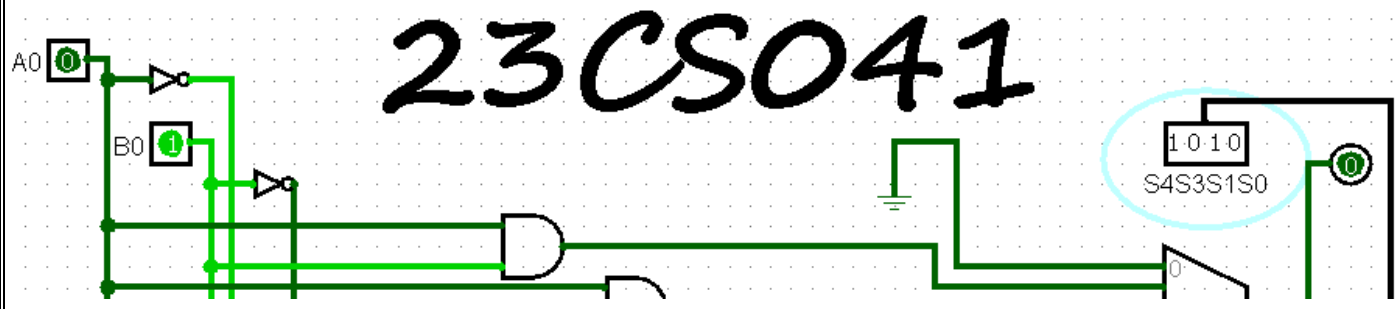
B0
1 0 0 0
S4S3S1S0


23CS041
A0
B0
1 0 0 1
S4S3S1S0


23CS041
A0
B0
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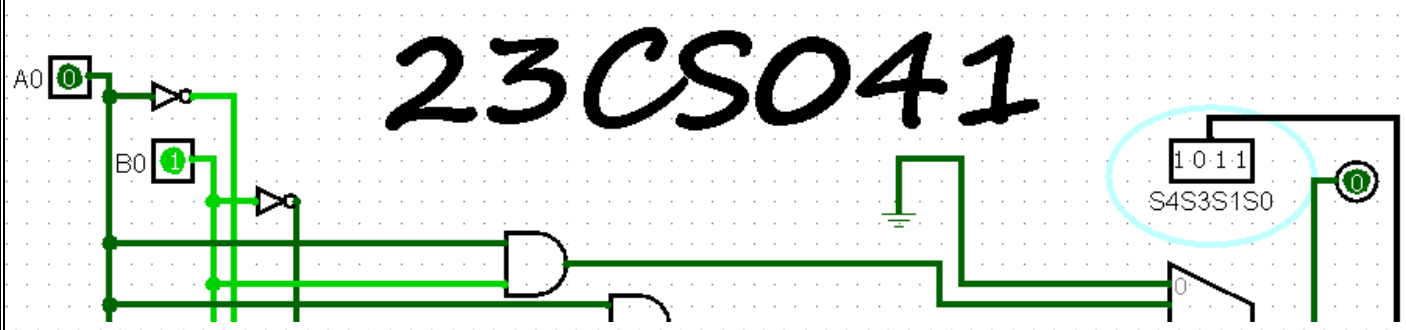
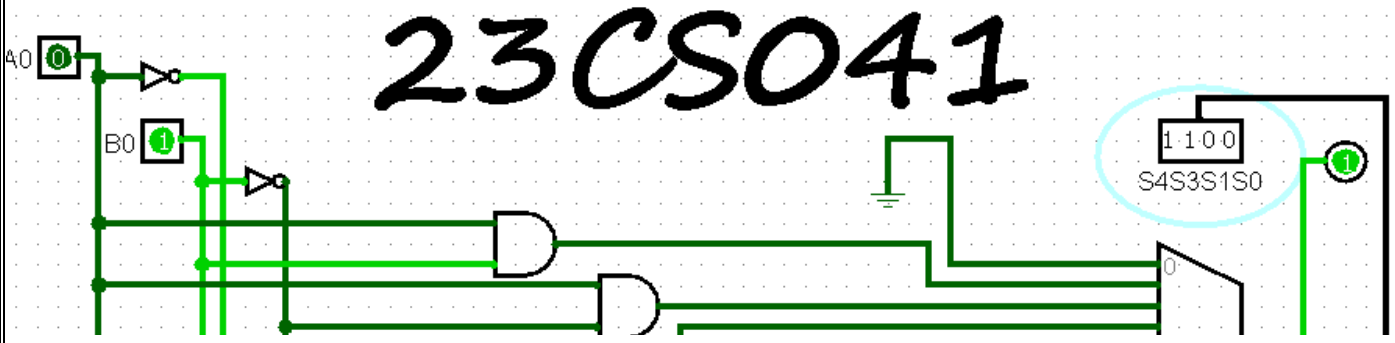
S4S3S1S0


23CS041
A0
B0
1 0 1 1
S4S3S1S0


23CS041
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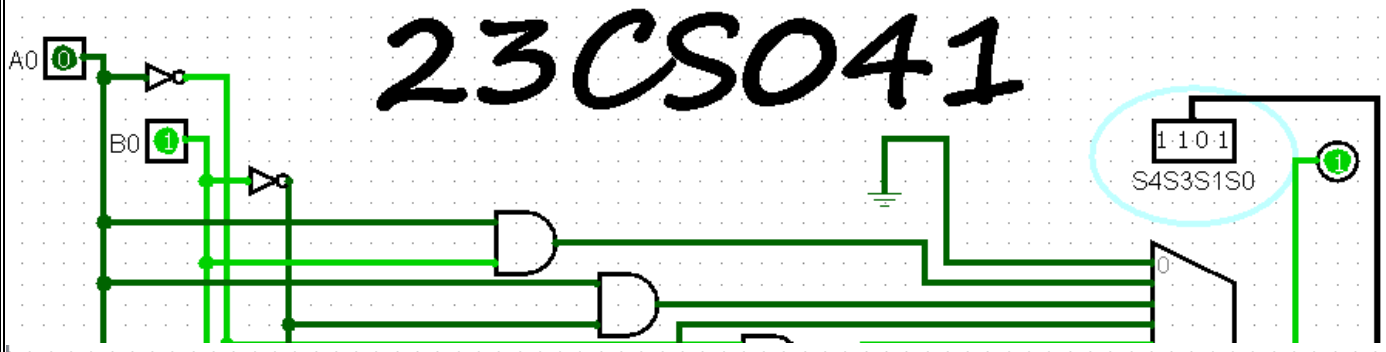
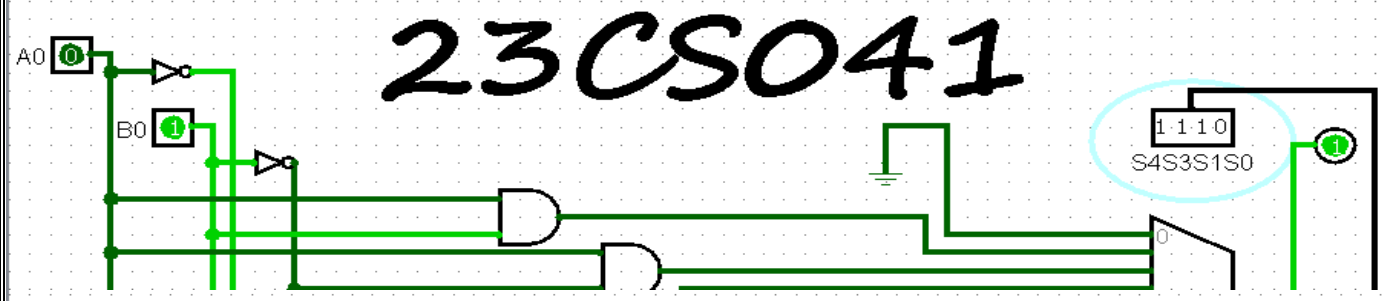
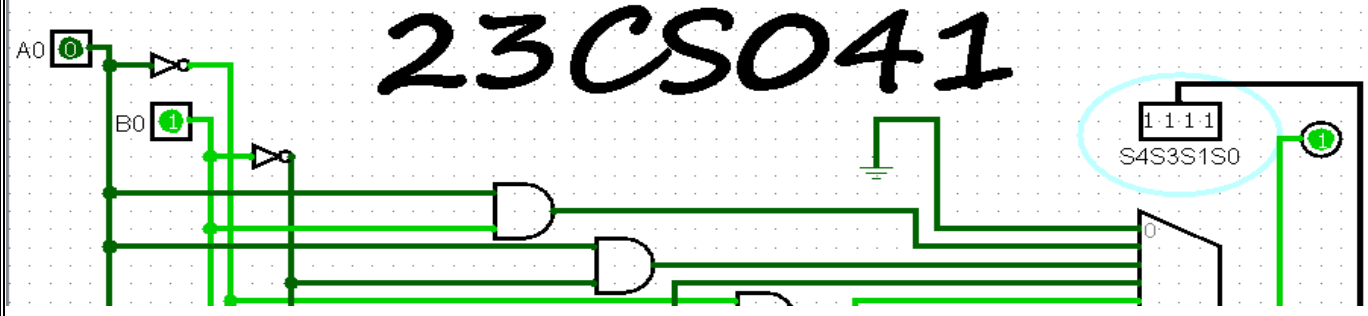
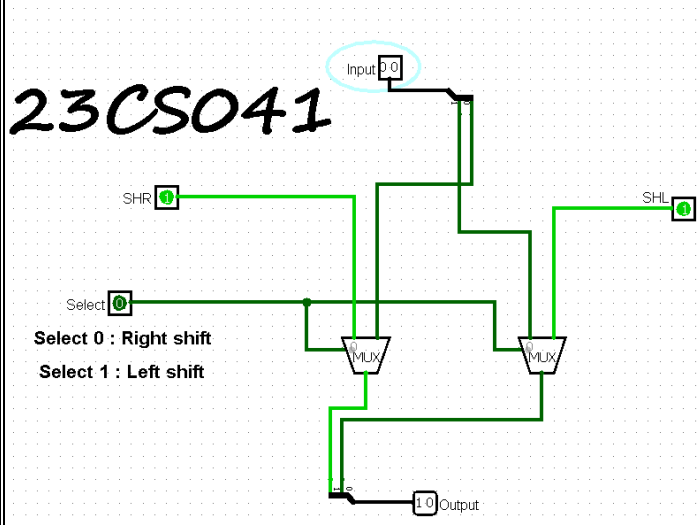
1 1 0 0
S4S3S1S0

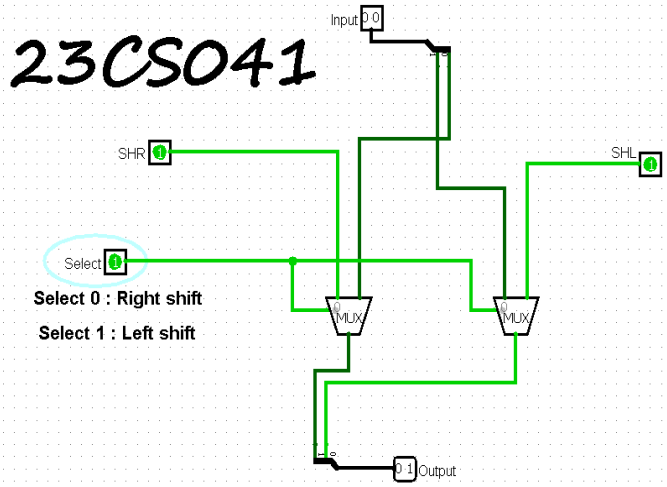

23CS041
A0
B0
1 1 0 1
S4S3S1S0

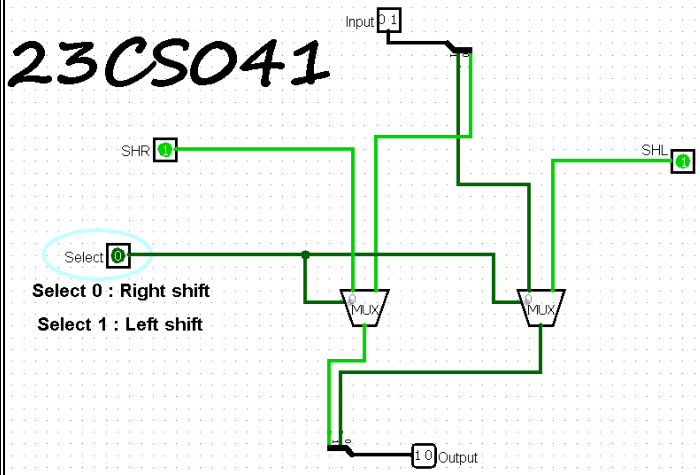

23CS041
A0
B0
1 1 1 0
S4S3S1S0

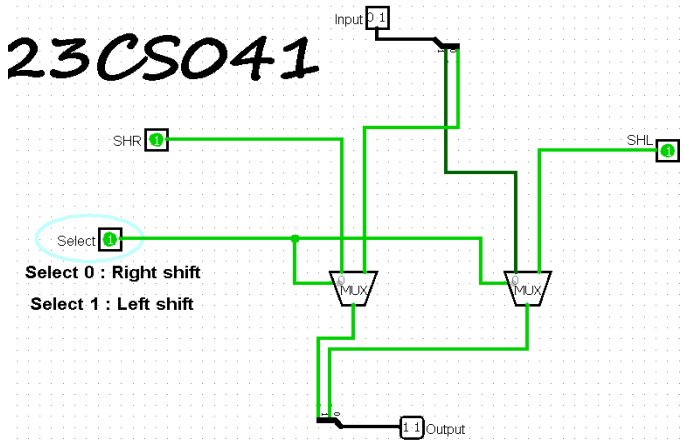

23CS041
A0
B0
1 1 1 1
S4S3S1S0

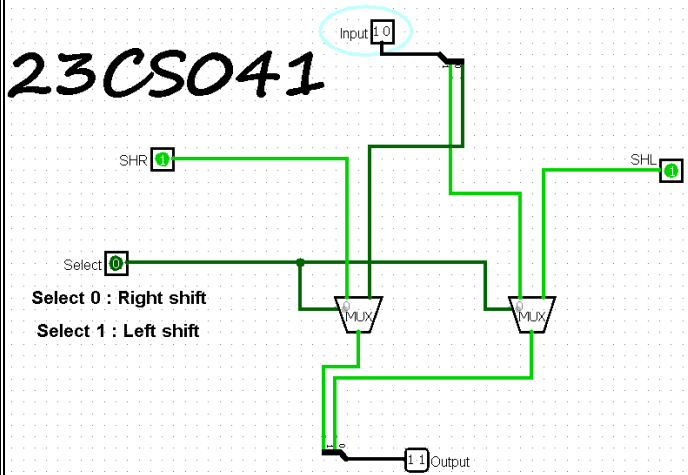
iv. 1) 2-bit bidirectional shifter

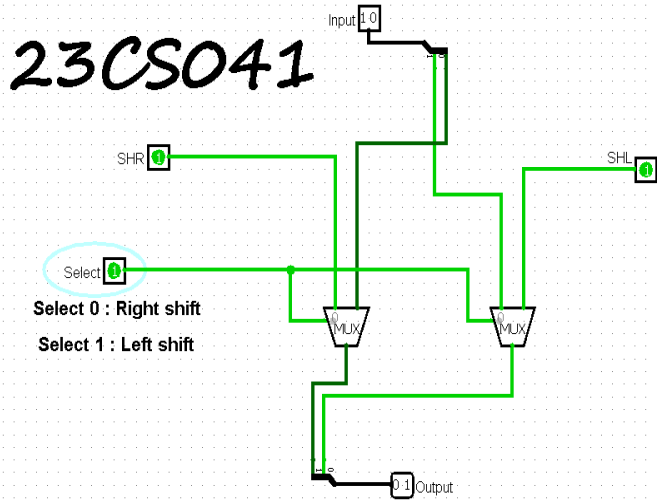


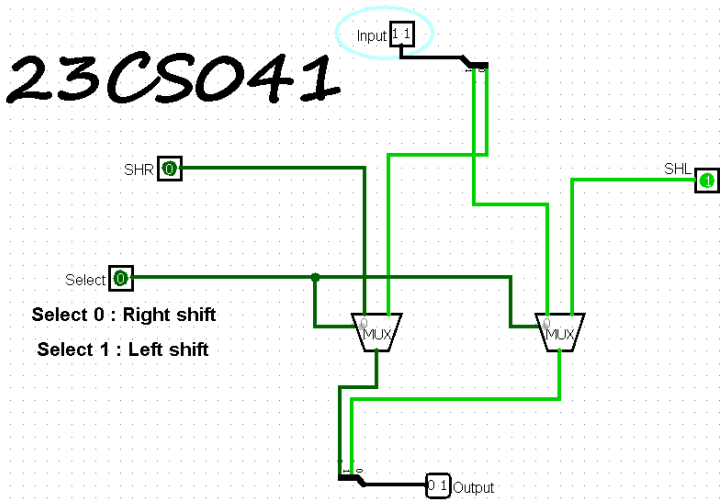


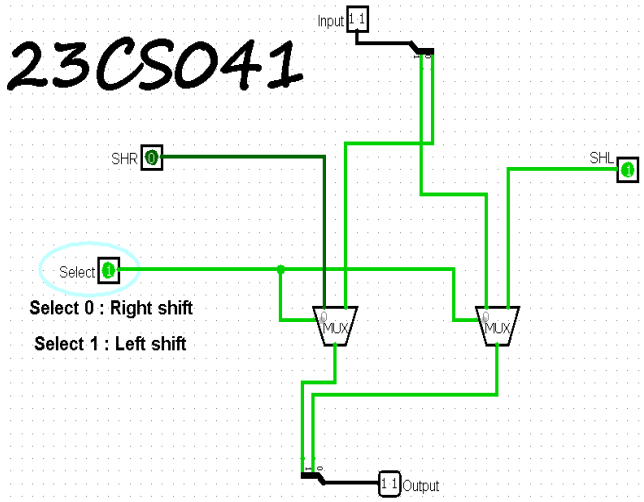




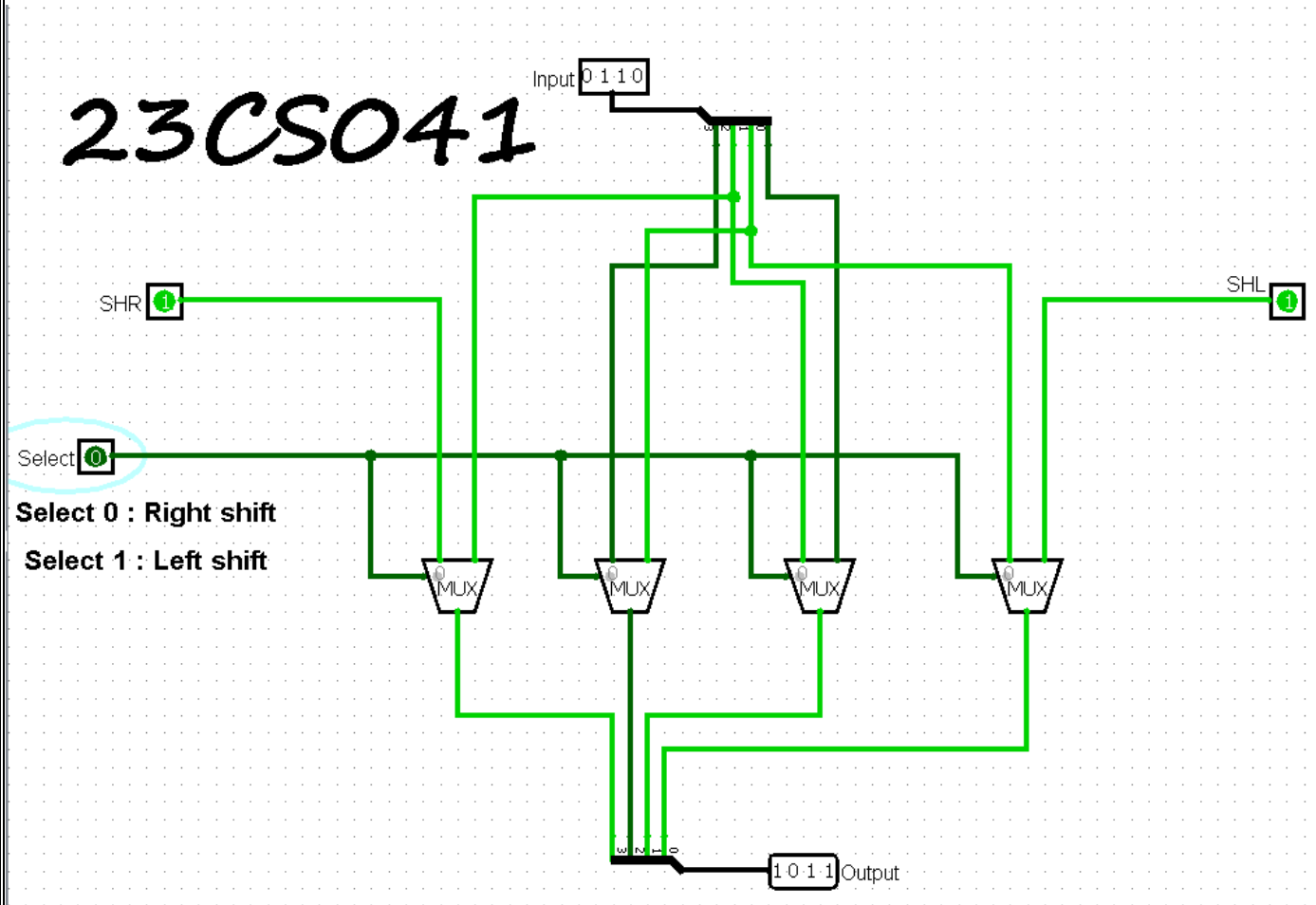


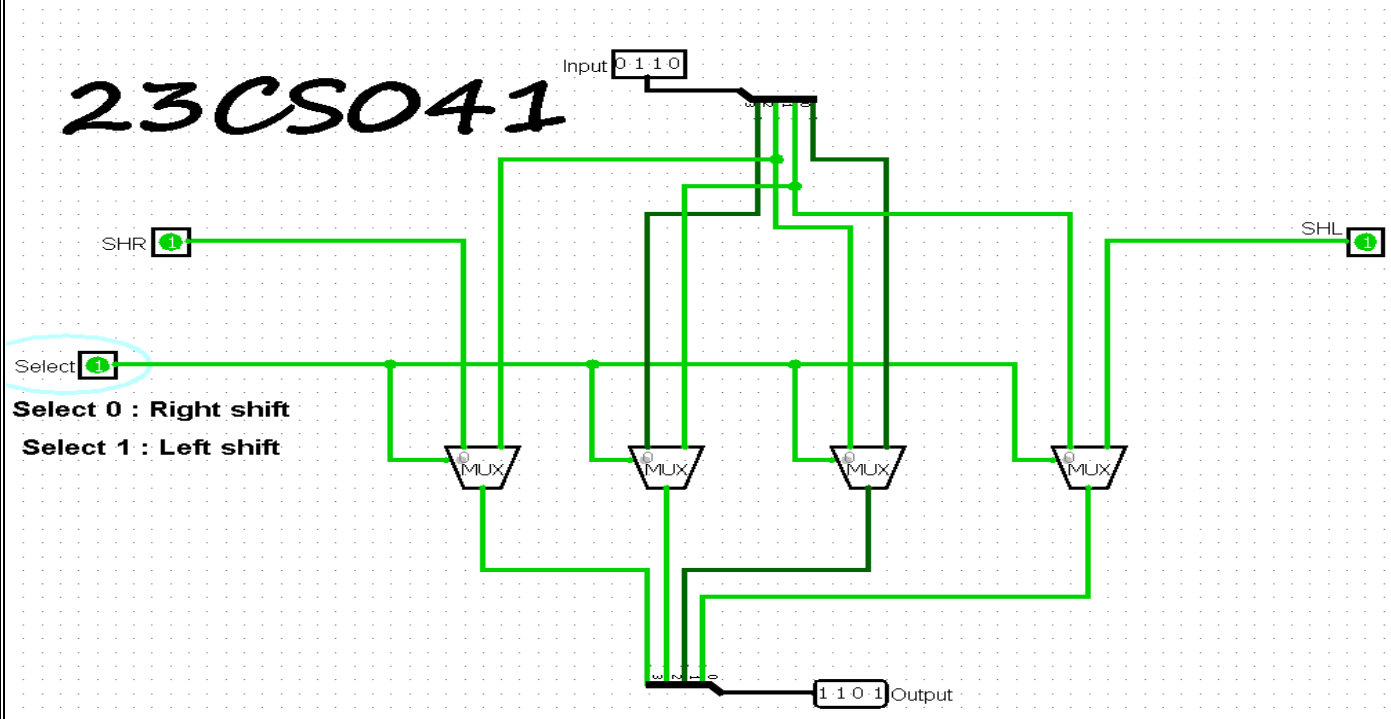




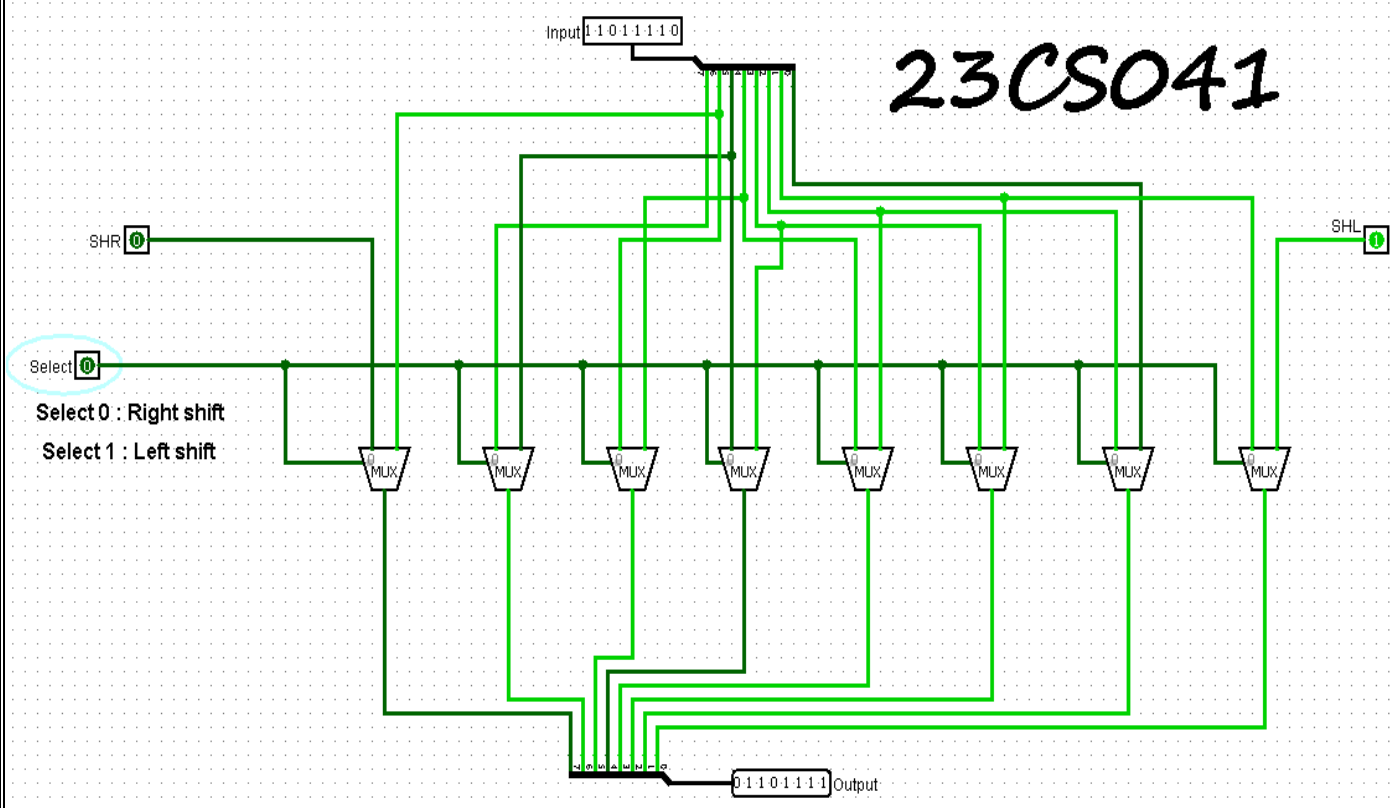


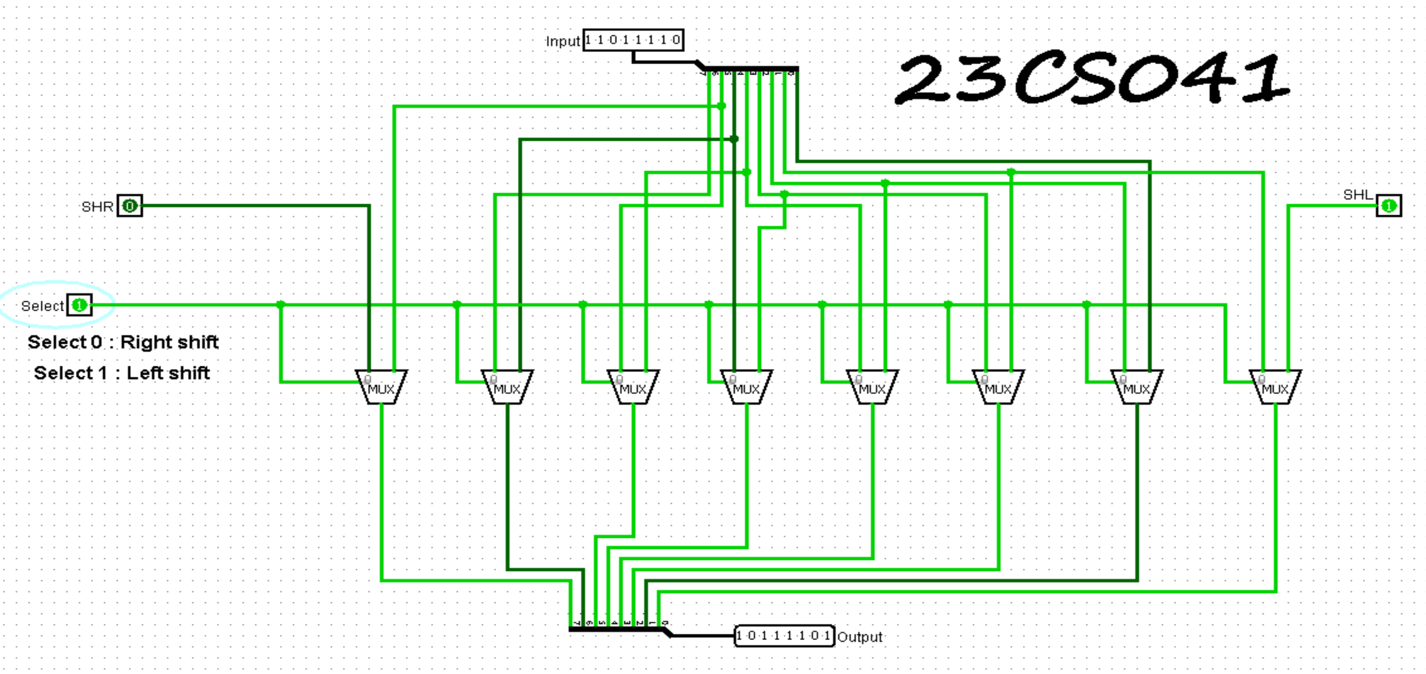
2) 4-bit bidirectional shifter



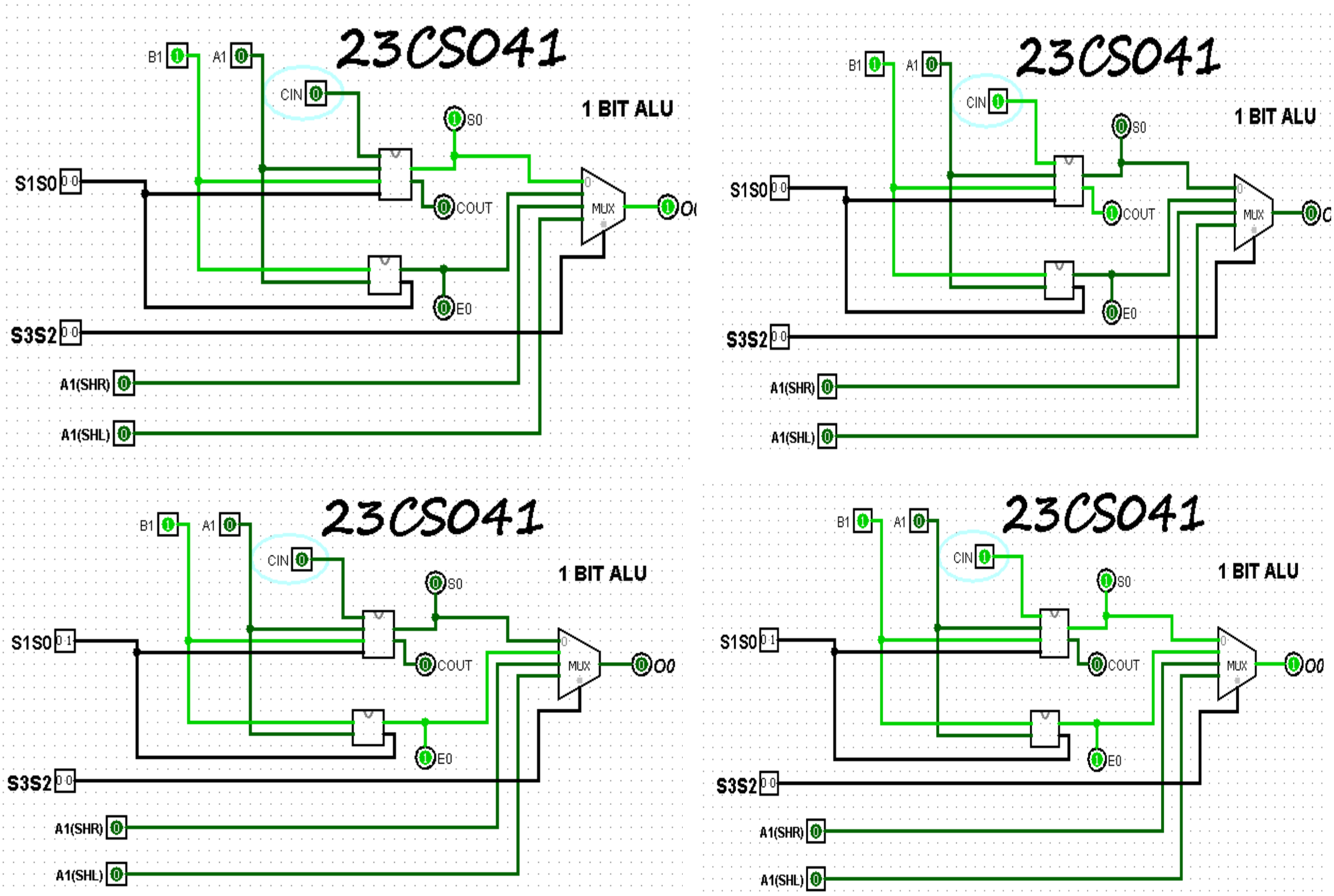


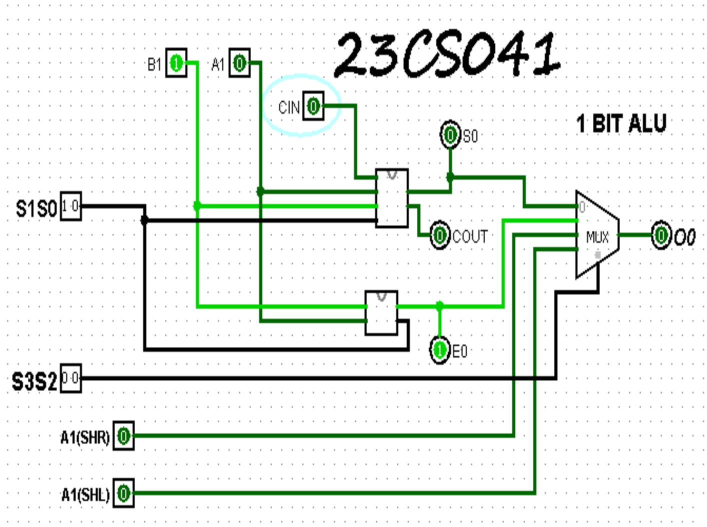
3) 8-bit bidirectional shifter

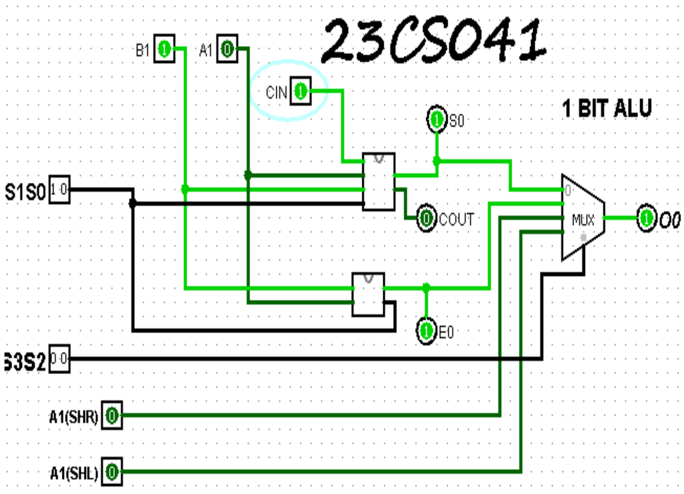


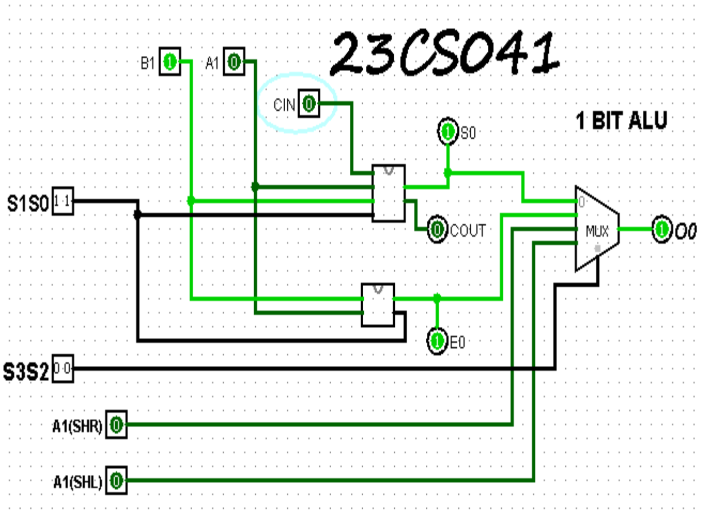

Input 1 1 0 1 1 1 1 0
23CS041
SHR 0
SHL 1
Select 1
Select 0 : Right shift
Select 1 : Left shift
MUX
1 0 1 1 1 1 0 1 Output

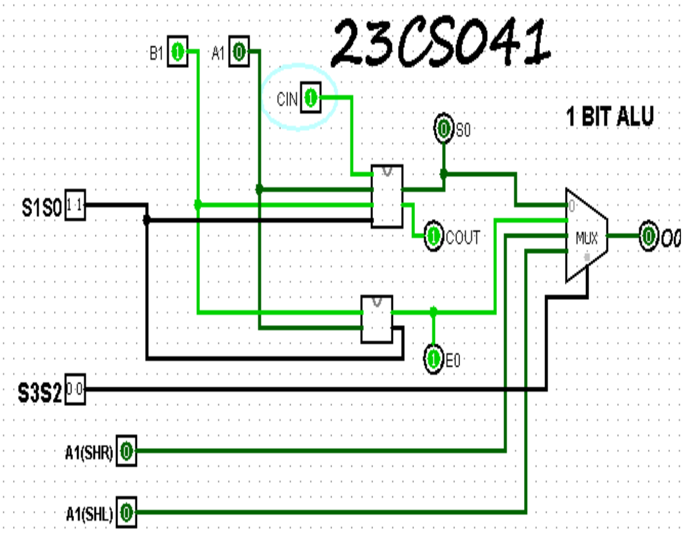
v. 1) 1-bit ALU

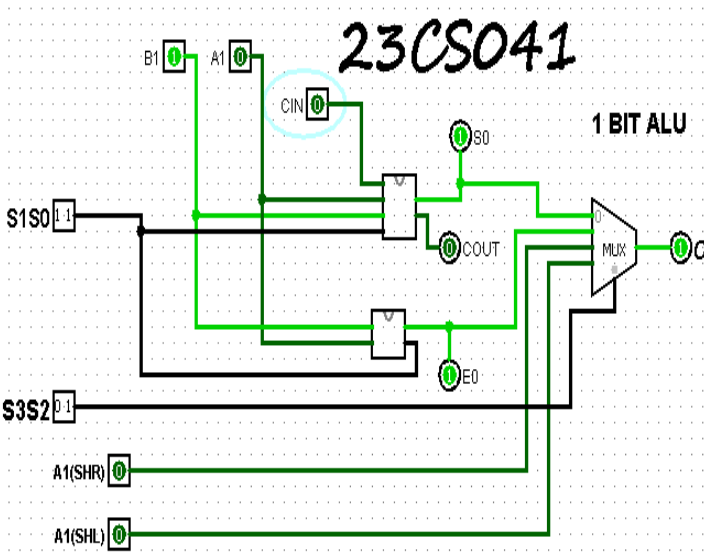

23CS041
1 BIT ALU
B1 1
A1 0
CIN 0
S0
COUT
E0
MUX
S1S0 0 0
S3S2 0 0
A1(SHR) 0
A1(SHL) 0
S1S0 0 1

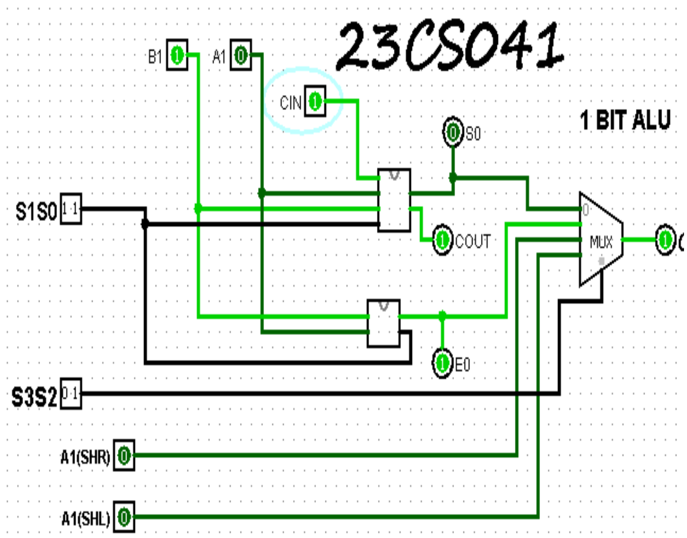

23CS041
1 BIT ALU
B1
A1
CIN
S0
COUT
MUX
O0
E0
S1S0
S3S2
A1(SHR)
A1(SHL)


23CS041
1 BIT ALU
B1
A1
CIN
S0
COUT
MUX
O0
E0
S1S0
S3S2
A1(SHR)
A1(SHL)

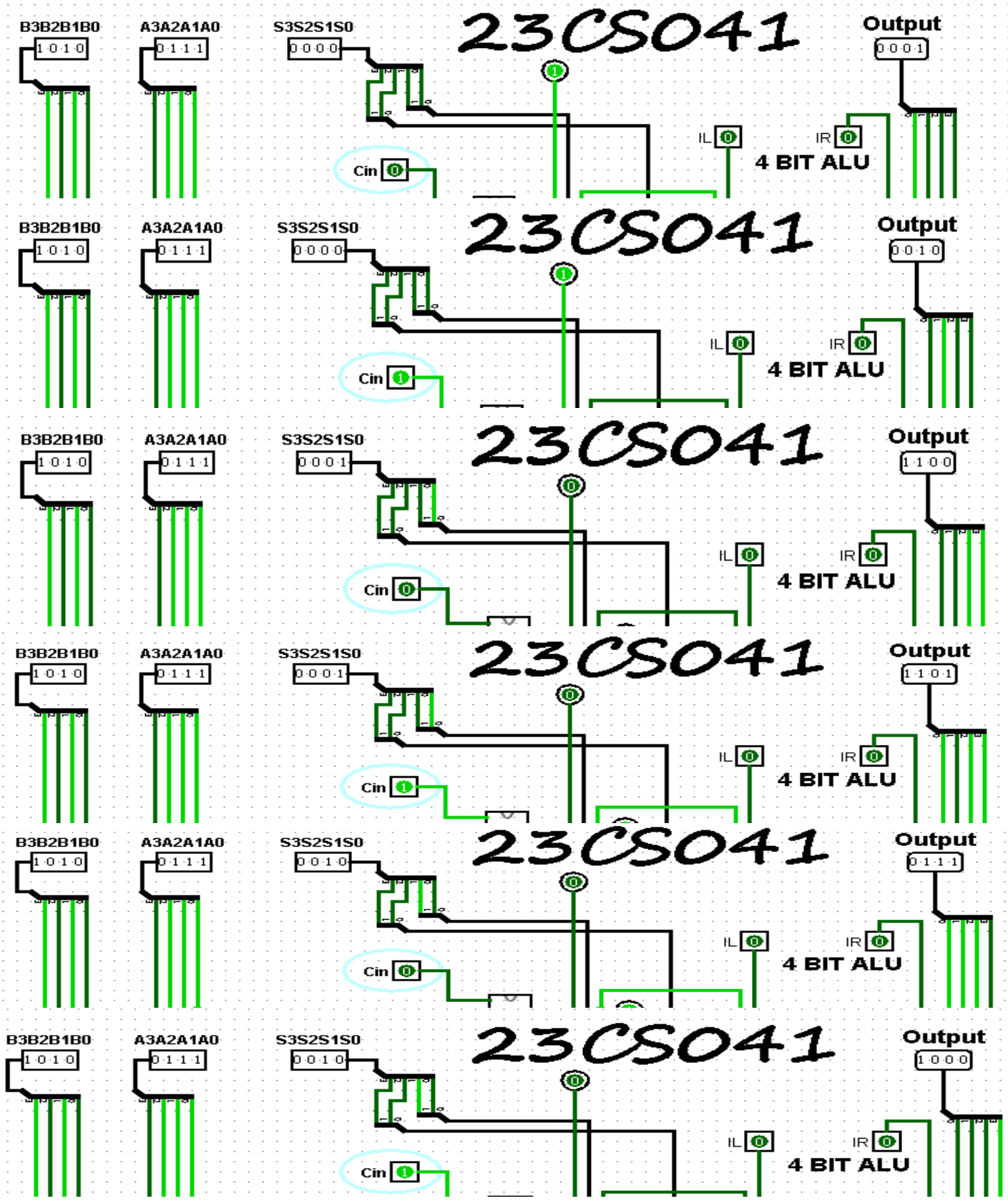

23CS041
1 BIT ALU
B1
A1
CIN
S0
COUT
MUX
O0
E0
S1S0
S3S2
A1(SHR)
A1(SHL)

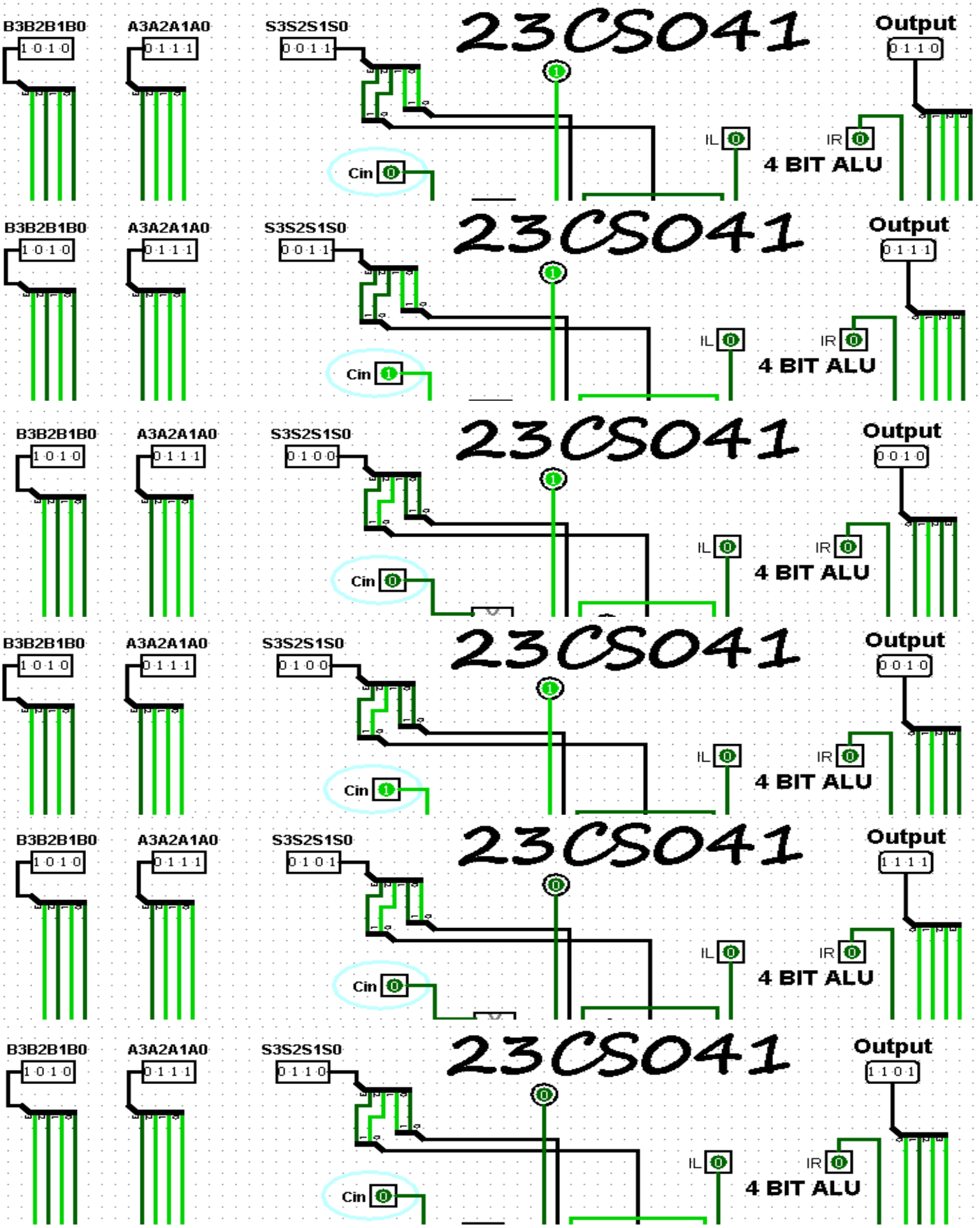

23CS041
1 BIT ALU
B1
A1
CIN
S0
COUT
MUX
O0
E0
S1S0
S3S2
A1(SHR)
A1(SHL)

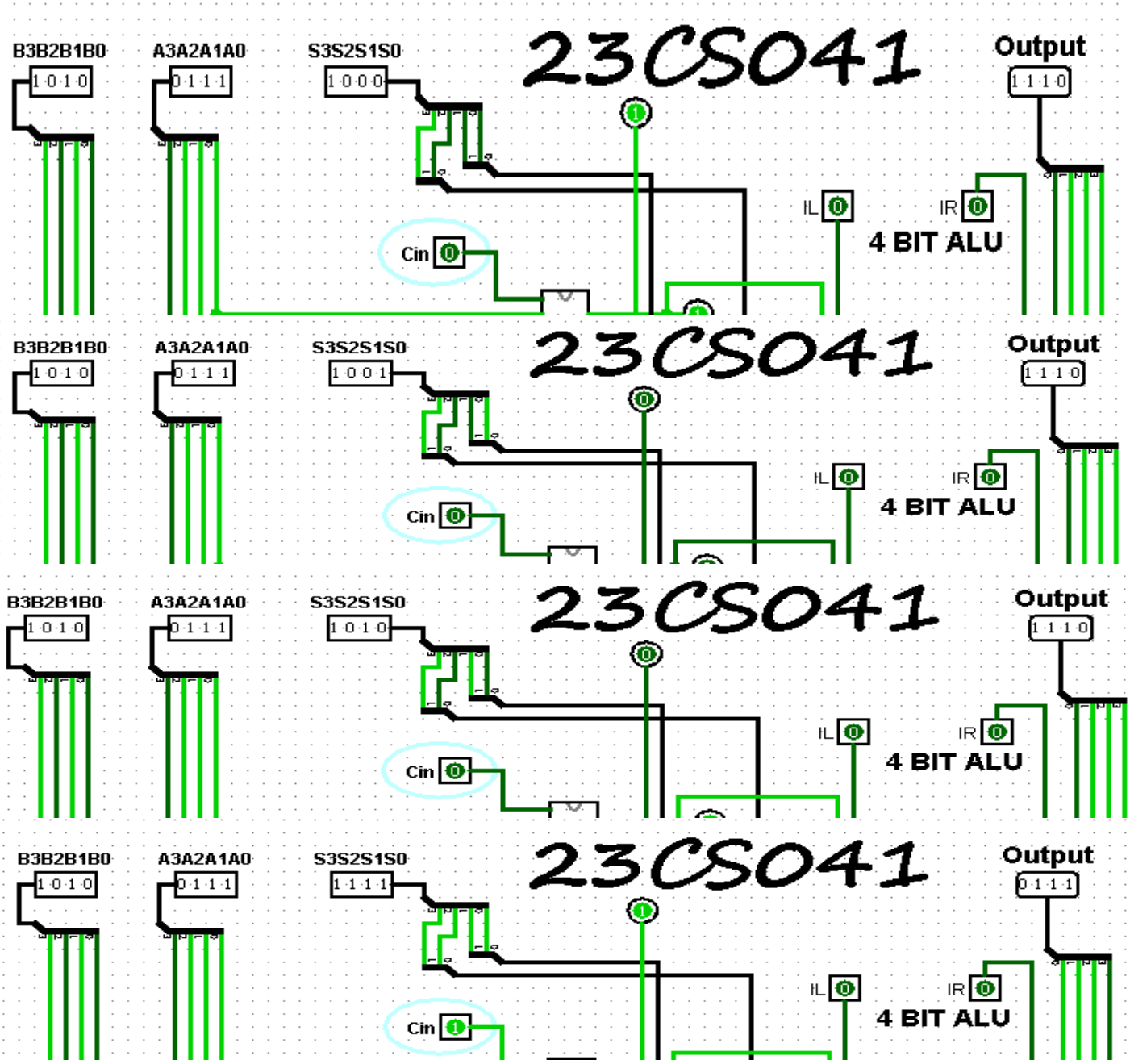

23CS041
1 BIT ALU
B1
A1
CIN
S0
COUT
MUX
E0
S1S0
S3S2
A1(SHR)
A1(SHL)


23CS041
1 BIT ALU
B1
A1
CIN
S0
COUT
MUX
E0
S1S0
S3S2
A1(SHR)
A1(SHL)

2) 4-bit ALU


B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 0 0
23CS041
Output
0 0 0 1
IL 0
IR 0
Cin 0
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 0 0
23CS041
Output
0 0 1 0
IL 0
IR 0
Cin 1
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 0 1
23CS041
Output
1 1 0 0
IL 0
IR 0
Cin 0
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 0 1
23CS041
Output
1 1 0 1
IL 0
IR 0
Cin 1
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 1 0
23CS041
Output
0 1 1 1
IL 0
IR 0
Cin 0
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 1 0
23CS041
Output
1 0 0 0
IL 0
IR 0
Cin 1
4 BIT ALU


B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 1 1
23CS041
Output
0 1 1 0
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 0 1 1
23CS041
Output
0 1 1 1
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 1 0 0
23CS041
Output
0 0 1 0
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 1 0 0
23CS041
Output
0 0 1 0
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 1 0 1
23CS041
Output
1 1 1 1
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
0 1 1 0
23CS041
Output
1 1 0 1
IL
IR
Cin
4 BIT ALU


B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
1 0 0 0
23CS041
Output
1 1 1 0
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
1 0 0 1
23CS041
Output
1 1 1 0
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
1 0 1 0
23CS041
Output
1 1 1 0
IL
IR
Cin
4 BIT ALU
B3B2B1B0
1 0 1 0
A3A2A1A0
0 1 1 1
S3S2S1S0
1 1 1 1
23CS041
Output
0 1 1 1
IL
IR
Cin
4 BIT ALU

CONCLUSION: