Date:

# EXPERIMENT NO. 5

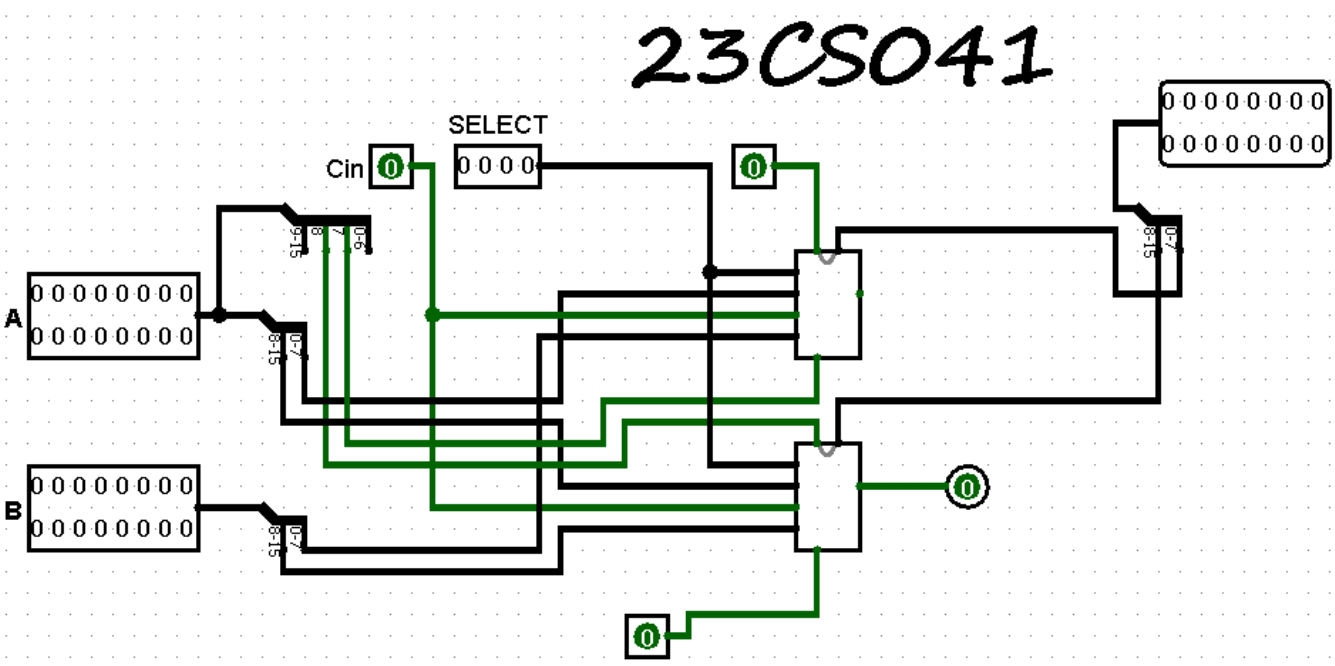
**AIM: Implement a common bus system with ALU, 8 registers and 1 memory unit with necessary control signals.**

**OBJECTIVES:**

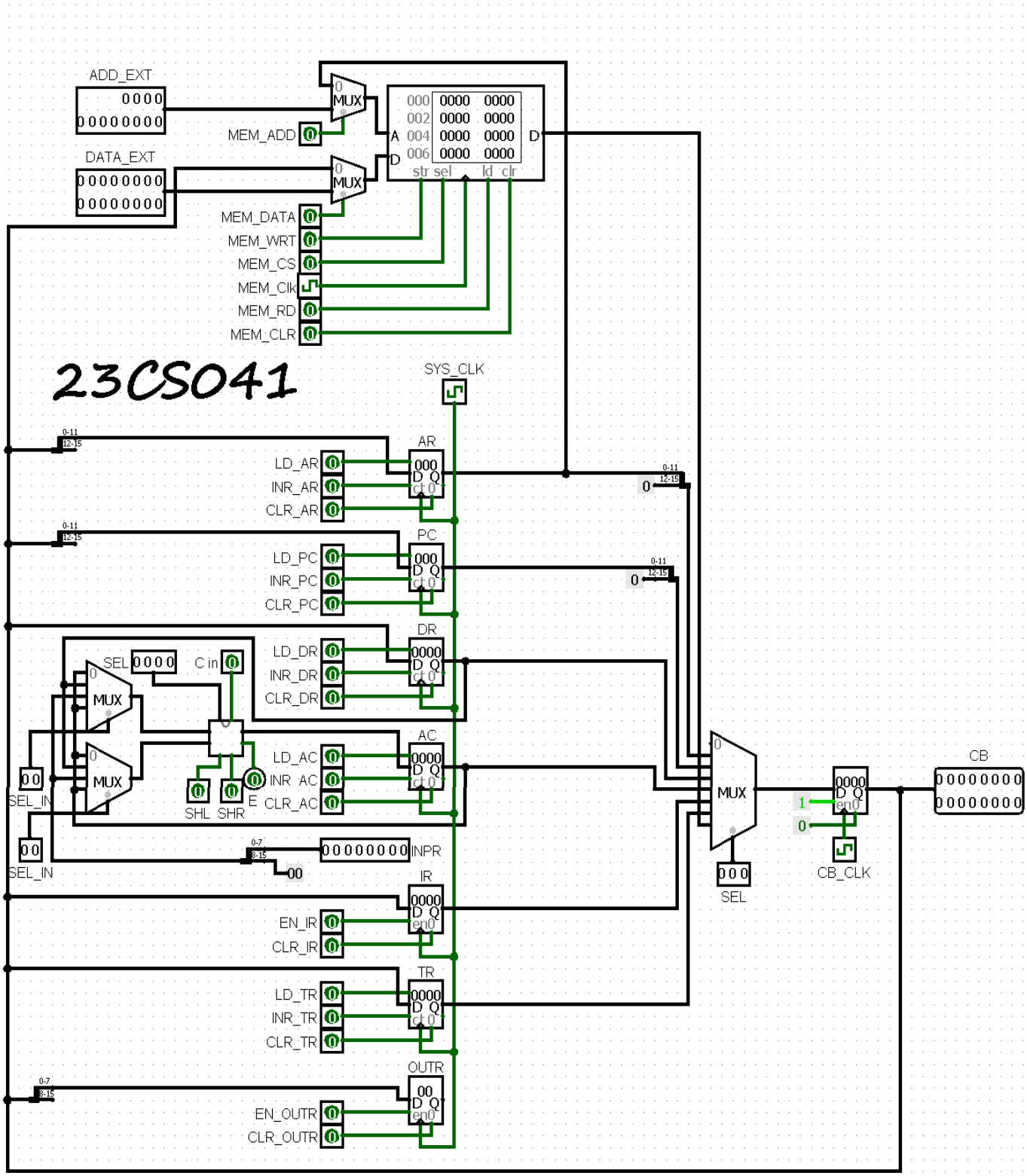
**i. Implement 16-bit ALU that is suitable for common bus system**
**ii. Implement 16-bit common bus system with ALU, 8 registers and 1 memory unit**

**CIRCUITS:**

**i.**

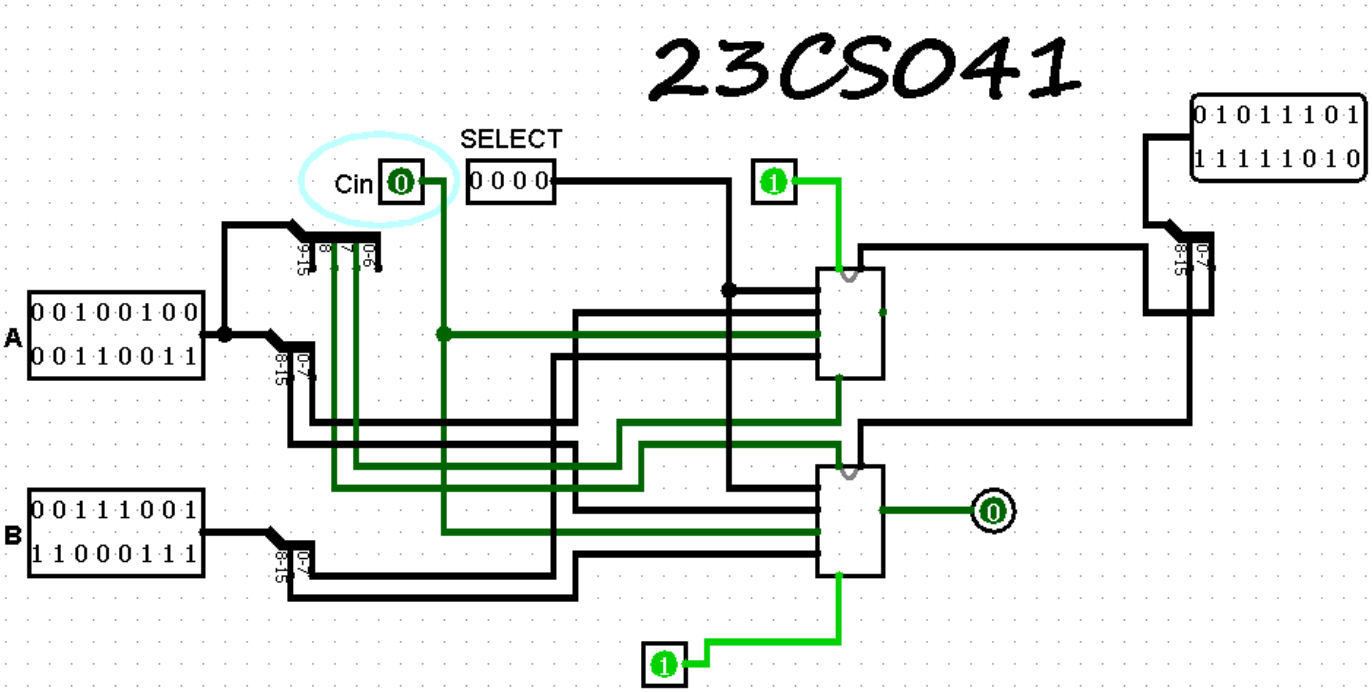


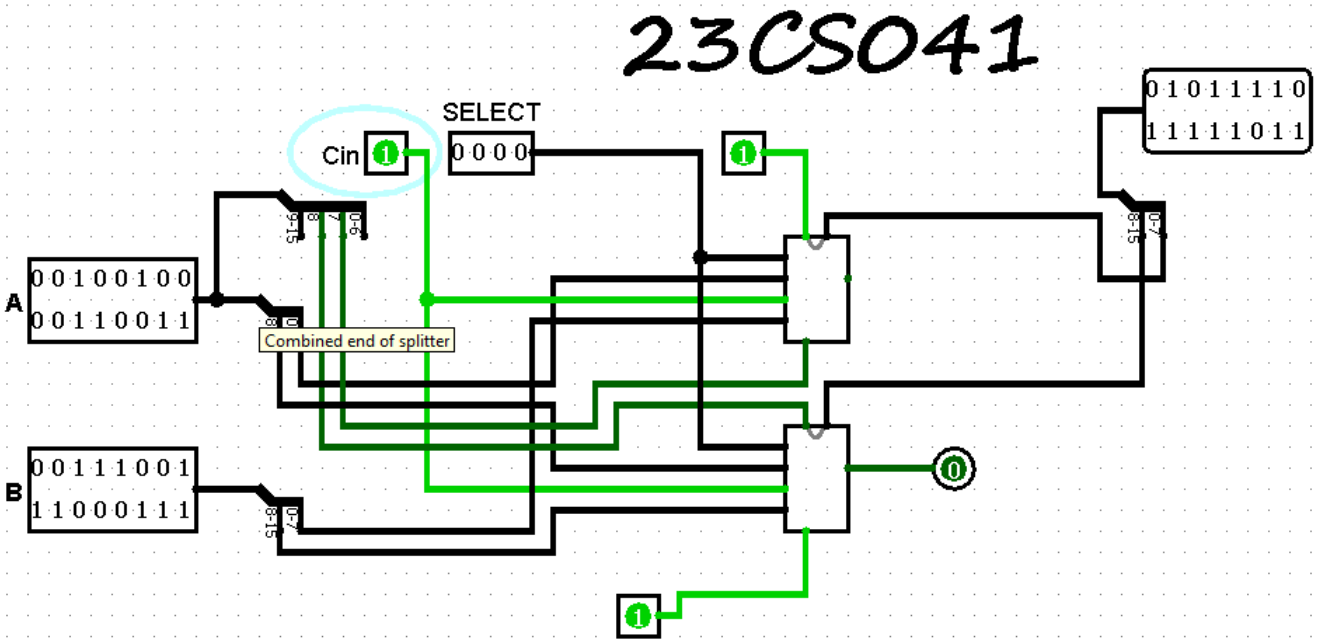
**ii.**

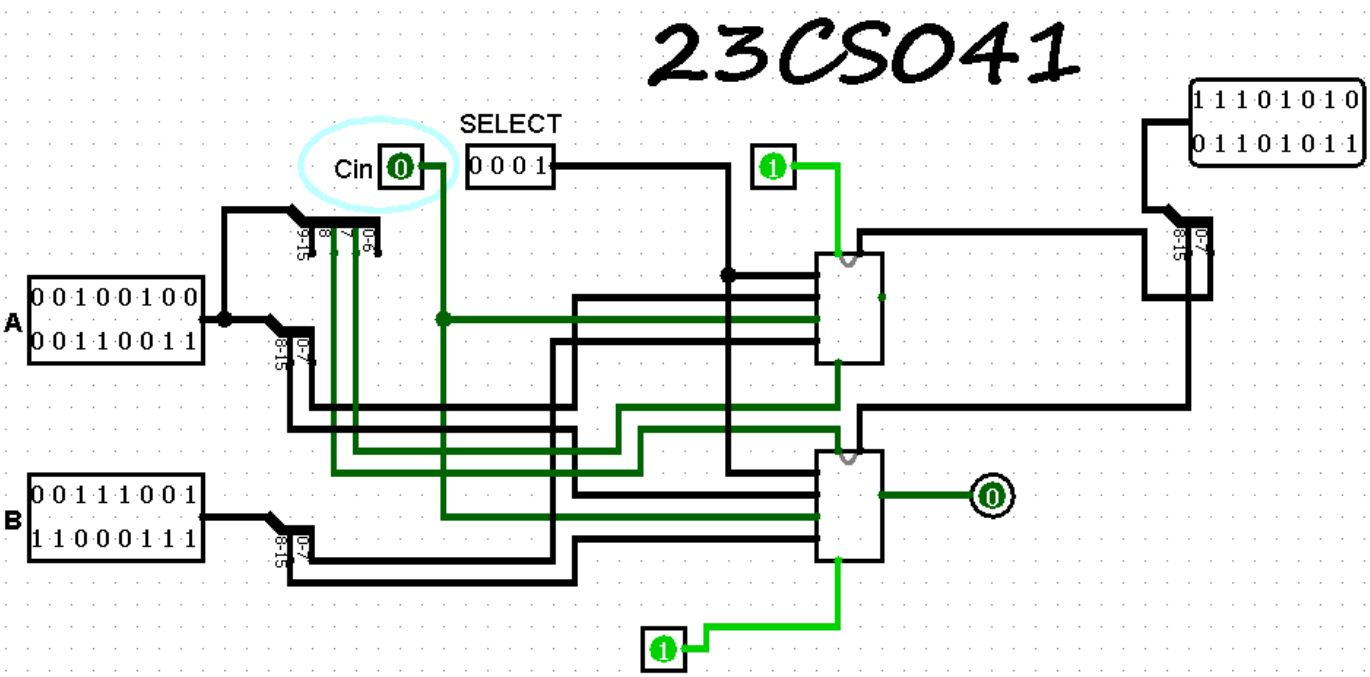

ADD_EXT
MEM_ADD
DATA_EXT
MEM_DATA
MEM_WRT
MEM_CS
MEM_Clk
MEM_RD
MEM_CLR
MUX
000 0000 0000
002 0000 0000
004 0000 0000
006 0000 0000
A
D
str sel ld clr
23CS041
SYS_CLK
AR
LD_AR
INR_AR
CLR_AR
PC
LD_PC
INR_PC
CLR_PC
DR
LD_DR
INR_DR
CLR_DR
AC
LD_AC
INR_AC
CLR_AC
SEL
C in
SHL
SHR
E
SEL_IN
INPR
IR
EN_IR
CLR_IR
TR
LD_TR
INR_TR
CLR_TR
OUTR
EN_OUTR
CLR_OUTR
CB
CB_CLK

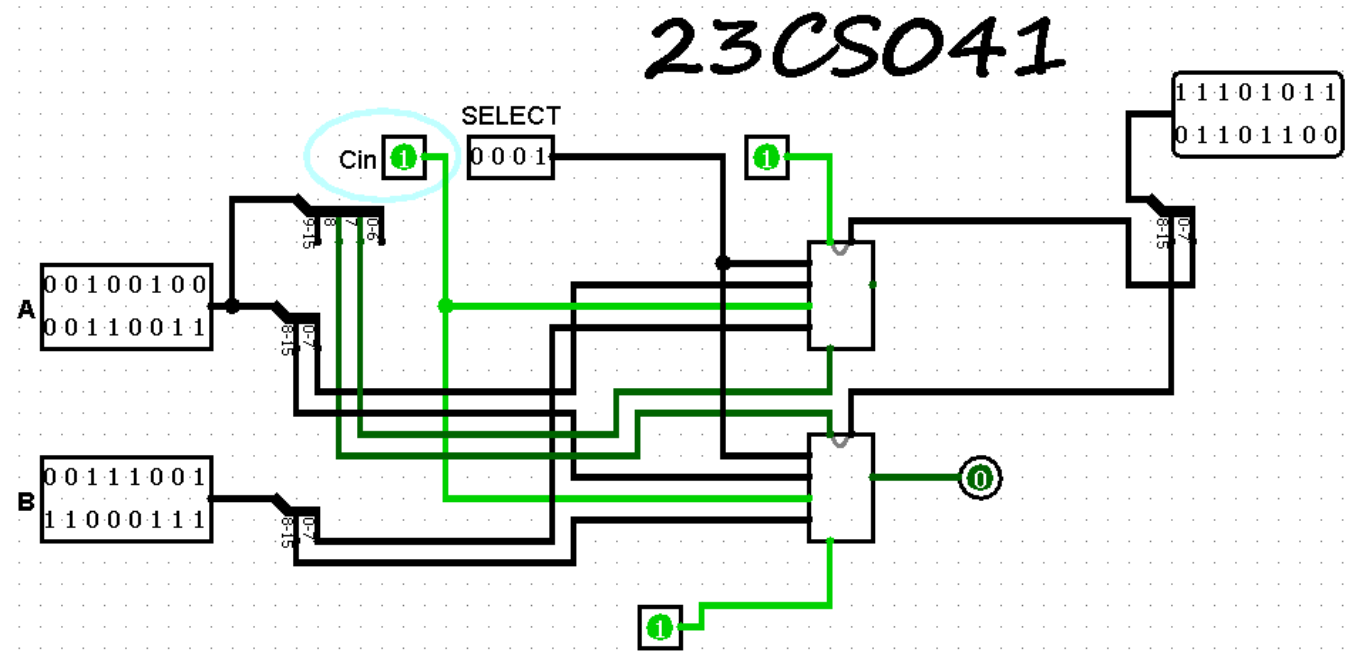
**OUTPUTS:**

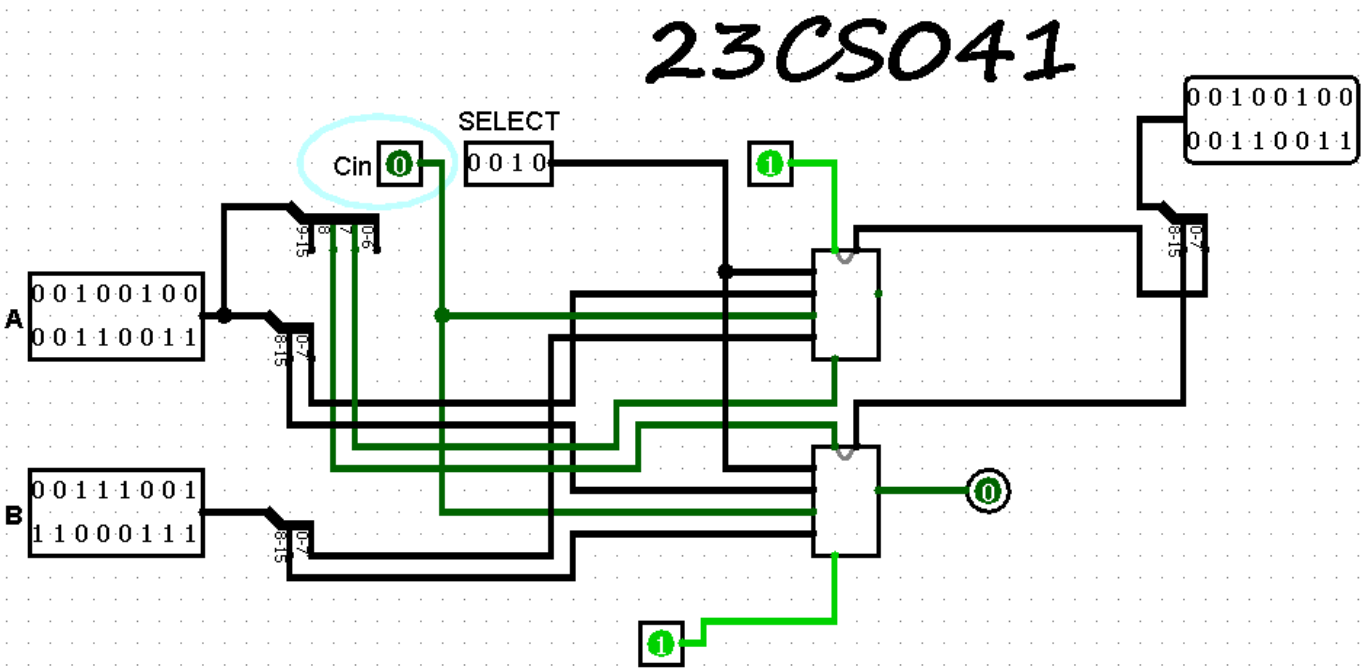
**i.**

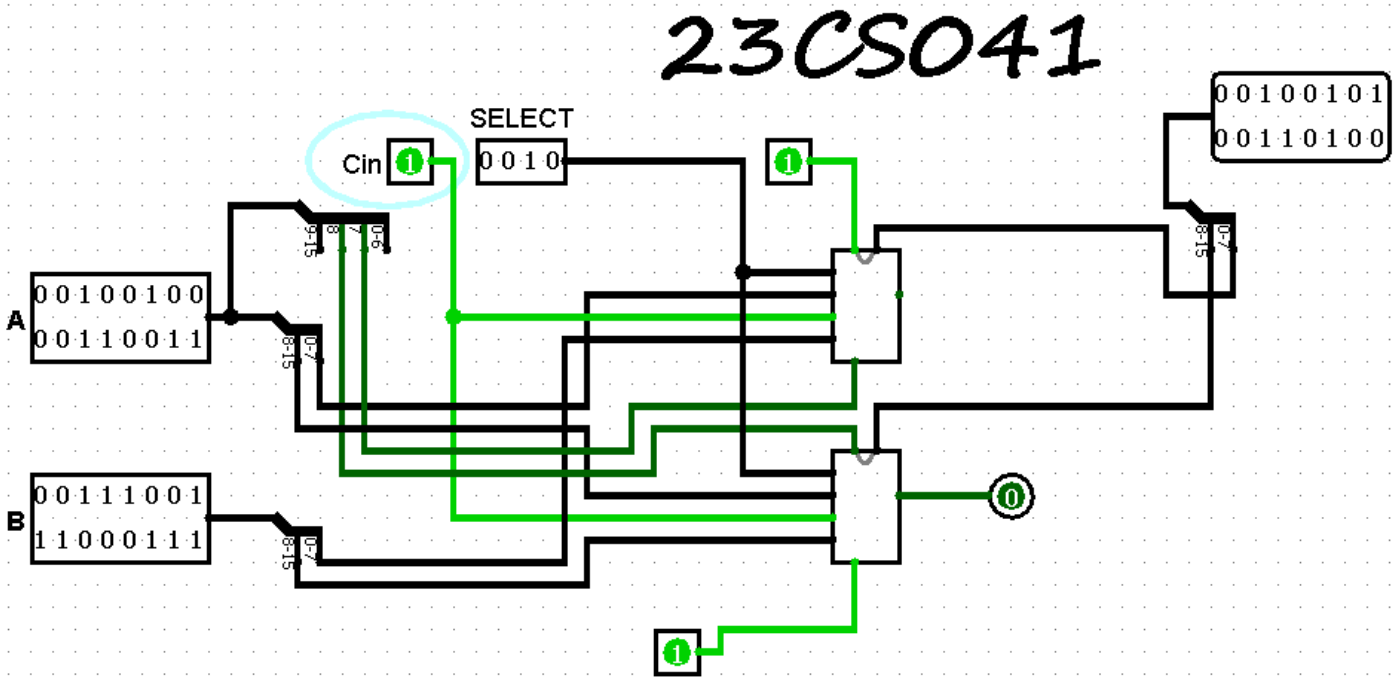

23CS041
SELECT
Cin
0 0 0 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
0 1 0 1 1 1 0 1
1 1 1 1 1 0 1 0

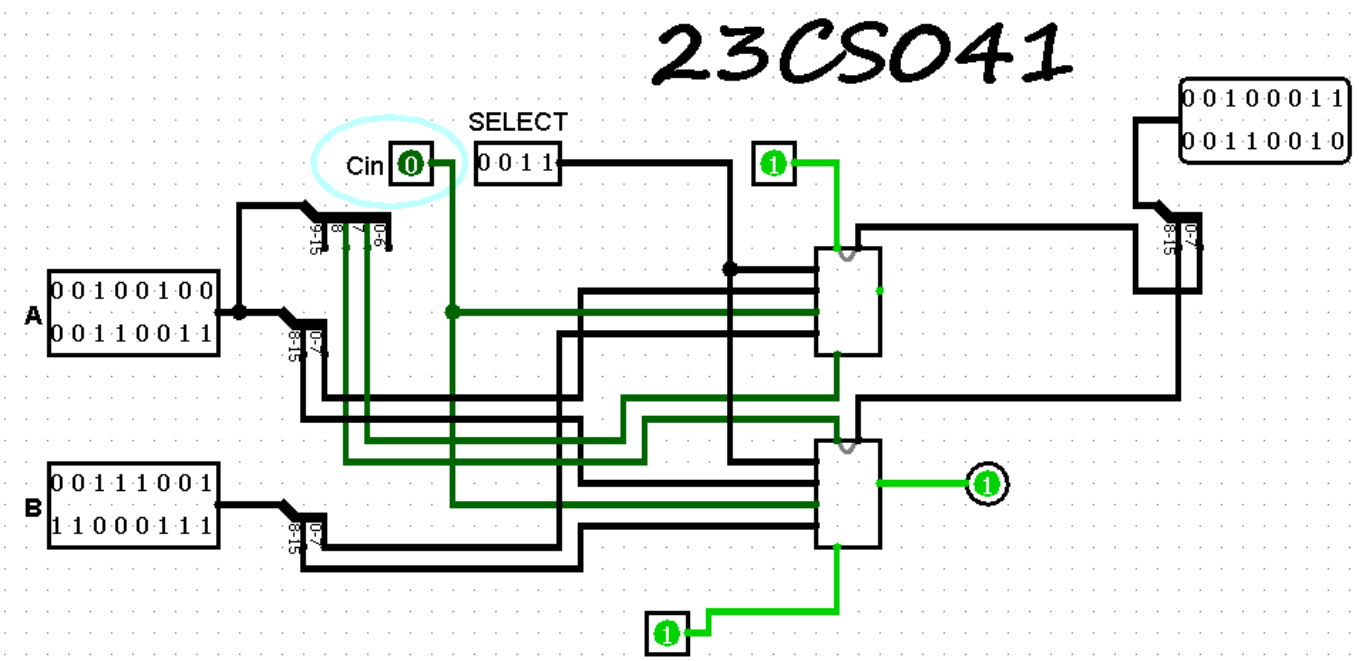

23CS041
SELECT
Cin
0 0 0 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
Combined end of splitter
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
0 1 0 1 1 1 1 0
1 1 1 1 1 0 1 1

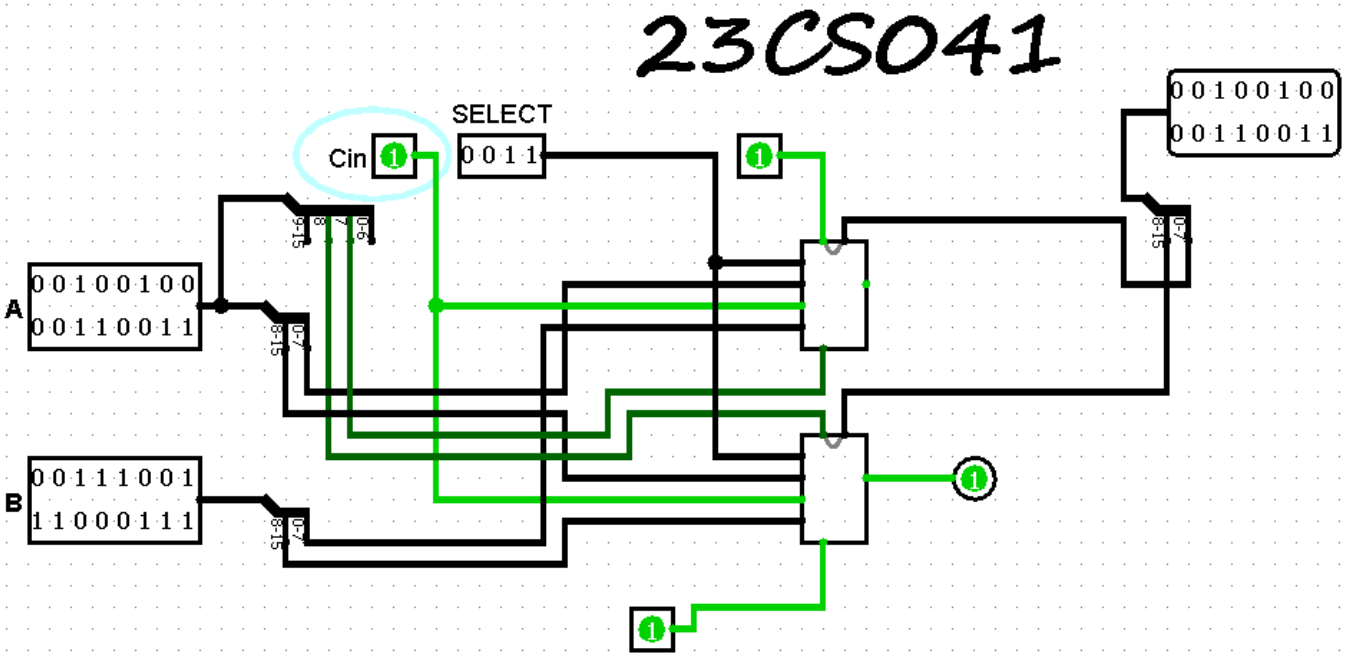

23CS041
SELECT
Cin
0 0 0 1
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
1 1 1 0 1 0 1 0
0 1 1 0 1 0 1 1

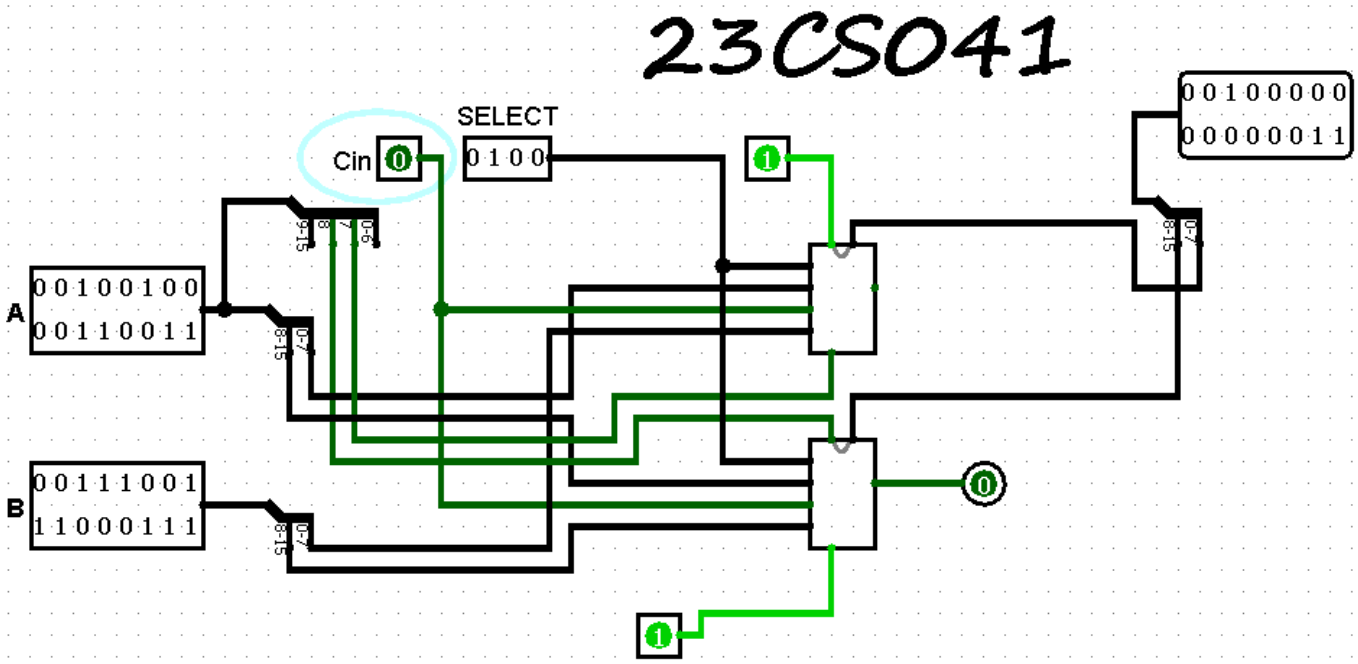

23CS041
SELECT
Cin
0 0 0 1
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
1 1 1 0 1 0 1 1
0 1 1 0 1 1 0 0

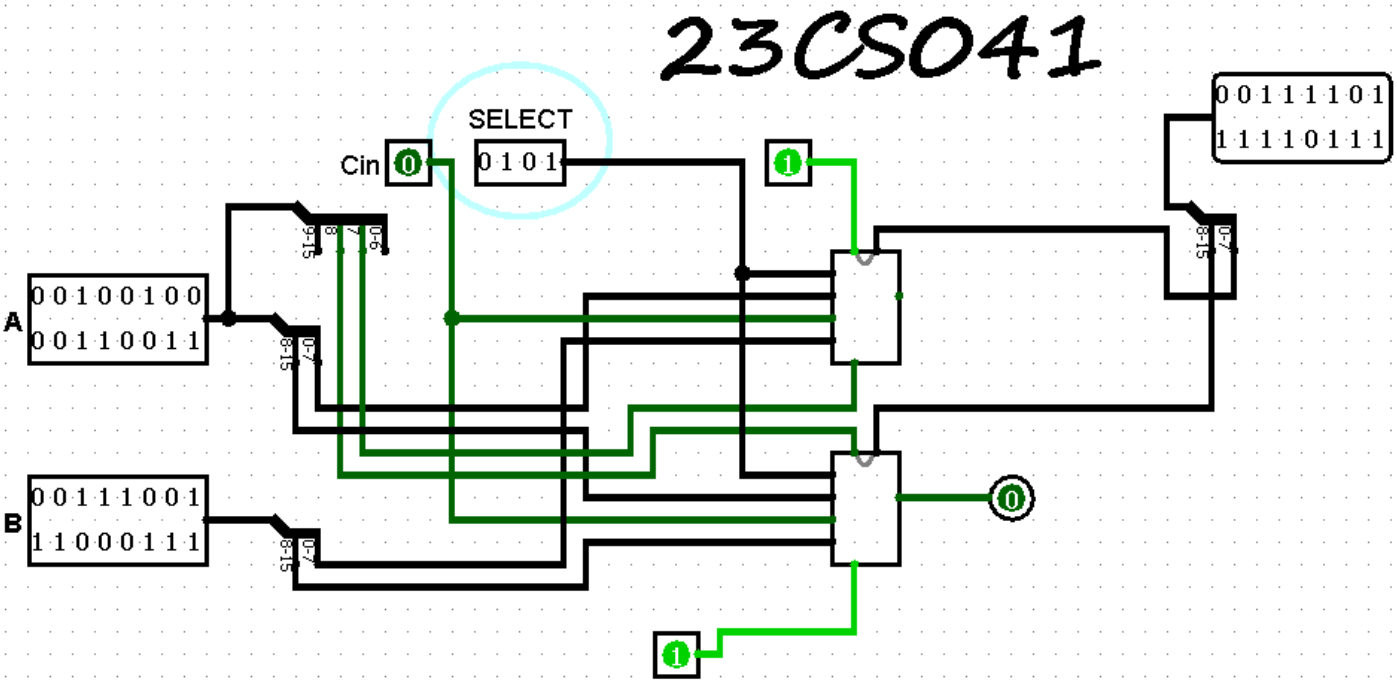

23CS041
SELECT
Cin
0 0 1 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1

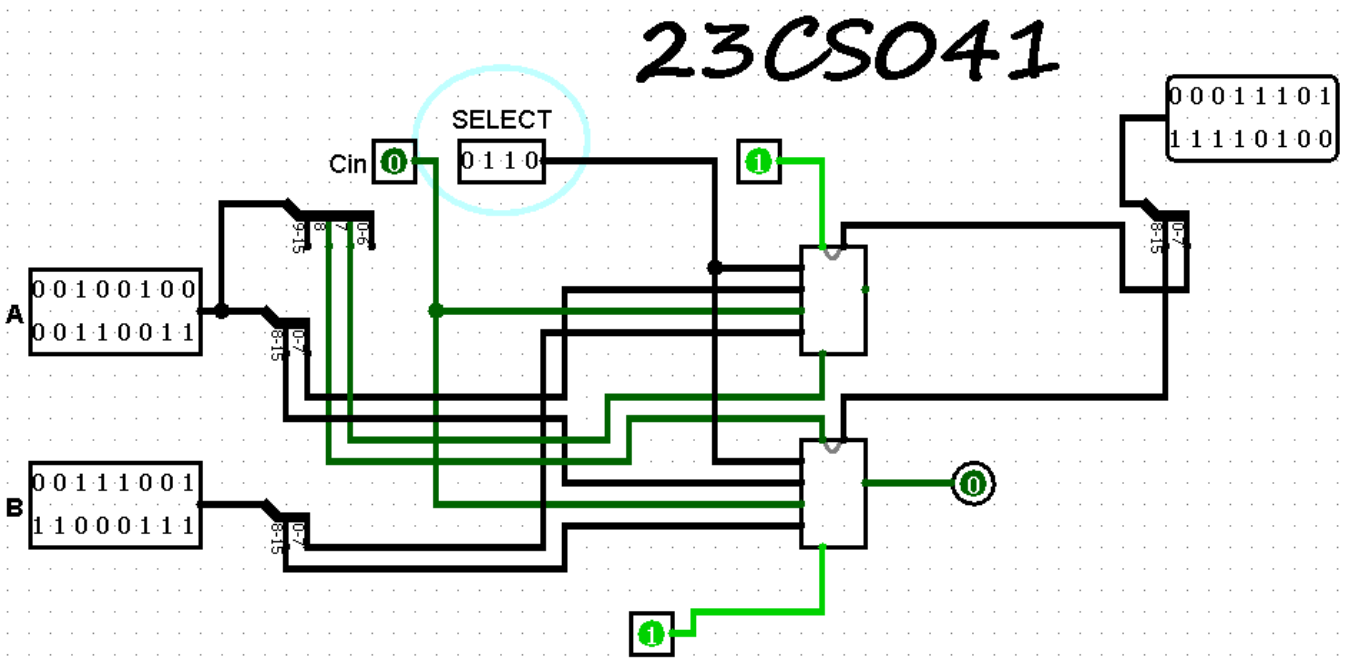

23CS041
SELECT
Cin
0 0 1 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
0 0 1 0 0 1 0 1
0 0 1 1 0 1 0 0

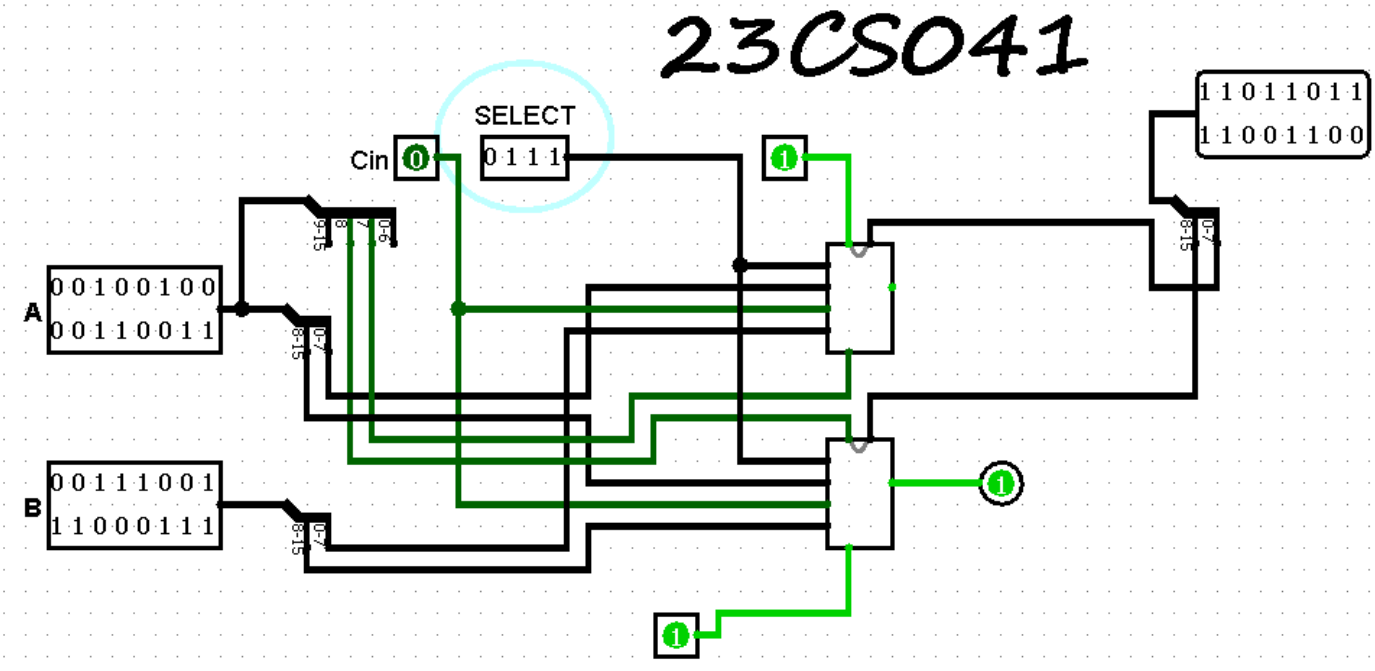

23CS041
SELECT
Cin
0 0 1 1
0 0 1 0 0 0 1 1
0 0 1 1 0 0 1 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1


23CS041
SELECT
Cin
0 0 1 1
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1

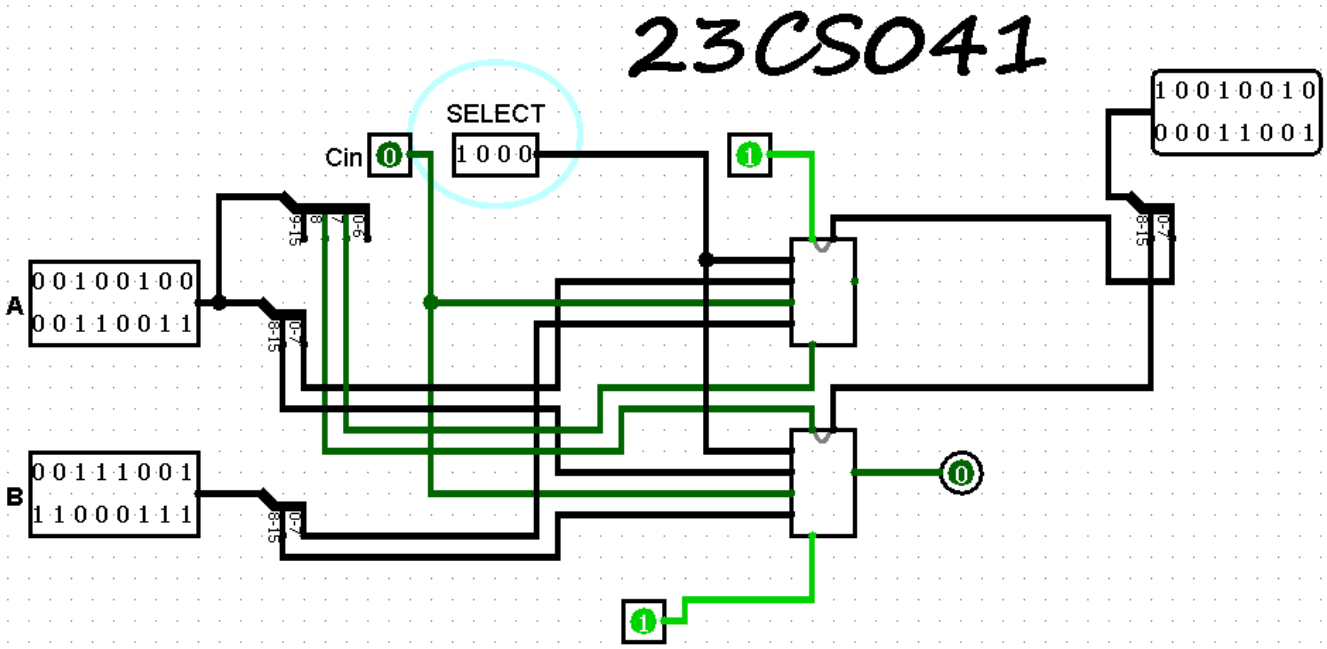

23CS041
SELECT
Cin
0 1 0 0
0 0 1 0 0 0 0 0
0 0 0 0 0 0 1 1
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1

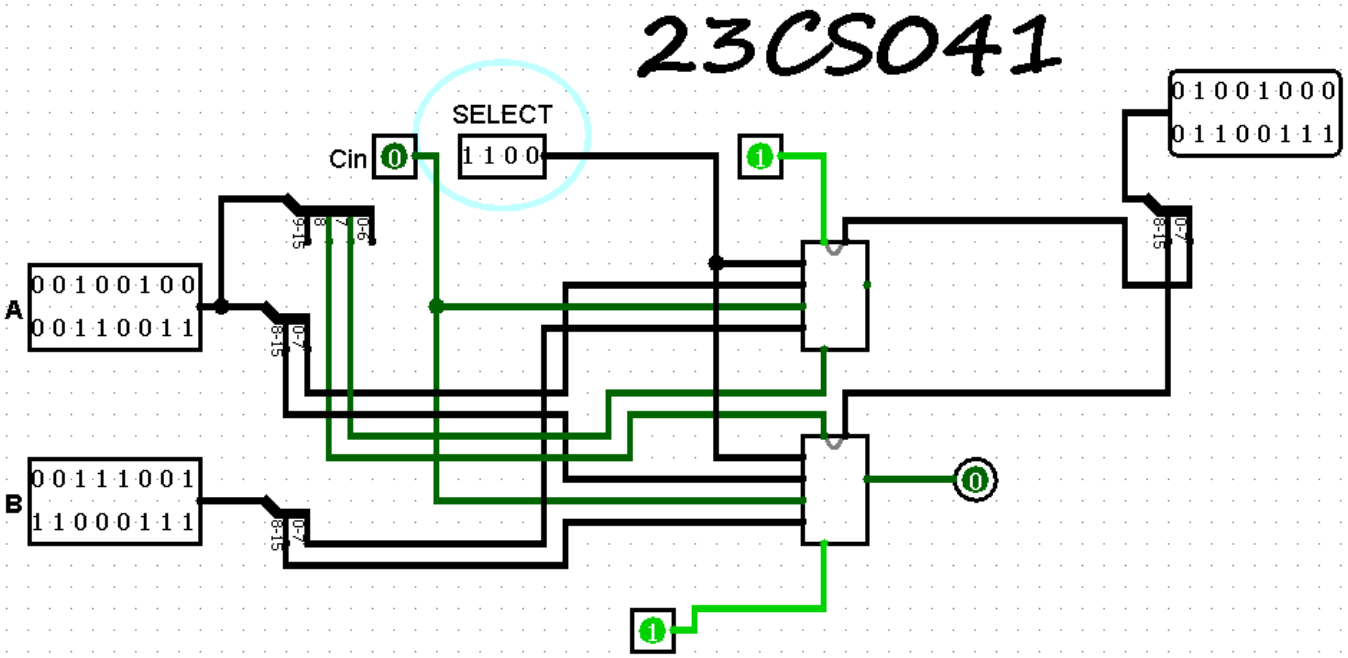

23CS041
SELECT
Cin
0 1 0 1
0 0 1 1 1 1 0 1
1 1 1 1 0 1 1 1
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1


23CS041
SELECT
Cin
0 1 1 0
0 0 0 1 1 1 0 1
1 1 1 1 0 1 0 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1


23CS041
SELECT
Cin
0 1 1 1
1 1 0 1 1 0 1 1
1 1 0 0 1 1 0 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1

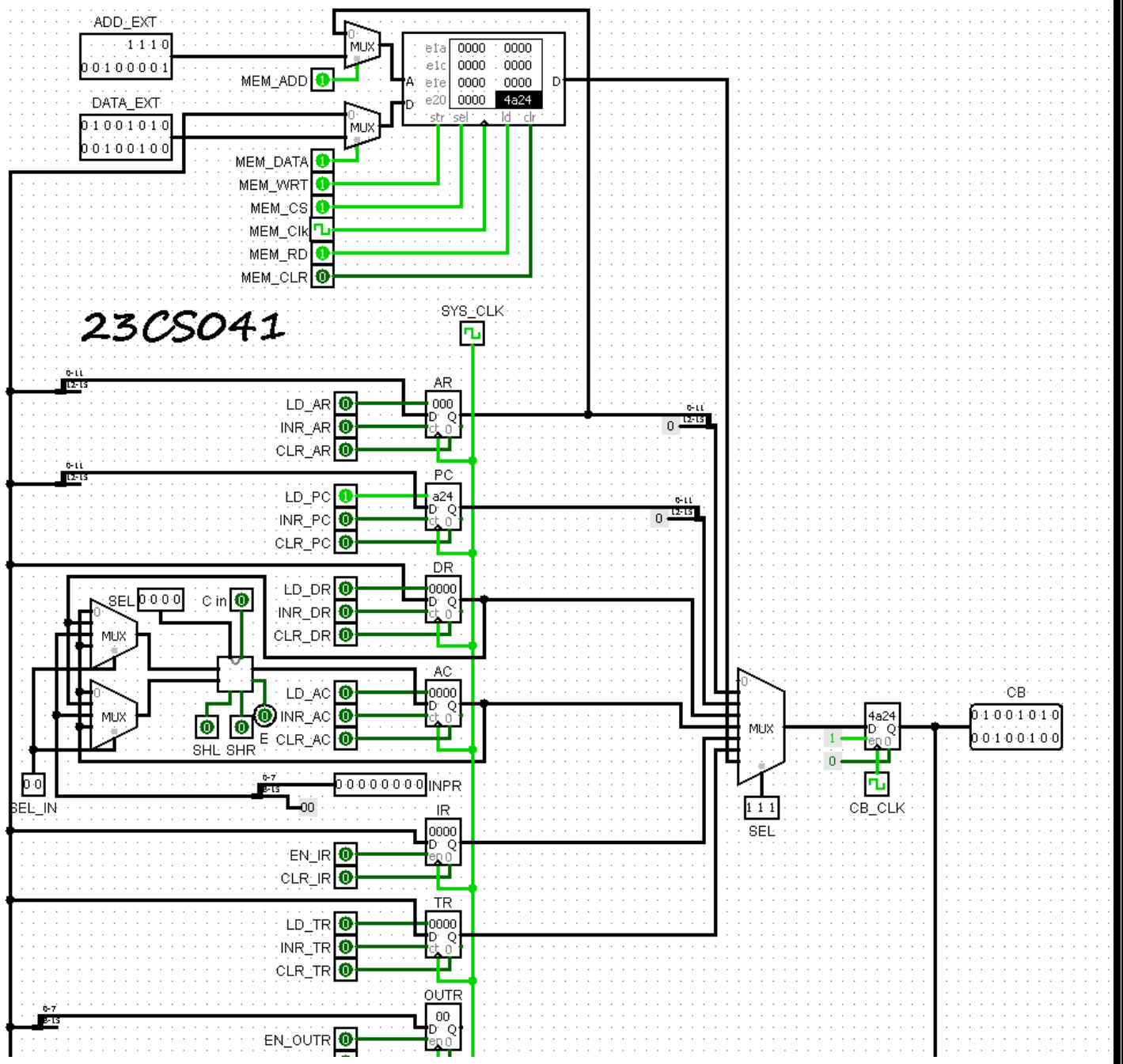
\


23CS041
SELECT
Cin
1 0 0 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
1 0 0 1 0 0 1 0
0 0 0 1 1 0 0 1

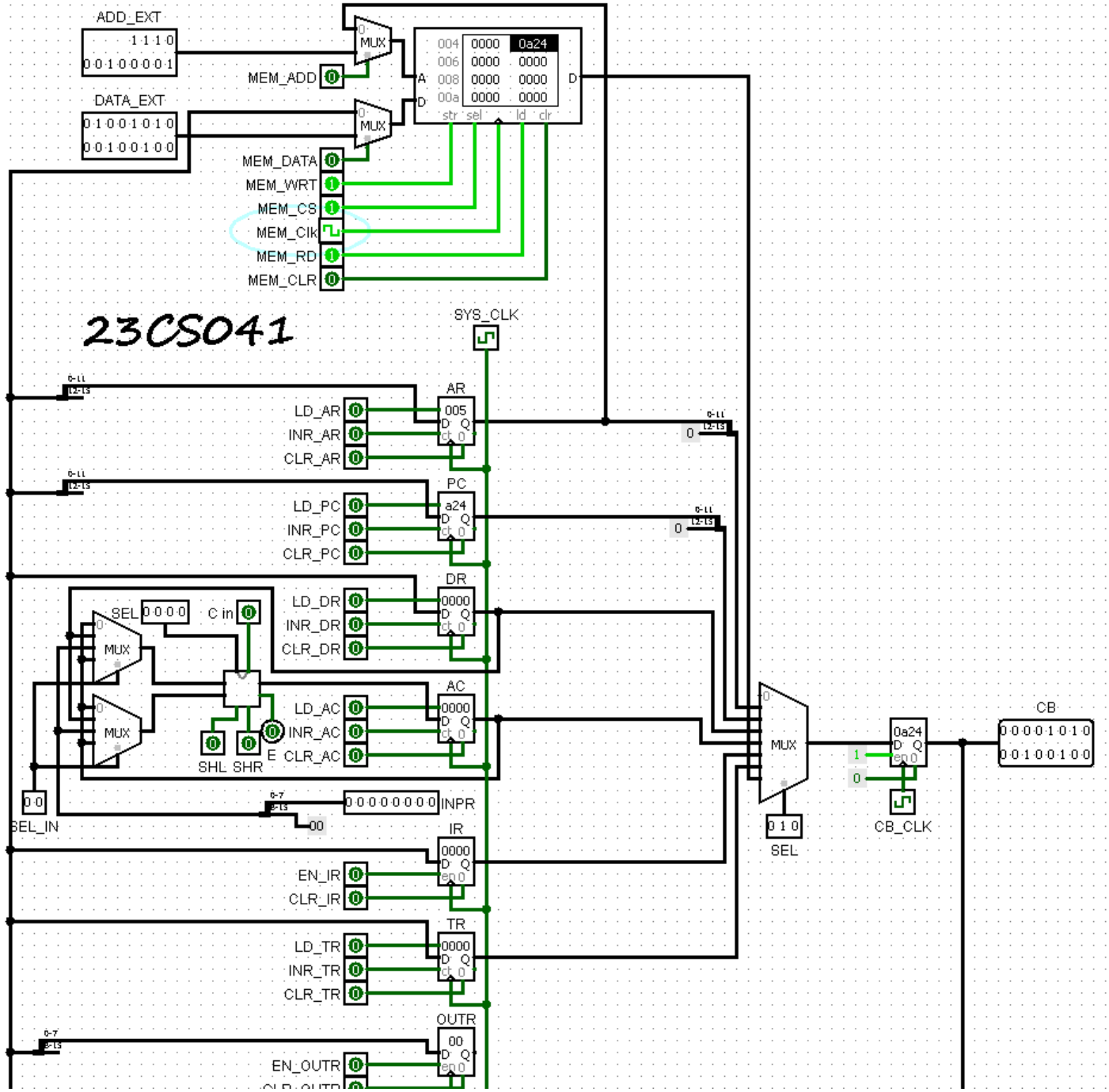

23CS041
SELECT
Cin
1 1 0 0
A
0 0 1 0 0 1 0 0
0 0 1 1 0 0 1 1
B
0 0 1 1 1 0 0 1
1 1 0 0 0 1 1 1
0 1 0 0 1 0 0 0
0 1 1 0 0 1 1 1

**ii.**

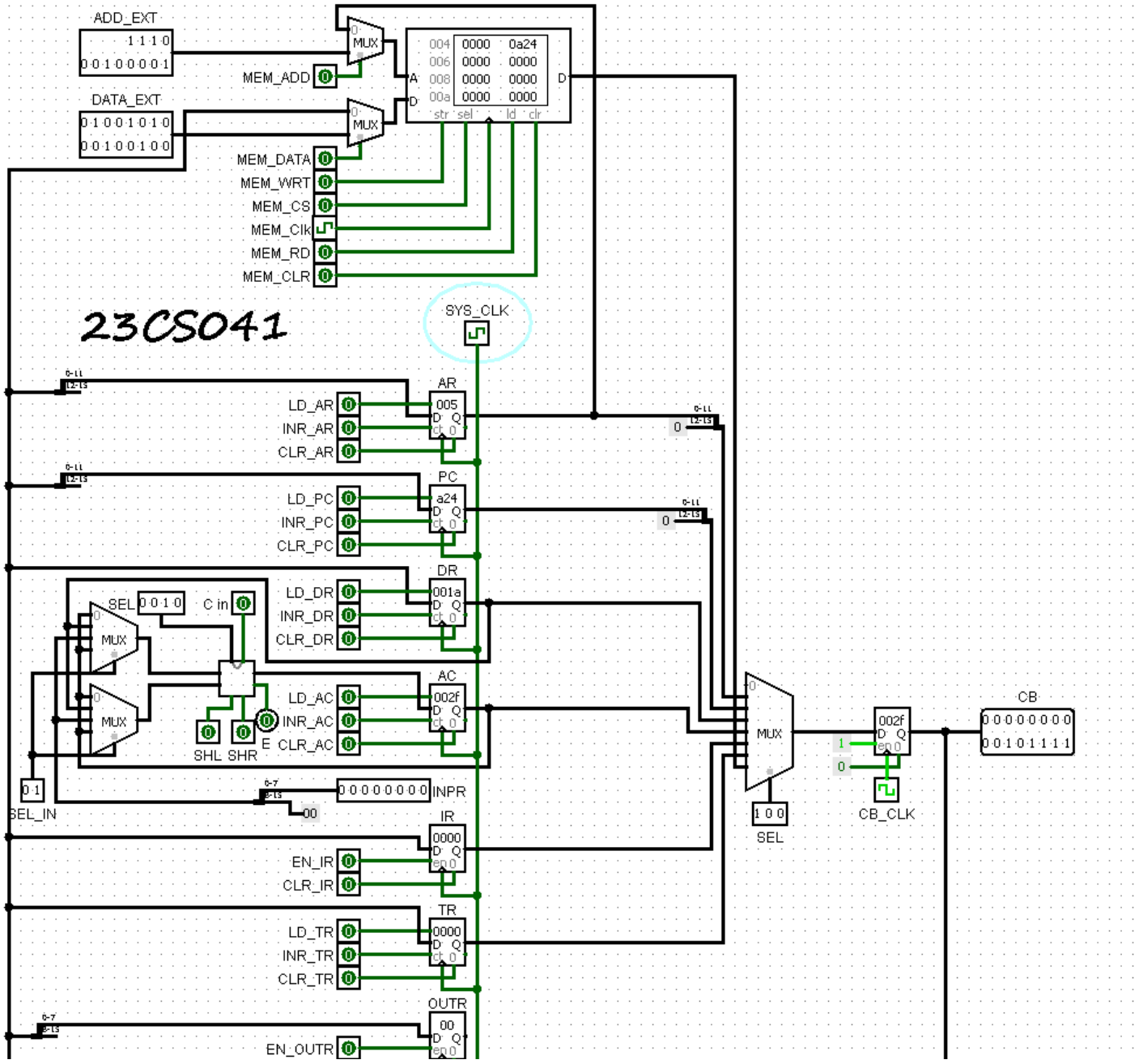
# PC<-MEM[AR]


ADD_EXT
MEM_ADD
DATA_EXT
MEM_DATA
MEM_WRT
MEM_CS
MEM_CIK
MEM_RD
MEM_CLR
MUX
23CS041
SYS_CLK
AR
LD_AR
INR_AR
CLR_AR
PC
LD_PC
INR_PC
CLR_PC
DR
LD_DR
INR_DR
CLR_DR
SEL
C in
AC
LD_AC
INR_AC
CLR_AC
SHL
SHR
E
SEL_IN
INPR
IR
EN_IR
CLR_IR
TR
LD_TR
INR_TR
CLR_TR
OUTR
EN_OUTR
CB
CB_CLK

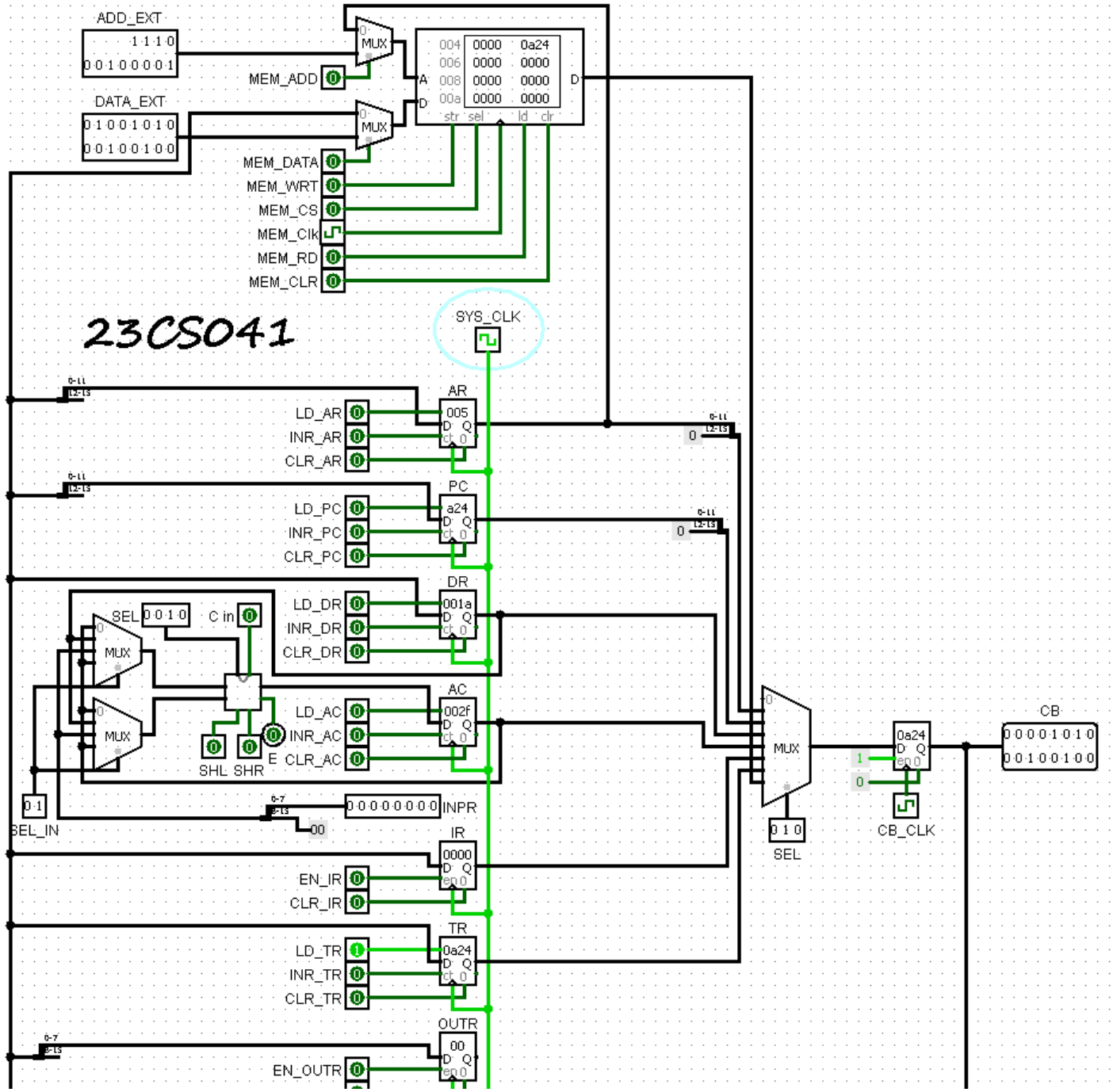
# CB<-PC


ADD_EXT
DATA_EXT
MEM_ADD
MEM_DATA
MEM_WRT
MEM_CS
MEM_Clk
MEM_RD
MEM_CLR
MUX
23CS041
SYS_CLK
AR
PC
DR
AC
IR
TR
OUTR
INPR
LD_AR
INR_AR
CLR_AR
LD_PC
INR_PC
CLR_PC
LD_DR
INR_DR
CLR_DR
LD_AC
INR_AC
CLR_AC
EN_IR
CLR_IR
LD_TR
INR_TR
CLR_TR
EN_OUTR
SEL
C in
SHL
SHR
E
SEL_IN
CB
CB_CLK

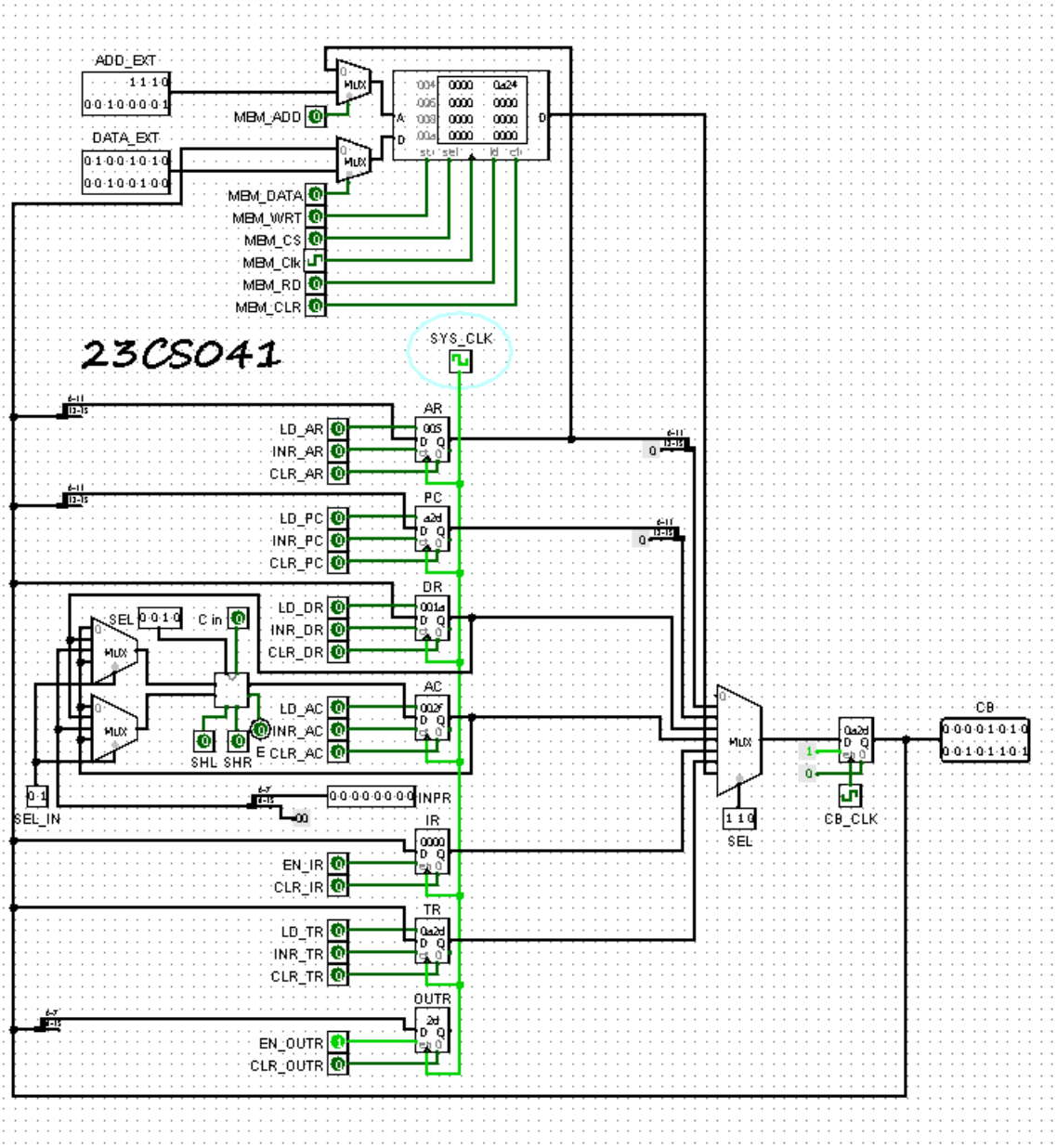
# CB<-AC


ADD_EXT
MEM_ADD
DATA_EXT
MEM_DATA
MEM_WRT
MEM_CS
MEM_Clk
MEM_RD
MEM_CLR
MUX
23CS041
SYS_CLK
AR
LD_AR
INR_AR
CLR_AR
PC
LD_PC
INR_PC
CLR_PC
DR
LD_DR
INR_DR
CLR_DR
AC
LD_AC
INR_AC
CLR_AC
SEL
C in
SHL
SHR
E
SEL_IN
INPR
IR
EN_IR
CLR_IR
TR
LD_TR
INR_TR
CLR_TR
OUTR
EN_OUTR
CB
CB_CLK

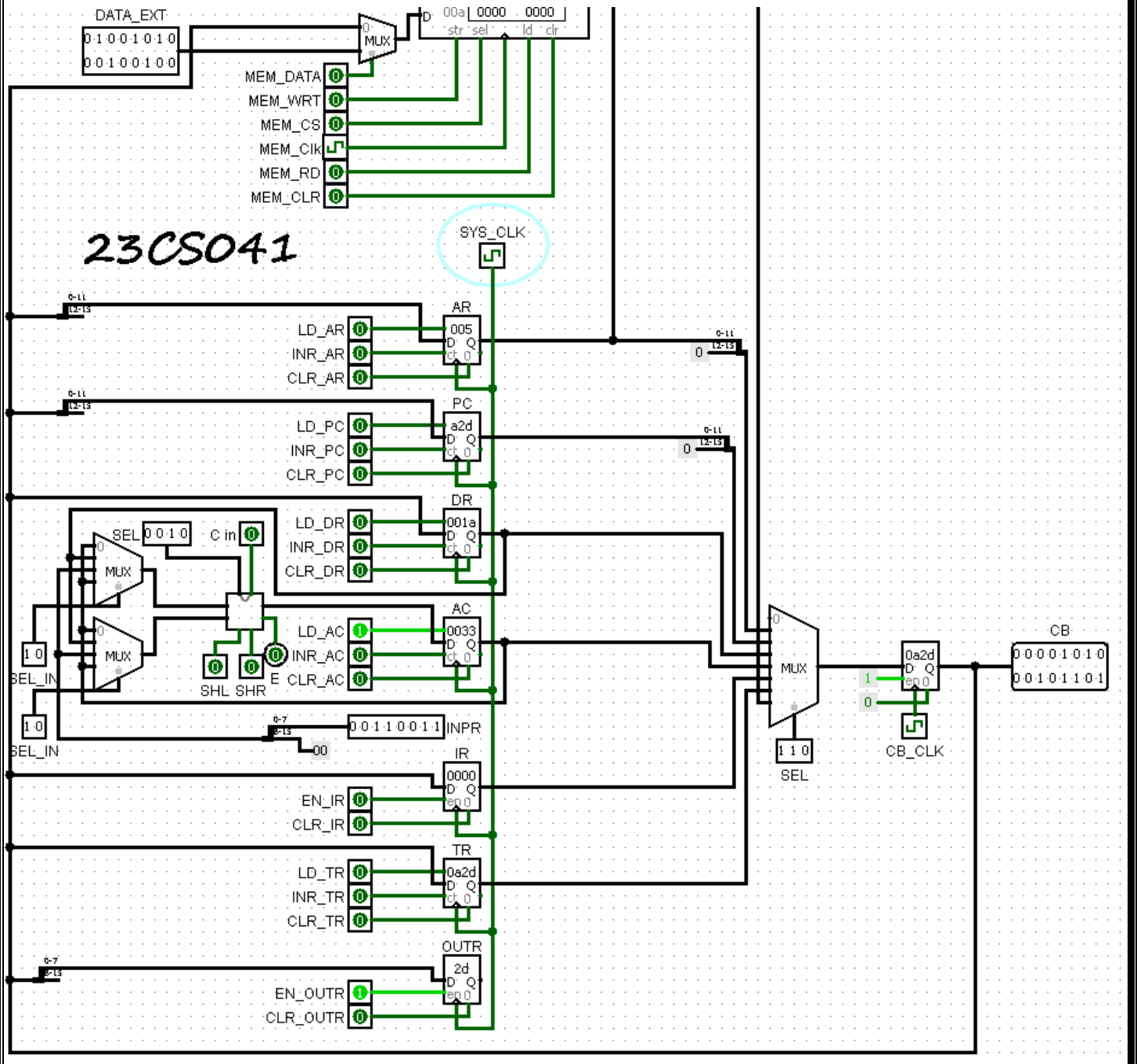
# CB<-TR


ADD_EXT
MEM_ADD
DATA_EXT
MEM_DATA
MEM_WRT
MEM_CS
MEM_Clk
MEM_RD
MEM_CLR
MUX
23CS041
SYS_CLK
AR
LD_AR
INR_AR
CLR_AR
PC
LD_PC
INR_PC
CLR_PC
DR
LD_DR
INR_DR
CLR_DR
SEL
C in
SHL
SHR
E
AC
LD_AC
INR_AC
CLR_AC
SEL_IN
INPR
IR
EN_IR
CLR_IR
TR
LD_TR
INR_TR
CLR_TR
OUTR
EN_OUTR
CB
CB_CLK

# OUTR<-CB


ADD_EXT
MBM_ADD
DATA_EXT
MBM_DATA
MBM_WRT
MBM_CS
MBM_Clk
MBM_RD
MBM_CLR
23CS041
SYS_CLK
AR
LD_AR
INR_AR
CLR_AR
PC
LD_PC
INR_PC
CLR_PC
DR
LD_DR
INR_DR
CLR_DR
SEL
C in
AC
LD_AC
INR_AC
CLR_AC
SHL
SHR
E
SEL_IN
INPR
IR
EN_IR
CLR_IR
TR
LD_TR
INR_TR
CLR_TR
OUTR
EN_OUTR
CLR_OUTR
MUX
CB
CB_CLK

# AC<-INPR


DATA_EXT
0 1 0 0 1 0 1 0
0 0 1 0 0 1 0 0
MUX
D
00a
0000
0000
str sel ld clr
MEM_DATA
MEM_WRT
MEM_CS
MEM_CIK
MEM_RD
MEM_CLR
23CS041
SYS_CLK
AR
005
LD_AR
INR_AR
CLR_AR
PC
a2d
LD_PC
INR_PC
CLR_PC
DR
001a
LD_DR
INR_DR
CLR_DR
SEL
0 0 1 0
C in
AC
0033
LD_AC
INR_AC
CLR_AC
SHL SHR E
SEL_IN
0 0 1 1 0 0 1 1
INPR
IR
0000
EN_IR
CLR_IR
TR
0a2d
LD_TR
INR_TR
CLR_TR
OUTR
2d
EN_OUTR
CLR_OUTR
1 1 0
SEL
CB_CLK
CB
0 0 0 0 1 0 1 0
0 0 1 0 1 1 0 1

**CONCLUSION:**