Date:

# EXPERIMENT NO. 4

#### AIM: Implement arithmetic and logic unit circuits in Logisim.

#### OBJECTIVES:

#### Implement 1-bit, 2-bit, 4-bit and 8-bit arithmetic unit circuits

#### Implement 1-bit, 2-bit, 4-bit and 8-bit logical unit circuits for four logical functions

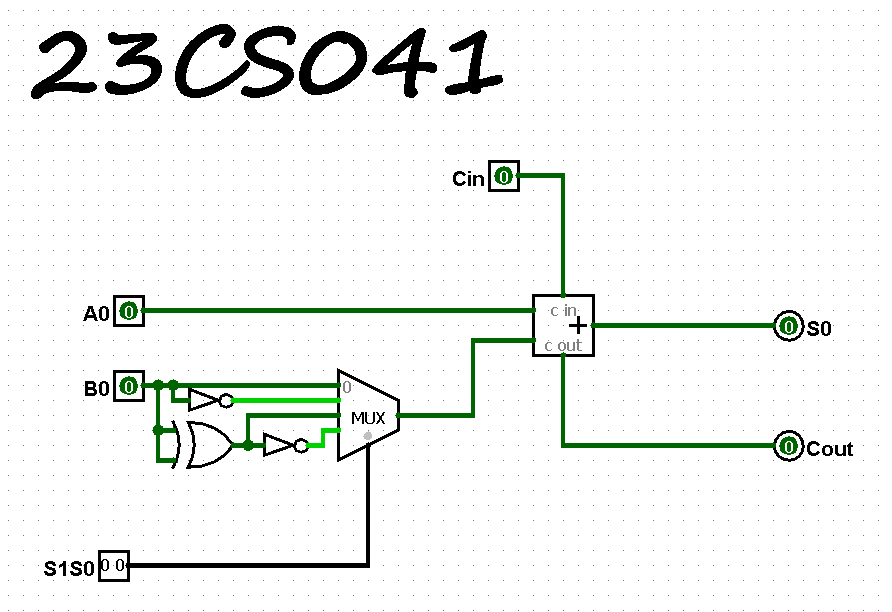
#### Implement 1-bit and 2-bit logical unit circuits for sixteen logical functions

#### Implement 2-bit, 4-bit and 8-bit bidirectional shifter

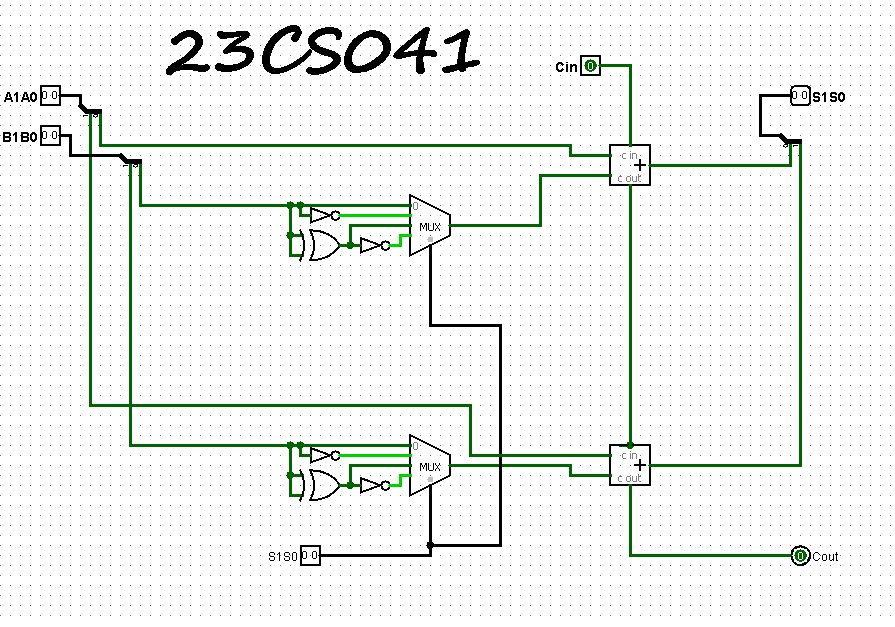
#### Implement 1-bit, 2-bit, 4-bit and 8-bit ALU

**CIRCUITS:**

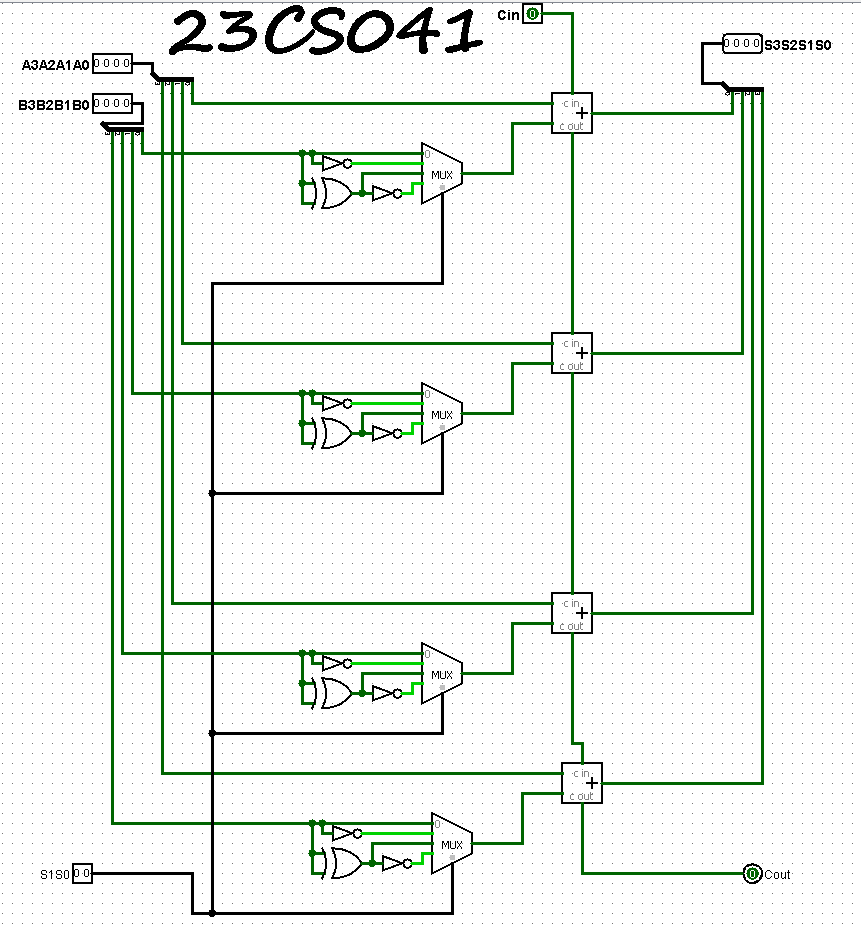
1. **1) 1-bit arithmetic**

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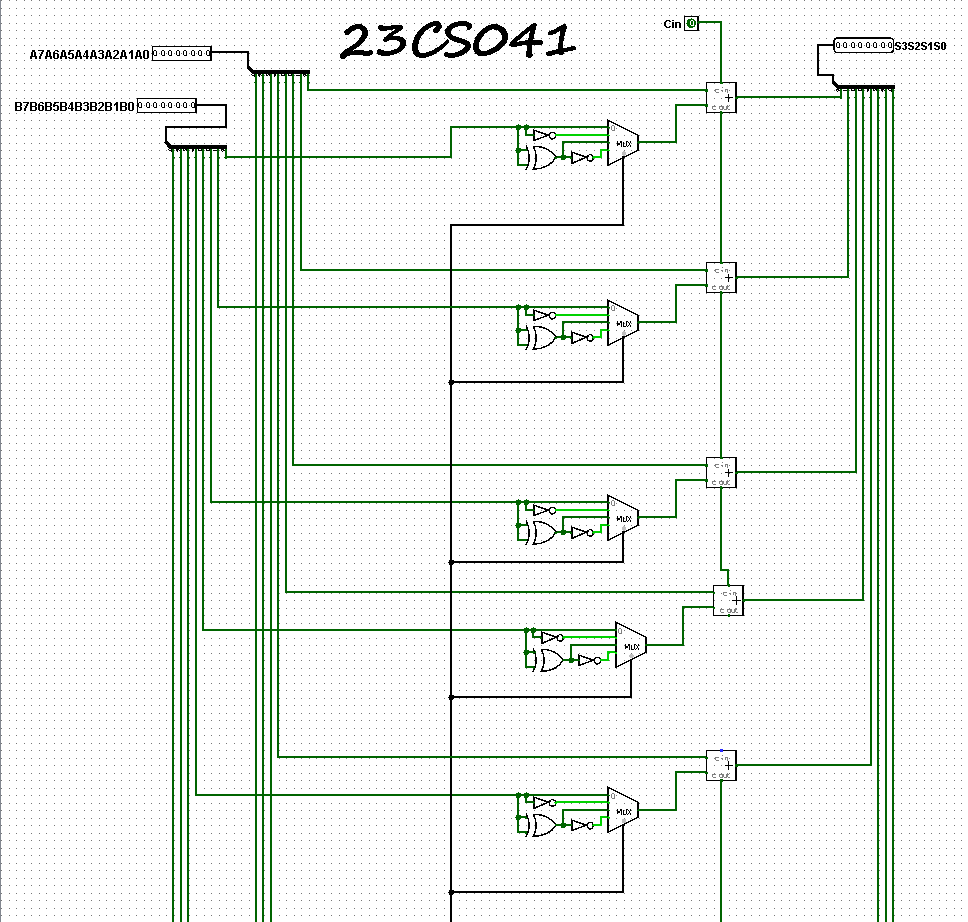
**2) 2-bit arithmetic**

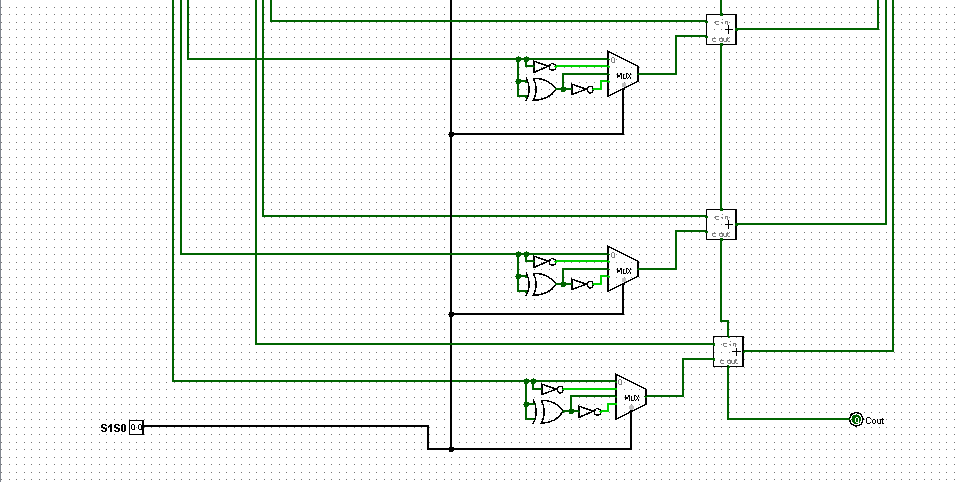
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**3) 4-bit arithmetic**

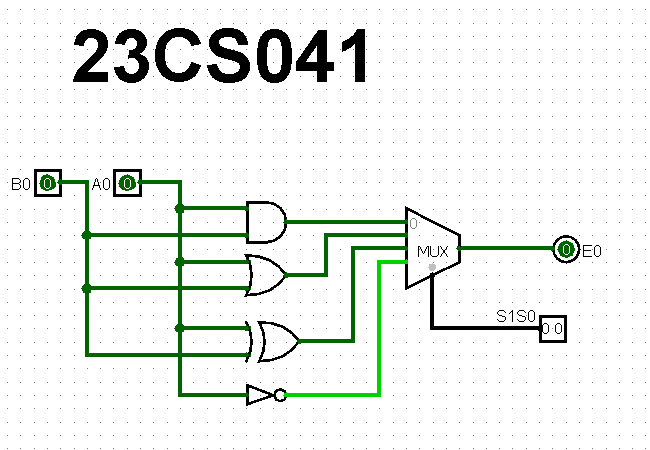
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**4) 8-bit arithmetic**

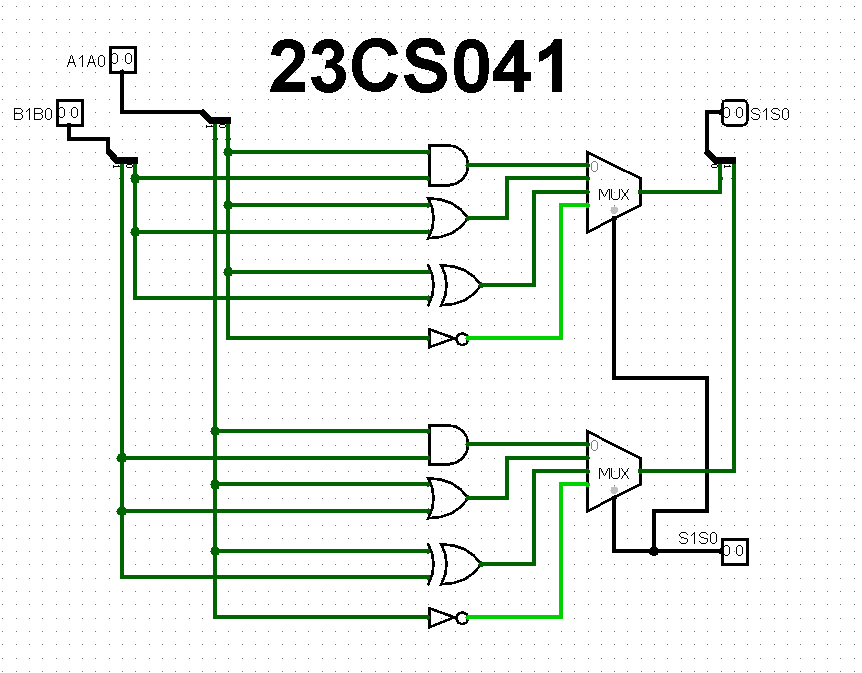
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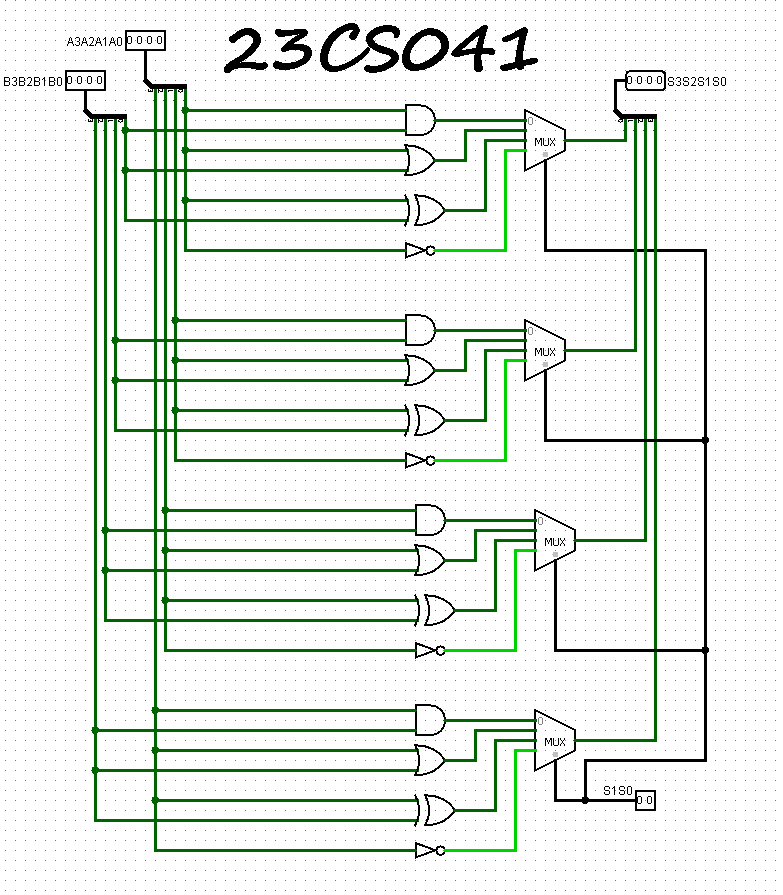
1. **1) 1-bit logical**

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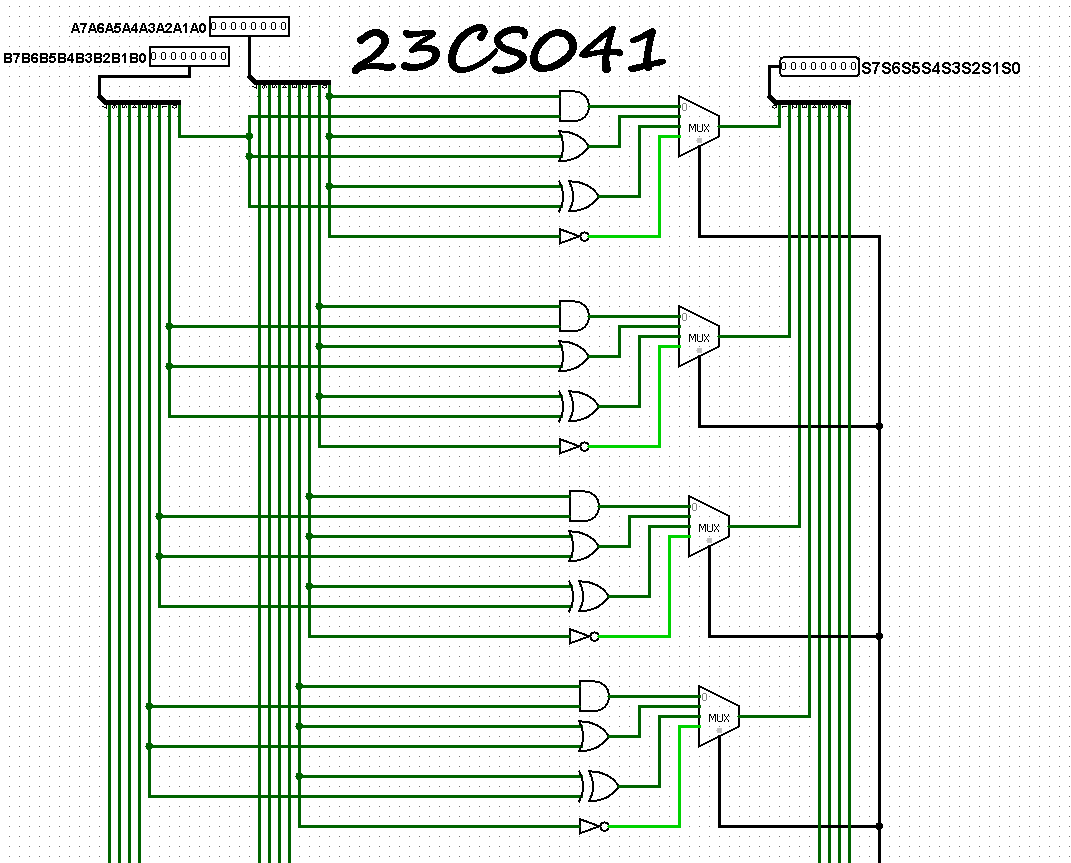
**2) 2-bit logical**

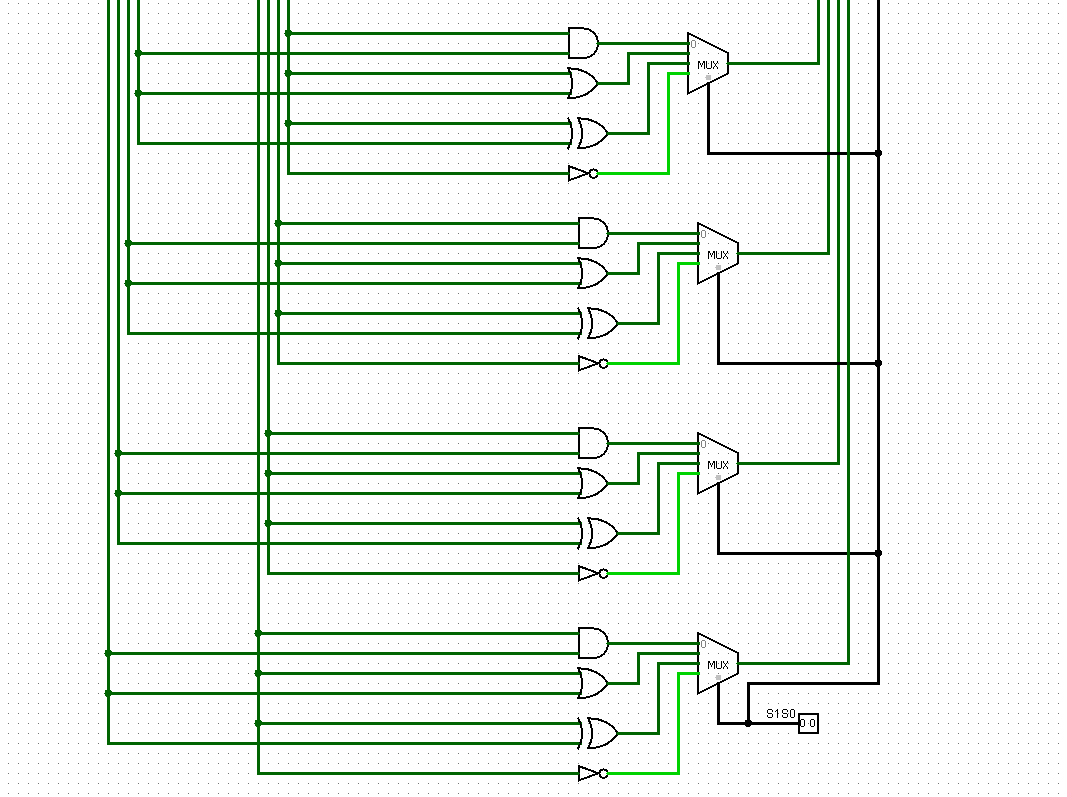
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**3) 4-bit logical**

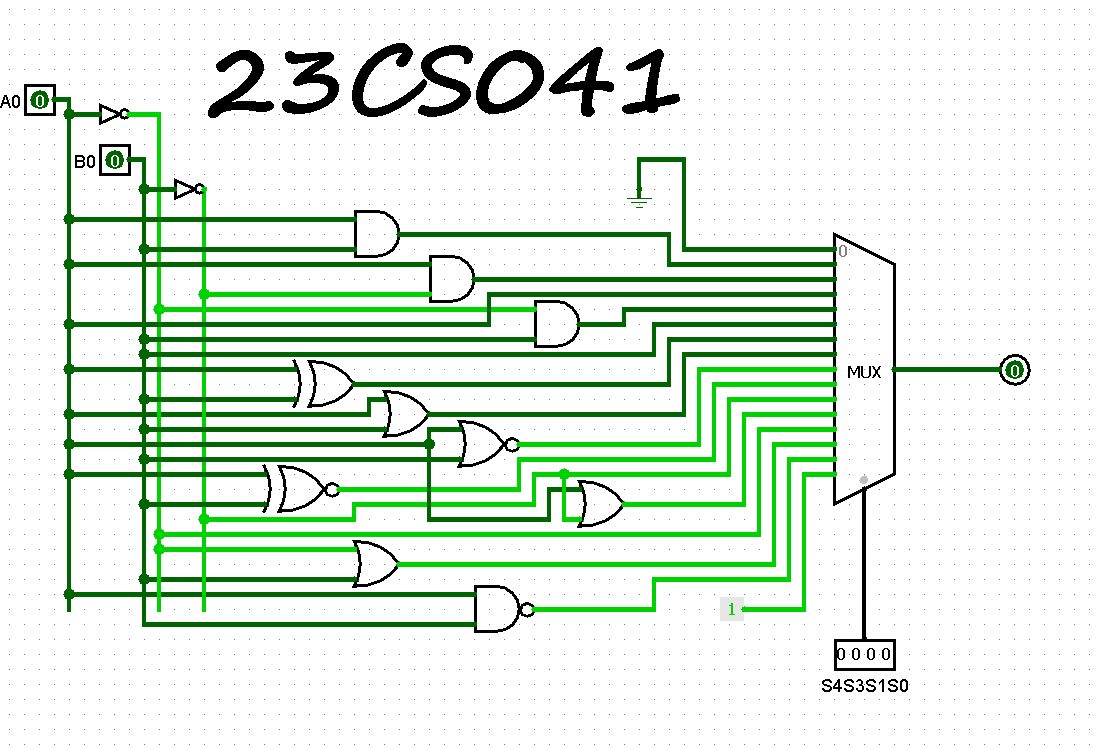
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**4) 8-bit logical**

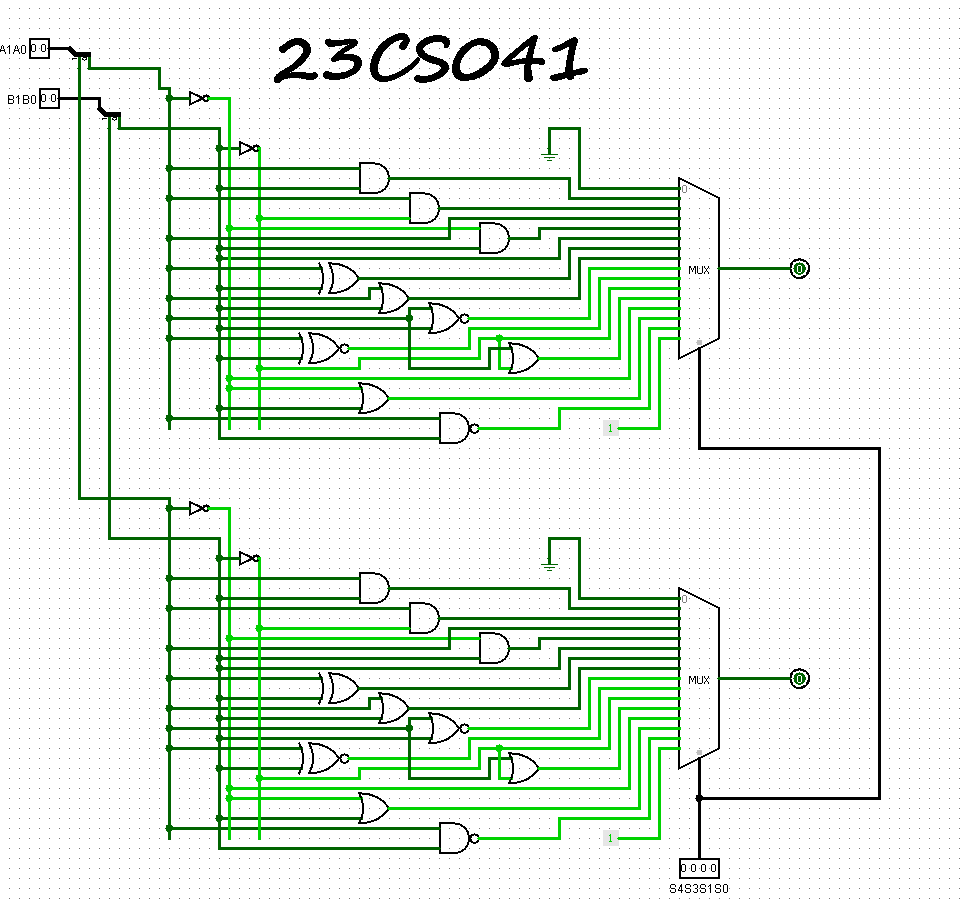
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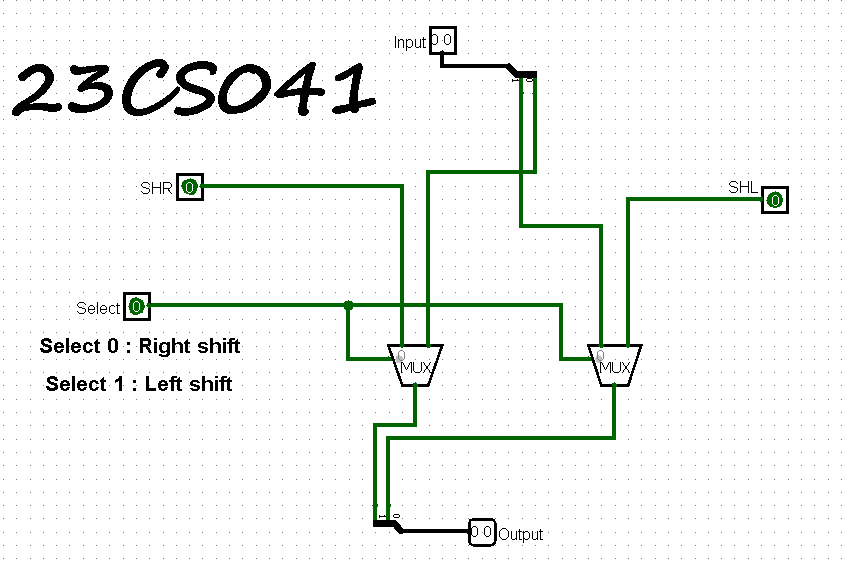
1. **1)** **1-bit** **logical circuits for sixteen logical functions**

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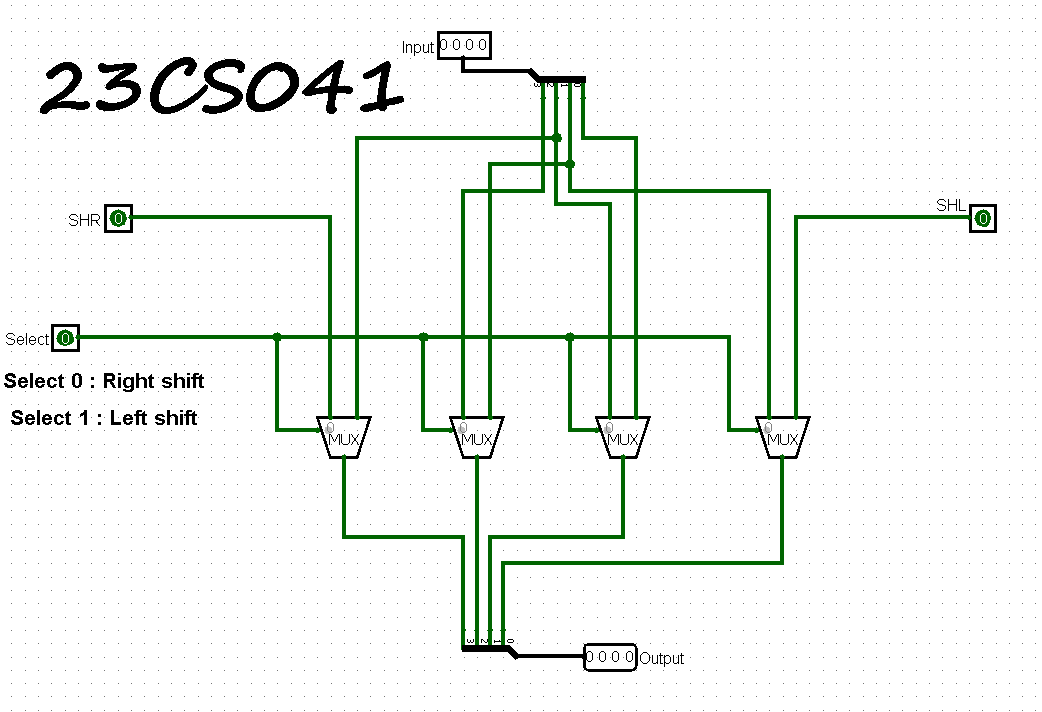
**2)** **2-bit** **logical circuits for sixteen logical functions**

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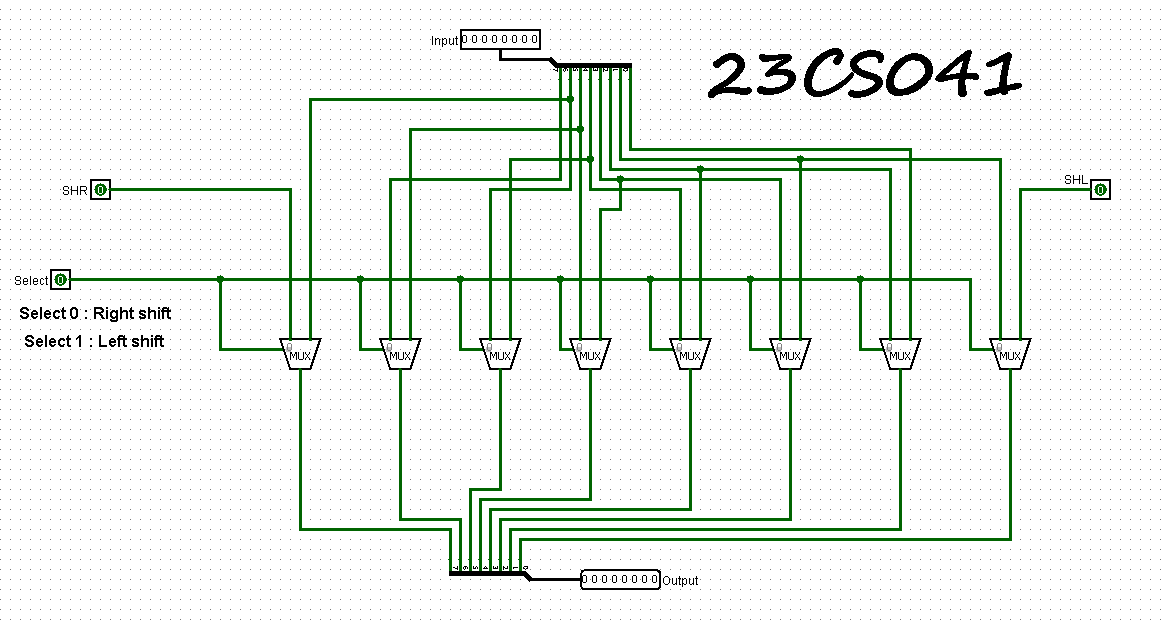
1. **1) 2-bit bidirectional shifter**

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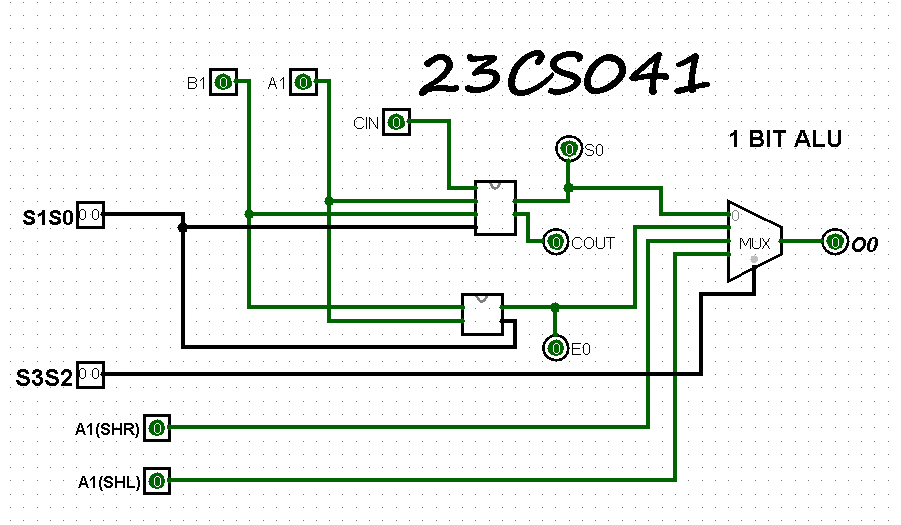
**2) 4-bit bidirectional shifter**

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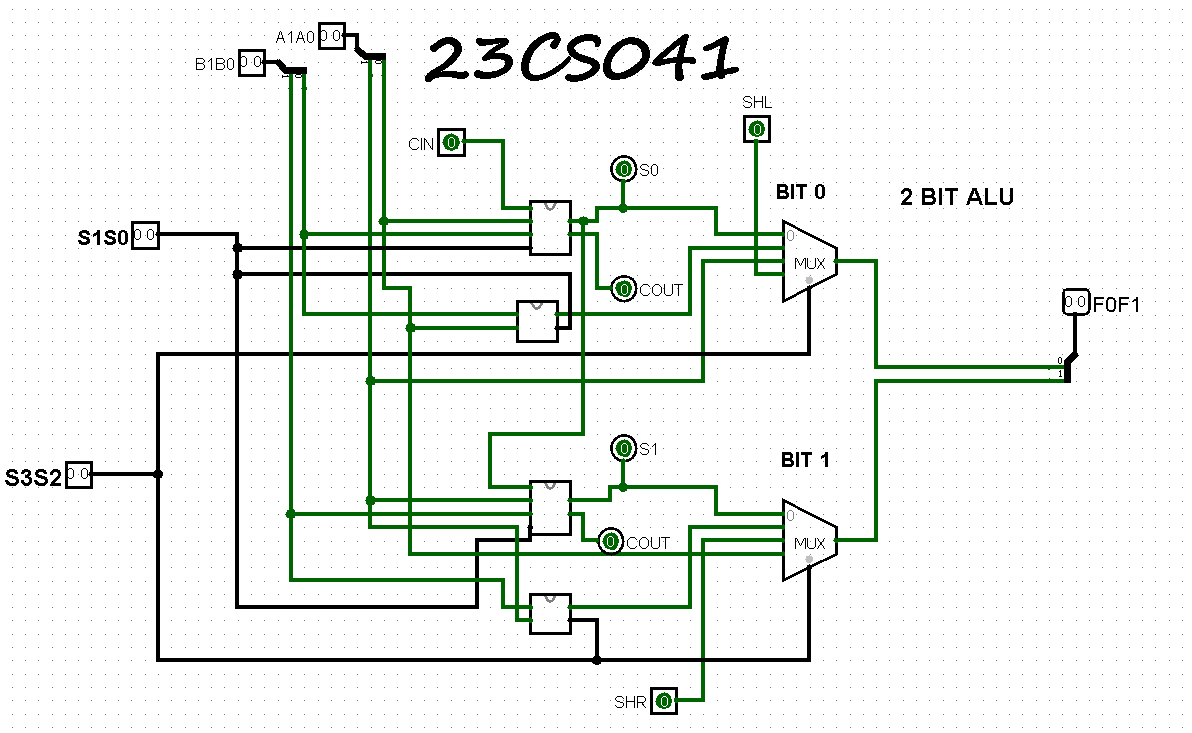
**3) 8-bit bidirectional shifter**

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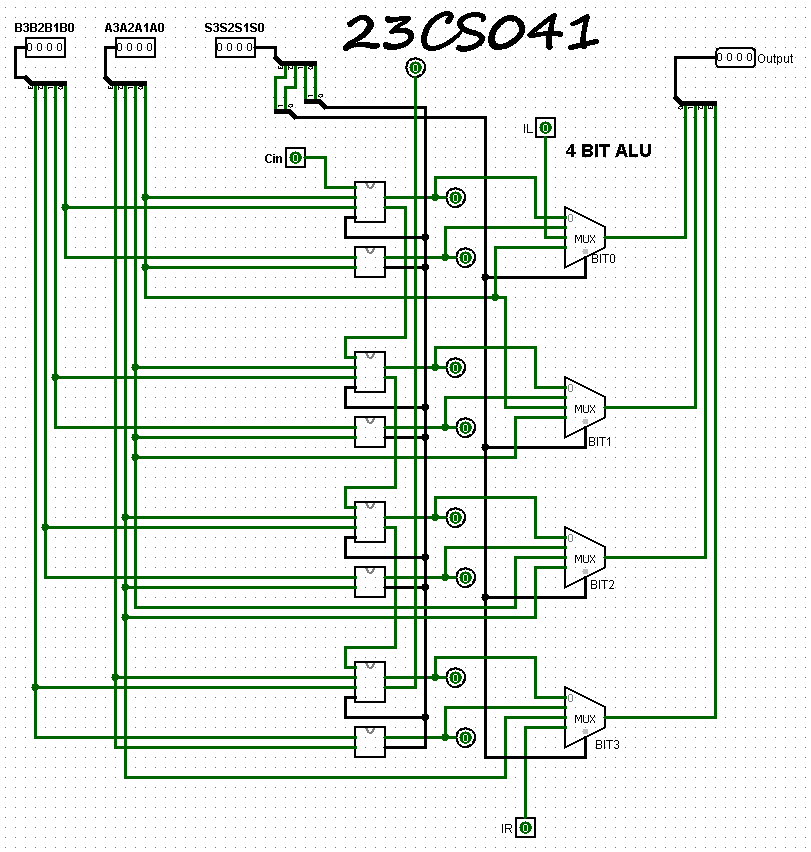
1. **1) 1-bit ALU**

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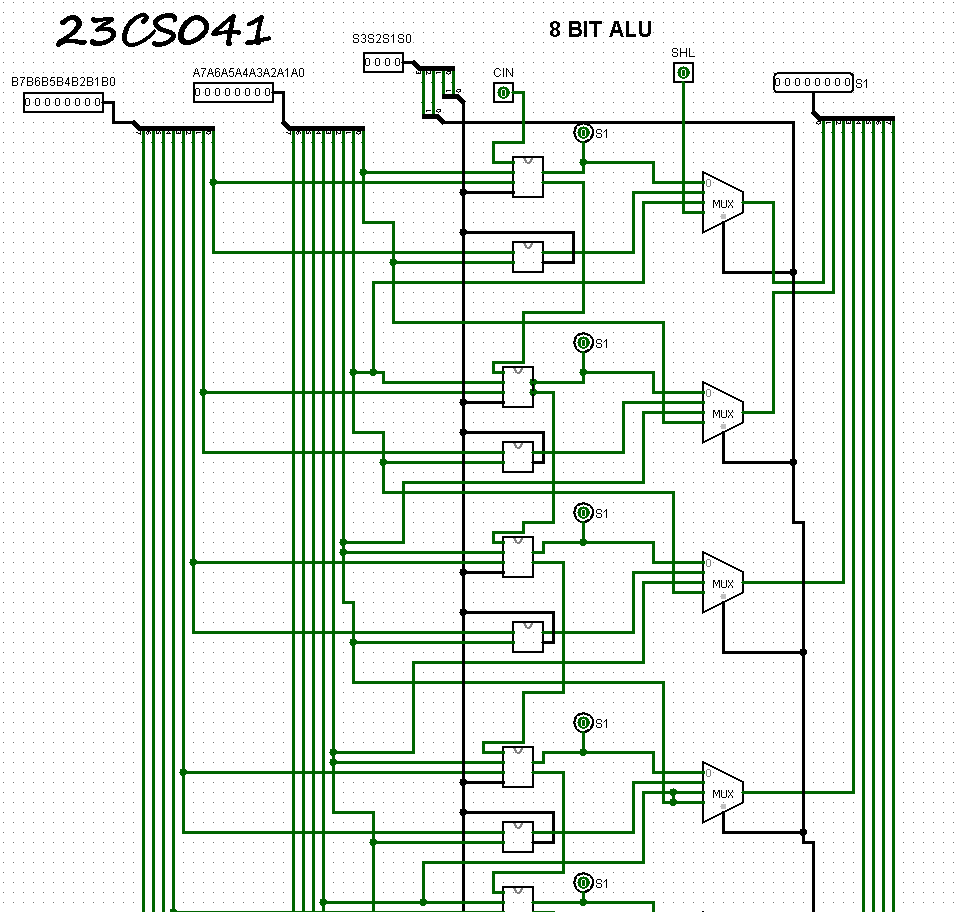
**2) 2-bit ALU**

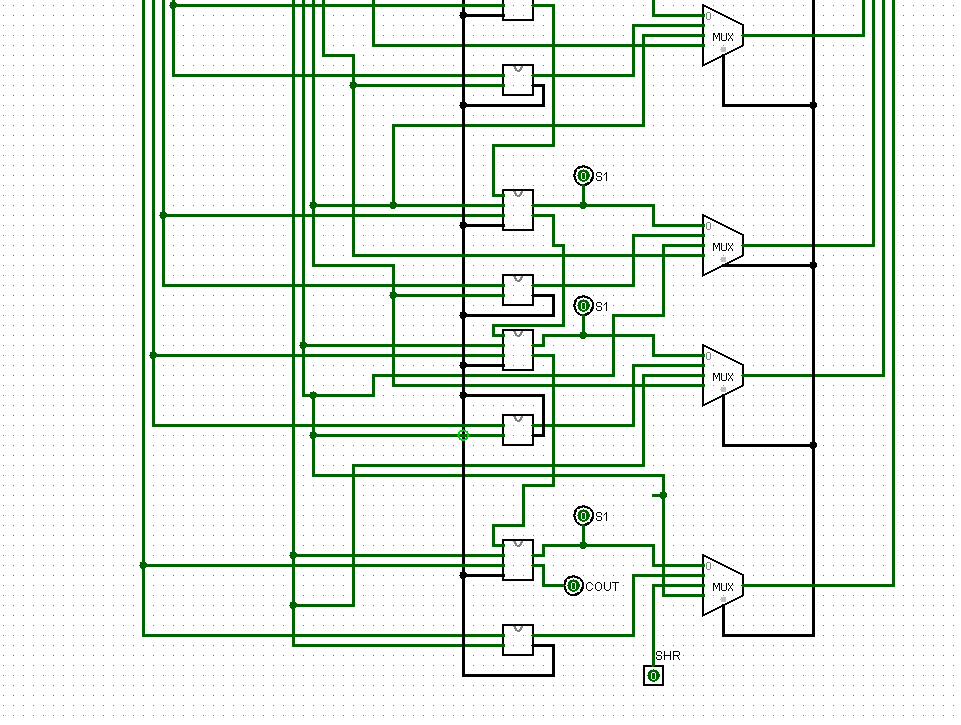
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**3) 4-bit ALU**

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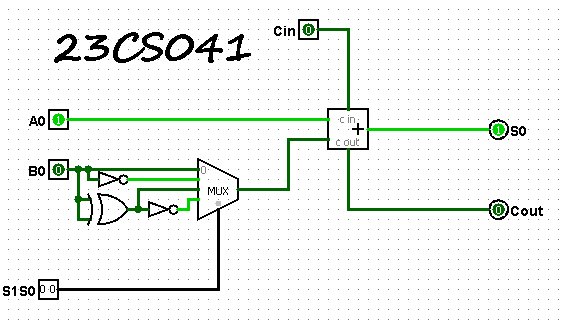
**4) 8-bit ALU**

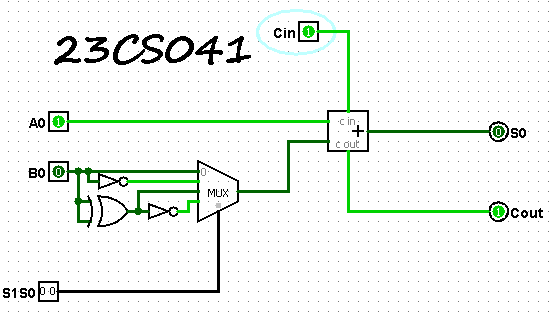
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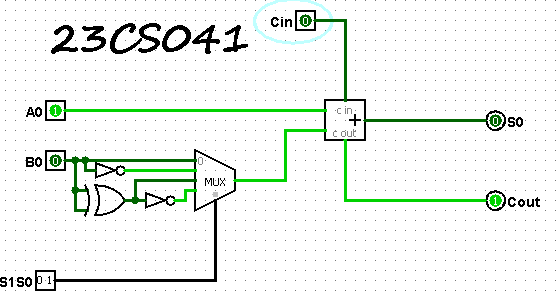
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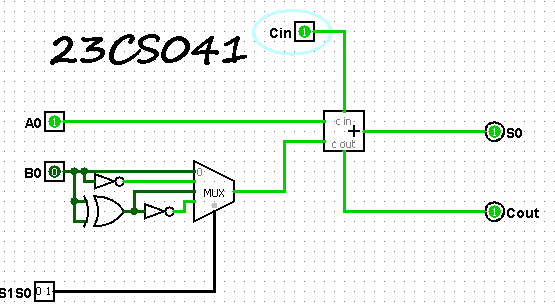
**OUTPUTS:**

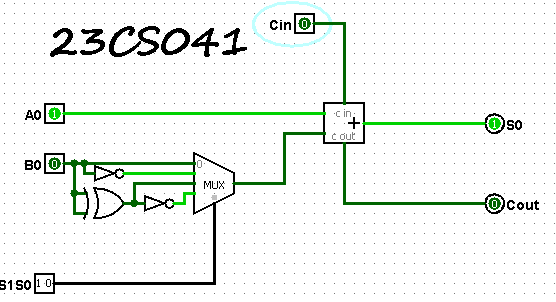
1. **1) 1 bit arithmetic**

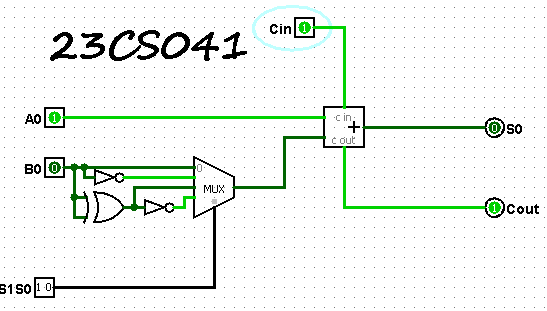
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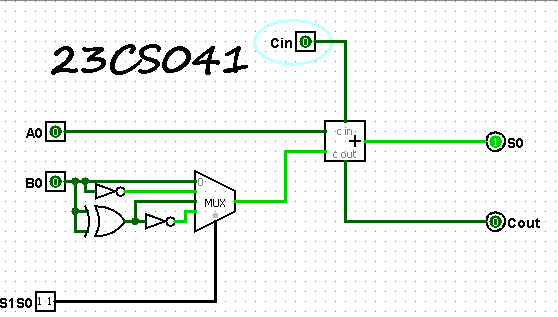
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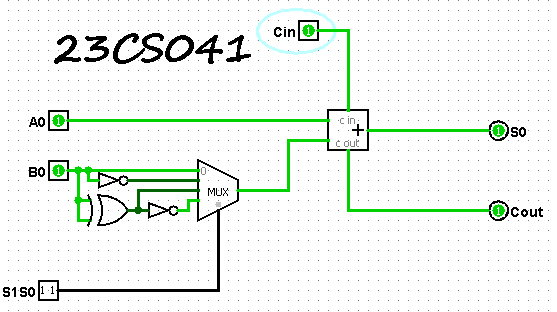
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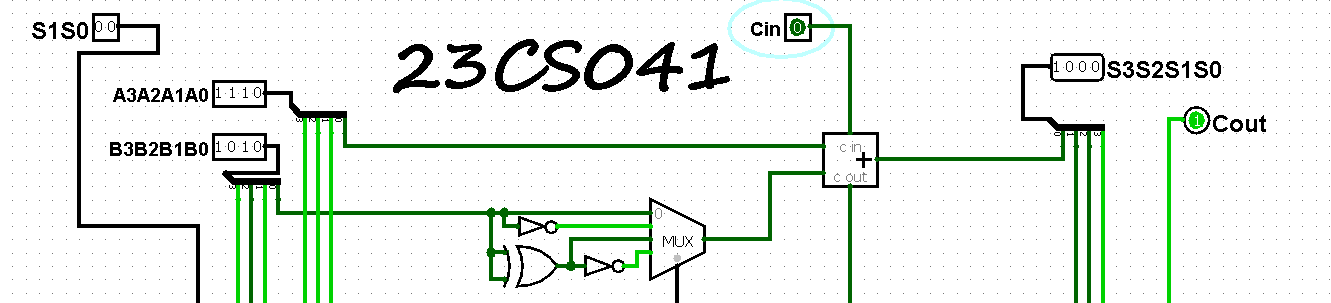
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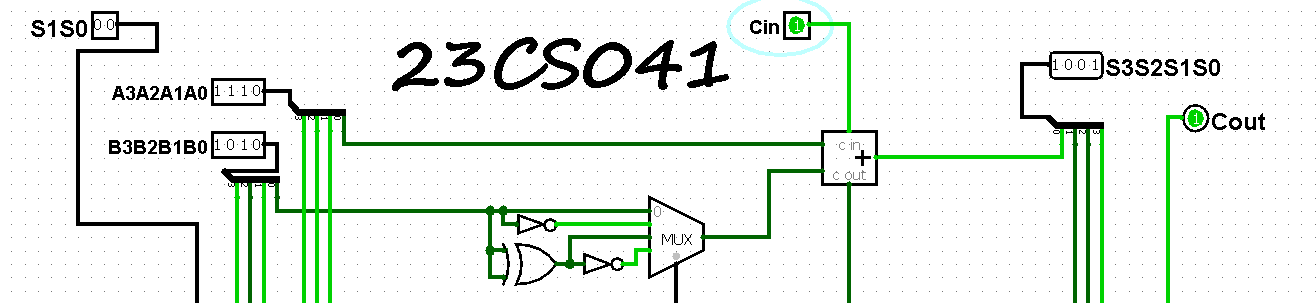


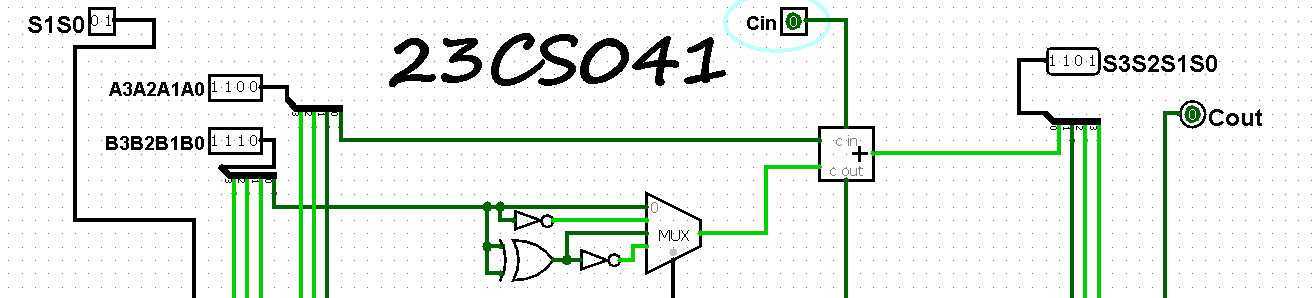
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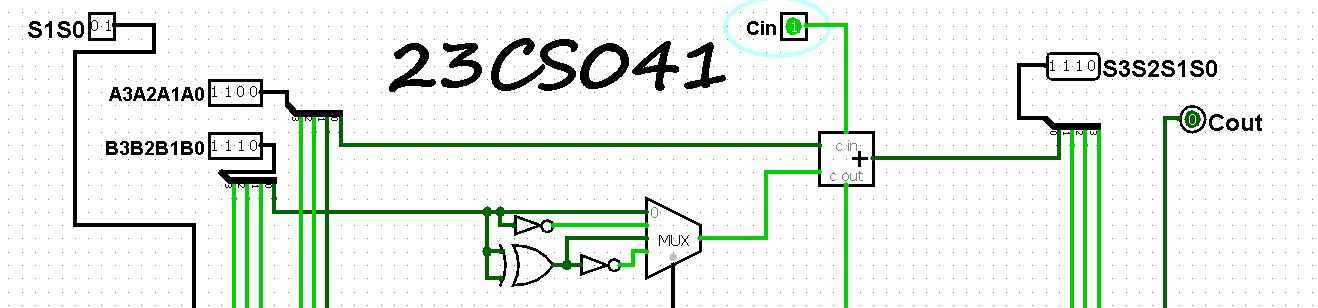


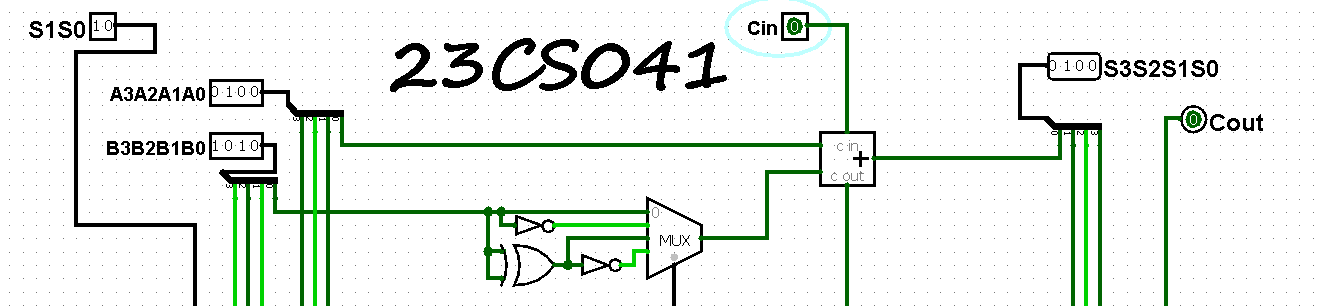
**2) 4 bit arithmetic**

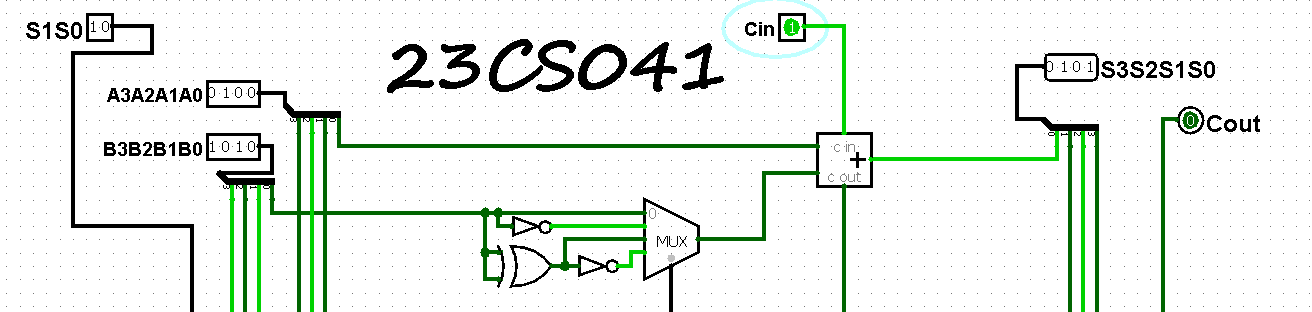
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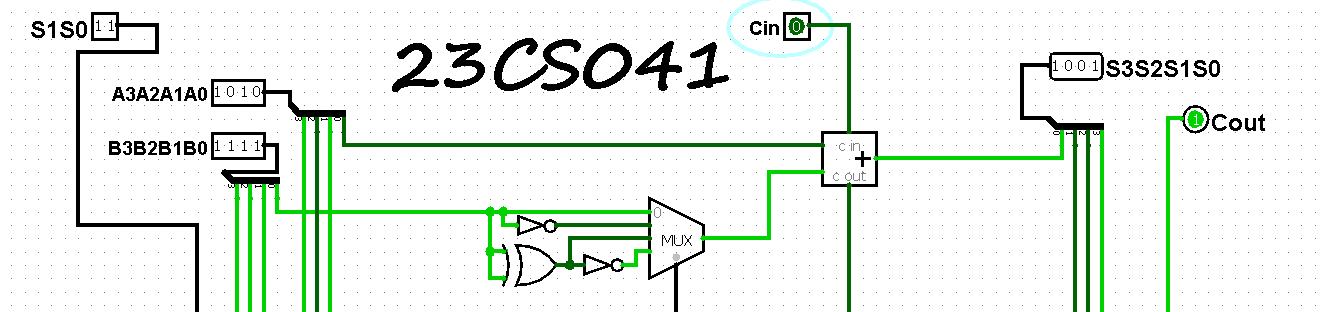
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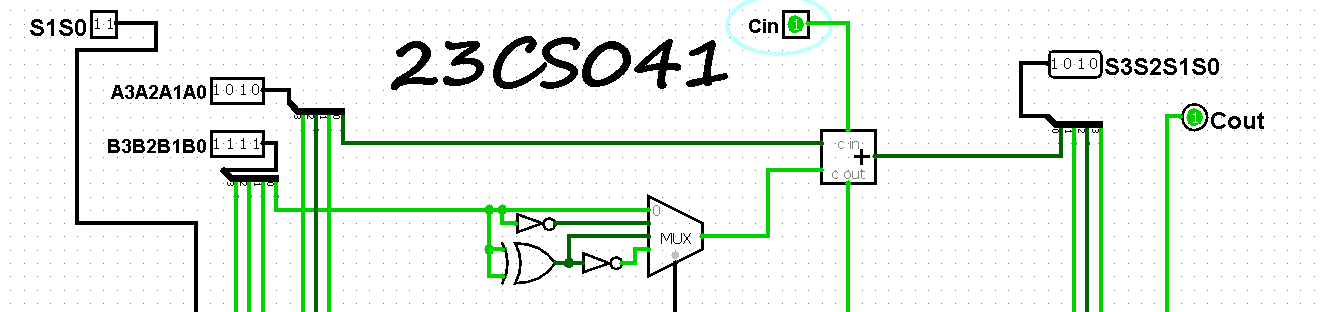
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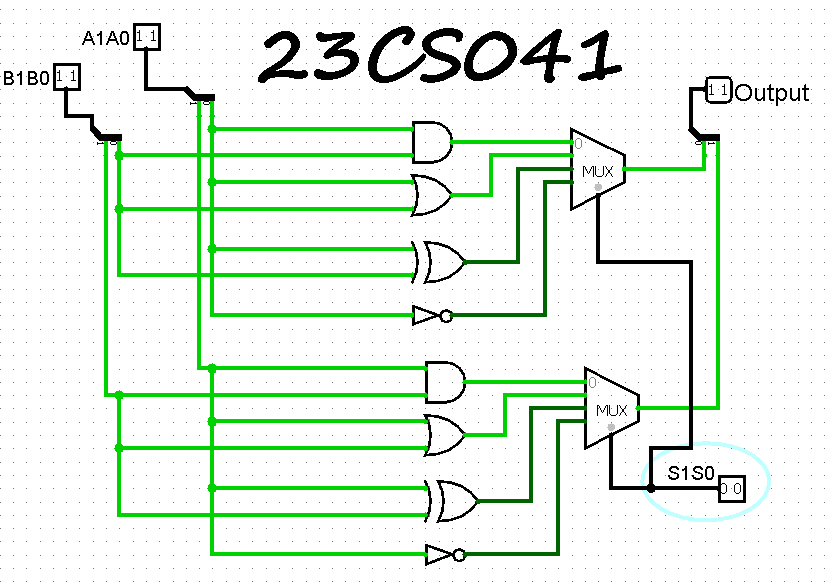
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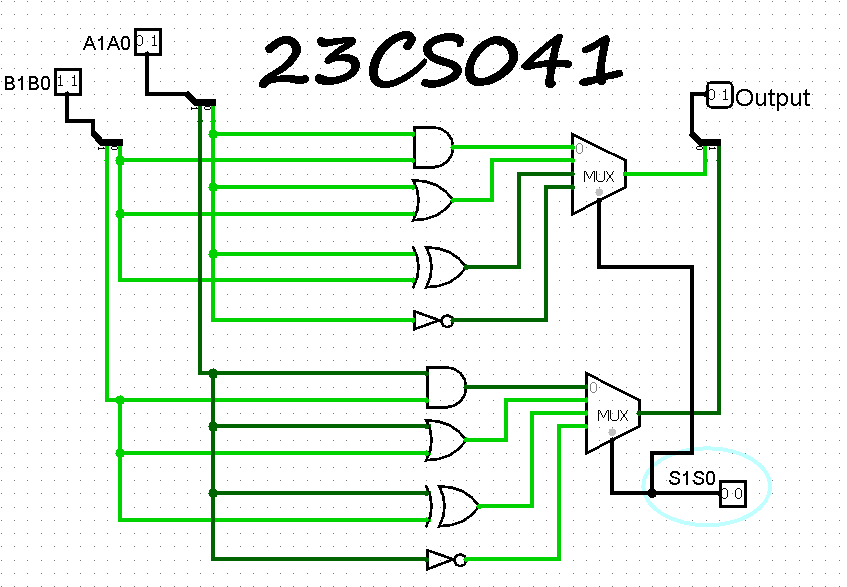
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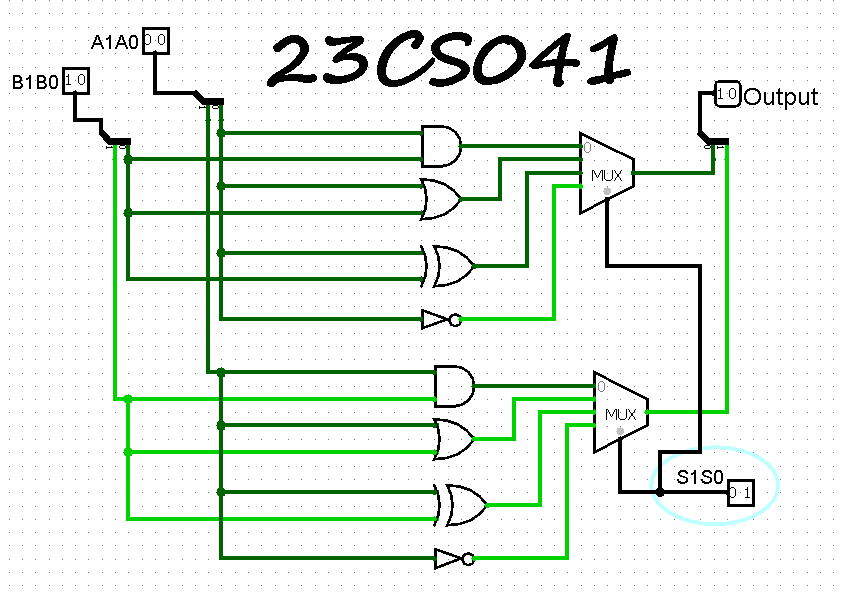
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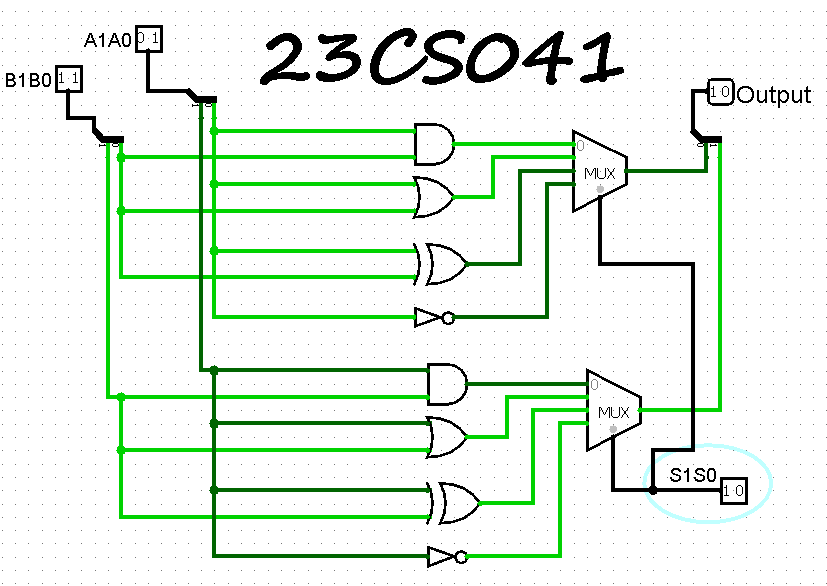
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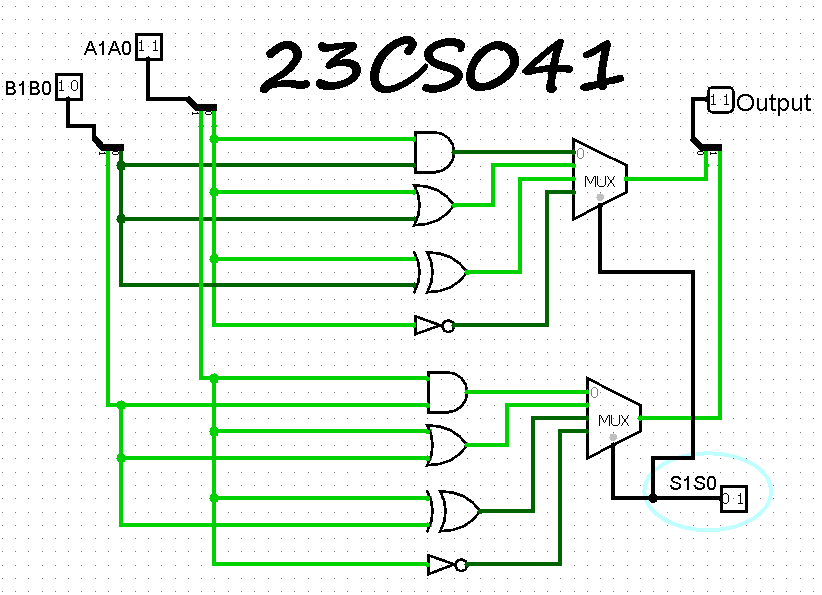
1. **1) 2 bit logical**

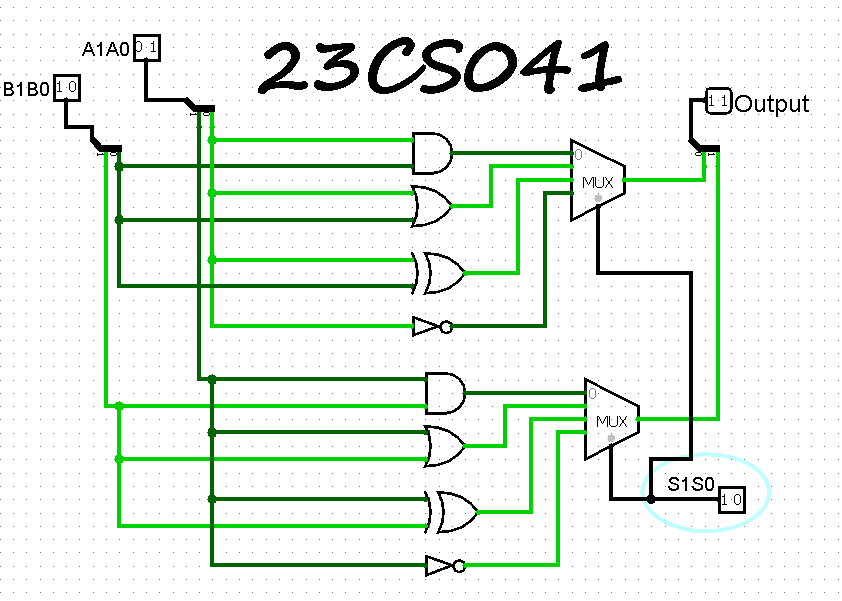


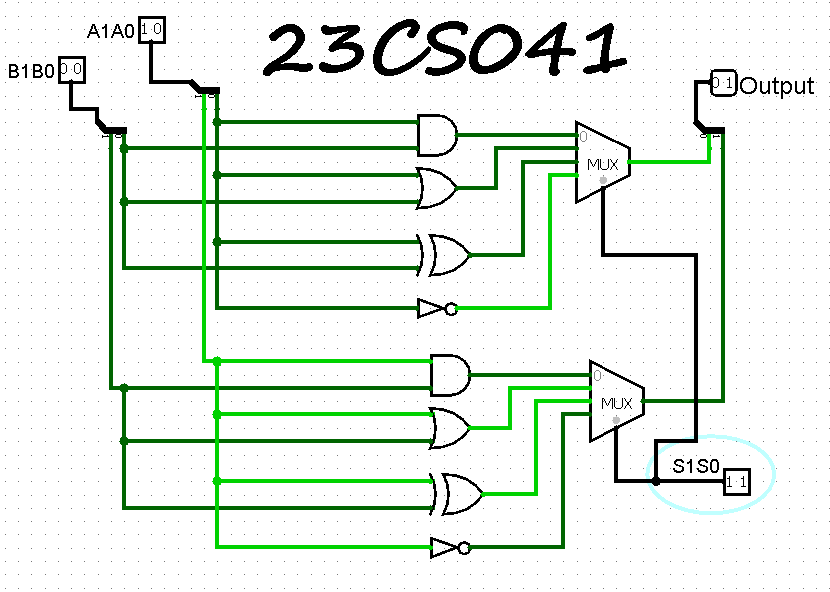
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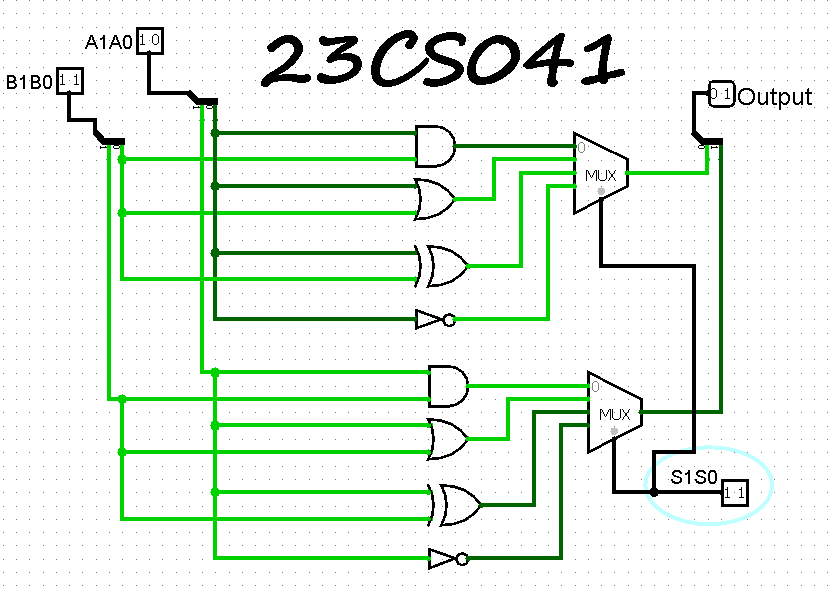
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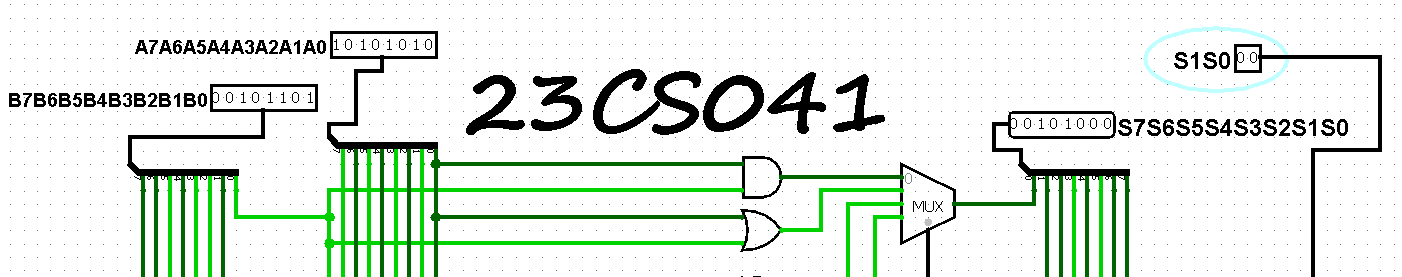


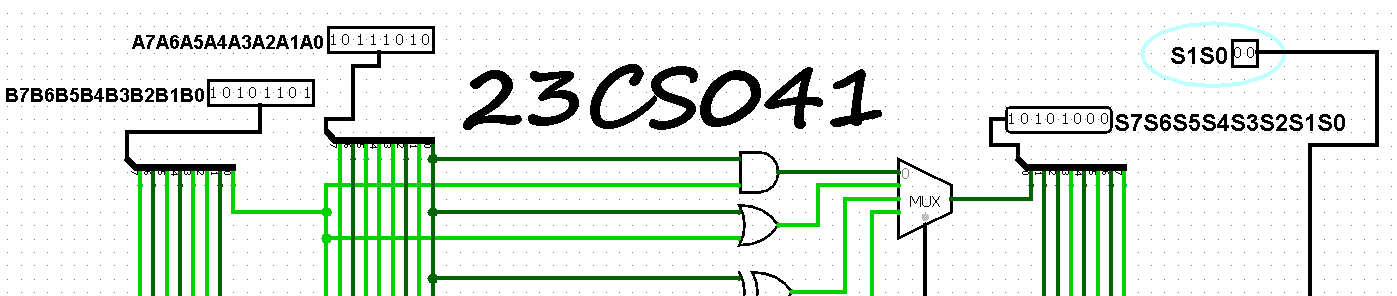
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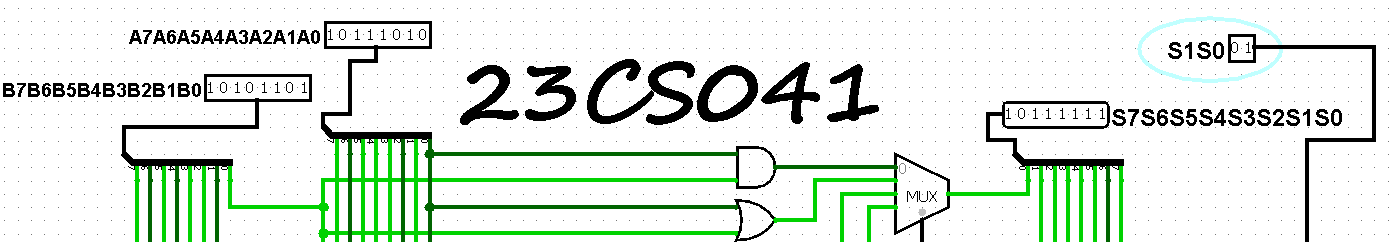


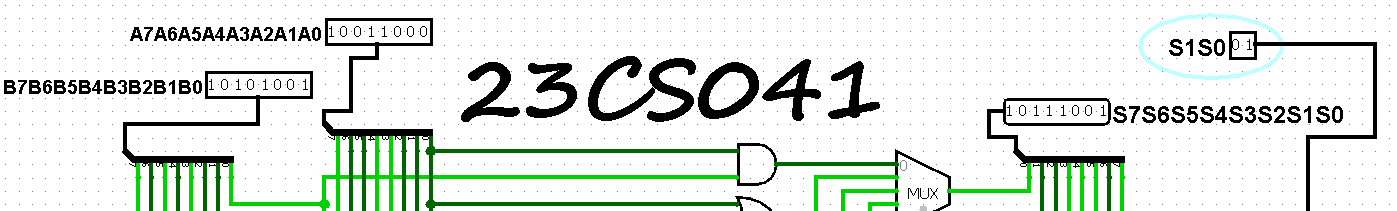
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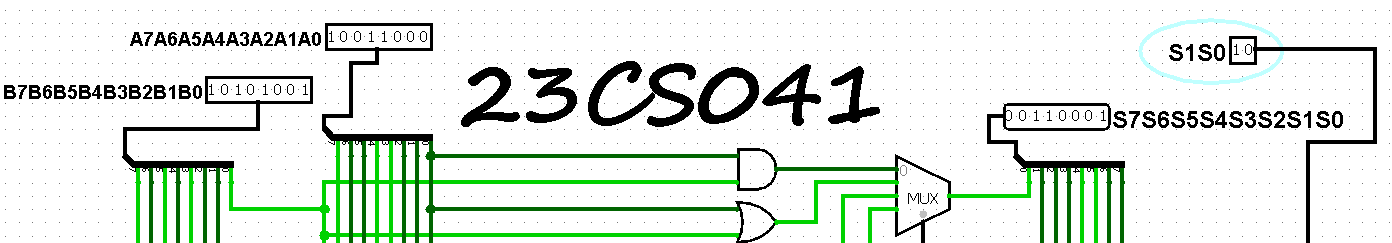
**2) 8 bit logical**

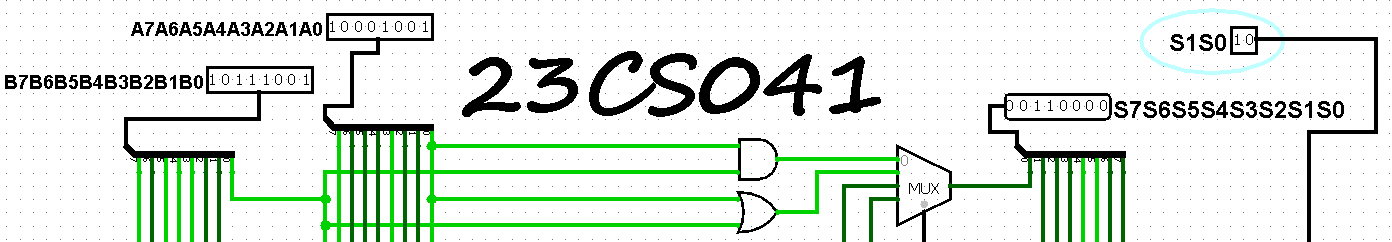
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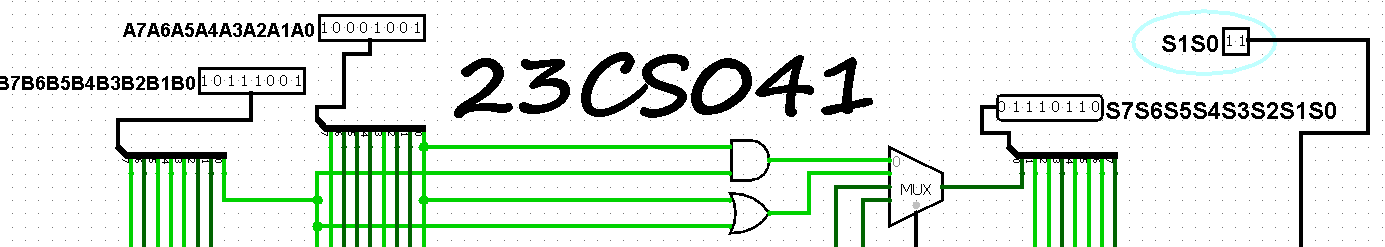
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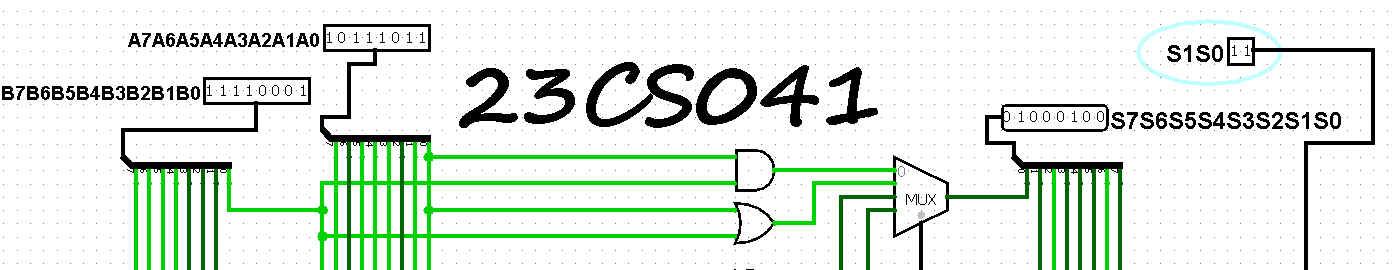
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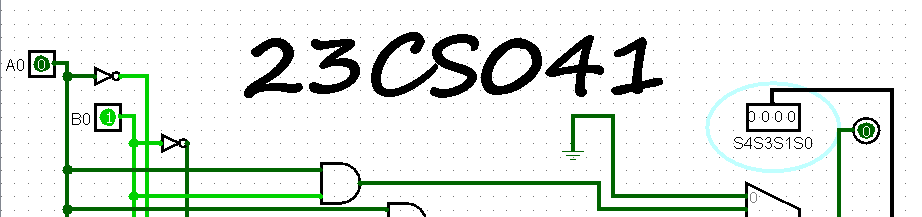
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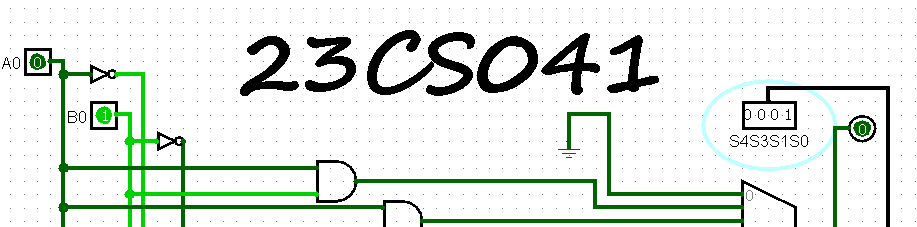
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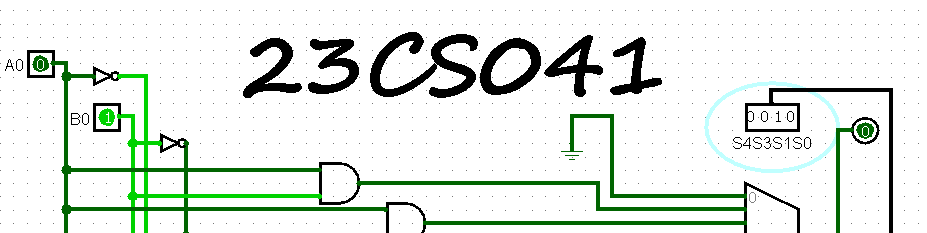
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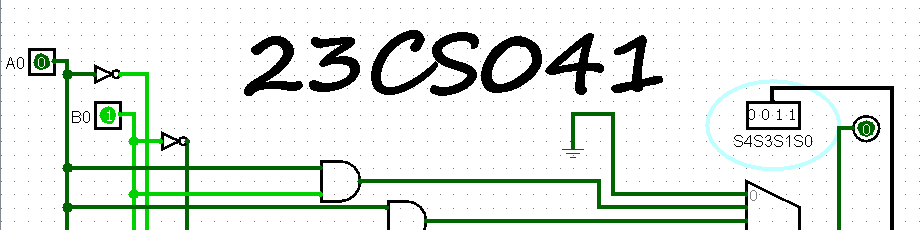
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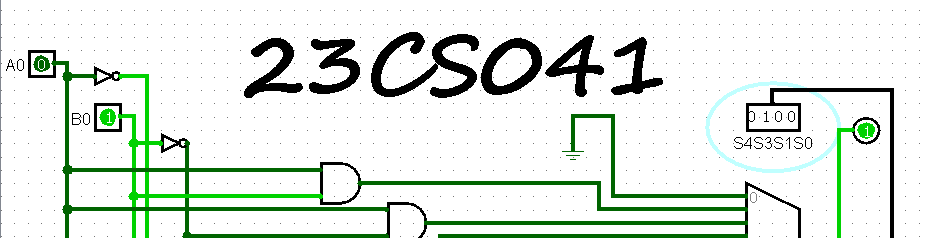
1. **1)** **1-bit**  **16 logical functions**

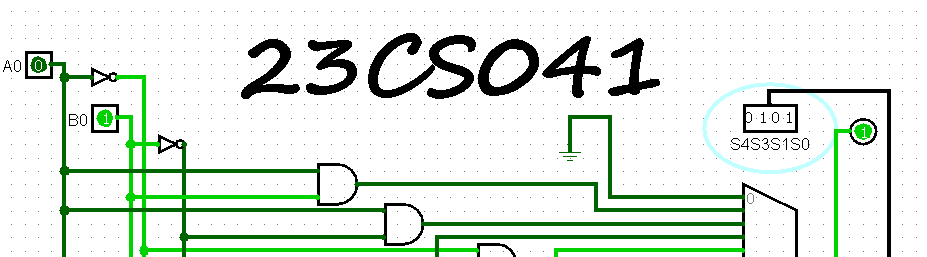
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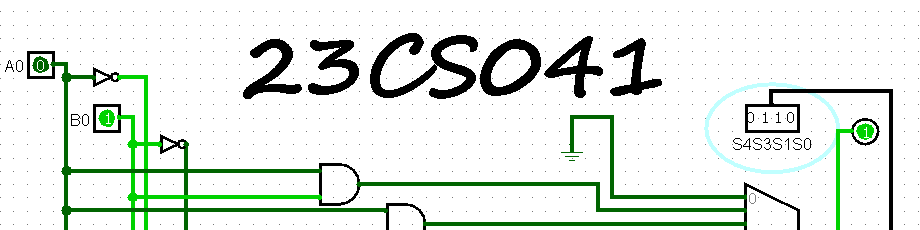
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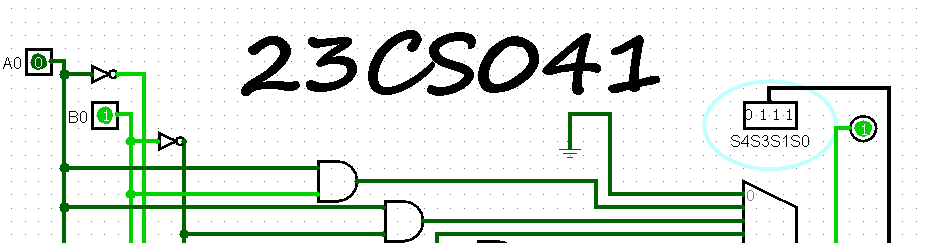
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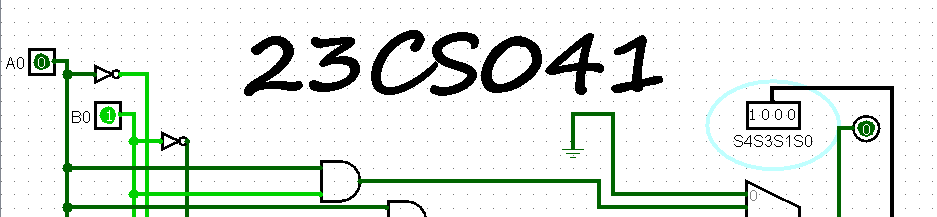
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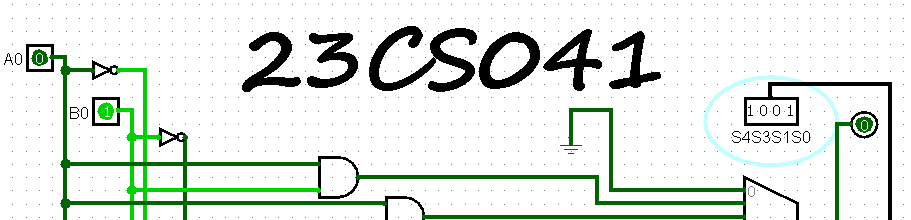
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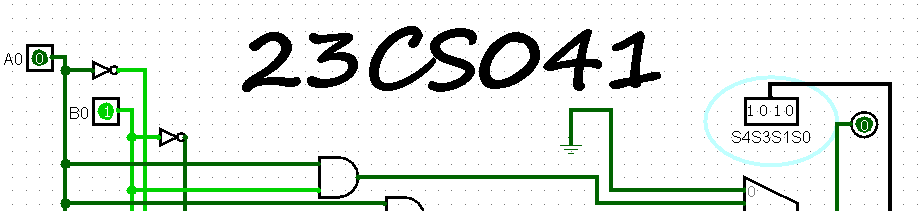
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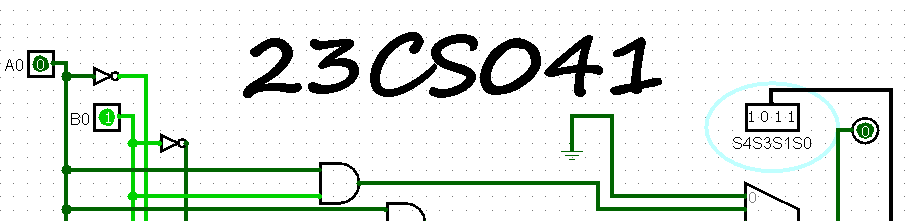
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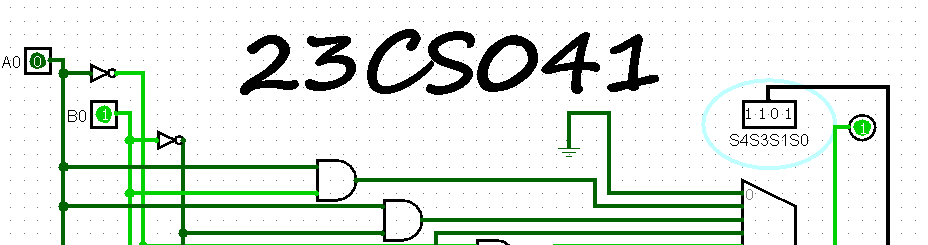
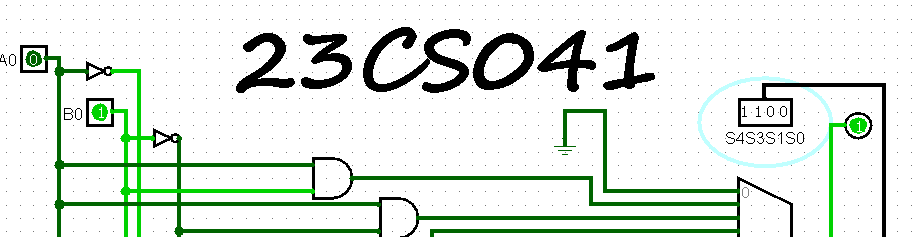
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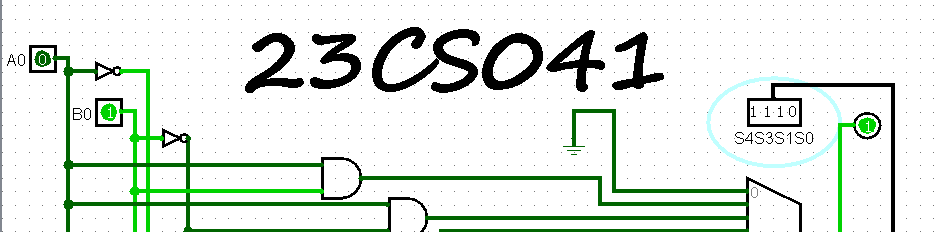
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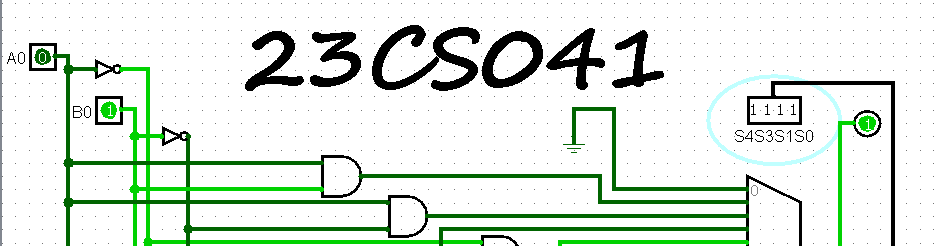
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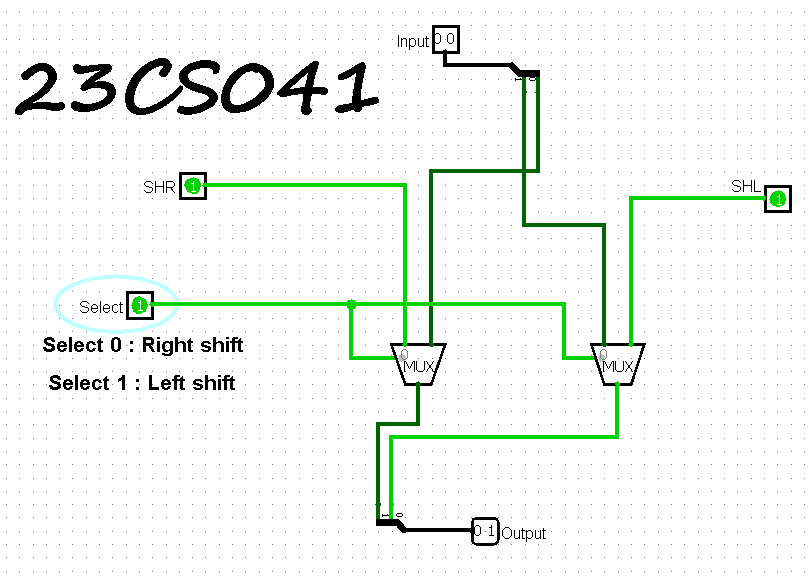
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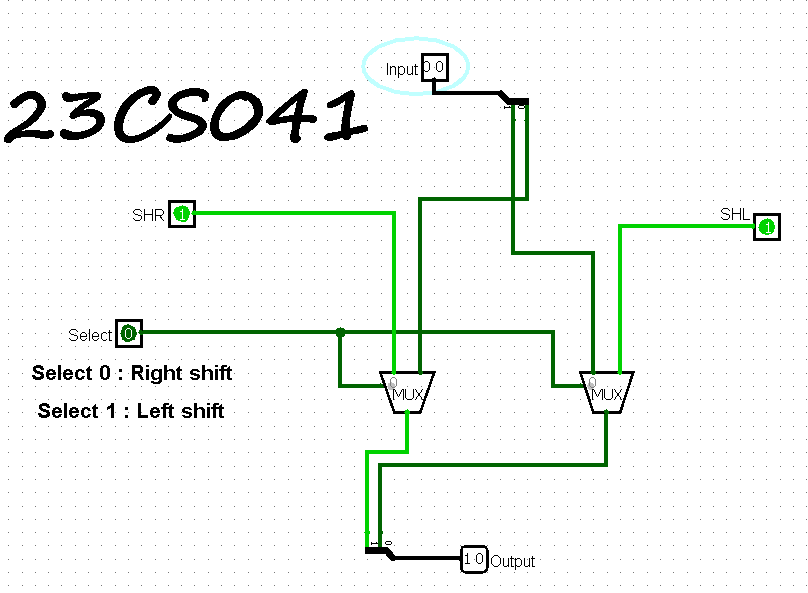
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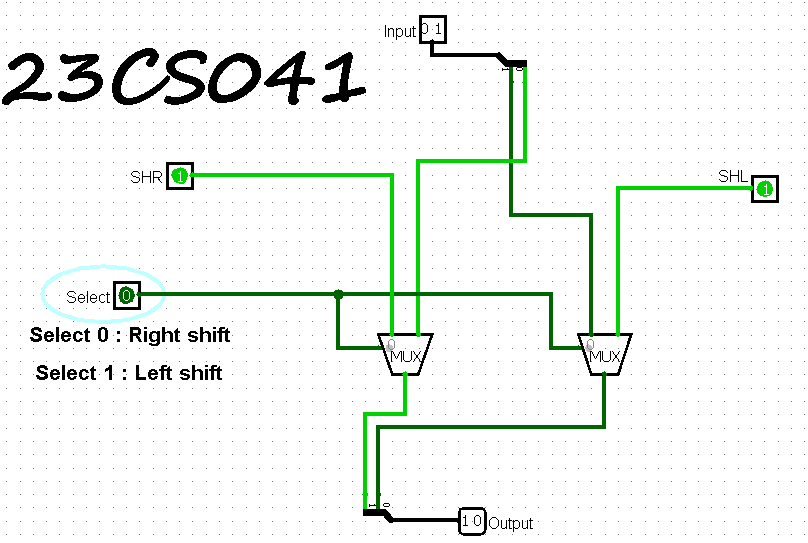
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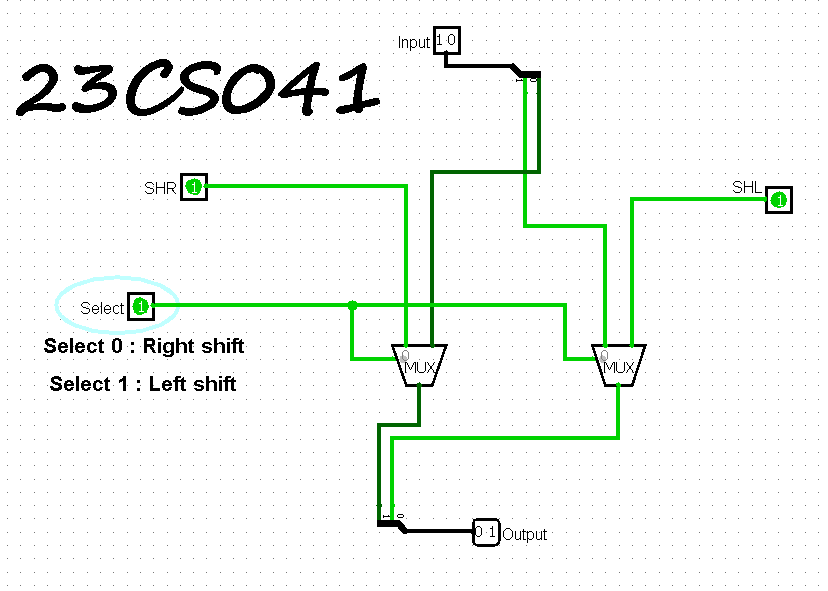
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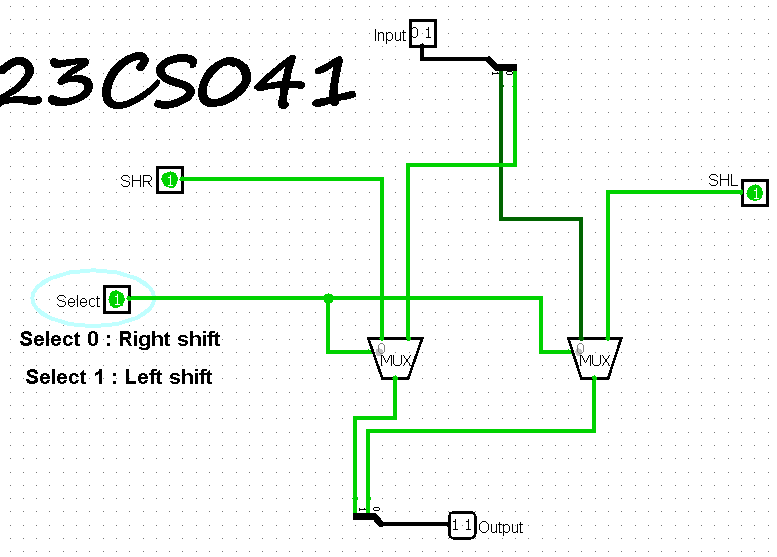
1. **1)** **2-bit bidirectional shifter**

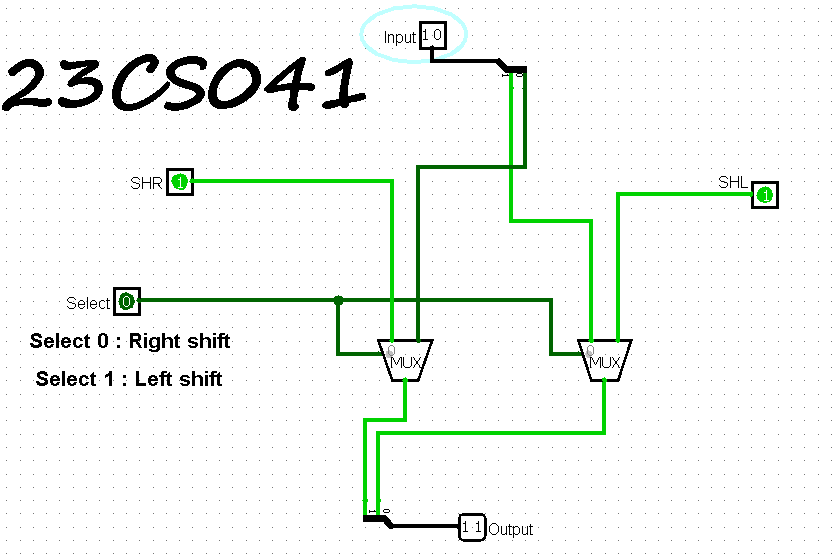


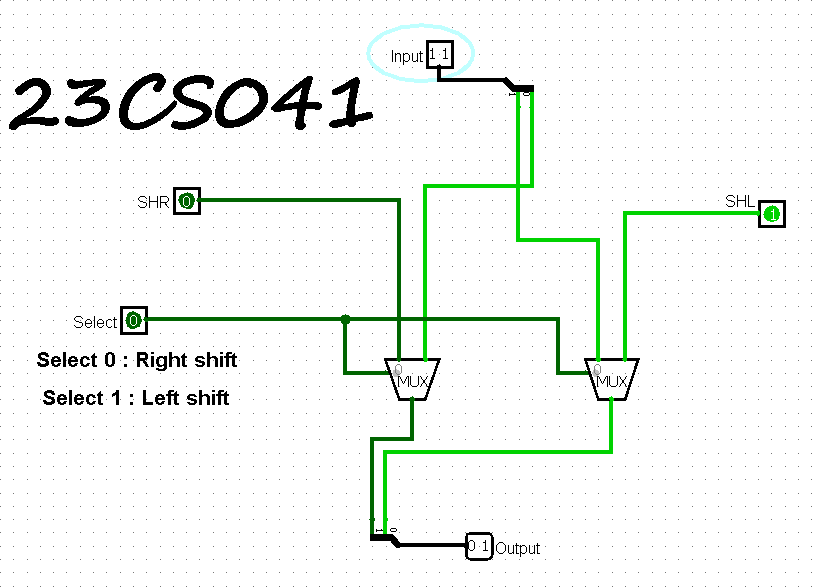
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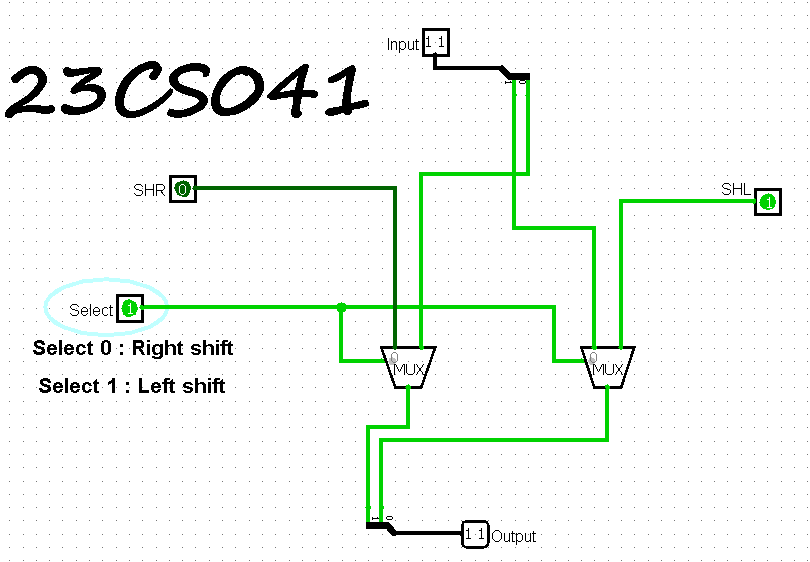
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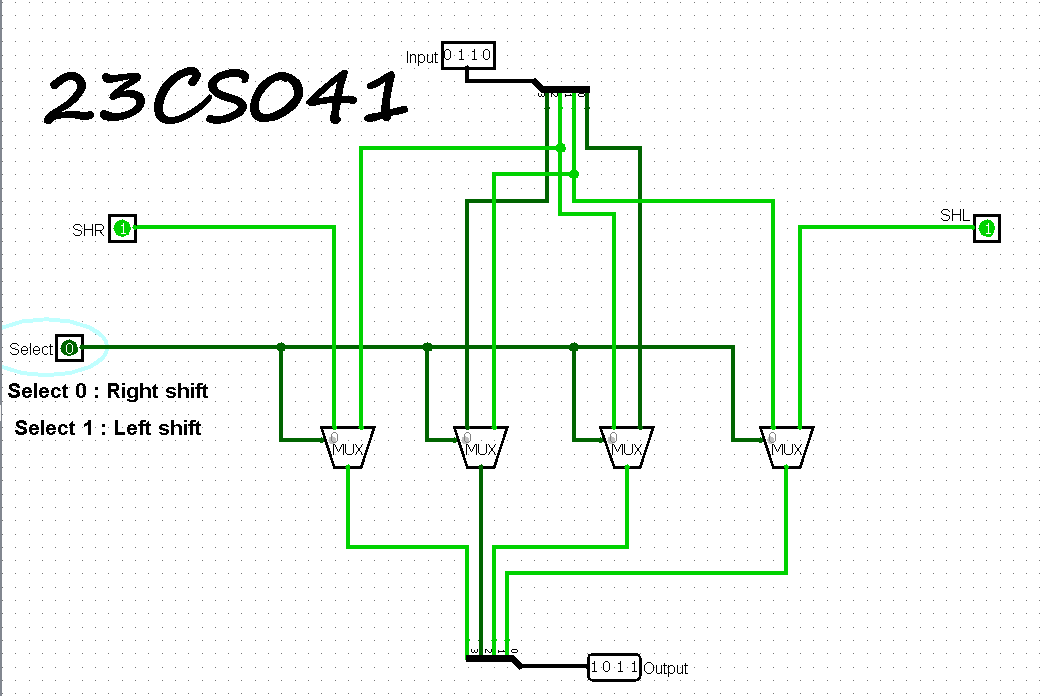


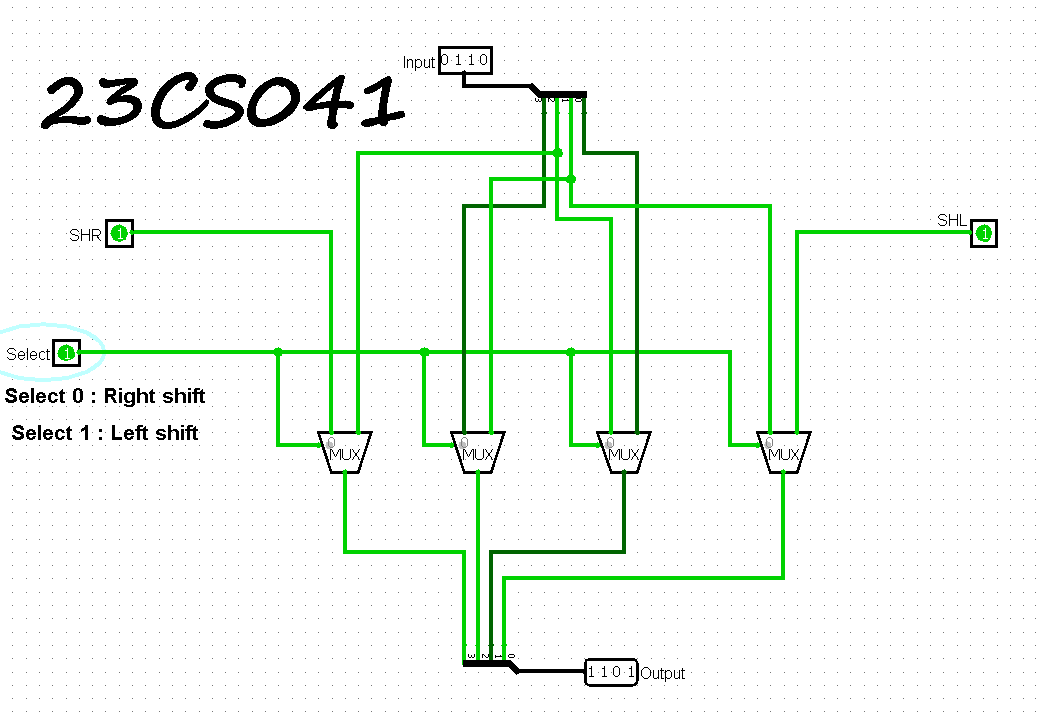
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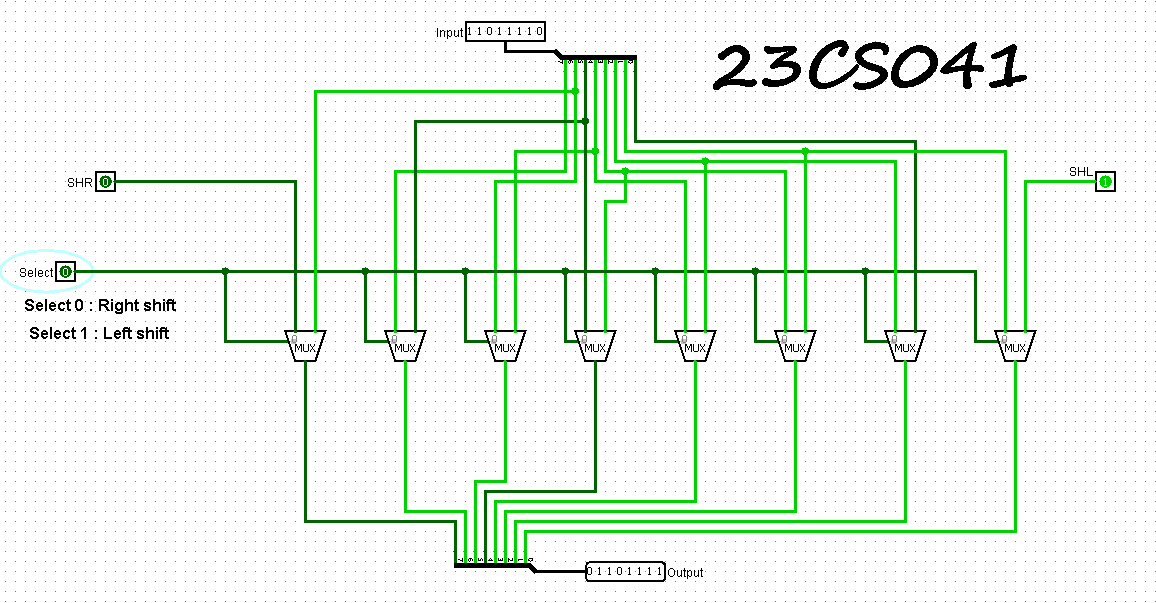


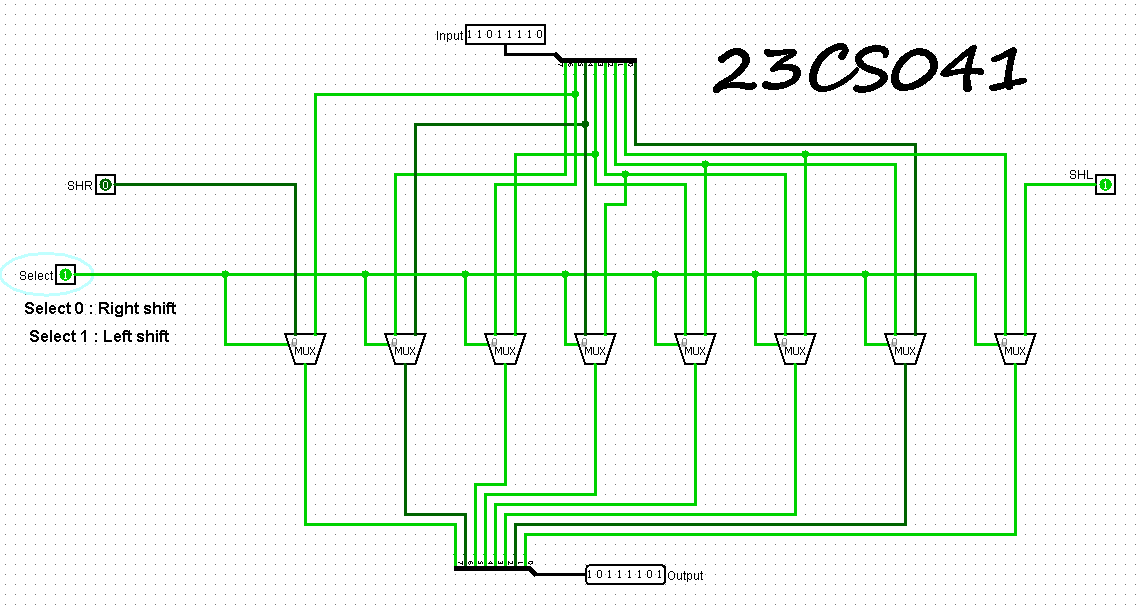
**2)**  **4-bit bidirectional shifter**

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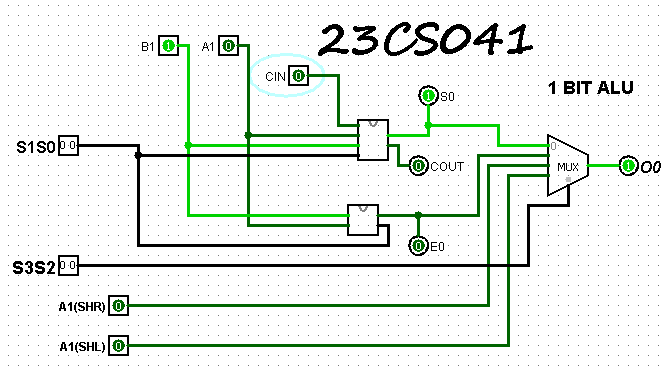
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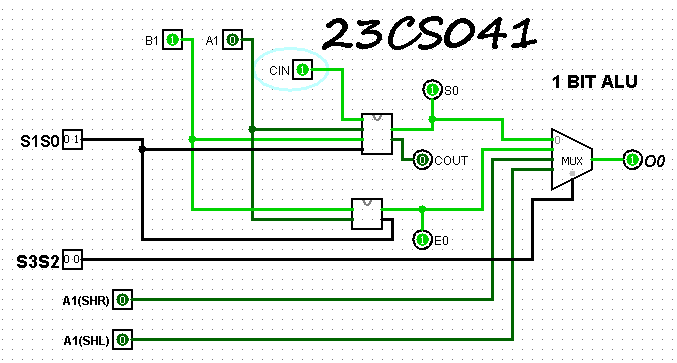
**3)**  **8-bit bidirectional shifter**

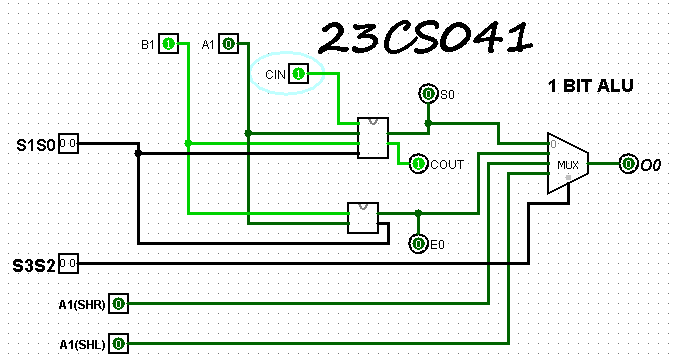
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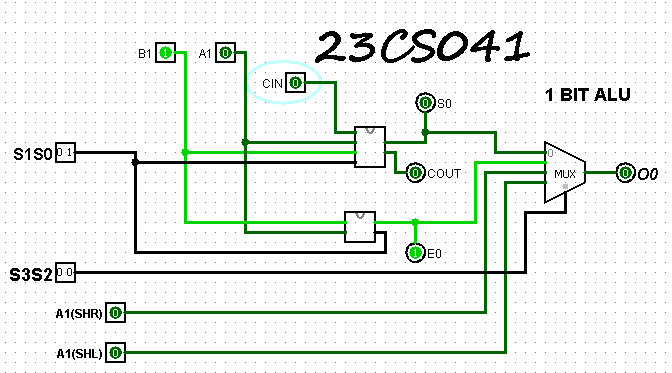
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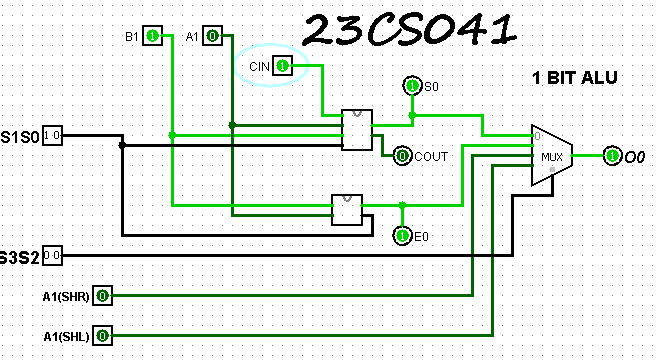
1. **1) 1-bit ALU**

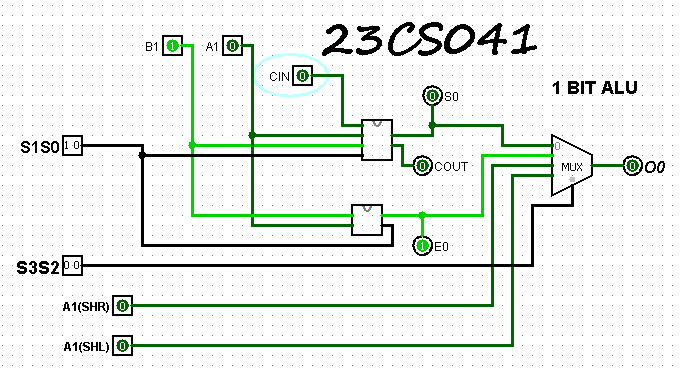
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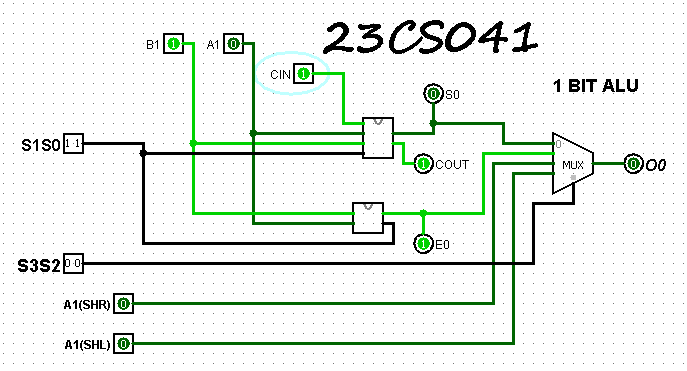


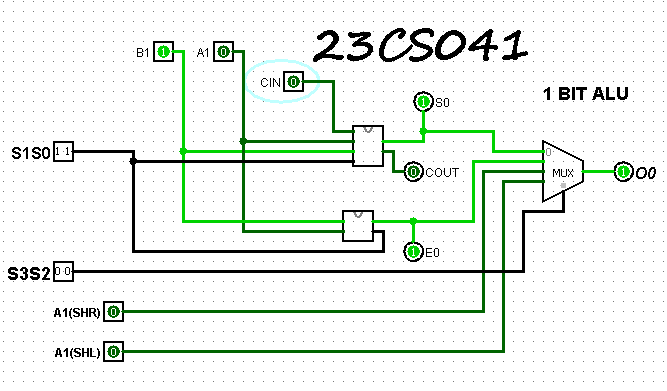


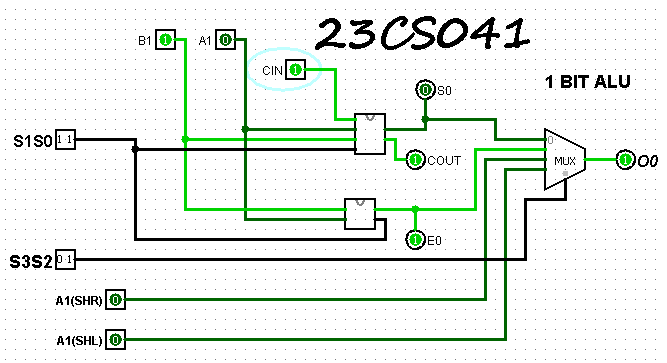
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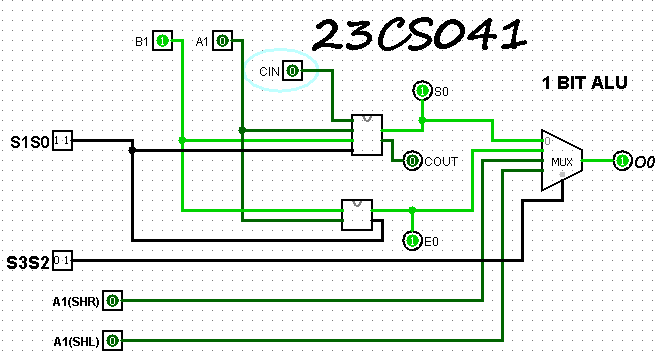


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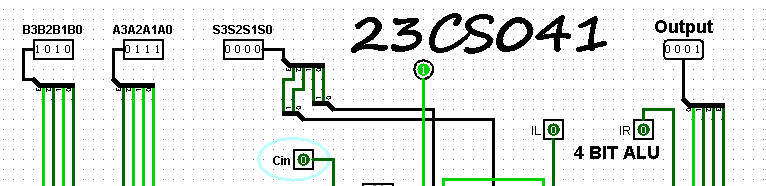


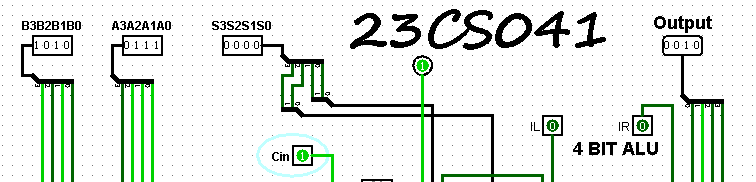
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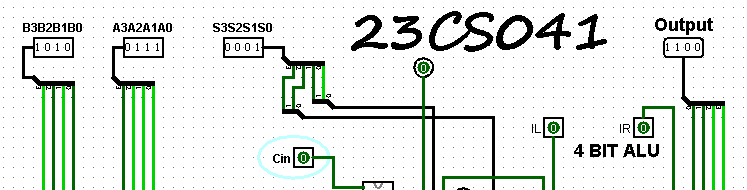


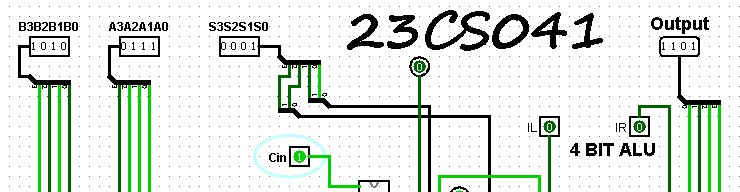
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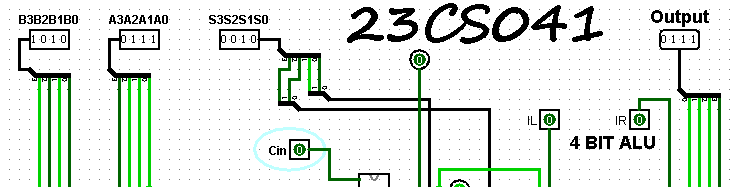
**2) 4-bit ALU**

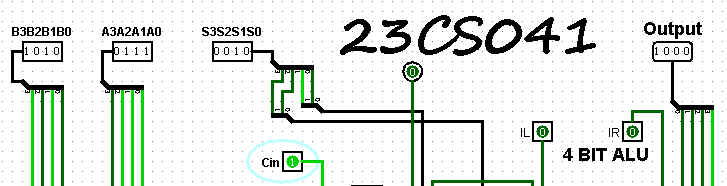
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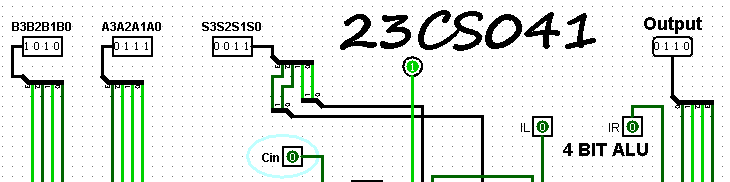
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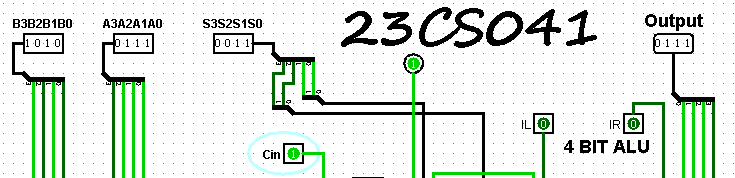
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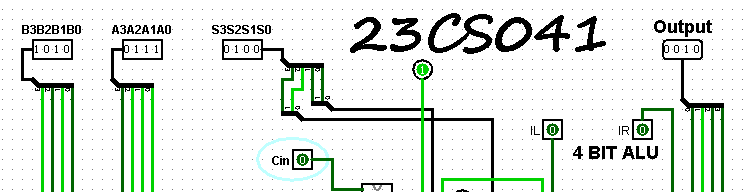
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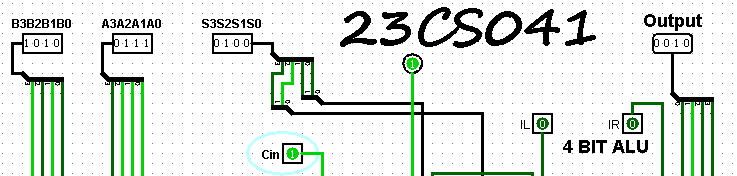
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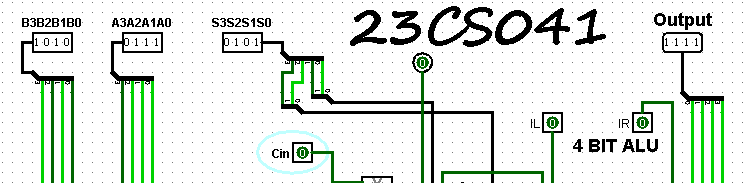
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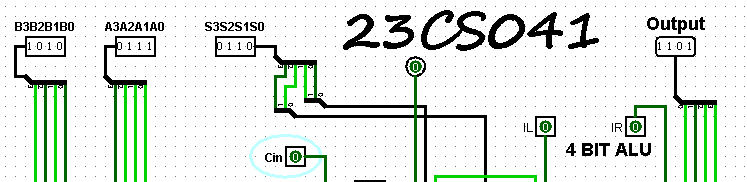
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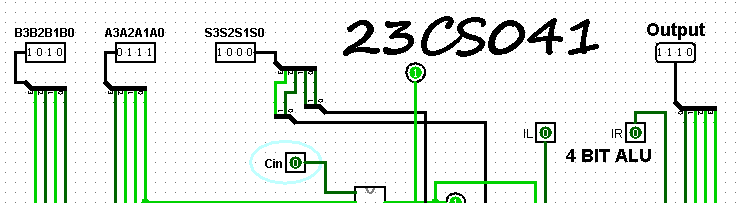
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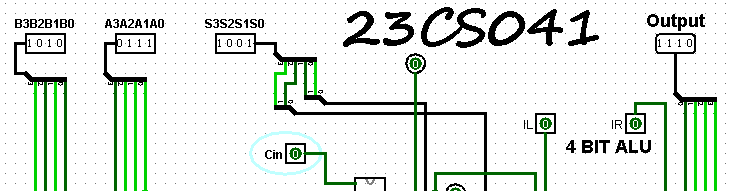
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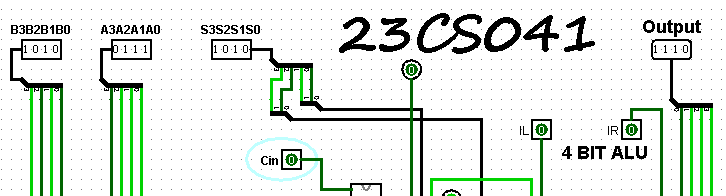
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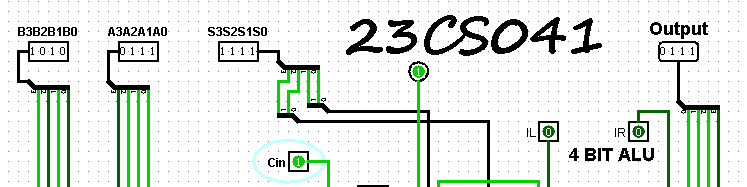
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**CONCLUSION:**