Date:

# EXPERIMENT NO. 5

#### AIM: Implement a common bus system with ALU, 8 registers and 1 memory unit

#### with necessary control signals.

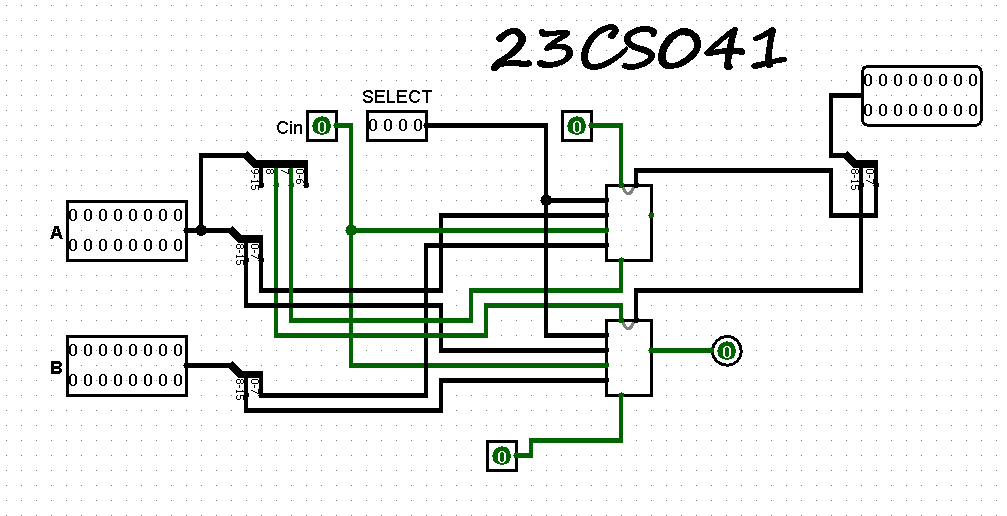
#### OBJECTIVES:

#### Implement 16-bit ALU that is suitable for common bus system

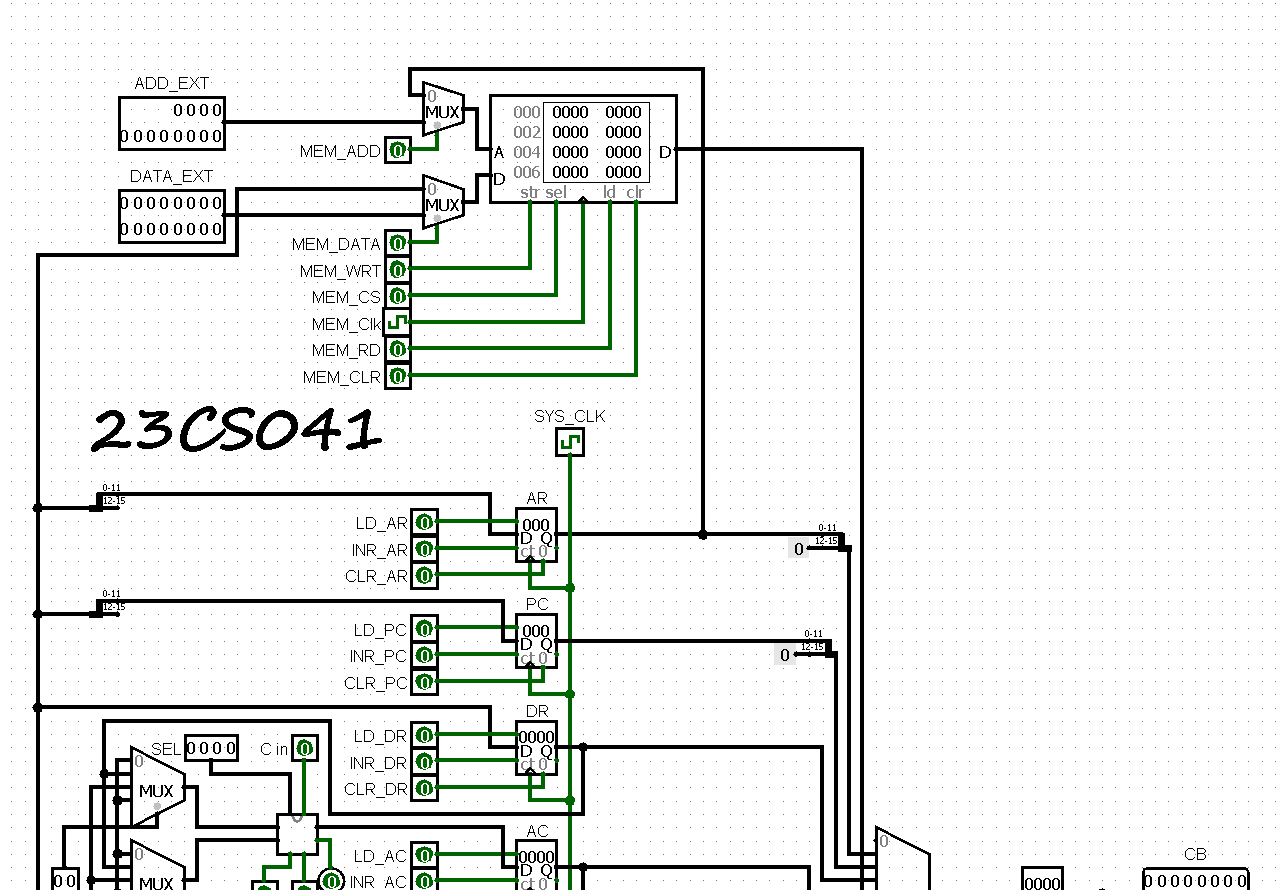
#### Implement 16-bit common bus system with ALU, 8 registers and 1 memory unit

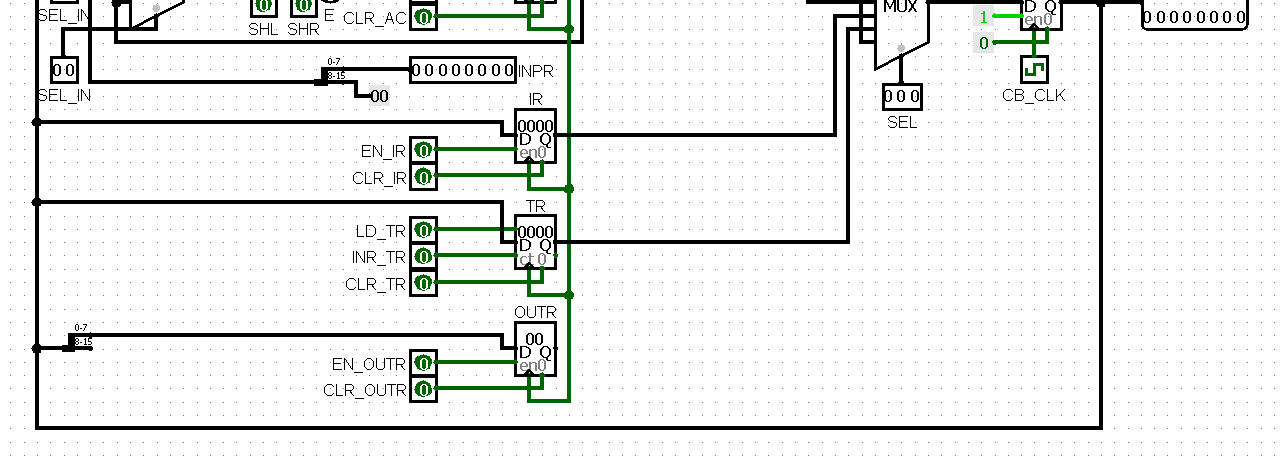
**CIRCUITS:**

**i.**

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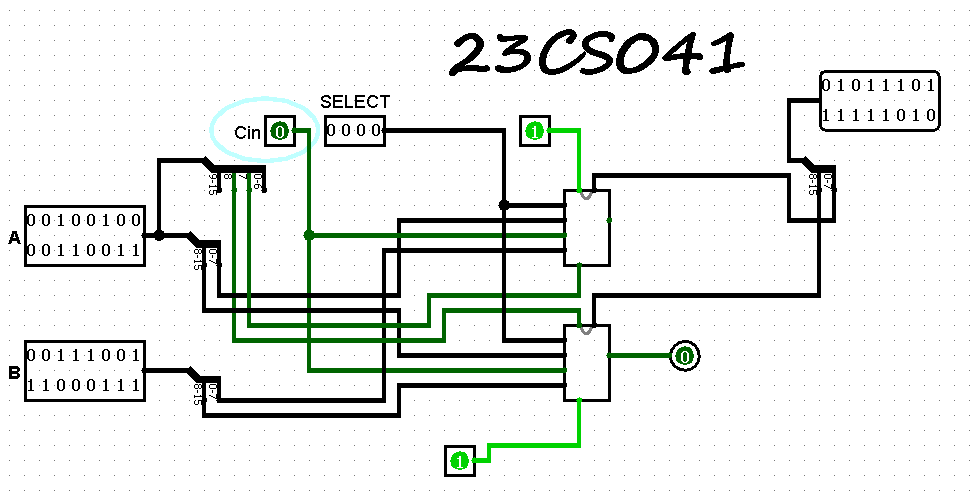
**ii.**

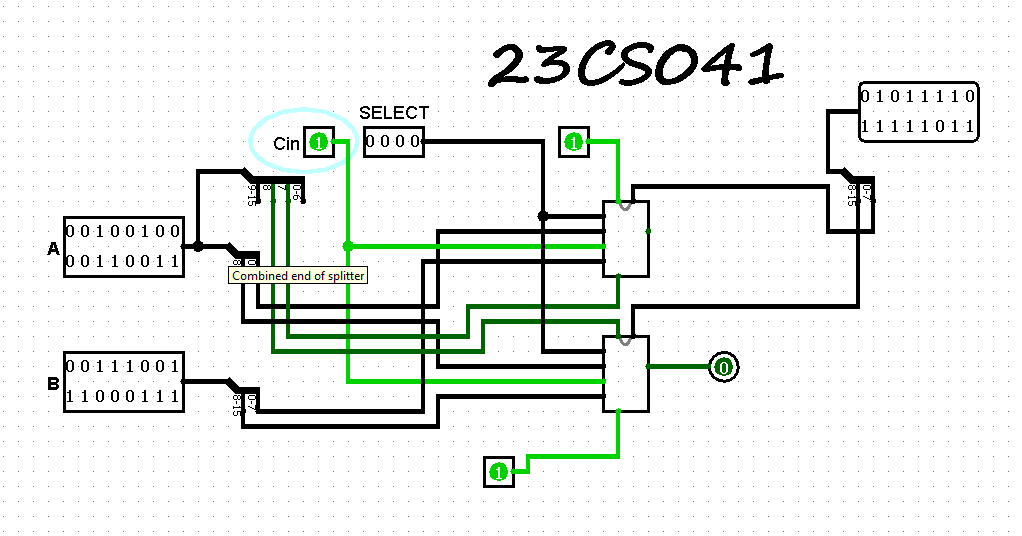
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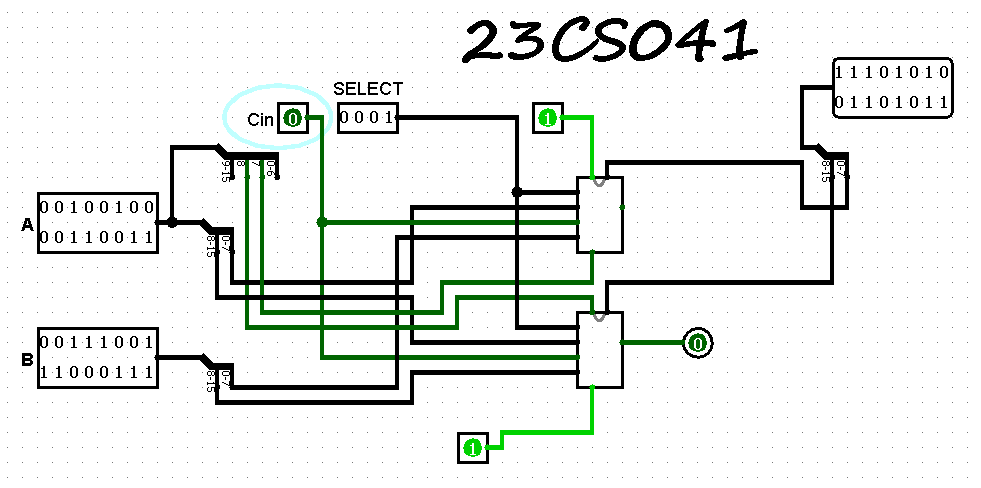
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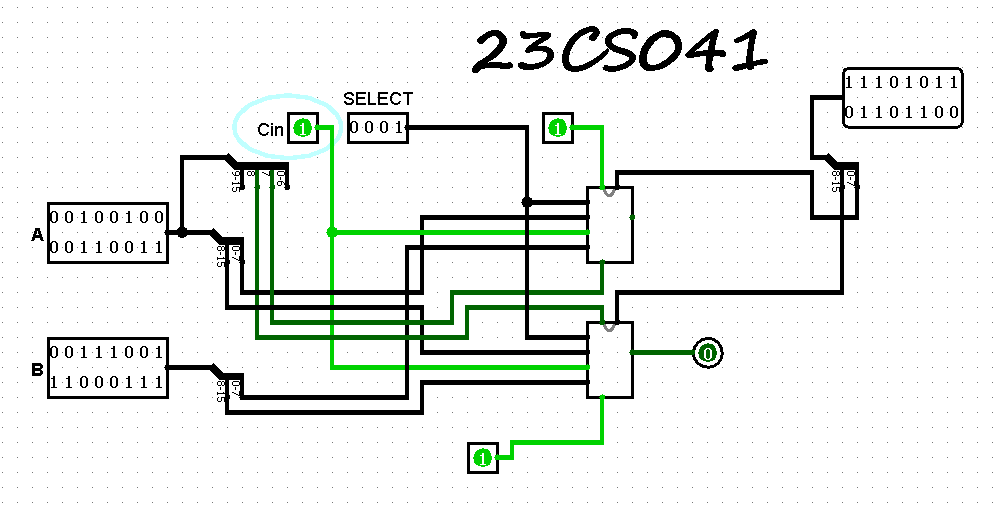
**OUTPUTS:**

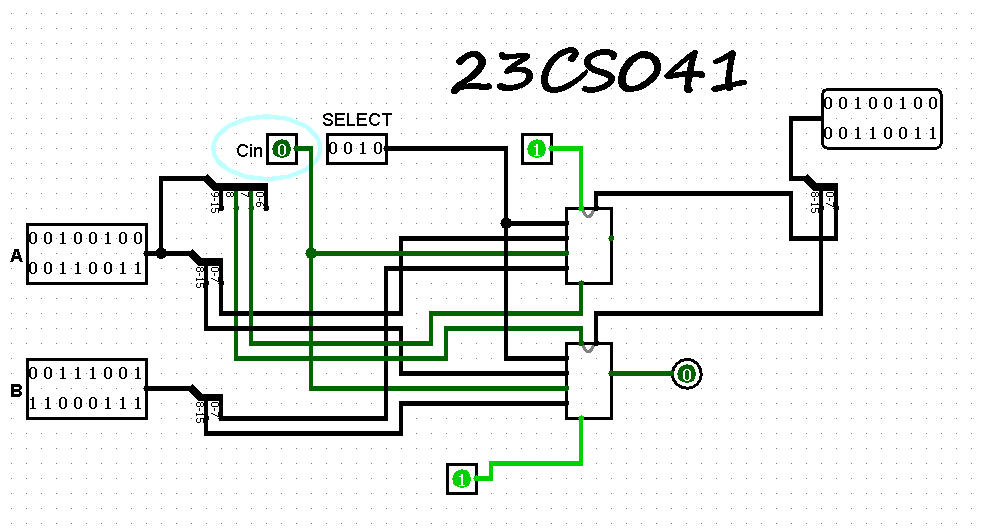
**i.**

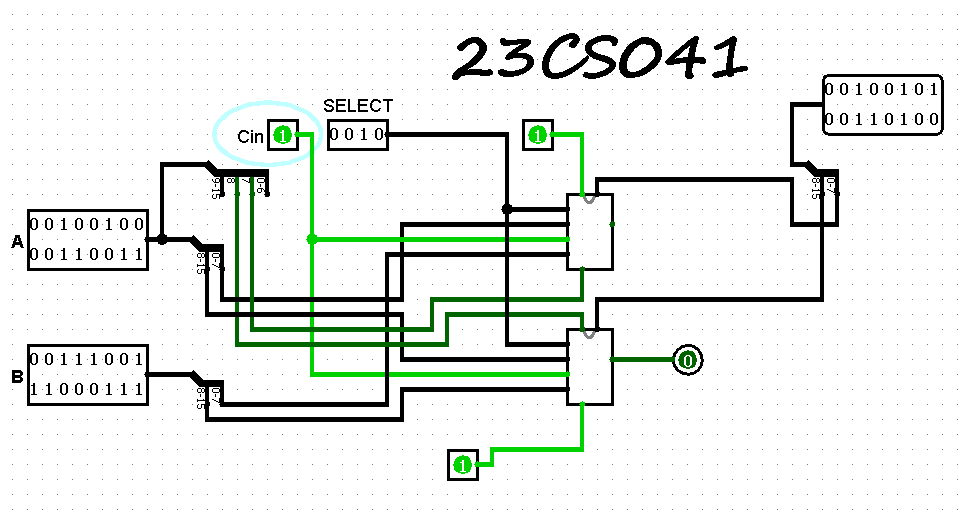
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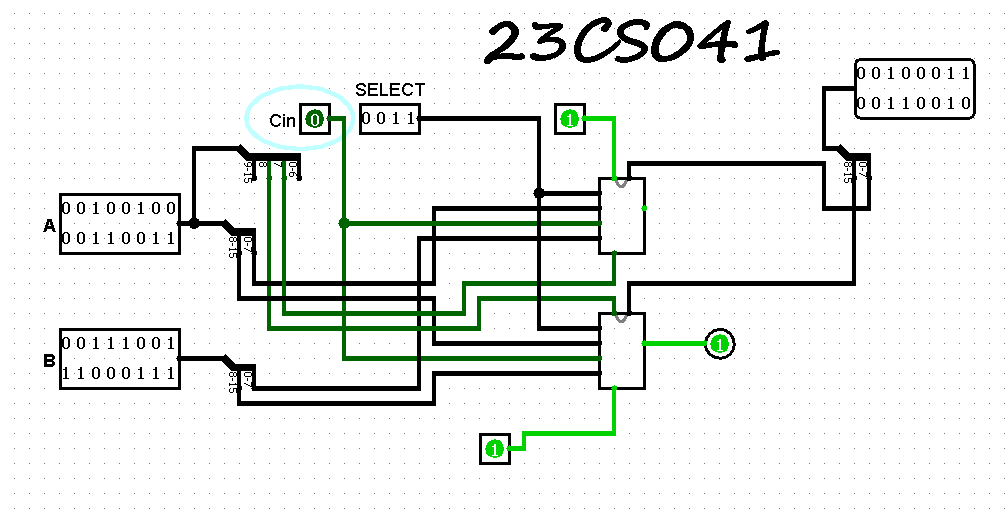
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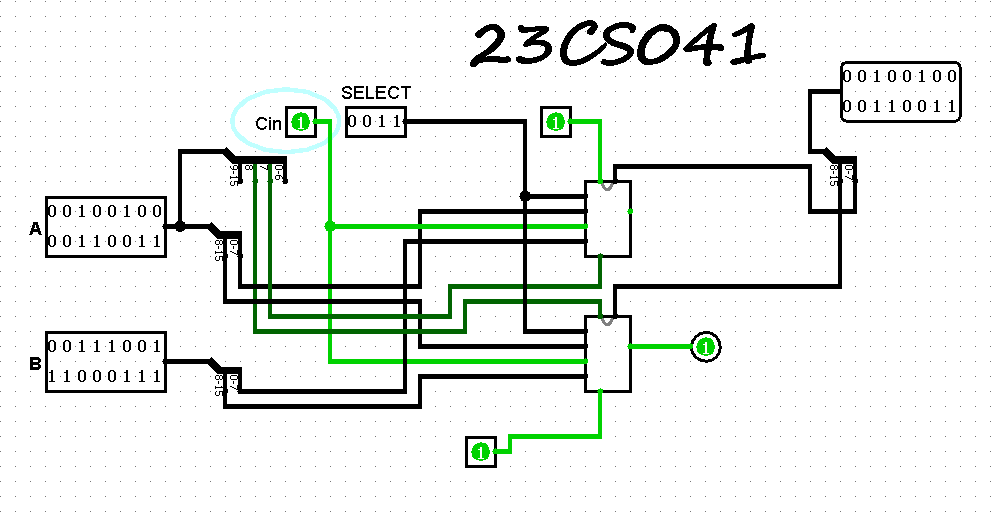
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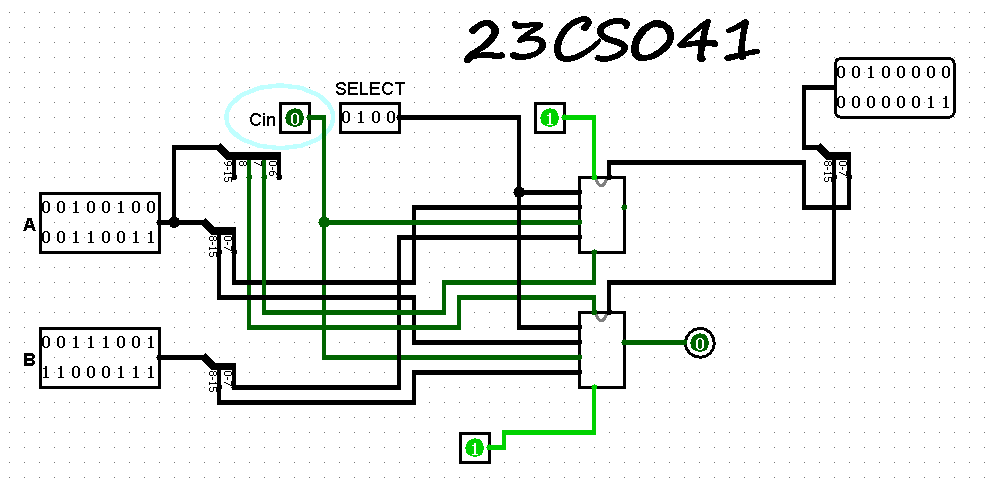
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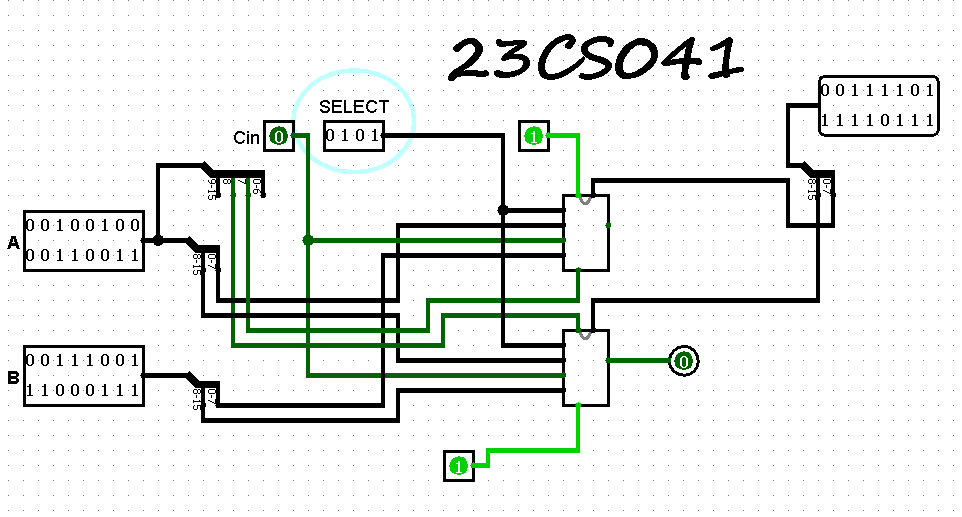
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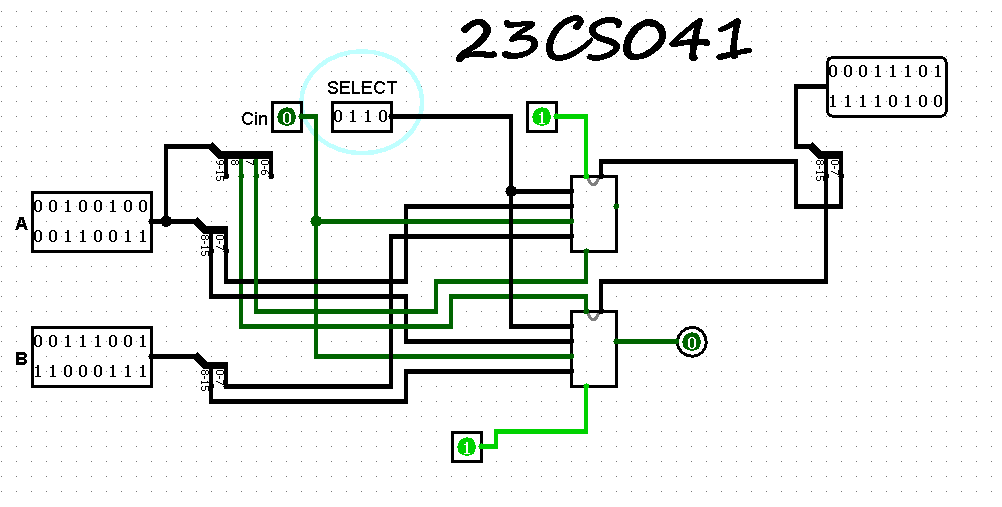
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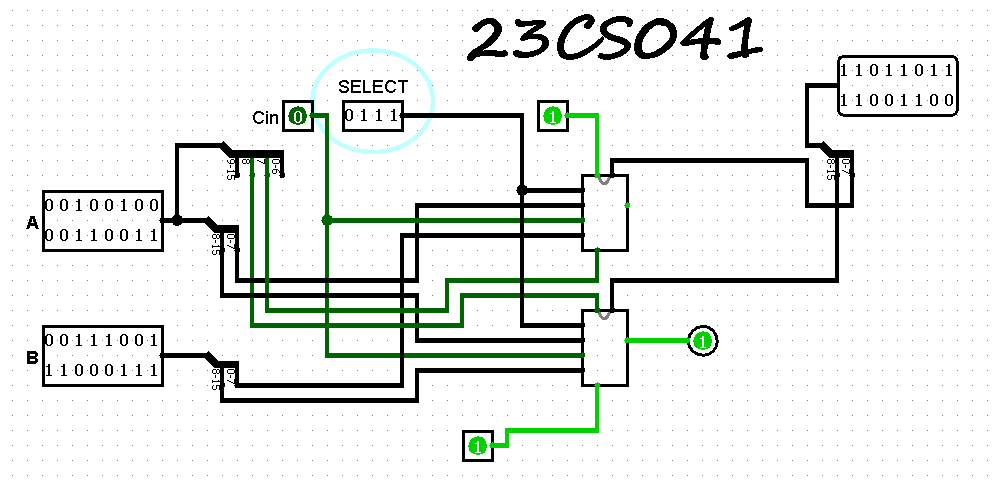
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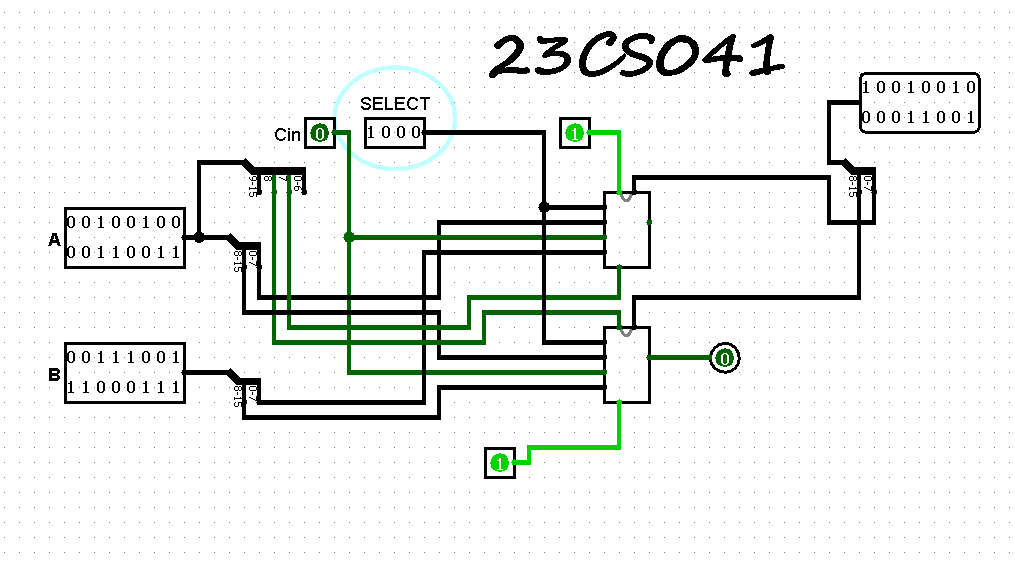
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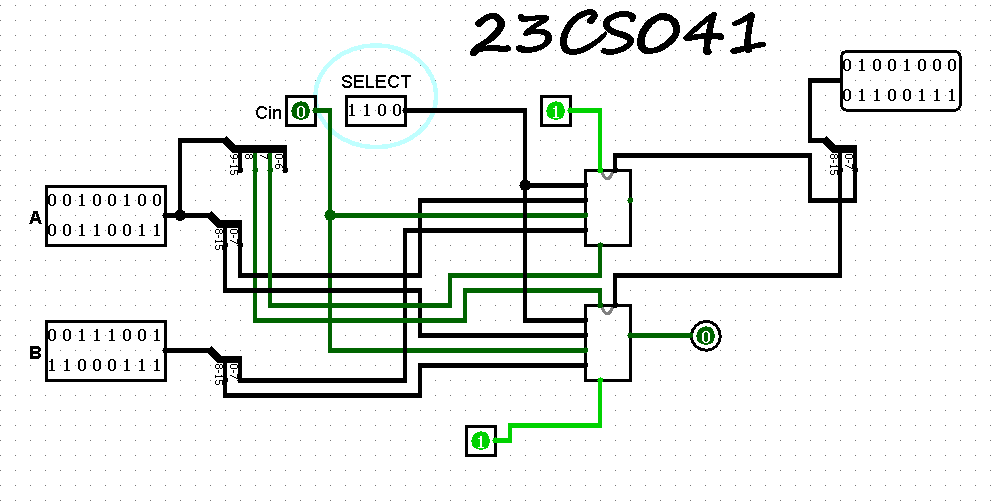
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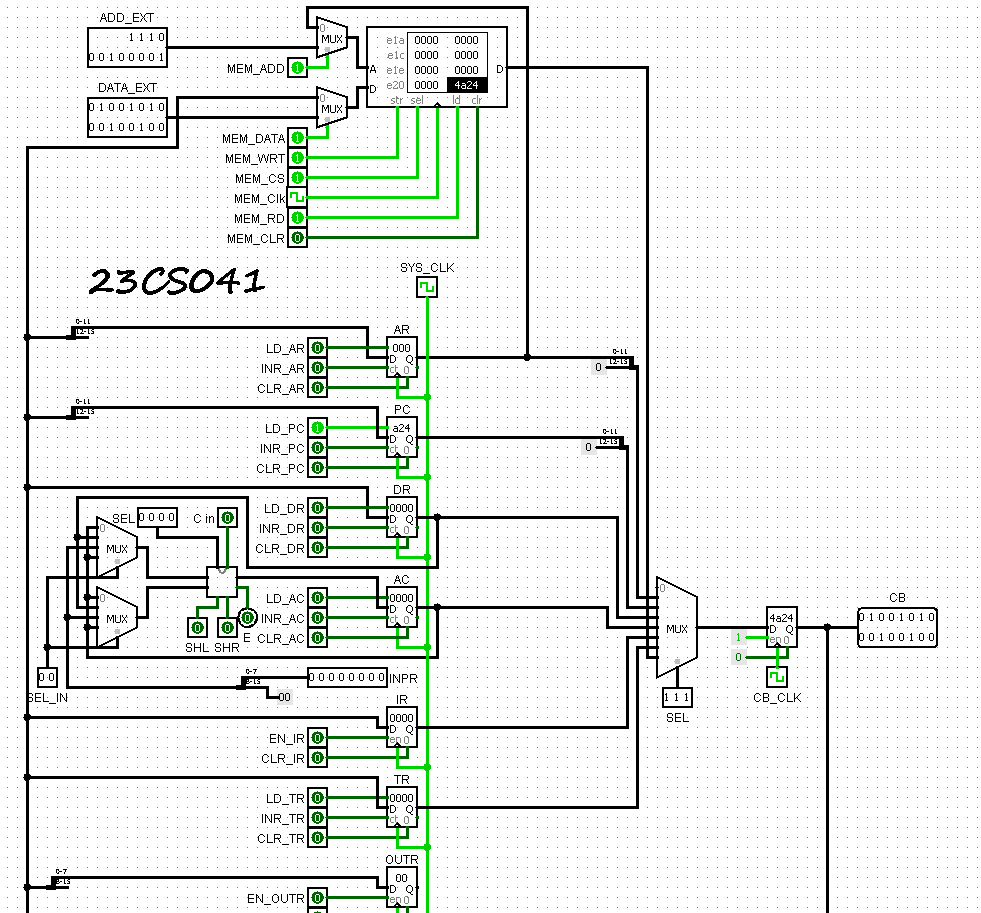
**\**

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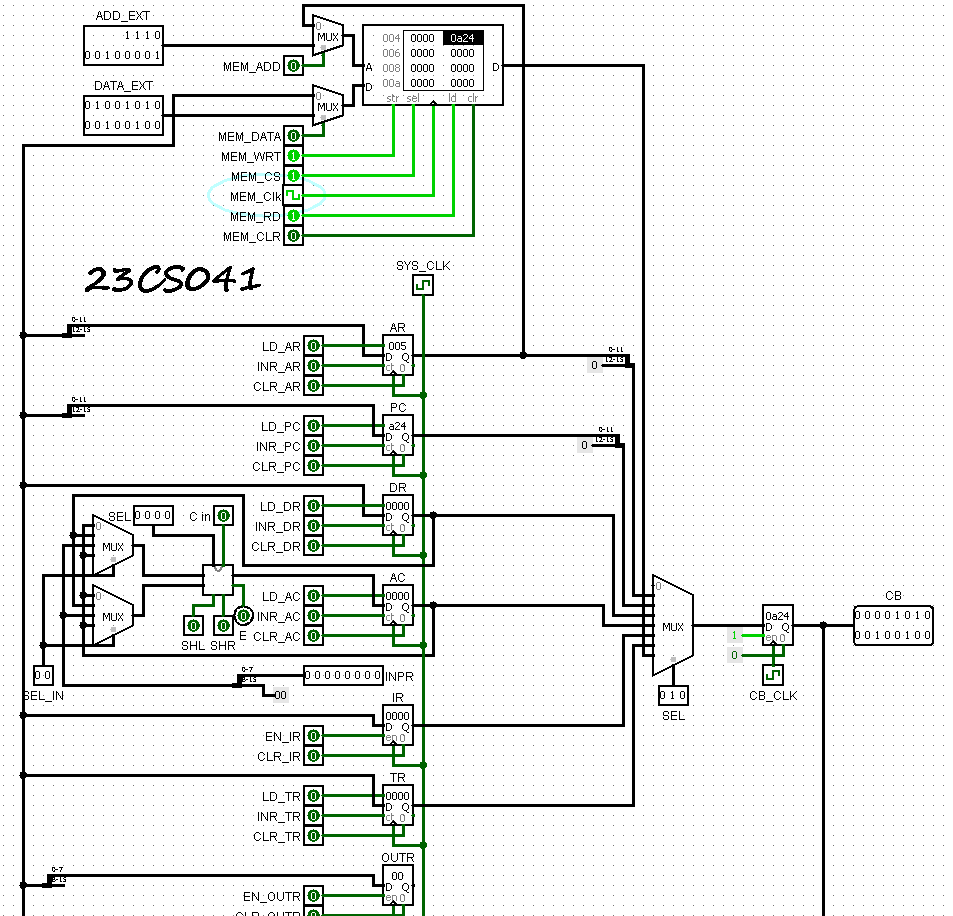
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**ii.**

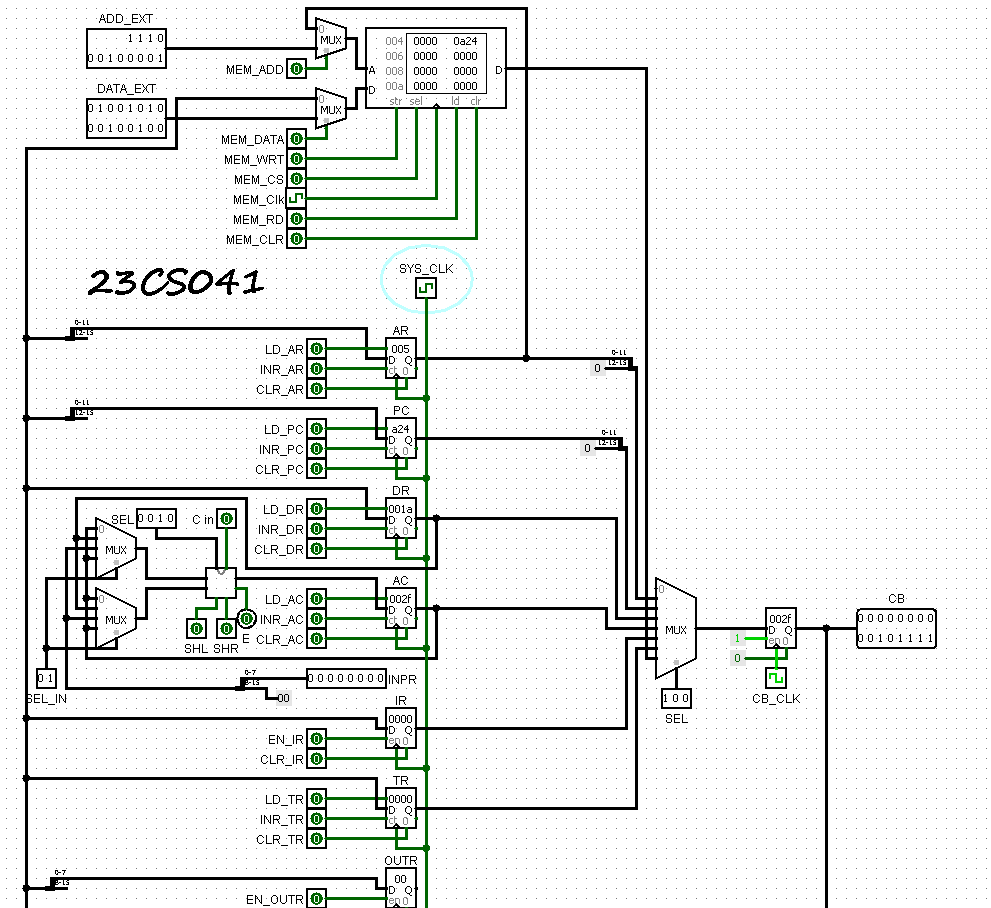
**PC<-MEM[AR]**

****

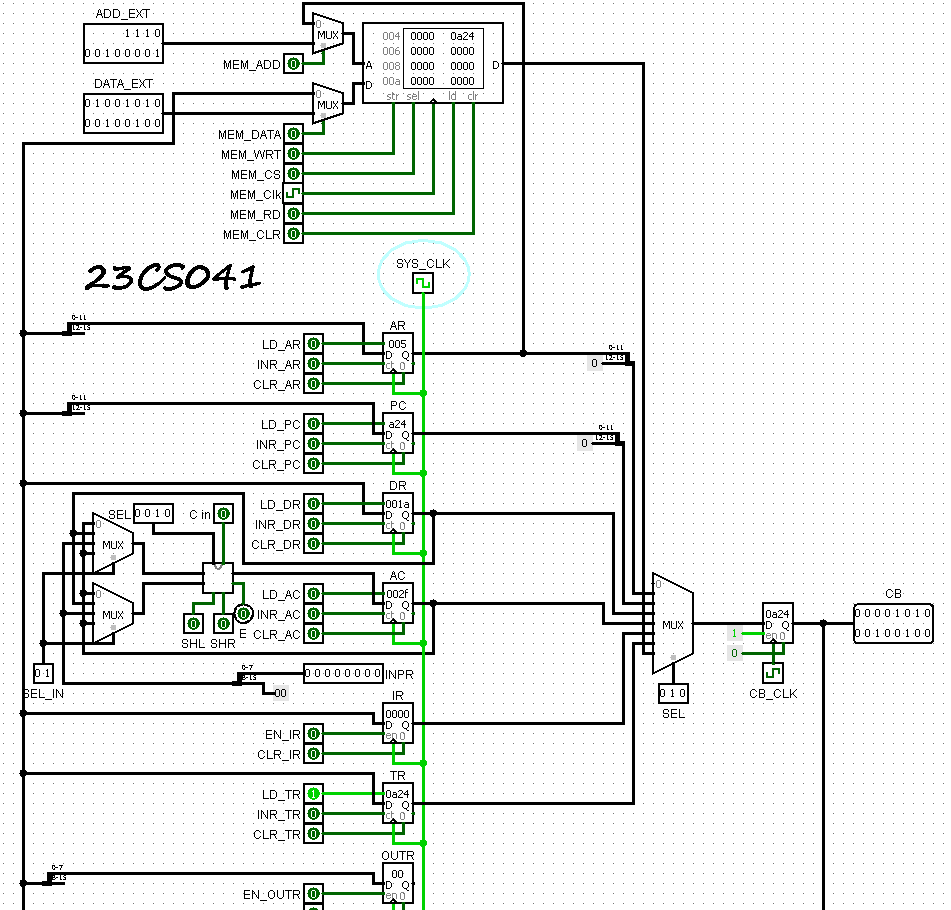
**CB<-PC**

****

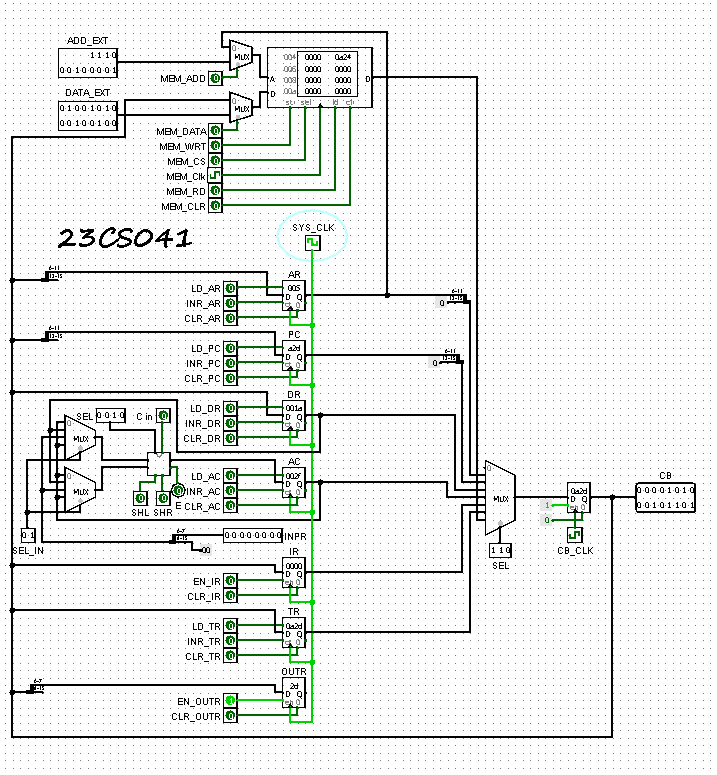
**CB<-AC**

****

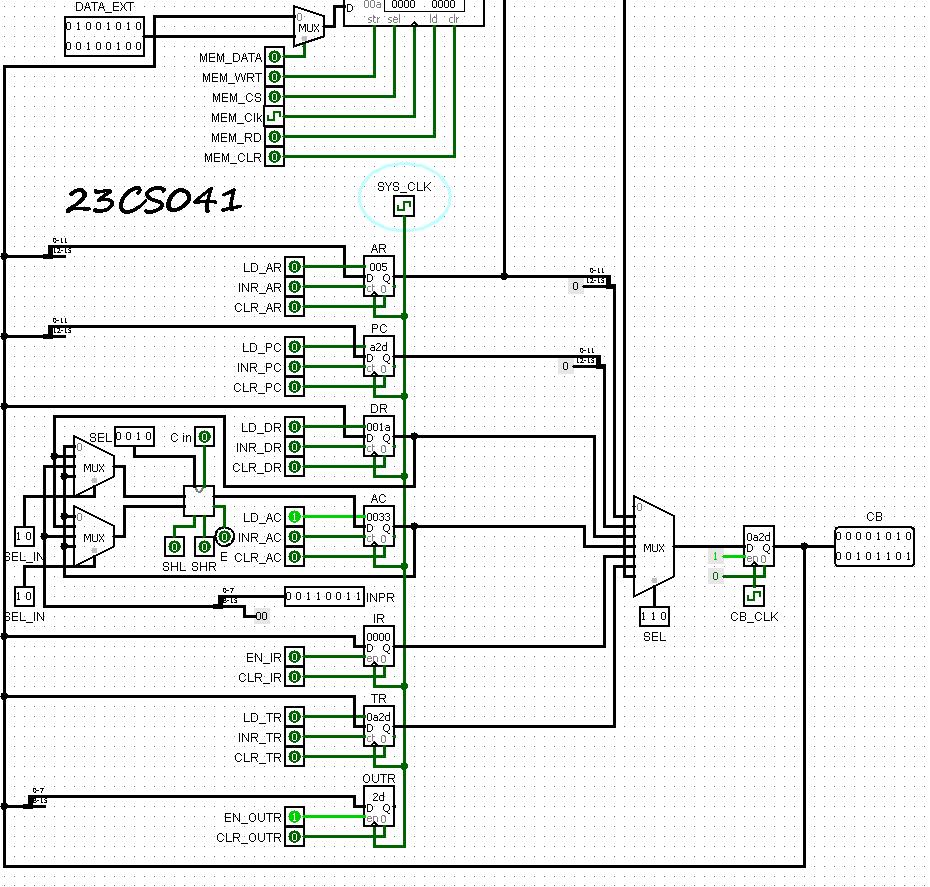
**CB<-TR**

****

**OUTR<-CB**

****

**AC<-INPR**

****

**CONCLUSION:**