Design Project #4: MOSFET XOR Gate

Electronic Devices and Circuits - 2EI4

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Circuit Schematic

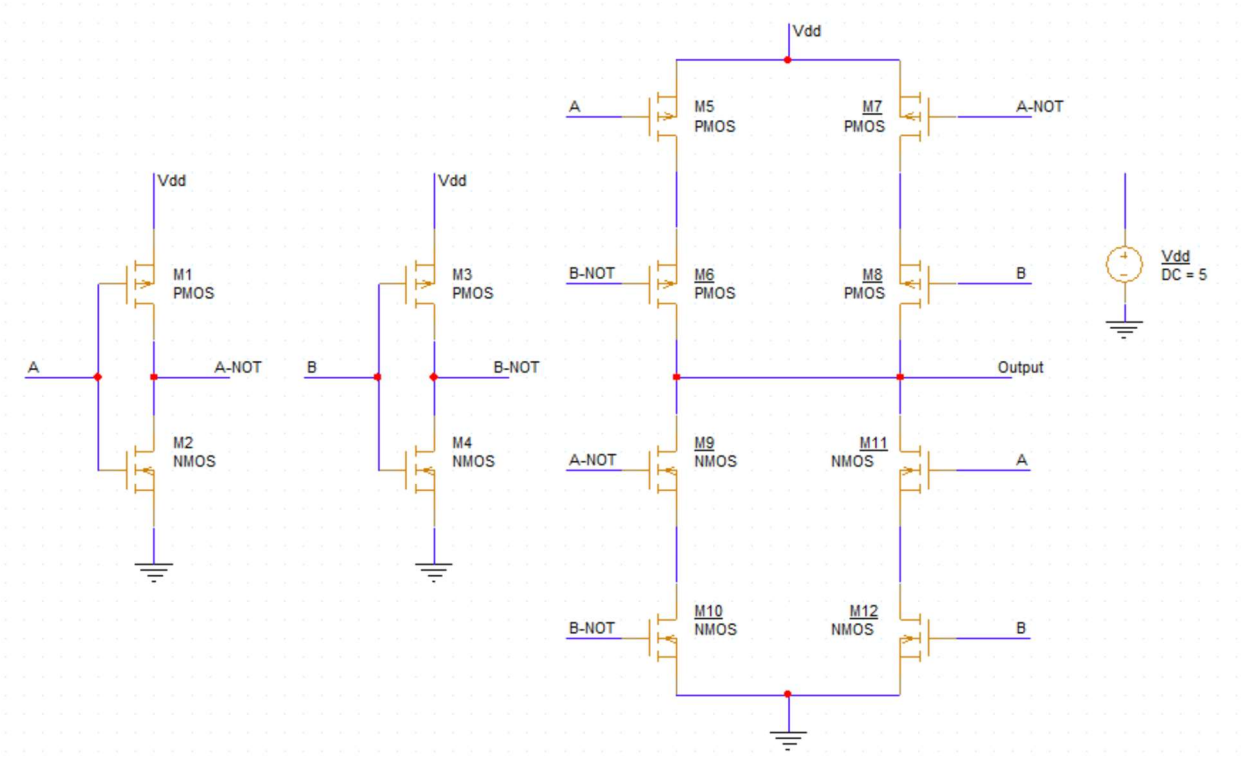

Figure 1: Circuit Schematic

Ideal Sizing

In CMOS design, the ideal sizing ratio between the PMOS and NMOS transistors is used to compensate for the difference in carrier mobility between the two. Electrons in NMOS transistors move faster than the holes in PMOS transistors, specifically with a 2.5 ratio. In order to equalize the circuit, the PMOS transistors need to be larger in size.

We know that $\left(\frac{W}{L}\right)_{PMOS} = \frac{5}{1}$ and $\left(\frac{W}{L}\right)_{NMOS} = \frac{2}{1}$. Therefore, the ratio of PMOS to NMOS size is $\frac{5}{2}$. This means each PMOS transistor should ideally be 2.5 times larger than the NMOS.

Implementation Feasibility

It is indeed possible to implement this ideal sizing within the circuit. Looking at the schematic, it can be seen that the longest past from Vdd to ground goes through 2 PMOS and 2 NMOS transistors. This symmetry aligns with our ideal sizing assumption and supports a $\frac{5}{2}$ sizing ratio. Being able to implement the ideal sizing will balance the delay

within the pull down and pull up networks, giving symmetrical rise and fall times and reduces the chance of outputs not matching XOR logic.

Physical Circuit

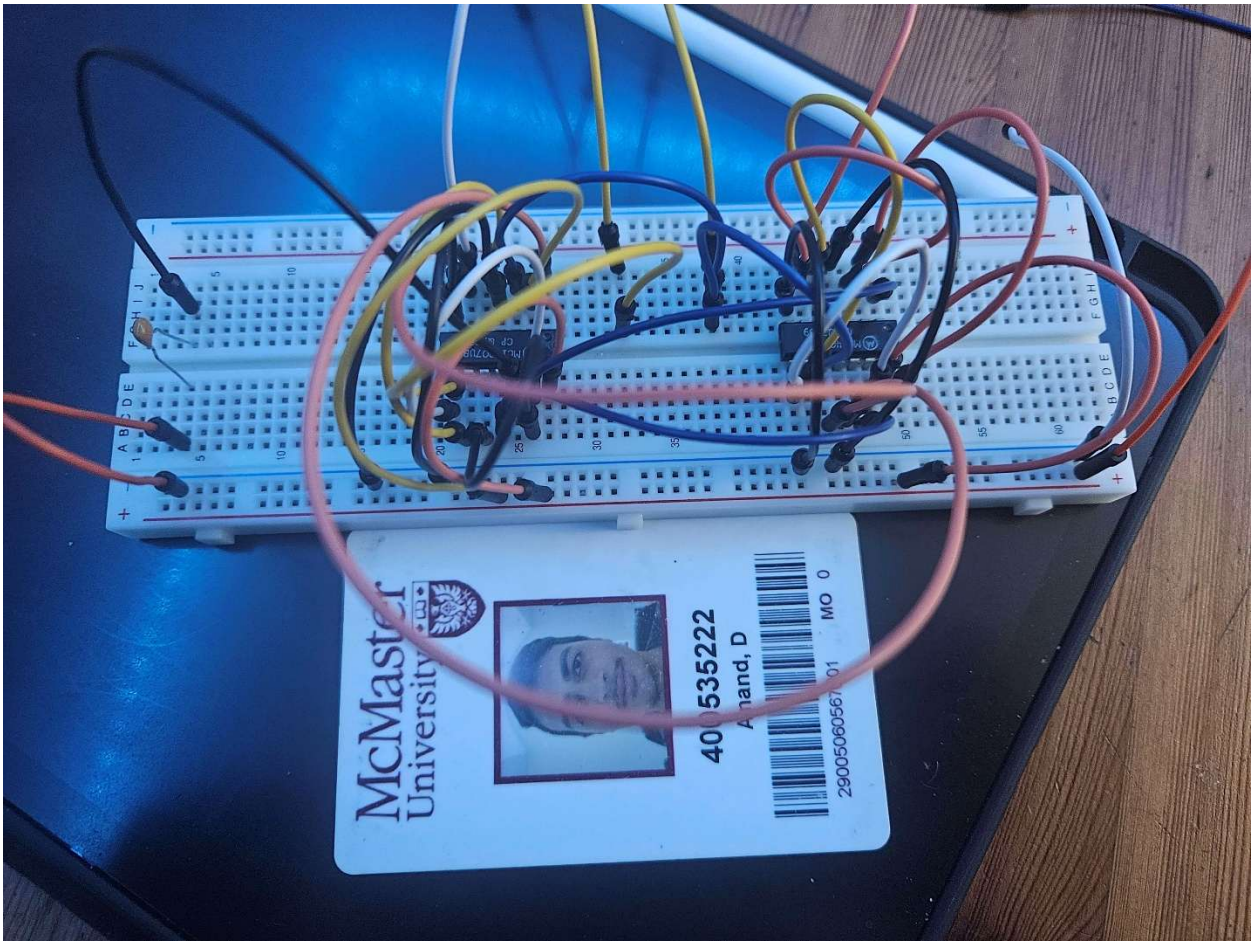

Figure 2: Physical implementation

Functional Testing

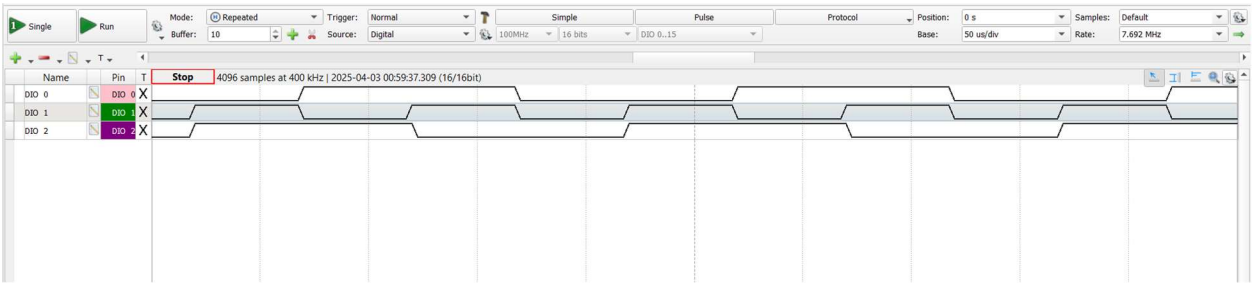

Figure 3: Logic testing of XOR circuit

Analysing the above image, where DIO 2 is the output, we can see that XOR logic is being followed. DIO 2 is only high (1) when either DIO 0 or DIO 1 is high (1), but not both.

DIO 0	DIO 1	DIO 2
0	0	0
1	0	1
0	1	1
1	1	0

Table 1: XOR truth table

Static Level Testing

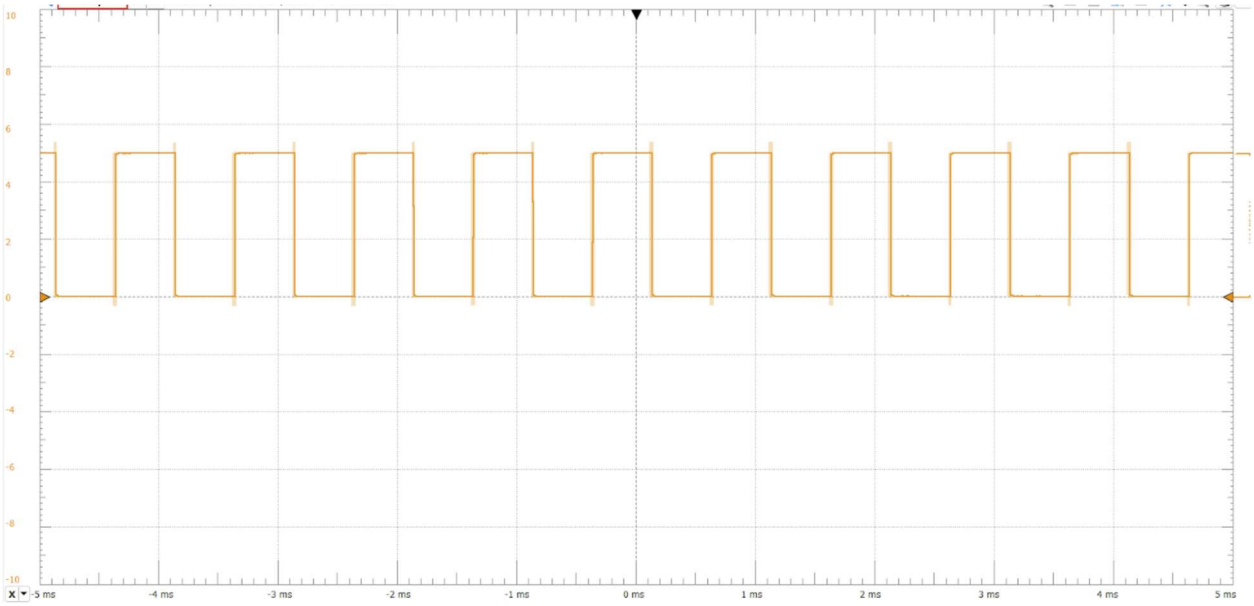

Figure 4: Test 1 - Output voltage with A set to 5V (logic high) and B set to a 0-5V square wave

In test 1, setting input A = 5V and input B = 0-5V square wave, we can observe from the graph that $V_H \approx 4.98V$ and $V_L \approx 3.11mV$

In test 2, setting input A = 0-5V square wave, and input B = 5V, we can observe from the graph that $V_H \approx 4.97V$ and $V_L \approx 2.42mV$

After analysing the graphs, it can be seen that V_H and V_L are about the exact same in both tests. The percent difference between V_H is 0.2%, and between V_L is 24.96%. The difference in the low voltages is likely due to noise and poor connections between wires.

Timing

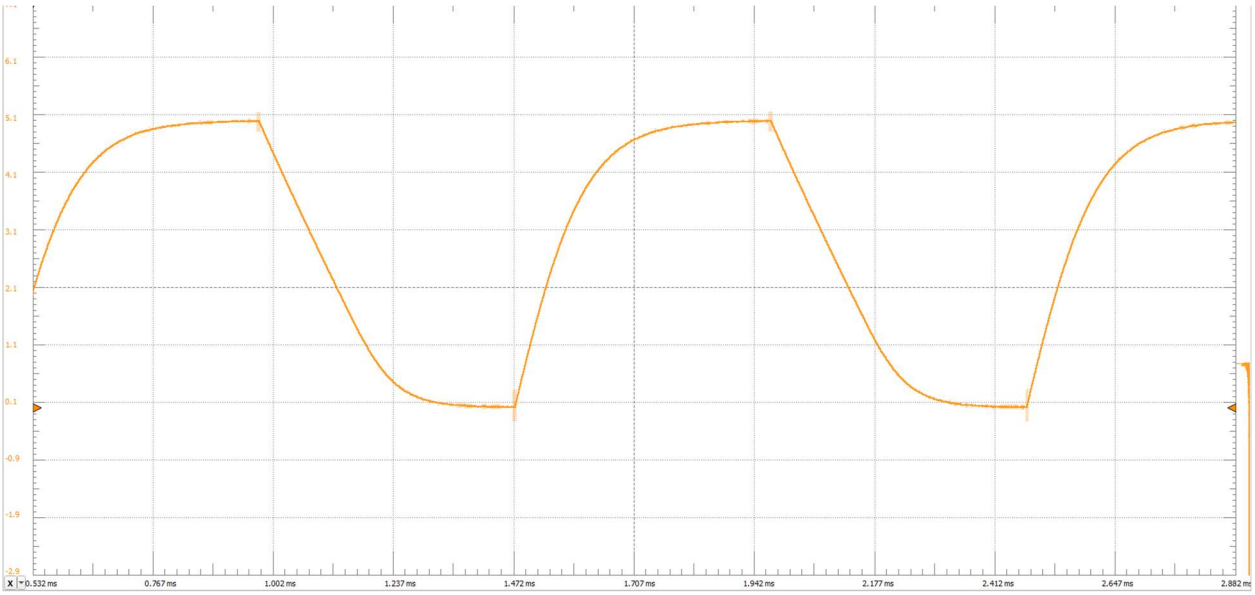

Figure 5: Output voltage at 100nF capacitor with A set to 5V (logic high) and B set to a 0-5V square wave

Analysing the graph, the rise and fall time can be found by measuring the time it takes for the graph to rise from 10% of its max to 90% of its max output, and the time it takes to fall from 90% to 10%. Through this analysis, the rise time of the output is found to be 223.7us, and the fall time is 213.2us.

Using this information, we can find that:

$$\tau_{plh} = \frac{1}{2}(rise\ time) = \frac{1}{2}(223.7) = 111.85\mu s$$

$$\tau_{phl} = \frac{1}{2}(fall\ time) = \frac{1}{2}(213.2) = 106.6\mu s$$

$$\tau_p = \frac{\tau_{plh} + \tau_{phl}}{2} = \frac{111.85 + 106.6}{2} \approx 109.23\mu s$$