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the path computation algorithm used by Interior Gateway Protocols

(IGPs). This information is available to controllers such as the

Path Computation Element (PCE) via topology learning. This document

proposes an approach for informing headend routers regarding the SR-

Algorithm associated with each Prefix SID used in PCE-computed paths,

as well as signalling a specific SR-Algorithm as a constraint to the

· Plain text as .txt

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Input file Choose file draft-ietf-pce-sid-algo-10.xml Diff with latest Text **HTML XML PDF** Validate (idnits) draft-ietf-pce-sid-algo-09.txt draft-ietf-pce-sid-algo-10.txt skipping to change at page 1, line 15 skipping to change at page 1, line 15 Intended status: Standards Track Cisco Systems, Inc. Intended status: Standards Track Cisco Systems, Inc. Expires: 9 December 2024 S. Peng Expires: 9 December 2024 S. Peng ZTE Corporation ZTE Corporation S. Pena S. Pena Huawei Technologies Huawei Technologies A. Stone A. Stone Nokia Nokia 7 June 2024 7 June 2024 Carrying SR-Algorithm information in PCE-based Networks. Carrying SR-Algorithm information in PCE-based Networks. draft-ietf-pce-sid-algo-09 draft-ietf-pce-sid-algo-10 Abstract Abstract The SR-Algorithm associated with a Prefix Segment-ID (SID) defines The SR-Algorithm associated with a Prefix Segment-ID (SID) defines

the path computation algorithm used by Interior Gateway Protocols

(IGPs). This information is available to controllers such as the

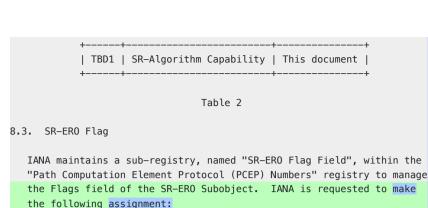
Path Computation Element (PCE) via topology learning. This document

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		2.1/	
skipping to change at <b>page 3, line 15</b>		skipping to change at page 3, line 15	
	7. Security Considerations	7. Security Considerations	
	8. IANA Considerations	8. IANA Considerations	
	8.1. SR Capability Flag	8.1. SR Capability Flag	
	8.2. SRv6 PCE Capability Flag	8.2. SRv6 PCE Capability Flag	
	8.3. SR-ERO Flag	8.3. SR-ERO Flag	
	8.4. SRv6-ERO Flag	8.4. SRv6-ER0 Flag	
	8.5. PCEP TLV Types	8.5. PCEP TLV Types	
	8.6. Metric Types	8.6. Metric Types	
	9. References	9. References	
	9.1. Normative References	9.1. Normative References	
	9.2. Informative References	9.2. Informative References	
	Appendix A. Contributors	Appendix A. Contributors	
	Authors' Addresses	Authors' Addresses	
	1. Introduction	1. Introduction	
	A PCE can compute SR—TE paths using SIDs with different SR—Algorithms depending on the use—case, constraints, etc. While this information	A PCE can compute SR-TE paths using SIDs with different SR-Algorithms depending on the use-case, constraints, etc. While this information	
	is available on the PCE, there is no method of conveying this information to the headend router.	is available on the PCE, there is no method of conveying this information to the headend router.	
	Similarly, the headend can also compute SR-TE paths using different	Similarly, the headend can also compute SR—TE paths using different	
skipping to change at page 15, line 46		skipping to change at <i>page 15, line 46</i>	
	Considerations section of [RFC9350], but which are also applicable to path computation done by PCE.	Considerations section of [RFC9350], but which are also applicable to path computation done by PCE.	
	8. IANA Considerations	8. IANA Considerations	
8.1. SR Capability Flag		8.1. SR Capability Flag	
IANA maintains a sub-registry, named "SR Capability Flag Field",		IANA maintains a sub-registry, named "SR Capability Flag Field",	
	within the "Path Computation Element Protocol (PCEP) Numbers"	within the "Path Computation Element Protocol (PCEP) Numbers"	
	registry to manage the Flags field of the SR-PCE-CAPABILITY TLV.	registry to manage the Flags field of the SR-PCE-CAPABILITY TLV.	
IANA is requested to make the following assignment:		IANA is requested to confirm the following early allocation:	
	+====+======+	+====+===++	
	Bit   Description   Reference	Bit   Description   Reference	
	+====+======+	+====++==+++++++++++++++++++++++++++++	
	++	++	
	5   SR-Algorithm Capability   This document   ++	5   SR-Algorithm Capability   This document	
	Table 1	Table 1	
	. 43 66 1		



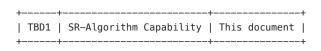


Table 2

8.3. SR-ERO Flag

IANA maintains a sub-registry, named "SR-ERO Flag Field", within the "Path Computation Element Protocol (PCEP) Numbers" registry to manage the Flags field of the SR-ERO Subobject. IANA is requested to confirm the following early allocation:



Table 3



Table 3



Table 4

8.5. PCEP TLV Types

IANA maintains a subregistry, named "PCEP TLV Type Indicators", within the "Path Computation Element Protocol (PCEP) Numbers" registry. IANA is requested to allocate a new TLV type for the new LSPA TLV specified in this document.

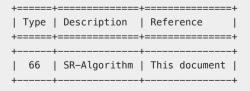


Table 5

8.6. Metric Types

IANA maintains a subregistry for "METRIC Object T Field" within the

Table 4

8.5. PCEP TLV Types

IANA maintains a subregistry, named "PCEP TLV Type Indicators", within the "Path Computation Element Protocol (PCEP) Numbers" registry. IANA is requested to confirm the early allocation of a new TLV type for the new LSPA TLV specified in this document.

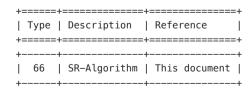


Table 5

8.6. Metric Types

IANA maintains a subregistry for "METRIC Object T Field" within the

"Path Computation Element Protocol (PCEP) Numbers" registry. IANA is requested to allocate a new values for metric types defined in this document:

1 21	Description	Reference
+	+	This document
23	P2MP Path Min Delay Metric	This document
24(TBA)	Bandwidth Metric +	This document   +
25(TBA)	P2MP Bandwidth Metric	This document   +
128-255 (TBA) +	User Defined Metric	This document   +

"Path Computation Element Protocol (PCEP) Numbers" registry. IANA is requested to confirm the early allocated codepoints as follows:

+=====+=========++======++						
Type   Description	Reference					
+=====+================================	+=====+					
+	++					
22   Path Min Delay Metric	This document					
+	++					
23   P2MP Path Min Delay Metric	This document					
+	++					

Table 6

## Table 6

IANA is requested to allocate new values for the following metric types defined in this document. Please note the suggested values for the IANA to consider.

Type   Description   Reference   ++	+	-=====+	-======================================	-=====+
++   24(TBA)   Bandwidth Metric   This document   +		Type	Description	Reference
++	+	-======+	-========++	-=====+
++	+	+		+
	1	24(TBA)	Bandwidth Metric	This document
DOMO Dondwidth Matric I This decument I	+	+		+
Z5(IDA)   PZMP BANGWIGTN METFIC   INIS GOCUMENT		25(TBA)	P2MP Bandwidth Metric	This document
++	+	+		+
128–255 (TBA)   User Defined Metric   This document		128-255 (TBA)	User Defined Metric	This document
++	+	+		+

Table 7

- 9. References
- 9.1. Normative References

[I-D.ietf-lsr-flex-algo-bw-con]

Hegde, S., Britto, W., Shetty, R., Decraene, B., Psenak, P., and T. Li, "Flexible Algorithms: Bandwidth, Delay, Metrics and Constraints", Work in Progress, Internet-Draft, draft-ietf-lsr-flex-algo-bw-con-12, 19 May 2024,

- 9. References
- 9.1. Normative References

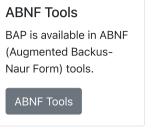
[I-D.ietf-lsr-flex-algo-bw-con]

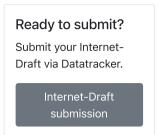
Hegde, S., Britto, W., Shetty, R., Decraene, B., Psenak, P., and T. Li, "Flexible Algorithms: Bandwidth, Delay, Metrics and Constraints", Work in Progress, Internet—Draft, draft—ietf—lsr—flex—algo—bw—con—12, 19 May 2024,

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