Toronto Metropolitan University

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| Course Title | ELE 404 |
| Course Name | Electronic Circuits I |
| Semester/Year | W2024 |
| Lab Name | Design Project |

## Table of Contents

## Introduction

The report is about the Design Project, which was done over a 2 week period. This design project is about BJT transistors and its applications which was covered throughout this course. The goal of this project is to design a multi-stage amplifier that meets a series of requirements that are presented.

## Objectives

The main objective of this design project is to design a multi-stage amplifier that meets the specification provided.

The specifications that the circuit should meet are stated below:

- Power Supply: **+10V** relative to the ground
- Quiescent current drawn from the power supply: **no larger than 10 mA**
- No-Load voltage gain (at 1 kHz): **$|A_{vo}|$ = 50 (± 10%)**
- Maximum no-load output voltage swing (at 1 kHz): **no smaller than 8 V peak to peak**
- Loaded voltage gain (at 1 kHz and with $R_L$ = 1 kΩ): **no smaller than 90% of the no-load voltage gain**
- Maximum loaded output voltage swing (at 1 kHz and $R_L$ = 1 kΩ): **no smaller than 4 V peak to peak**
- Input resistance (at 1 kHz): **no smaller than 20 kΩ)**
- Amplifier type: **inverting or non-inverting**
- Frequency response: **20 Hz to 50 kHz (-3 dB response)**
- Type of transistors: **BJT**
- Number of transistors (stages): **no more than 3**

- Resistances permitted: **values smaller than 220 kΩ from the E24 series**
- Capacitors permitted: **0.1 µF, 1.0 µF, 2.2 µF, 4.7 µF, 10 µF, 47 µF, 100 µF, 220 µF**
- Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE404 lab kit**

**Design Approach**

The proposed circuit consists of 3 stages where 2 common emitter stages were used and 1 common collector was used as well. The proposed circuit configuration is a common emitter followed by another common emitter and the last stage is the common collector. The reason for choosing the common emitter transistor for stage 1 and 2 is because it allows the input resistance to be large. Using 2 common emitter transistors enables the total gain 50 to be split between the 2 stages. Specifically, stage 1 has a gain of approximately 5, while stage 2 has a gain of approximately 10. Additionally, using a common collector transistor ensures that the gain with and without load are similar in order to meet one of the requirements. The common collector gain is always around 1 which is why it acts as an emitter follower and prevents the loss of gain when a load is connected. For each stage the $I_C$ current value was assumed to be a specific value which was less than the threshold value of 10 mA. Additionally, the DC analysis was initially conducted independently for each stage, by beginning off with an approximation of $I_C$ to calculate the other quiescent parameters of each stage. Furthermore, the gain of each stage is calculated and especially for the stage 3, the gain is calculated for both with and without load.

The resistors values are chosen based on the $I_C$ value of each stage and the approximation of the relationship between $R_C$ and $R_E$ for the respective stage with an ideal

factor of 10 is considered between the ratio $R_C$ / $R_E$. Each stage has biasing resistors to control the $V_B$ according to the $I_C$. The $I_C$ value was chosen in any way to make the input resistance as large as possible. The reason for using this approach is that a shunt capacitor is not used in parallel with $R_E$ meaning that the voltage gain for each stage independently is approximately $R_C$ / $R_E$ for stage 1 and stage 2 without the consideration of the input of the other stage as it might reduce the gain. This approach is only used stage 1 and stage 2 because it is a common emitter amplifier. The $V_B$ is determined based on using the $I_E$, $R_E$, and $\beta$ in which the $V_B$ is used to calculate $R_1$ and $R_2$. $R_1$ and $R_2$ are determined based on the KCL at $V_B$ where an approximation is made of assuming one the resistors to be fairly large in order to get a higher input resistance for the whole circuit. The capacitor values are chosen to ensure that the DC signal is blocked from transmitting to the next stage. These capacitors are called coupling capacitors since they are placed between stages. The values of these capacitors are large enough to ensure that the circuit operates over a frequency range of 20 Hz to 50 kHz. The capacitors are chosen in a way so that there is a low impedance for the minimum frequency of 20 Hz.

**Theoretical Calculations**

**Figure 1** shows the calculations for the DC analysis for stage 1 and stage 2. **Figure 2** shows the calculations for DC analysis for stage 3 and $R_{in}$ for the circuit. **Figure 3** shows the calculations for voltage gain for stage 1 and stage 2. **Figure 4** shows the calculations for voltage gain for stage 3 with and without load. **Figure 5** shows the calculations for the overall gain for the circuit with and without load, as well capacitor values for the circuit at different frequencies.

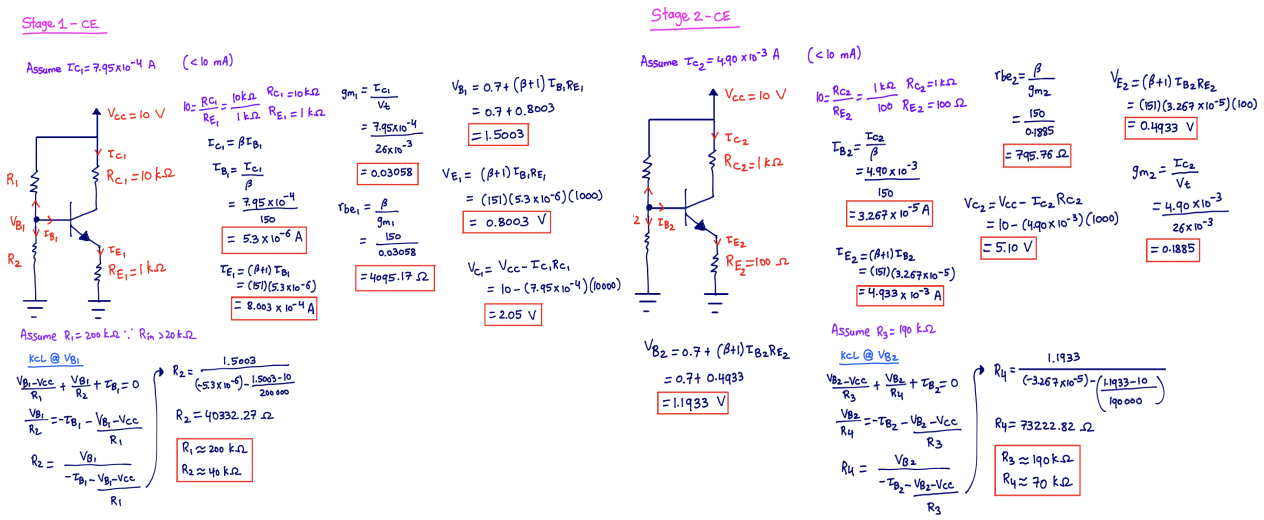


**Figure 1: DC analysis calculations for stage 1 and stage 2.**

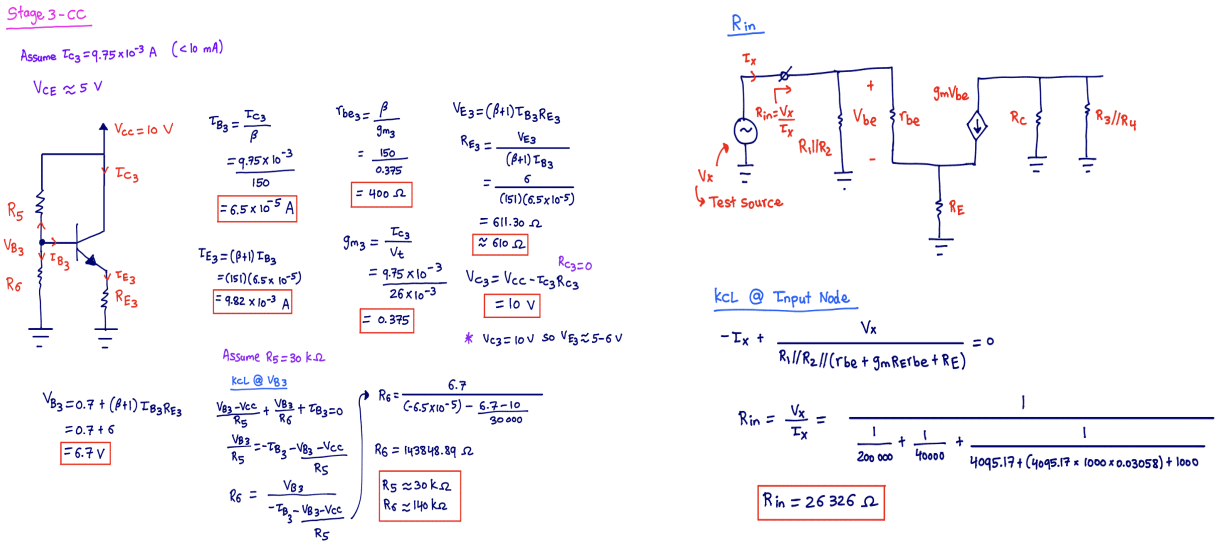


**Figure 2: DC analysis calculations for stage 3 and $R_{in}$ calculation for the circuit.**

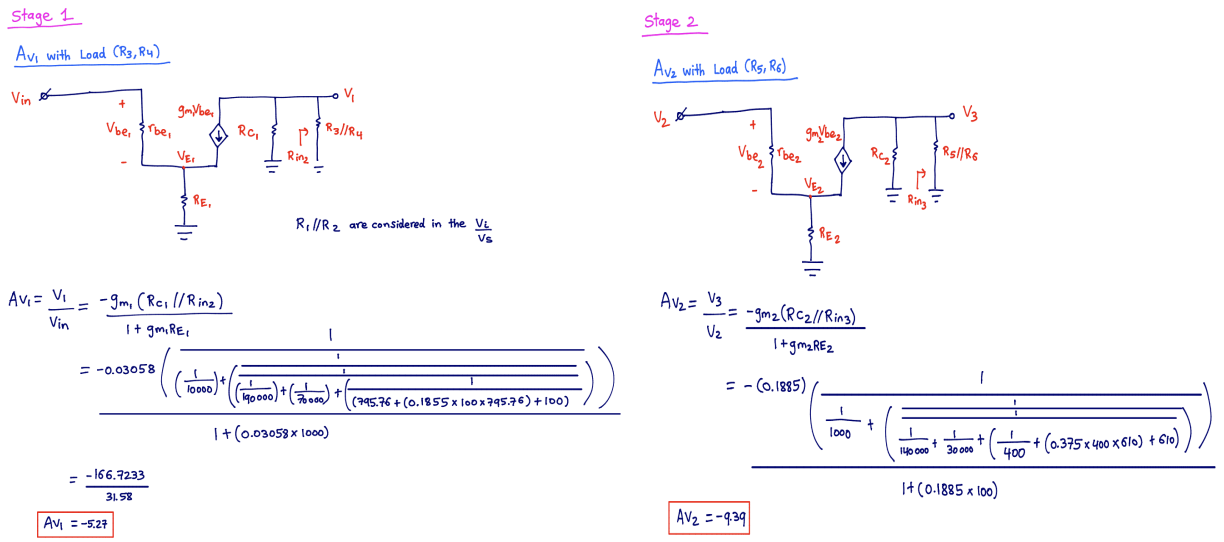


**Figure 3: Voltage gain calculations for stage 1 and stage 2.**

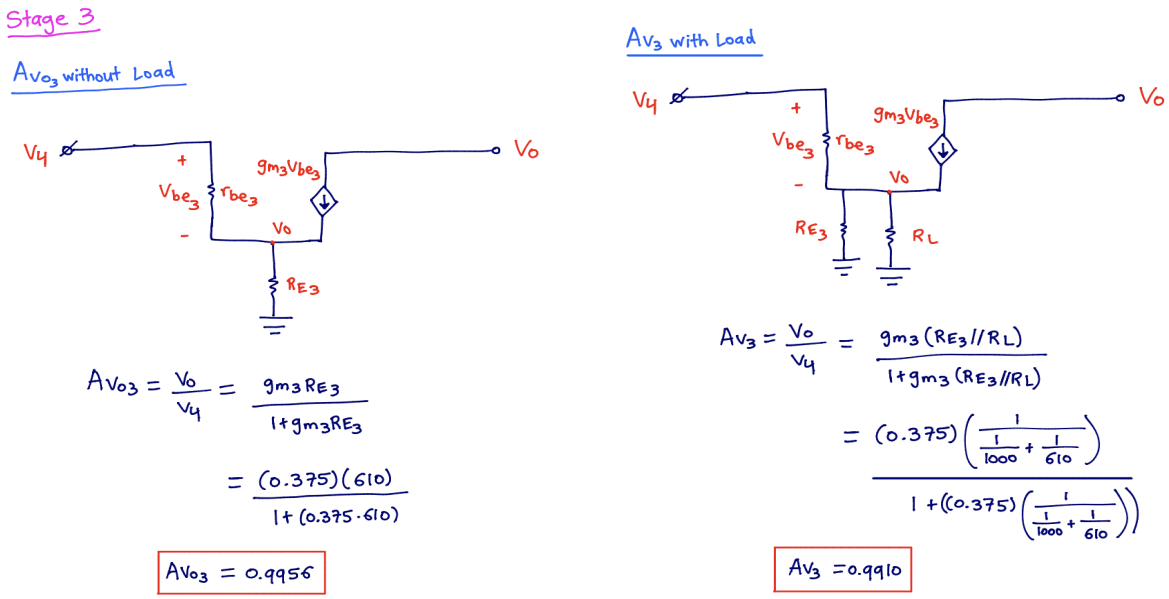


**Figure 4: Voltage gain calculations for stage 3 for with and without load.**

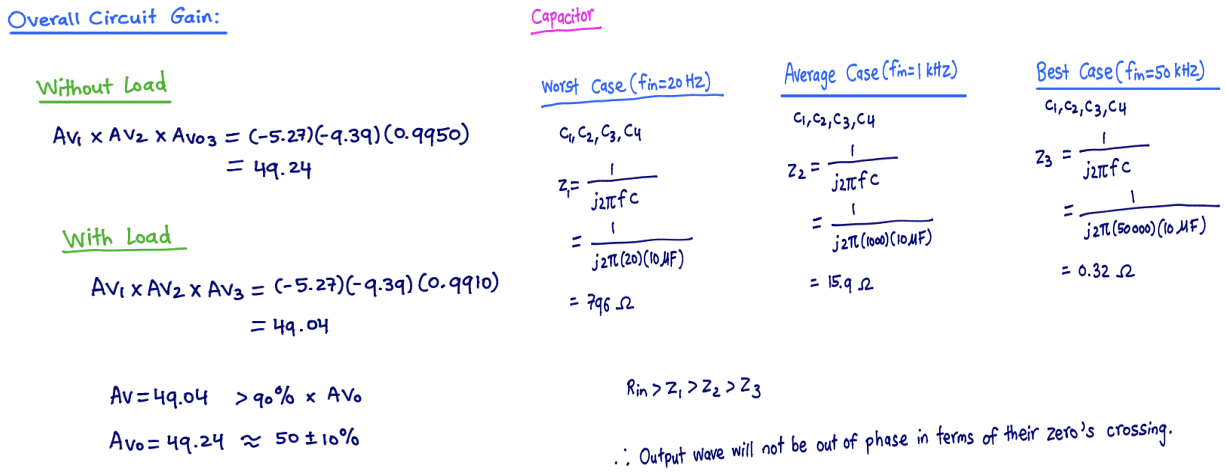


**Figure 5: Calculations for overall circuit gain and capacitor values.**

The theoretical calculation results are placed in the respective table below. **Table 1** contains the values for the biasing resistors. **Table 2** contains the values for the collector and emitter resistors. **Table 3** contains the values for the biasing resistors. **Table 4**, **Table 5**, and **Table 6** contain the quiescent values for stage 1, stage 2, and stage 3, respectively. **Table 7** contains the values for the capacitors.

**Table 1: Biasing Resistor Values**

| $R_1$ (kΩ) | $R_2$ (kΩ) | $R_3$ (kΩ) | $R_4$ (kΩ) | $R_5$ (kΩ) | $R_6$ (kΩ) |
|---|---|---|---|---|---|
| 200 | 40 | 190 | 70 | 30 | 140 |

**Table 2: Collector and Emitter Resistor Values**

| $R_{C1}$ (kΩ) | $R_{E1}$ (kΩ) | $R_{C2}$ (kΩ) | $R_{E2}$ (kΩ) | $R_{C3}$ (kΩ) | $R_{E3}$ (kΩ) |
|---|---|---|---|---|---|
| 10 | 1 | 1 | 0.100 | 0 | 0.610 |

**Table 3: CE Stage 1 Quiescent Values**

| $I_{B1}$ (μA) | $I_{C1}$ (μA) | $I_{E1}$ (μA) | $V_{B1}$ (V) | $V_{C1}$ (V) | $V_{E1}$ (V) | $g_{m1}$ (s) | $r_{be1}$ (Ω) |
|---|---|---|---|---|---|---|---|
| 5.3 | 795 | 800.3 | 1.503 | 2.05 | 0.8003 | 0.03058 | 4095.17 |

**Table 4: CE Stage 2 Quiescent Values**

| $I_{B2}$ (μA) | $I_{C2}$ (μA) | $I_{E2}$ (μA) | $V_{B2}$ (V) | $V_{C2}$ (V) | $V_{E2}$ (V) | $g_{m2}$ (s) | $r_{be2}$ (Ω) |
|---|---|---|---|---|---|---|---|
| 32.67 | 4900 | 4933 | 1.1933 | 5.10 | 0.4933 | 0.1885 | 795.76 |

**Table 5: CC Stage 3 Quiescent Values**

| $I_{B3}$ (μA) | $I_{C3}$ (μA) | $I_{E3}$ (μA) | $V_{B3}$ (V) | $V_{C3}$ (V) | $V_{E3}$ (V) | $g_{m3}$ (s) | $r_{be3}$ (Ω) |
|---|---|---|---|---|---|---|---|
| 65 | 9750 | 9820 | 6.7 | 10 | 5 | 0.375 | 400 |

**Table 6: Capacitors Values**

| $C_1$ (μF) | $C_2$ (μF) | $C_3$ (μF) | $C_4$ (μF) |
|---|---|---|---|
| 10 | 10 | 10 | 10 |

**Circuit Under Test**

**Figure 6** below shows the schematic diagram of the proposed circuit for the design project. The **Figure 6** schematic is constructed on Multisim and simulated. **Figure 7** below shows the schematic diagram on Multisim. The circuit consists of 3, 2N3904 BJT transistors which are labeled as Q1, Q2 and Q3. The power sources used are a $V_{CC}$ power supply of 10 V and a sinusoidal waveform function generator with an input voltage of 86 mV at 1 kHz.

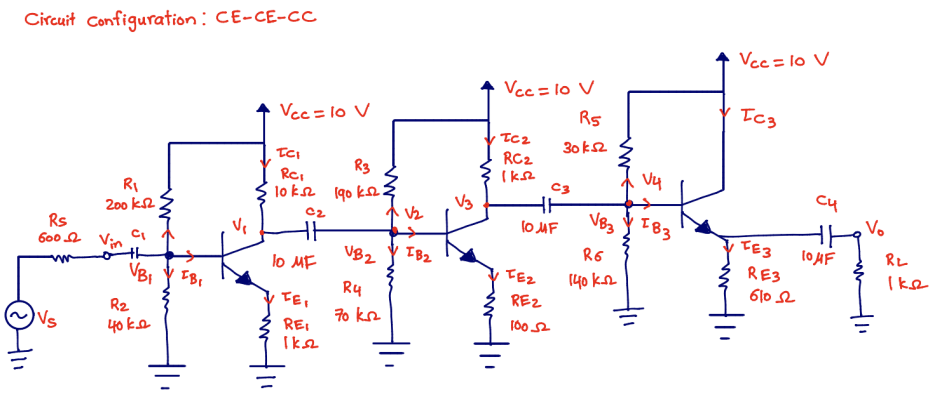


**Figure 6: Final circuit configuration including all stages.**

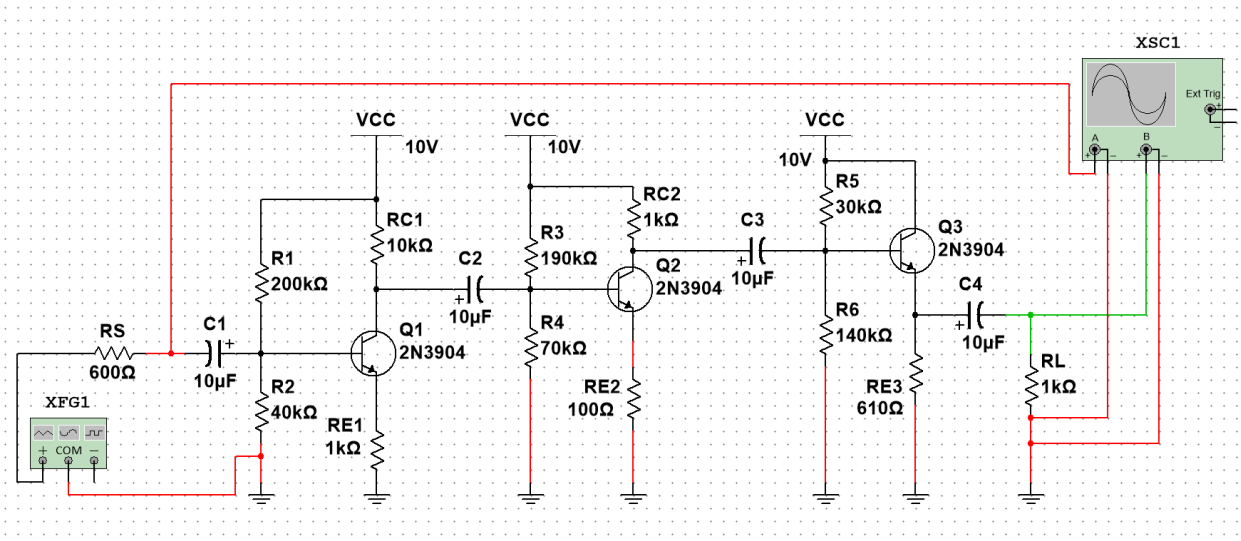


**Figure 7: Multisim circuit for the proposed circuit (Figure 6).**

## Experimental Results

**Figure 8** and **Figure 9** below shows the waveform formed on Multisim, for input and output voltage for with load and without load, respectively. **Table 7** and **Table 8** below shows the voltage gain for with and without load.

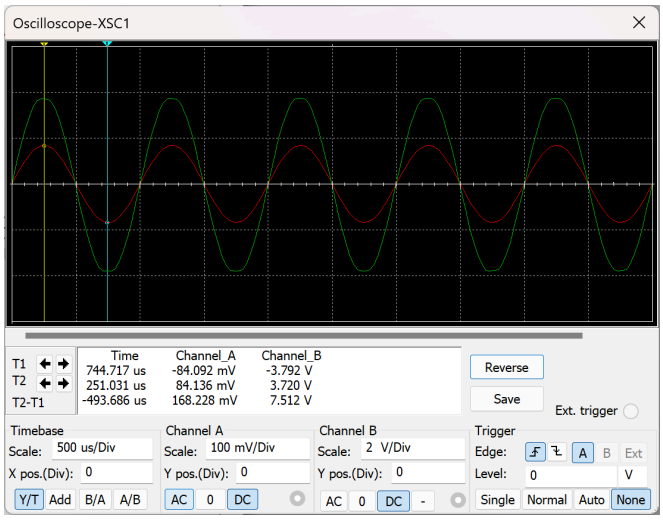


**Figure 8: The waveform for input and output voltage with load ($R_L$ = 1 kΩ).**

**Table 7: Values for Voltage Gain for with Load Using Figure 8**

| $V_{O\ P\text{-}P}$ (V) | $V_{I\ P\text{-}P}$ (mV) | $A_V$ |
|---|---|---|
| 7.512 | 168.228 | 44.64 |

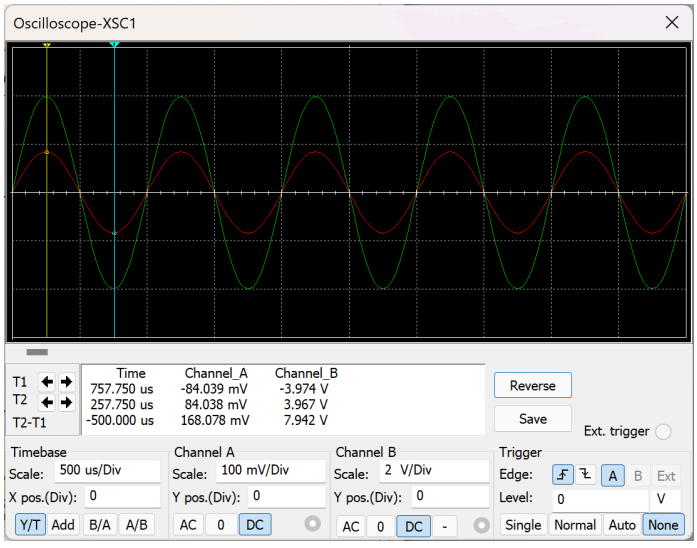


**Figure 9: The waveform for input and output voltage without load.**

**Table 8: Values for Voltage Gain for without Load Using Figure 9**

| $V_{O\ P\text{-}P}$ (V) | $V_{I\ P\text{-}P}$ (mV) | $A_{VO}$ |
|---|---|---|
| **7.942** | **168.078** | **47.25** |

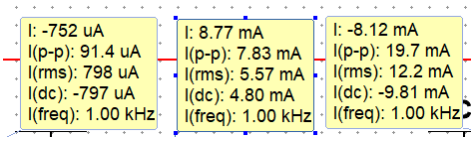


**Figure 10: The quiescent value for stage 1, stage 2 and stage 3, respectively.**

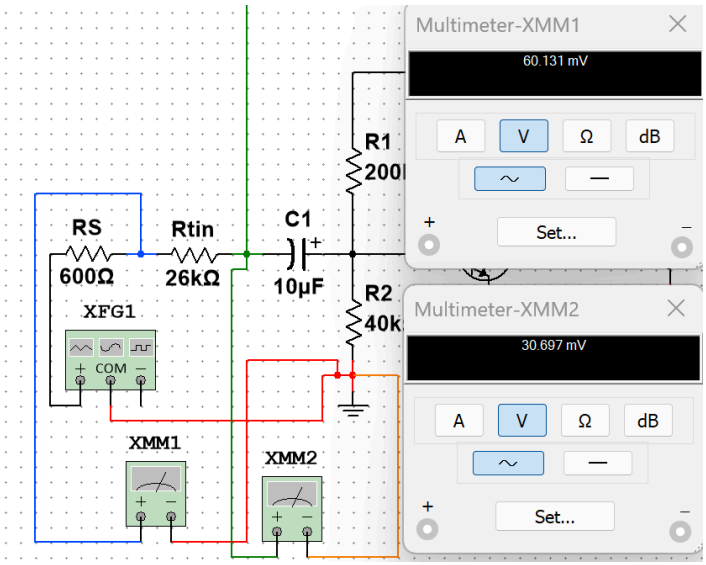


**Figure 11: The Values for $V_t$ , and $V_I$ by using $R_{t,in}$ .**

$$R_{in} = R_{t,in}\ (V_I / (V_t - V_I))$$

**Table 9: The Values Used to Calculate the $R_{in}$ for Multisim**

| $V_t$ (mV) | $V_I$ (mV) | $R_{t,in}$ (kΩ) | $R_{in\ (calculated)}$ (kΩ) | $R_{in}$ (kΩ) |
|---|---|---|---|---|
| 60.131 | 30.687 | 26 | 26.326 | 27.116 |

**Conclusion and Remarks**

| Specification | Calculated | Measured | % Error | Success |
|---|---|---|---|---|
| Quiescent current 1: no larger than 10 mA | 0.795 mA | 0.797 mA | 0.25% | Yes |
| Quiescent current 2: no larger than 10 mA | 4.90 mA | 4.80 mA | 2.08% | Yes |
| Quiescent current 3: no larger than 10 mA | 9.75 mA | 9.81 mA | 0.61% | Yes |
| $\lvert A_{vo} \rvert$ = 50 (± 10%) | 49.24 | 47.25 | 4.21% | Yes |
| Minimum no-load output swing | 8 $V_{p-p}$ | 7.942 $V_{p-p}$ | 0.73% | Yes |
| Loaded voltage gain: no smaller than 90% of $A_{vo}$ | 49.04 | 44.64 | 9.86% | Yes |
| Minimum load output swing | 4 $V_{p-p}$ | 7.512 $V_{p-p}$ | N/A | Yes |
| Input resistance: no smaller than 20 kΩ | 26.326 kΩ | 27.116 kΩ | 2.91% | Yes |

The specification for the design project was met as the percent error is fairly low. The Multisim were slightly different since in the calculators there were some approximations made that could have affected the resistor values such as the biasing resistors since those values were approximated to a certain degree. This approximation has slightly affected the voltage gain value as on Multisim the voltage gain for with and without load is lower compared to the calculation values. The rounding of the biasing resistor could have played a role in the discrepancies for the voltage gain and the input resistance values. Furthermore, all of the specifications were met with minor errors due to these approximations and rounding for the calculations. Additionally, the format of a 3 stage, CE - CE - CC design was successful since all of the specifications adhered to the manual and calculations. Therefore, a 3 stage, CE - CE - CC design allows for the desirable no-load voltage around 50 even when the input voltage is 86 mV.