IMPLEMENTATION OF DIGITAL CIRCUITS USING QUANTUM CELL AUTOMATA

Mini Project - Report submitted by

DHRUV SHETTY

4NM21EC047

HEMANTH MURALI

4NM21EC056

KENDRIC CLEAVON SOANS

4NM21EC061

NAGESH

4NM21EC080

6th Semester B.E.

Under the Guidance of

Ms. LAVANYA B L
Assistant Professor Gd-II

In partial fulfillment of the requirements for the award of

the Degree of

Bachelor of Engineering in Electronics and Communication Engineering

from

Visvesvaraya Technological University, Belagavi

Department of Electronics and Communication Engineering

NMAM Institute of Technology, Nitte - 574110

(An Autonomous Institution affiliated to VTU, Belagavi)

MAY 2024

NITTE EDUCATION TRUST | N.M.A.M. INSTITUTE OF TECHNOLOGY
(An Autonomous Institution affiliated to Visvesvaraya Technological University, Belagavi)
Nitte – 574 110, Karnataka, India

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

Certified that the Mini project work entitled

"Implementation of Digital Circuits Using Quantum Cellular Automata"

is a bonafide work carried out by

DHRUV SHETTY	**HEMANTH MURALI**
4NM21EC047	4NM21EC056
KENDRIC CLEAVON SOANS	**NAGESH**
4NM21EC061	4NM21EC080

of 6th Semester B.E. in partial fulfilment of the requirements for the award of

Bachelor of Engineering Degree in Electronics and Communication Engineering

prescribed by ***Visvesvaraya Technological University, Belagavi***

during the year ***2023-2024.***

_____ _____

Signature of the Guide ***Signature of the HOD***

Viva Voce Examination

Name of the Examiners	**Signature with Date**
1. _____	_____
2. _____	_____

ACKNOWLEDGEMENT

The success of our project was significantly attributed to the invaluable encouragement, guidance, and support extended by various individuals of influence. First and foremost, we would like to express our sincere gratitude towards our project guide **Ms. Lavanya B L**, Assistant Professor Gd-II, Department of Electronics and Communication Engineering, N. M. A. M. Institute of Technology, Nitte, for their guidance, encouragement and inspiration throughout the project work.

We extend our gratitude to **Dr. K. V. S. S. S. S. Sairam**, Professor and Head, Department of Electronics and Communication Engineering, N.M.A.M. Institute of Technology, Nitte, for his encouragement and providing necessary facilities in the department. We wish to acknowledge the support of **Dr. Niranjan N Chiplunkar**, Principal, N.M.A.M. Institute of Technology, Nitte, for providing motivational academic environment.

We would like to express our sincere thanks to all the teaching and non-teaching staff of the department of Electronics and Communication Engineering, N.M.A.M Institute of Technology, Nitte, for their patience and help during our project work.

Finally, we would like to thank all our friends and well-wishers who have helped us whenever needed and supported us.

Dhruv Shetty
Hemanth Murali
Kendric Cleavon Soans
Nagesh

ABSTRACT

Quantum Dot Cellular Automata (QCA) is one of the emerging trends in the field of nanotechnology which help to overcome the limitations of CMOS technology. QCA is simple in structure having significantly lesser elements as compared to CMOS design. It has the potential for attractive features such as faster speed, smaller size and low power consumption than transistor-based technology. The quantum cell is used as a building block to construct gates, wires, and memories. By taking the advantages of QCA one is able to design interesting different digital circuits. Unlike conventional computers in which information is transferred from one place to another by means of electrical current, QCA transfers information by propagating a polarization state. The digital circuits are simulated using the QCADesigner-E tool. The waveform and lost energy are obtained. The values of area, cell count, latency (number of clock cycles) and cost is calculated accordingly. Different designs are compared with each other and tabulated.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

Shrinkage in feature size of CMOS circuits has become a controversial issue for designers to implement a circuit with low power consumption besides considerable decreasing in the size. Therefore, the necessity for an alternative technology which could offer revolutionary approach for working at Nano-scale was seemed more vital than ever. Accordingly, Quantum-dot Cellular Automata (QCA) is presented which can perform with ultra-low power despite its high performance. The basic unit in this technology is a cell which consists of four dots and two excess electrons and all the logic gates and circuits can be made based on it. The computation in an array of QCA cells is performed through Coulombic interaction. According to the considerable advances in semiconductor materials used in existing CMOS fabrication process, semiconductor implementation of QCA is so promising. The type of used technology is semiconductor QCA which is composed of four quantum-dots manufactured by semiconductive materials. Since there is no electrical current in QCA computations, the power consumption is considerably lower than conventional CMOS circuits. Nevertheless, it is necessary to characterize all aspects of a new technology, so several studies have been performed in the area of QCA power. One of the most accurate power dissipation models has been proposed by Timler and Lent and an upper bound power dissipation for QCA circuits is estimated by Srivastava et al. based on it. Furthermore, in recent years, lots of investigations have been launched in order to design various digital circuits based on this technology and QCA complex gate designs [1].

1.1 AIM OF PRESENT STUDY

The aim of "Implementation of Digital Circuits Using Quantum Cellular Automata" is to compare power consumption between QCA circuits to enhance QCA circuits' viability for future applications.

1.2 OBJECTIVES

- Design efficient circuit designs in Quantum-dot Cellular Automata (QCA) technology.
- Implement the designed circuits in QCADesigner-E software.
- Obtain waveform simulations to verify the functionality and performance of the designed circuits.
- Conduct energy dissipation and power analysis calculations for the designed circuits.
- Compare the energy consumption and performance metrics of the designed circuits with other existing designs in the literature.

1.3 LITERATURE REVIEW

Quantum-dot Cellular Automata (QCA) has emerged as a promising alternative to conventional CMOS technology due to its potential for ultra-low power consumption and high performance at the nanoscale [2]. QCA operates on the principle of Coulombic interaction between quantum dots, enabling the construction of logic gates and circuits using minimal components. Unlike CMOS, which relies on electrical currents for information transfer, QCA utilizes polarization states, resulting in significantly lower power consumption [3].

Recent research in QCA has explored novel approaches to circuit design and optimization, aiming to maximize performance while minimizing power consumption [4]. Investigations into fault tolerance and reliability of QCA circuits have led to the development of fault-tolerant designs and error-correction techniques. Additionally, efforts have been made to integrate QCA with other emerging technologies, such as spintronics and memristors, to enhance functionality and enable new computing paradigms [5] [6].

Research in semiconductor implementations of QCA circuits has shown promise, leveraging advancements in semiconductor materials used in existing CMOS fabrication processes [7]. Despite these advancements, challenges remain, including addressing issues related to clocking, interconnects, and fabrication scalability. Furthermore, research continues to explore the potential applications of QCA beyond traditional digital computing, including in areas such as cryptography, image processing, and neuromorphic computing [8].

To bridge the gap between theory and practical implementation, studies have investigated fabrication techniques and scalability of QCA circuits. Moreover, efforts have been made to develop QCA-based architectures suitable for emerging computing paradigms such as quantum computing and artificial intelligence [9] [10]. By building upon these advancements and addressing remaining challenges, QCA holds promise for revolutionizing computing at the nanoscale and unlocking new possibilities for future technologies.

CHAPTER 2

SYSTEM DESIGN

This chapter gives explanation of key factors that went in designing the project.

2.1 BLOCK DIAGRAM

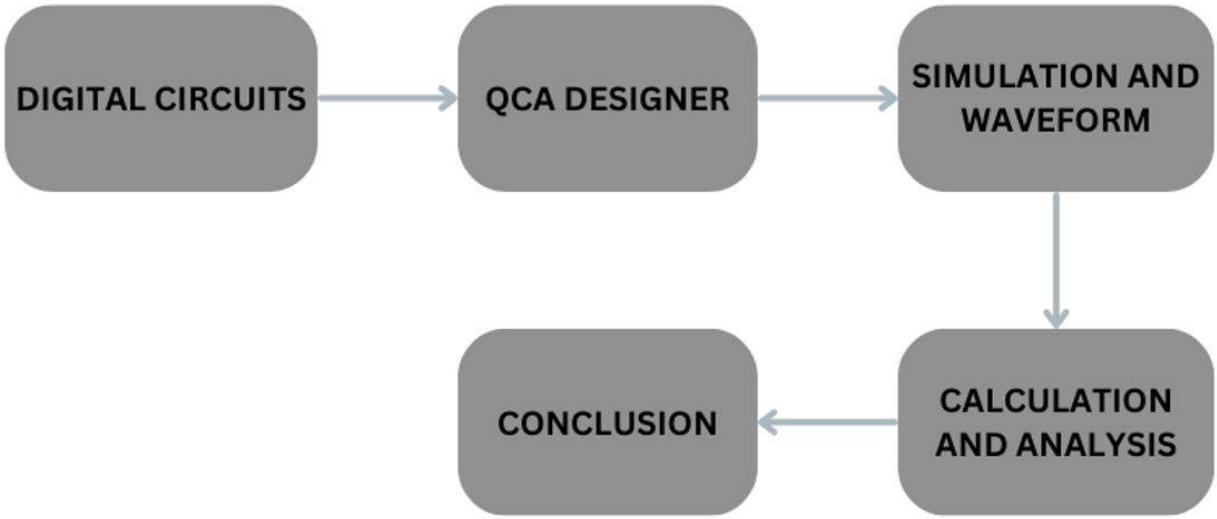

Figure. 2.1 Block Diagram

The block diagram of media control is shown in Figure. 2.1. It illustrates the systematic progression from initial digital circuit design to final comparison and conclusion. Each block represents a distinct phase, including circuit design using QCA principles, layout, and simulation using QCA Designer-E software, analysis of simulation waveforms, calculation of performance metrics, and comparison with existing literature. This visual representation offers a clear overview of the research workflow, guiding the investigation into the efficiency and viability of QCA technology for digital circuit implementation.

Digital Circuits: This stage marks the commencement of the study, focusing on the design of digital circuits utilizing Quantum-dot Cellular Automata (QCA) technology. Here, the emphasis lies on creating various digital components such as logic gates, wires, and memories, adhering to QCA principles.

QCA Designer: At this phase, QCA Designer software comes into play. It serves as a crucial tool for both layout and simulation of QCA circuits. Utilizing this software, the designed digital circuits from the previous stage are implemented, allowing for visualization of QCA layouts and simulation of their behaviour.

Simulation and Waveform: In this block, simulations of the QCA circuits are carried out using QCA Designer. The primary objective here is to analyse the behaviour of the circuits under different conditions and inputs. During simulation, particular attention is paid to observing and analysing the waveforms generated by the QCA circuits to verify their functionality and performance.

Calculation and Analysis: Following the simulation phase, the focus shifts to the calculation and analysis of various performance metrics associated with the QCA circuits. This may involve determining metrics such as energy consumption, latency, and area utilization. The analysis of simulation results is crucial in evaluating the efficiency and effectiveness of the designed circuits.

Comparison and Conclusion: In the final block, the performance of the designed QCA circuits is compared with existing designs documented in the literature. This comparison enables researchers to draw conclusions regarding the viability and effectiveness of QCA technology for digital circuit implementation. Insights gained from this comparison aid in understanding the relative advantages and limitations of QCA circuits when compared to other approaches.

2.2 QCA PRELIMINARIES

A QCA cell is composed of four quantum-dots and two excess electrons situated in a square. According to the existing coulombic interaction between the electronic charges, they can occupy diagonal antipodal sites through tunnelling junctions, quantum-mechanically. Therefore, a single QCA cell can accept two completely polarized states called cell polarization (P= +1, P= -1). By encoding these two ground states to binary digits, first digital concept is defined.

2.2.1 QCA CELL

In a deeper look, the cell polarization can be exhibited as the following equation [1]:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4}$$

where ‘ρi’ represents the electronic charge in dot ‘i’. Since the tunnelling energies are considerably less than coulombic energies, the cell will be well polarized. If the tunnelling energies take an equivalent value to columbic energies, the QCA cell will lose its polarization and thus becomes unpolarized. A QCA wire is constructed by placing QCA cells side-by-side.

2.2.2 CLOCKING

Clocking in Quantum-dot Cellular Automata (QCA) synchronizes information flow and provides power to the circuit. Adiabatic switching, introduced by Lent et al. [11] [12], addresses metastable states through slow capacitor discharging and charging. QCA clocking involves four phases across four zones, ensuring proper operation and synchronization. Proper clocking zone placement is crucial for design efficiency, while controlling potential barriers between adjacent quantum dots facilitates precise timing. Each clock signal, phase-shifted by 90 degrees, enables sequential operation. In the Switch phase, tunnelling barriers allow electron transfer; in Hold, barriers maintain polarization; in Release and Relax, barriers decrease for the next cycle.

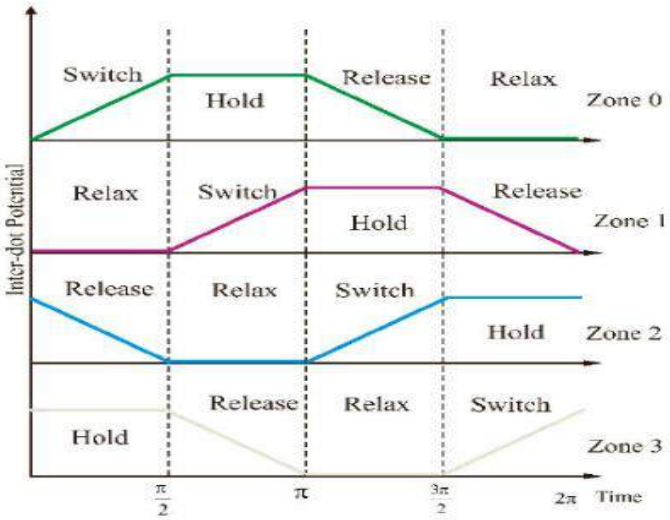

Figure. 2.2 QCA clocking phases [1]

CHAPTER 3

SOFTWARE IMPLEMENTATION

3.1 REQUIREMENTS

The software used is QCADesigner-E, version 2.0.3 of Konrad Walus [10]. It implements the estimation of the power dissipation of QCA circuits based on the works of Timler and Lent et al. [11] [12]. The extension is integrated as an additional simulation module that is based on the Coherence Vector Simulation Engine (CVSE). In order to choose the correct simulation engine, go to Simulation > Simulation Engine Setup and select Coherence Vector (w/ Energy). In order to modify the simulation options, go to Simulation > Simulation Engine Setup and select Options. Following window in Figure. 3.1 will appear.

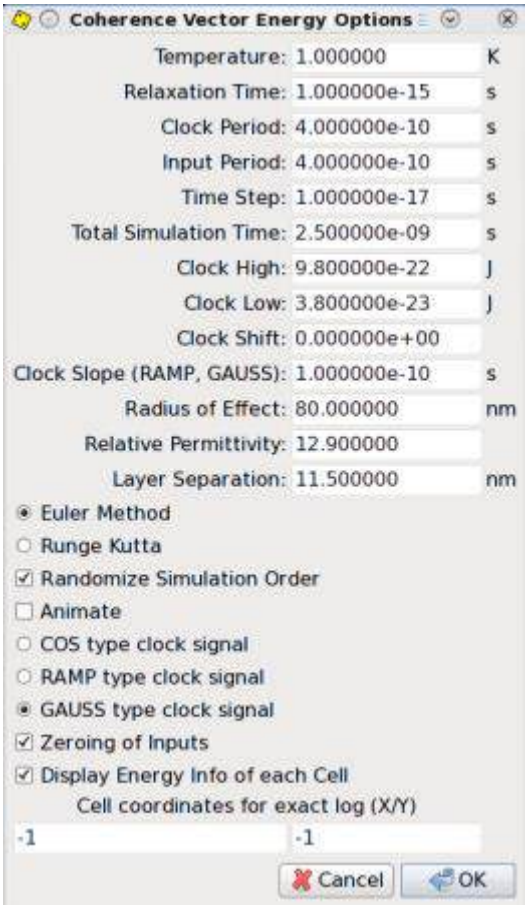

Figure. 3.1 Simulation parameters [13]

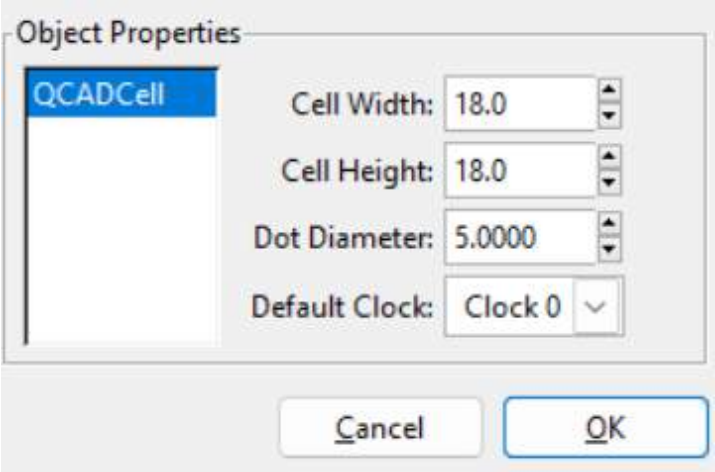

Figure. 3.2 Cell properties

Figure. 3.2 shows the cell properties that have been selected for designing.

3.2 WORKING OF MODEL

The following designs are the proposed circuits:

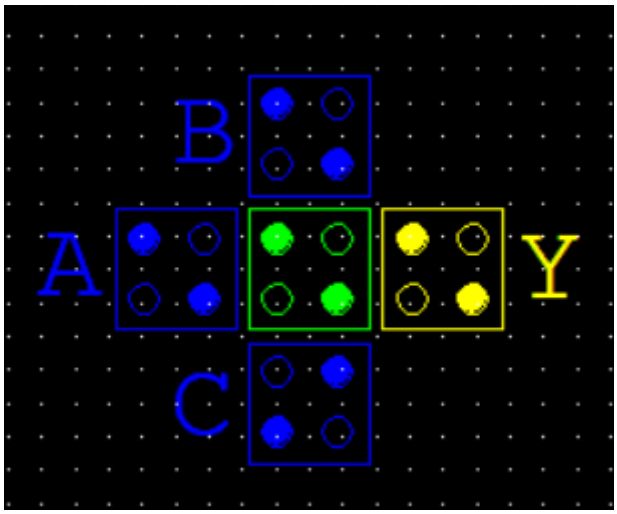

Figure. 3.3 Majority 3 gate

Figure. 3.3 shows a Majority 3 Gate of 5 cells in the ‘001’ state. A ‘Maj3’ gate passes the majority input to the output. From this logic either an ‘OR’ gate or an ‘AND’ gate can be constructed by applying polarities ‘1’ or ‘0’ respectively. ‘OR’ and ‘AND’ gates are the basic gates through which complex circuits can be constructed.

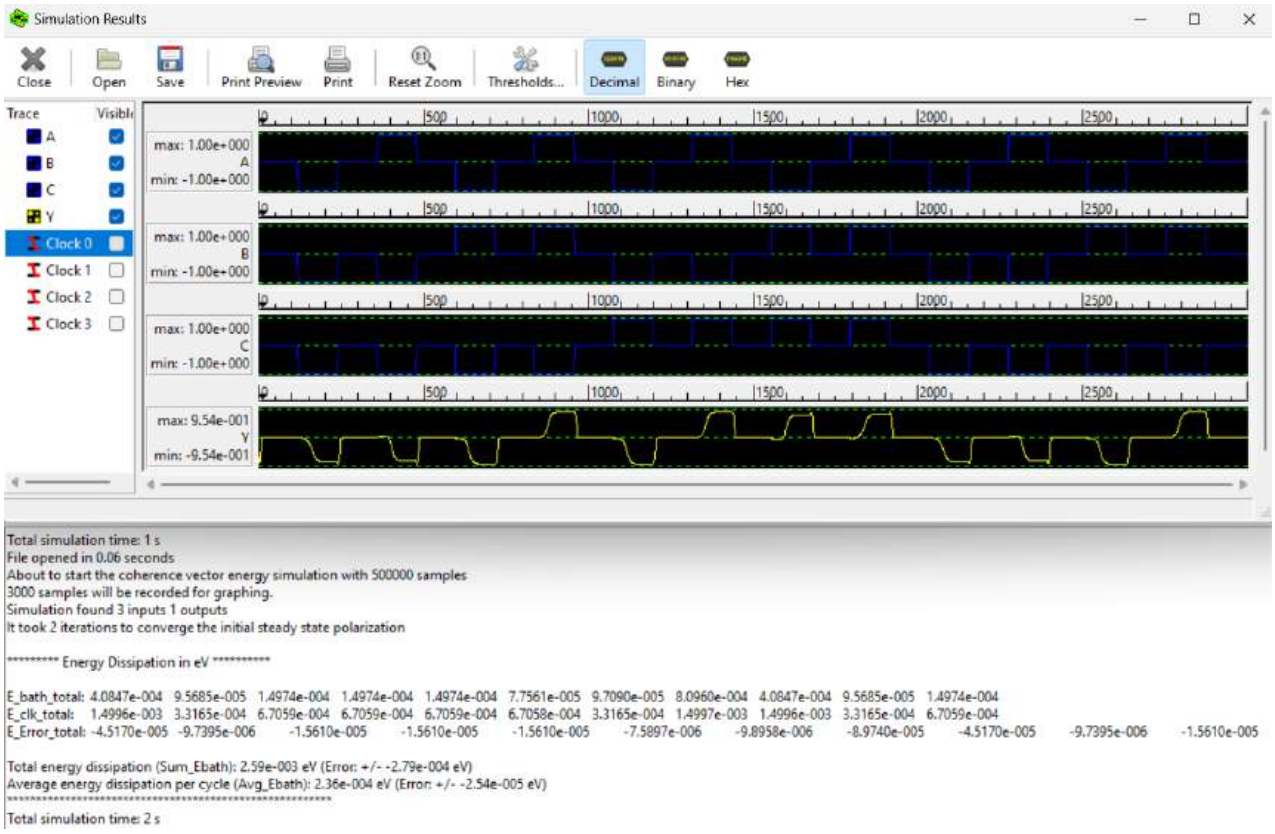

Figure. 3.4 Output of Majority 3 gate

Figure. 3.4 shows the waveforms obtained when the design is simulated and also the energy dissipation analysis.

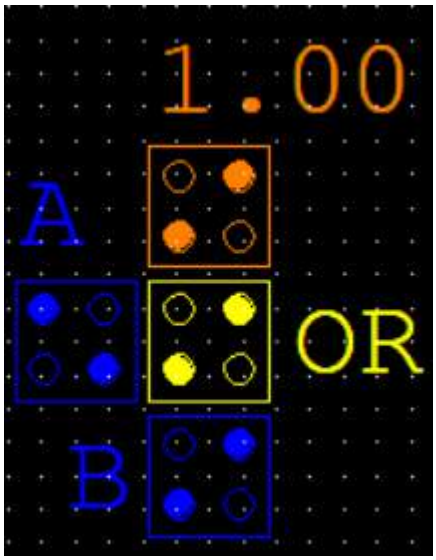

Figure. 3.5 OR gate

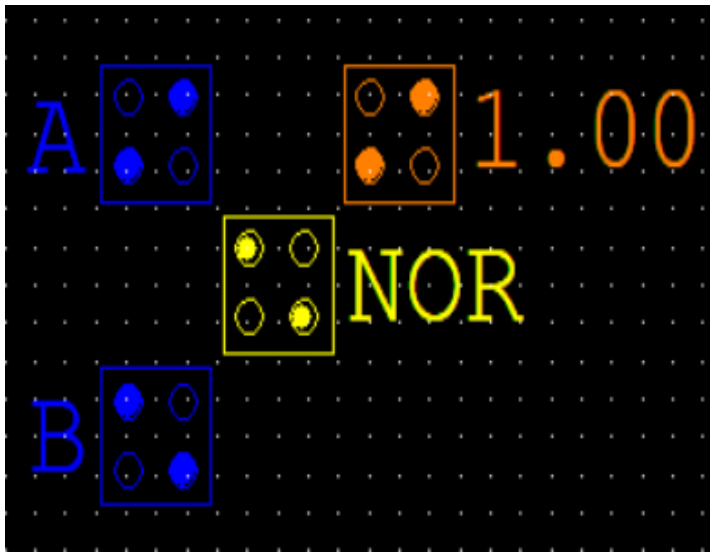

Figure. 3.6 NOR gate

Figure. 3.3 and Figure. 3.5 use 4 cells each of 90 degrees. But in Figure. 3.6 the output block i.e., ‘NOR’ block is a 180-degree cell. A 90-degree cell passes the input as it is whereas the output of a 180-degree rotated cell is the inverse of the input. For ‘AND’ gate change the polarisation to ‘-1.00’.

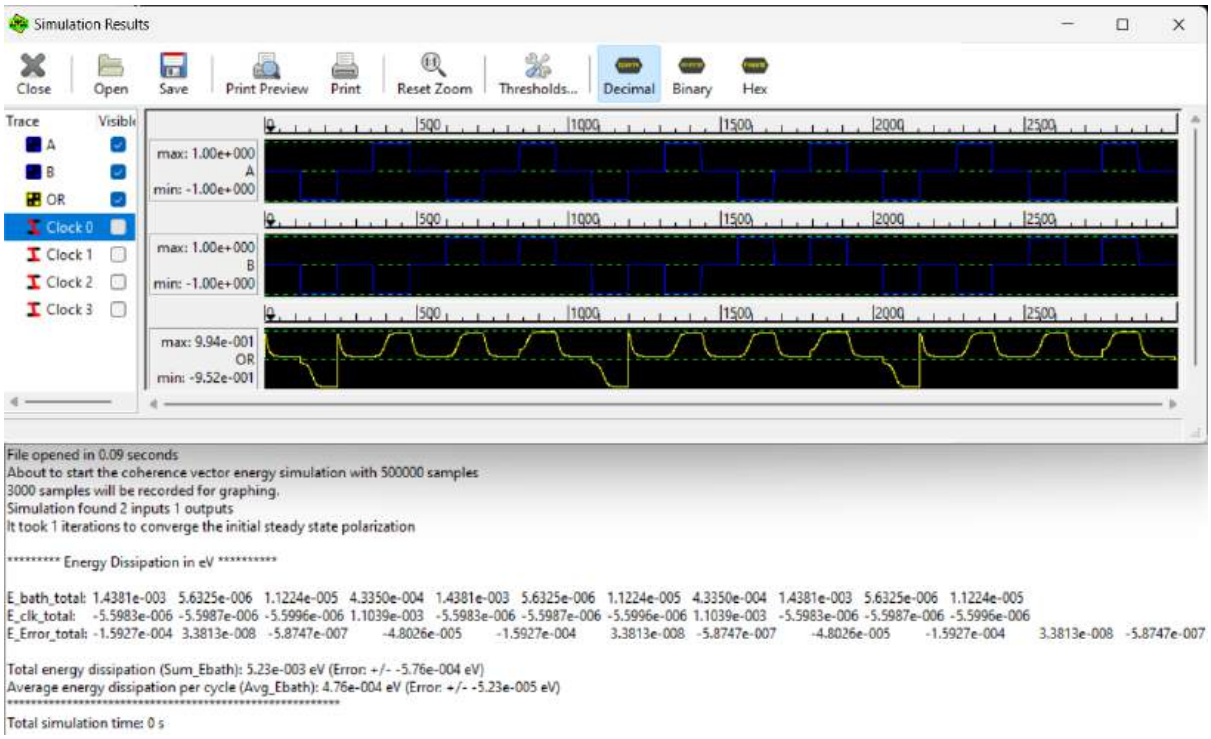

Figure. 3.7 Output of OR gate

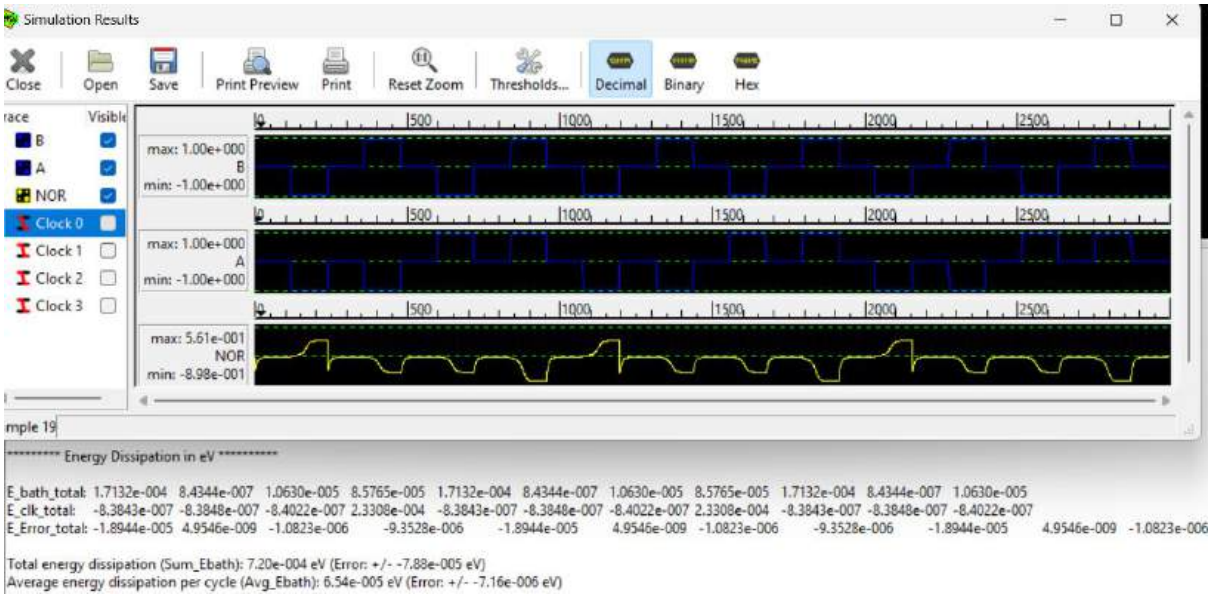

Figure. 3.8 Output of NOR gate

XOR

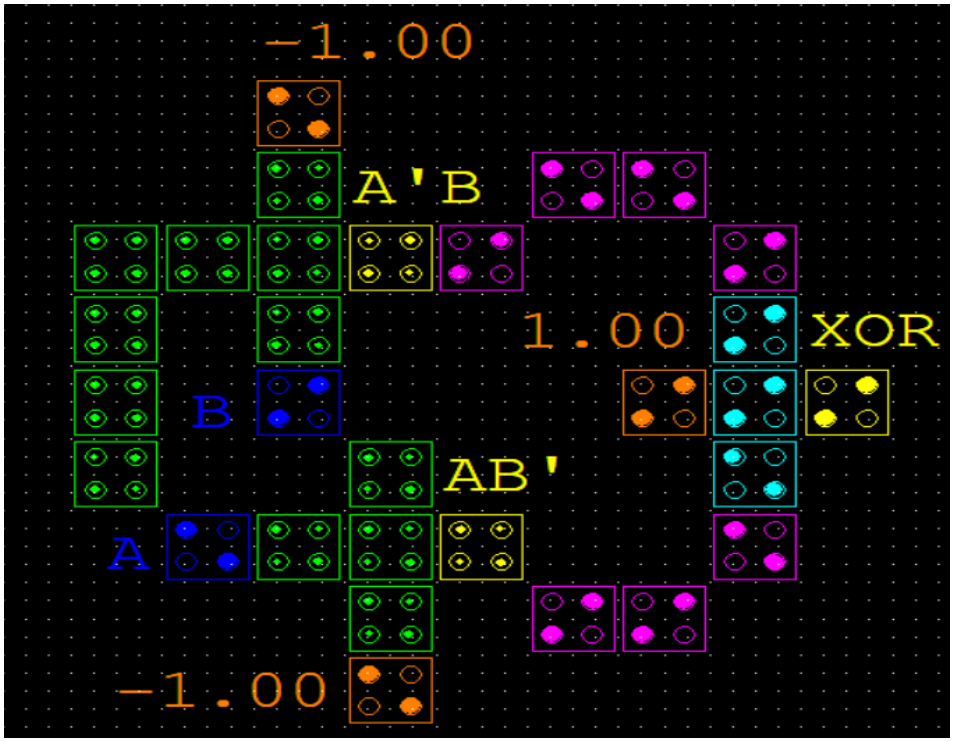

Figure. 3.9 XOR gate

Figure. 3.9 shows an XOR Gate of 30 cells constructed using the Boolean expression XOR = A'B + AB'. This design uses all the clocks to maintain the energy flow due to which there is a slight delay (latency).

Figure. 3.10 Output of XOR

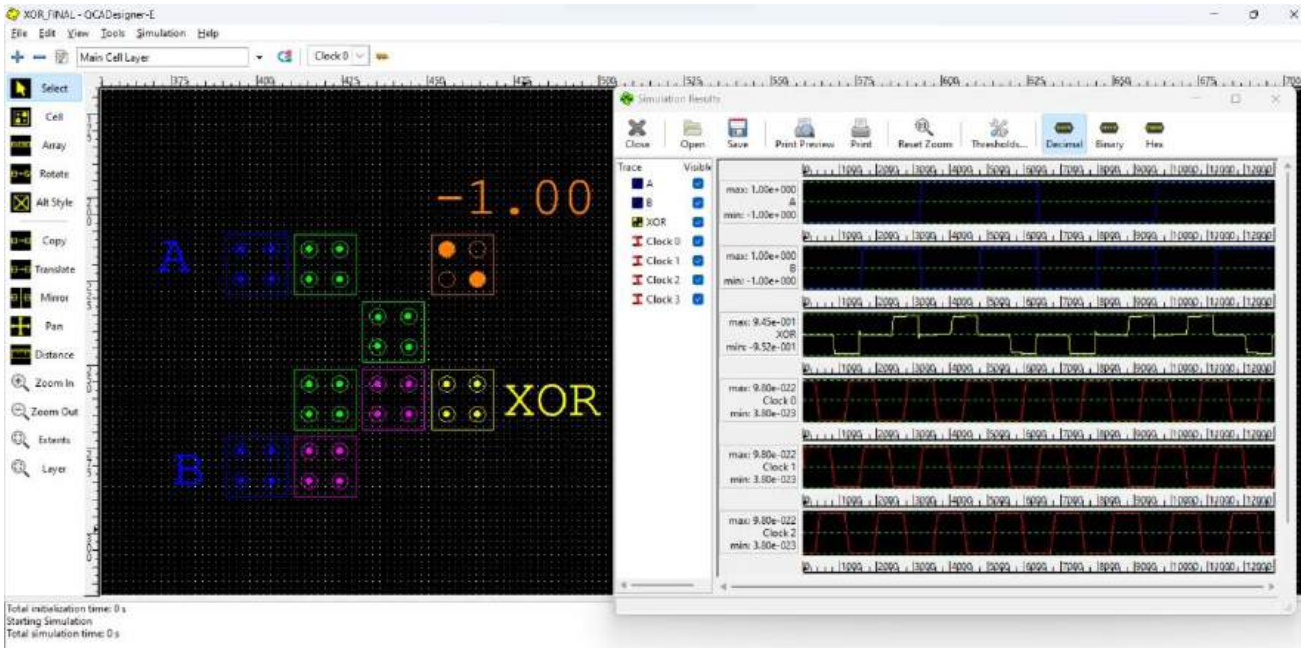

Figure. 3.11 Output of XOR (8 cells) [14]

In Figure. 3.11 to convert the design into ‘XNOR’ gate, change polarisation to ‘+1.00’.

To convert the 2 input XOR into 3 input XOR, replace the polarized cell by a third input.

2x1 MUX

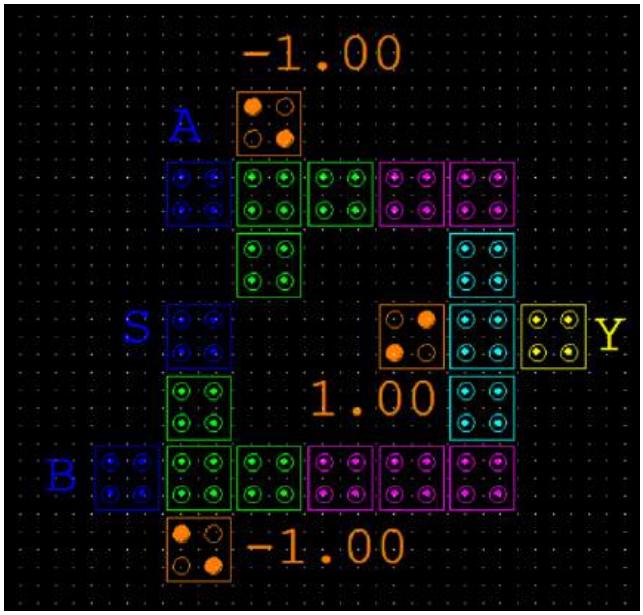

Figure. 3.12 2x1 MUX (21 cells)

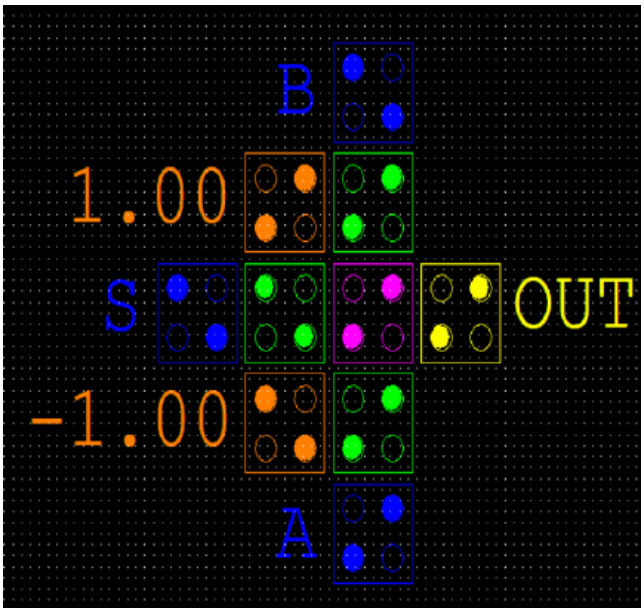

Figure. 3.13 2x1 MUX (9 cells)

Figure. 3.12 shows the design of a 2x1 MUX using the Boolean expression:

Y = AS + BS’

Figure. 3.14 Output of 2x1 MUX (9 cells)

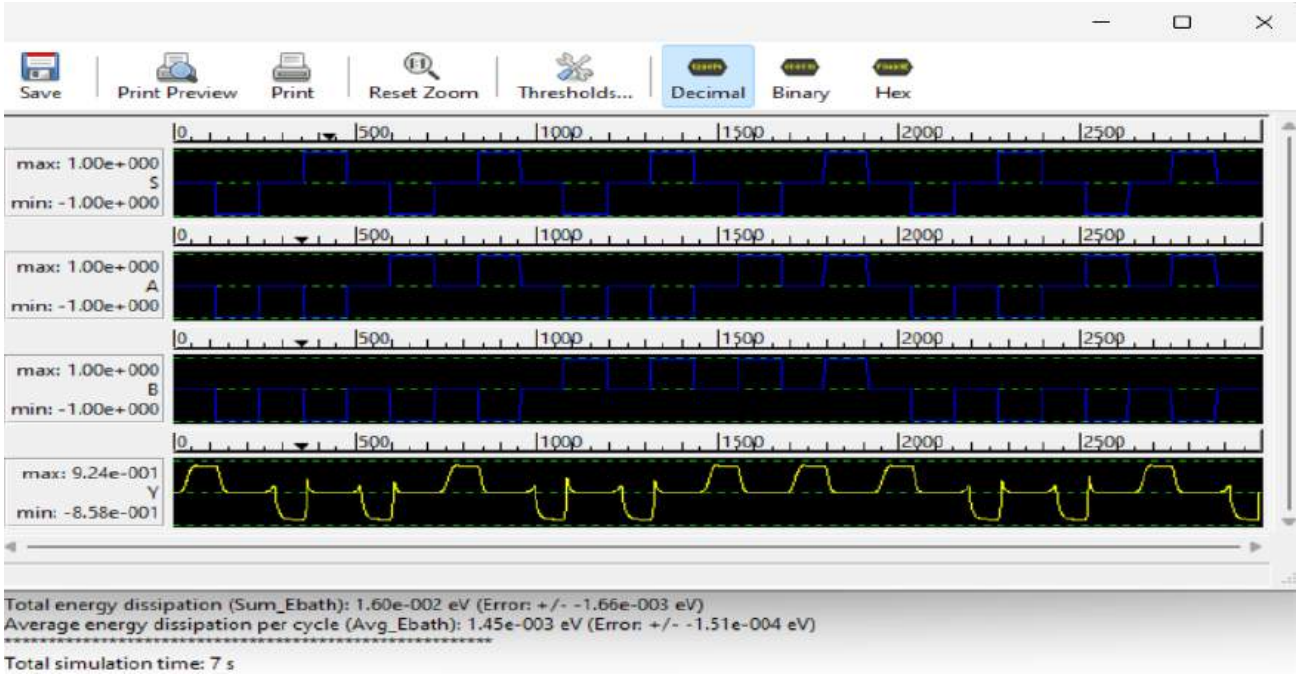

Figure. 3.15 Output of 2x1 MUX (21 cells)

The waveform of both Figure. 3.14 and Figure. 3.15 match the Table. 3.1.

Table 3.1 2x1 MUX Truth Table

A	B	S	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

HALF ADDER

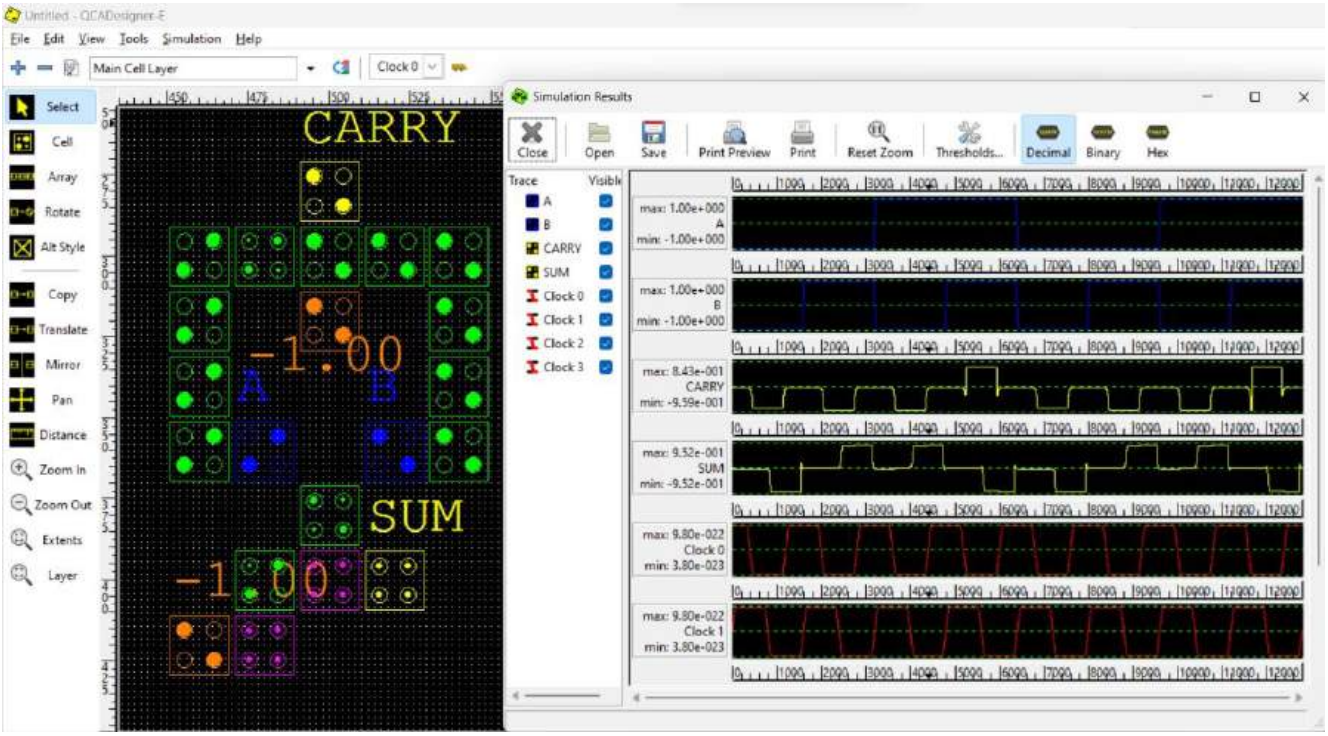

Figure. 3.16 Simulation of half adder

Figure. 3.16 shows the simulation of a half adder circuit of 21 cells. This circuit is according to the Boolean expression: SUM = A ⊕ B, CARRY = AB.

Figure. 3.17 shows a half adder design using only 10 cells with the output block rotated 180 degrees to invert the output.

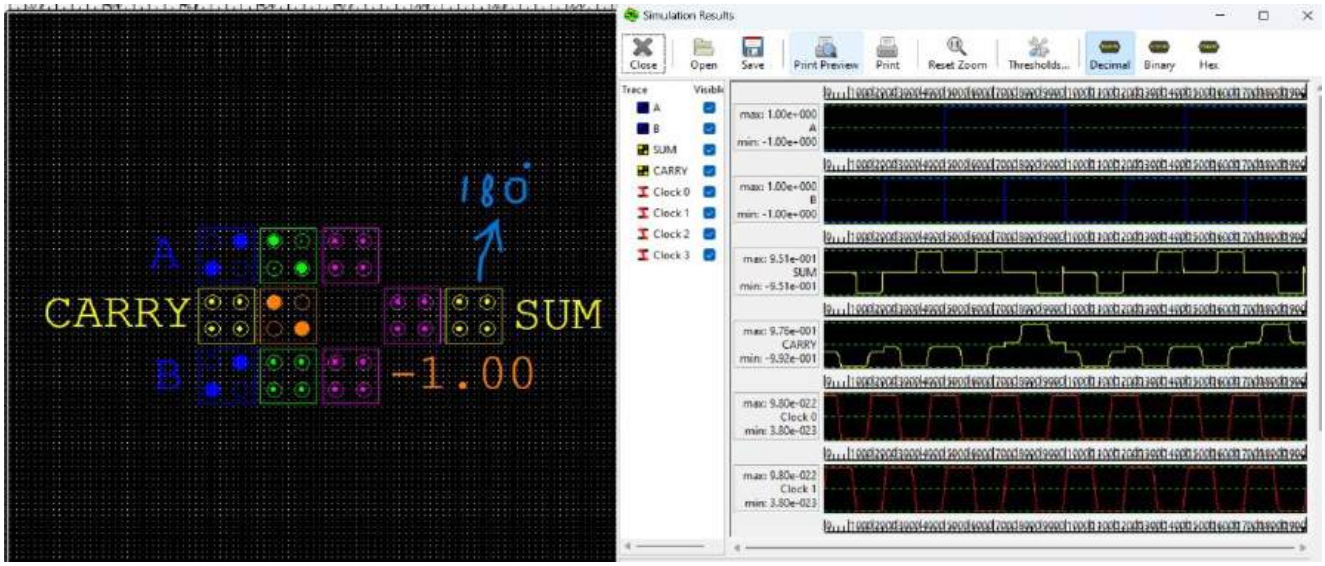

Figure. 3.17 Half adder (10 cells)

FULL ADDER

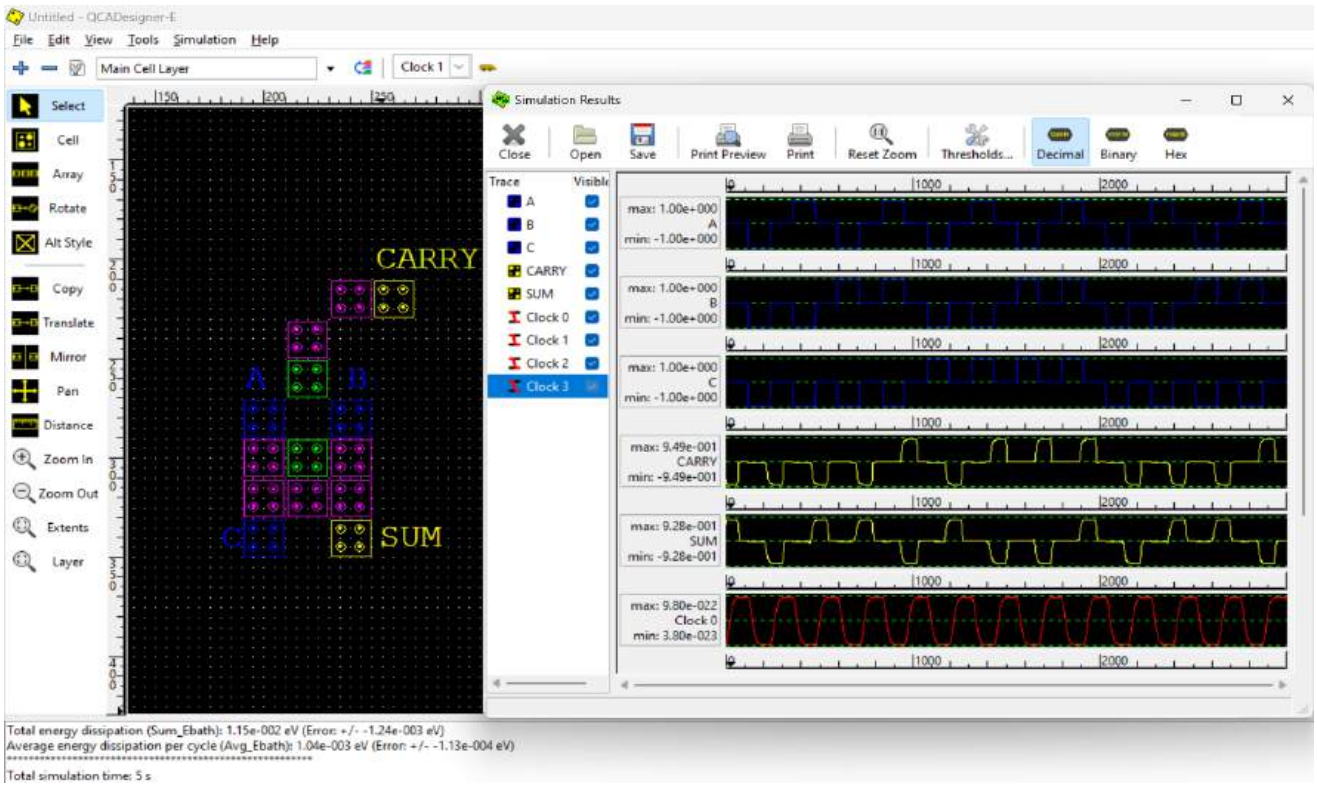

Figure. 3.18 Simulation of full adder [14]

ONE-BIT COMPARATOR

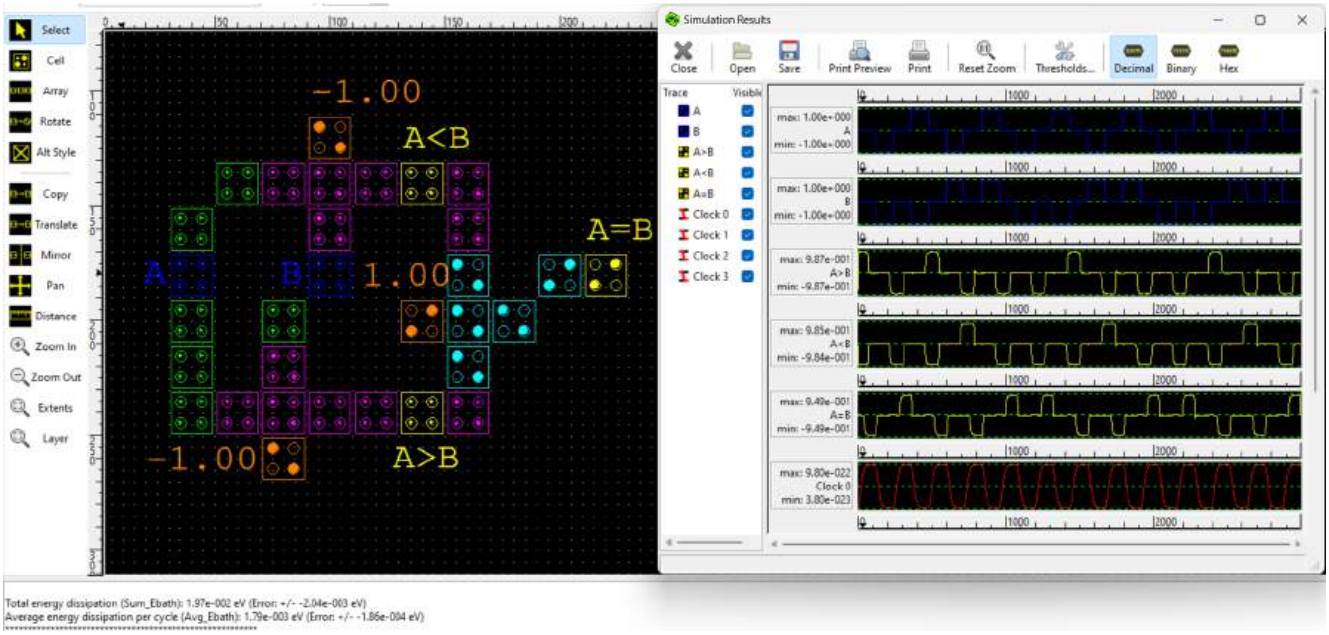

Figure. 3.19 One-bit comparator

Table. 3.2 One-bit comparator truth table

A	B	A>B	A<B	A=B
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

From the Figure. 3.19 we can observe that the output waveforms are similar to that of an XNOR gate. The output A>B is same as that of AB' and that of A<B is the same as A'B. Passing this through a NOR gate we get an XNOR gate which is in this case A=B.

CHAPTER 4

RESULTS AND DISCUSSIONS

The simulation output is compared with the results from other circuits. The detailed comparison is tabulated. To evaluate the proposed designs, we consider parameters of cell counts, occupied area, latency, cost, and the number of layers. The comparison tables show which of the design is better and more efficient. At the same time energy dissipation is also tabulated and the power dissipated can also be calculated.

Formulas [14]:

Cost = Cell count $*$ Area $*$ Latency

Power dissipated = Energy dissipated / time

Table. 4.1.1 Structural analysis of basic gates

Design	**Cell count**	**Area (μm^2)**	**Number of clocks**	**Cost**
2 input OR/AND/NOR/NAND	5	0.01	0.25	0.125
2 input OR/AND/NOR/NAND	4	0.01	0.25	0.01

Table. 4.1.2 Energy analysis of basic gates

Design	**Total energy dissipation (Sum_Ebath)**	**Average energy dissipation per cycle (Avg_Ebath)**	**Number of iterations**
Proposed 2 input OR	5.23e-003 eV	4.76e-004 eV	2
Proposed 2 input NOR	7.20e-004 eV	6.54e-005 eV	1

Table. 4.2.1 Structural analysis of XOR

Design	Cell count	Area (μm^2)	Number of clock cycles	Cost
Proposed 2 input XOR (Figure. 3.9)	30	0.04	0.75	0.9
Proposed 2 input XOR (Figure. 3.11)	8	0.01	0.50	0.04
2 input XOR [14]	10	0.01	0.50	0.05
2 input XOR [15]	51	0.08	1.25	5.1
2 input XOR [15]	48	0.06	0.75	2.16

Table. 4.2.2 Energy analysis of XOR

Design	Total energy dissipation (Sum_Ebath)	Average energy dissipation per cycle (Avg_Ebath)	Number of iterations
Proposed 2 input XOR (Figure. 3.9)	1.67e-002 eV	1.52e-003 eV	15
Proposed 2 input XOR (Figure. 3.11)	6.10e-003 eV	5.55e-004 eV	5
2 input XOR [14]	9.52e-003 eV	8.66e-004 eV	5
2 input XOR [15]	2.46e-002 eV	2.24e-003 eV	7
2 input XOR [15]	1.84e-002 eV	1.67e-003 eV	15

Table. 4.3.1 Structural analysis of adders

Design	Cell count	Area (μm^2)	Number of clock cycles	Cost
Proposed half adder (Figure. 3.16)	21	0.02	0.50	0.2
Proposed half adder (Figure. 3.17)	10	0.01	0.50	0.05
Proposed full adder (Figure. 3.18)	14	0.02	0.50	0.14

Table. 4.3.2 Energy analysis of adders

Design	Total energy dissipation (Sum_Ebath)	Average energy dissipation per cycle (Avg_Ebath)	Number of iterations
Proposed half adder (Figure. 3.16)	7.66e-003 eV	6.96e-004 eV	5
Proposed half adder (Figure. 3.17)	9.44e-003 eV	8.59e-004 eV	5
Proposed full adder (Figure. 3.18)	1.15e-002 eV	1.04e-003 eV	6

Table. 4.4.1 Structural analysis of MUX and comparator

Design	Cell count	Area (μm^2)	Number of clock cycles	Cost
Proposed 2x1 MUX (Figure. 3.12)	21	0.03	0.75	0.4725
Proposed 2x1 MUX (Figure. 3.13)	10	0.01	0.50	0.05
Proposed comparator (Figure. 3.19)	31	0.04	0.75	0.93

Table. 4.4.2 Energy analysis of MUX and comparator

Design	Total energy dissipation (Sum_Ebath)	Average energy dissipation per cycle (Avg_Ebath)	Number of iterations
Proposed 2x1 MUX (Figure. 3.12)	1.60e-002 eV	1.45e-003 eV	5
Proposed 2x1 MUX (Figure. 3.13)	1.18e-002 eV	1.07e-003 eV	13
Proposed comparator (Figure. 3.19)	1.97e-002 eV	1.79e-003 eV	12

From these tables and comparison, we can get to know the most efficient design which consumes lesser area, latency (number of clock cycles), cost and also the least energy dissipated while tunnelling. This section comprehensively evaluates the proposed designs based on key performance metrics such as cell count, occupied area, latency, cost, and energy dissipation. Trade-offs between these metrics are analysed, highlighting the impact of design choices and optimizations on circuit performance. A comparison with state-of-the-art solutions underscores the competitiveness and innovation of the proposed designs. The discussion also addresses the robustness, reliability, scalability, and practical implications of the designs, along with identifying future research directions for further advancements in QCA circuit design.

CHAPTER 5

CONCLUSION

In conclusion, this study provides a thorough comparison of different designs for Quantum-dot Cellular Automata (QCA) circuits. The results show that the proposed designs are more efficient in terms of space, energy use, and speed compared to existing ones. These findings suggest that QCA technology has the potential to improve digital circuit design and advance nanotechnology applications. Future research should focus on refining these designs and exploring practical applications to fully harness the benefits of QCA technology. Overall, this study offers valuable insights for the ongoing development of QCA-based systems in modern computing.

REFERENCES

[1] Sheikhfaal, Shadi & Angizi, Shaahin & Sarmadi, Soheil & Moaiyeri, Mohammad & Sayedsalehi, Samira. (2015). Designing efficient QCA logical circuits with power dissipation analysis. Microelectronics Journal. 46. 462-471. 10.1016/j.mejo.2015.03.016.

[2] W. Porod, C.S. Lent, and G.H. Bernstein, "Quantum-dot cellular automata: architecture, and implementation", J. of Applied Physics, vol. 74, no. 5, pp. 3556-3564, 1993.

[3] M. N. Kiselev, D. A. Lyakhov, and S. N. Molotkov, "Complex gate design for quantum-dot cellular automata based digital circuits," Proceedings of the International Conference on Electron Devices and Solid State Circuit, pp. 1-4, 2022.

[4] G. Csaba, "The quantum-dot cellular automaton quantum computer," Nanotechnology, vol. 27, no. 24, p. 245201, 2016.

[5] S. Mukhopadhyay, A. Raychowdhury, and K. Roy, "Nanomagnet logic: overcoming fundamental challenges for energy-efficient computing," Proceedings of the IEEE, vol. 101, no. 2, pp. 249-271, 2013.

[6] R. L. Ruiz et al., "Design of low-power reversible circuits using quantum-dot cellular automata," Journal of Low Power Electronics and Applications, vol. 8, no. 1, pp. 1-10, 2018.

[7] J. Eshraghian et al., "Fault tolerance in quantum-dot cellular automata (QCA) circuits," Microelectronics Reliability, vol. 47, no. 12, pp. 2067-2075, 2007.

[8] S. K. M. Shamsuddin and M. M. Rahman, "Fault-tolerant design of reversible arithmetic logic unit using quantum-dot cellular automata," Journal of Computational Electronics, vol. 19, no. 4, pp. 1293-1309, 2020.

[9] M. Fathipour and S. A. Moosavi, "Spintronics-based memory design using quantum-dot cellular automata," Microelectronics Journal, vol. 44, no. 1, pp. 54-61, 2013.

[10] K. Walus, T. J. Dysart, G. A. Jullien, and R. A. Budiman, "QCADesigner: a rapid design and Simulation tool for quantum-dot cellular automata," IEEE Transactions on Nanotechnology, vol. 3, pp. 26-31, 2004.

[11] J. Timler and C. S. Lent, "Power gain and dissipation in quantum-dot cellular automata," Journal of Applied Physics, vol. 91, pp. 823-831, Jan 15 2002.

[12] C. S. Lent, L. Mo, and L. Yuhui, "Bennett clocking of quantum-dot cellular automata and the limits to binary logic scaling," Nanotechnology, vol. 17, p. 4240, 2006.

[13] FSillT. (n.d.). QCADesigner-E Manual. Retrieved from https://github.com/FSillT/QCADesigner-E/blob/master/Manual_QDE.

[14] Safaiezadeh, B., Haghparast, M., & Kettunen, L. (2023, February 27). Novel Efficient Scalable QCA XOR and Full Adder Designs. arXiv:2302.13946 [cs.ET]. Retrieved from https://doi.org/10.48550/arXiv.2302.13946.

[15] M. Beigh, M. Mustafa and F. Ahmad, "Performance Evaluation of Efficient XOR Structures in Quantum-Dot Cellular Automata (QCA)," *Circuits and Systems*, Vol. 4 No. 2, 2013, pp. 147-156. doi: 10.4236/cs.2013.42020.