

On-chip Clock Multiplier (Phase lock loop)

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Abstract— This paper discusses the block level schematic that comprises the Phase lock loop and its various applications such as clock recovery, skew elimination and primarily as, on-chip clock multiplier. It further discusses the Phased lock loop CMOS circuit and the working of the analog circuit and the architecture used to reduce jitter and overall PLL noise.

Keywords— Phased lock loop; filter loop; voltage controlled oscillator, clock generation; CMOS.

I. INTRODUCTION

Phase lock loop is a feedback control system which consists of a phase detector, voltage controlled oscillator (VCO), and a low pass filter. The oscillator maintains a constant phase angle relative to an input reference signal and is used to detect the phase difference between two signals. The PLL primary function is to generate stable output high frequency from a fixed lower frequency signal so the VCO output frequency can be a multiple of the reference input frequency. Therefore, used to generate a clock signal, synchronized or locked with input signal [1]

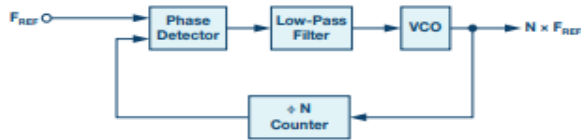


Fig 1: Block diagram of Phased Lock Loop [2]

II. BLOCK DIAGRAM

The PLL consists of the following parts: -

1. **Phase Frequency Detector:** The PFD compares the frequency and phase of the reference input to the frequency and phase of the feedback and gives the proportional phase difference as output. The circuit consists of two D-type flip flops. One output enables a positive current source while the other output enables a negative current source [2], and identifies which signal is leading or lagging, independent of the duty cycle.

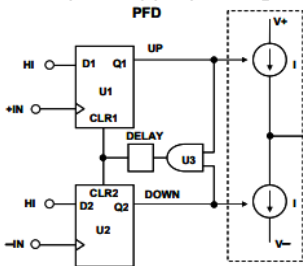


Fig 2: Schematic of PFD [3]

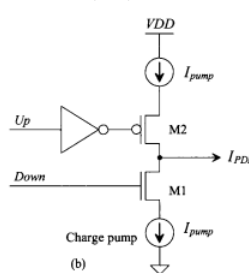


Fig 3: Schematic of Charge Pump [1]

2. **Loop Filter:** The loop filter consists of an RC network where the capacitors are made with MOSFET gate oxide, and the resistors are made with the n-well implant. It is an integral component to design a low-jitter and stable PLL, as it attenuates the reference signal level on output and shapes the phase noise characteristics of the output and ensures a timely locking of the loop.
3. **Voltage Control Oscillator:** The VCO is required to generate a range of higher frequencies as the output of the VCO is a higher multiple of the reference frequency.

Voltage-controlled oscillators contain a variable tuning element (varactor diode) which varies its capacitance with the input voltage, and the output is a proportionate range of frequencies [2]. The PLL is the control system for the VCO.

III.

WORKING OPERATION

The VCO, of the PLL, produces a signal which enters the phase-frequency detector and the phase of the signals from VCO and the reference signal are compared, as a result, a difference or error voltage is produced which corresponds to the phase difference between these two signals. The error signal passes through the loop filter, which removes any high-frequency elements on the signal and is then applied to the control terminal of the VCO as a tuning voltage, where the VCO tries to reduce the phase difference and the frequency of the VCO towards that of the reference until the capture range is reached, post which the loop is said to be locked. Once locked, a steady-state error voltage is produced indicating the two signals have an equal frequency. So it is used to generate clock signals.

The PLL design includes differential circuit topology for the VCO with common-mode rejection for minimizing the phase noise from the power supply, and the low pass filter is precisely placed to ensure lowest rms jitter [2].

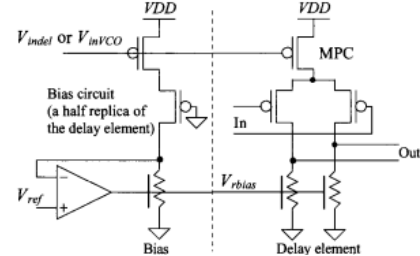


Fig 4: CMOS Circuit of VCO [1]

IV.

APPLICATION

Our PLL on-clock clock multiplier will generate 40-100 MHz clock frequency from a low-frequency input clock of 5-12 MHz and minimize noise, a low N value is desired. Clocking tends to be fixed frequency, so the frequencies are chosen to ensure that the reference frequency is an integer multiple of the input frequency [3]. For clocking circuits, the rms jitter of the clock is the key performance parameter.

V.

CONCLUSION & FUTURE SCOPE

Therefore, it is evident that emphasis should be laid on the design of the PLL with uniform phase difference and a low jitter coefficient to be appropriately used as an on-chip clock.

VI.

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