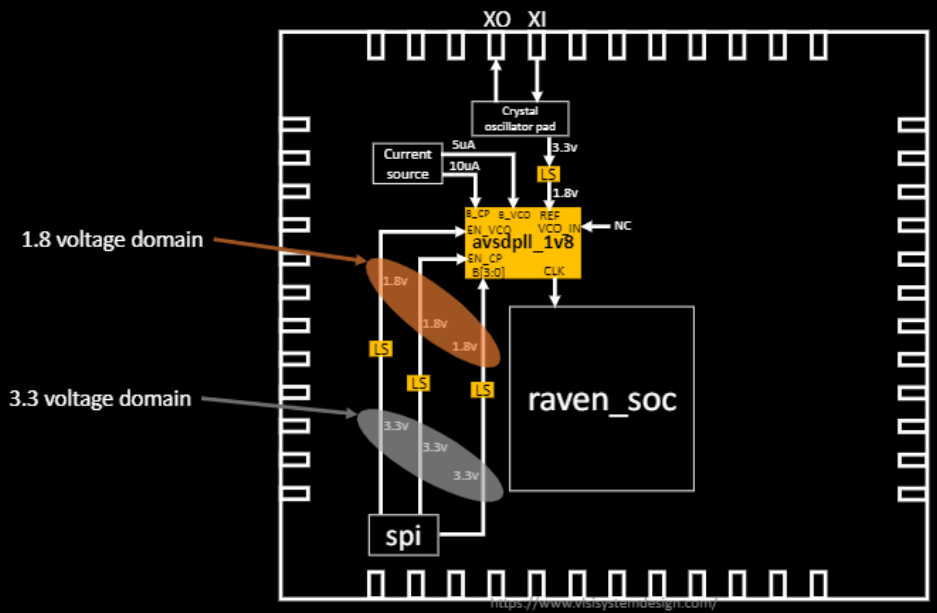
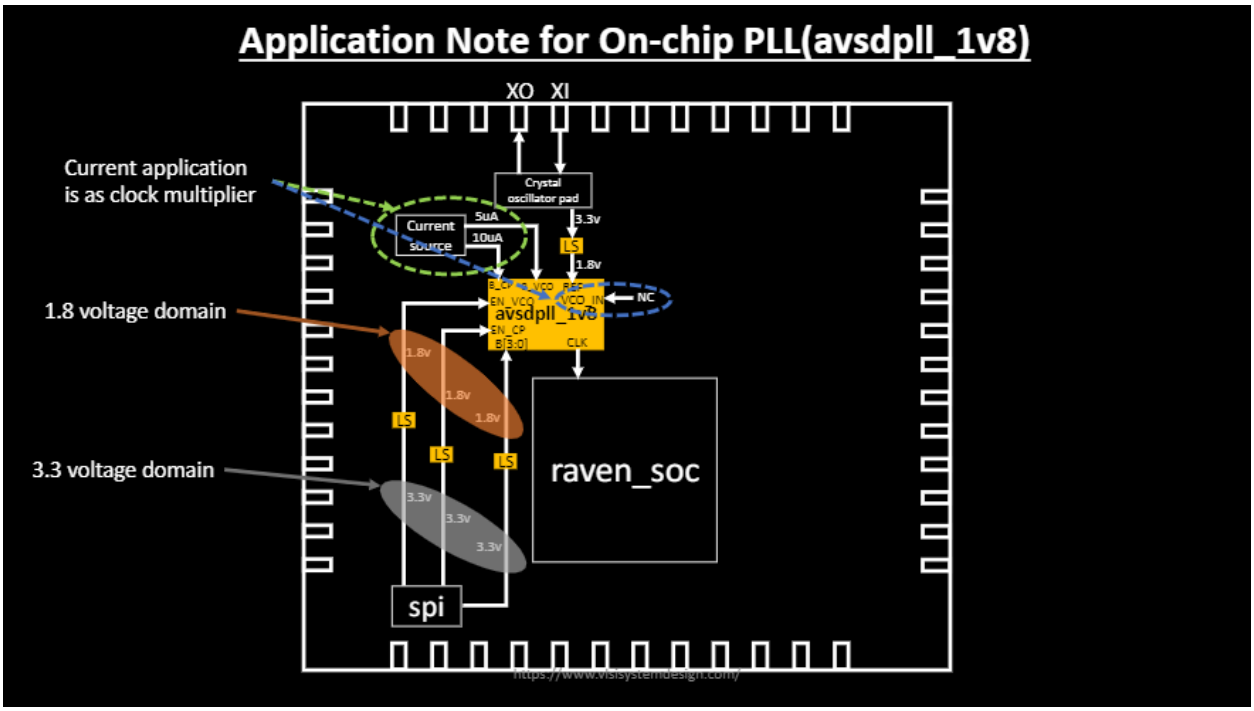
On-chip PLL (avsdpll_3v3) spec sheet for 180nm tech node

- Specs released under APACHE LICENSE 2.0
- Please contact Kunal at kunalpghosh@gmail.com in case of any doubts

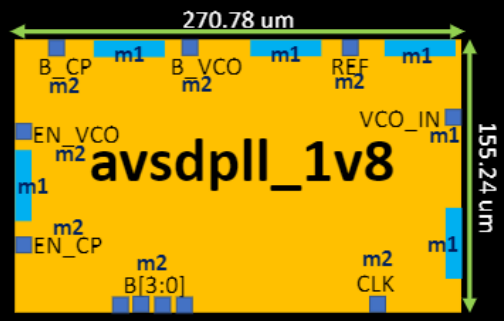
Application Note for On-chip PLL(avsdpll_1v8)



Application Note for On-chip PLL(avsdpll_1v8)



avsdpll_1v8 preferred dimensions, pin locations and metal layers



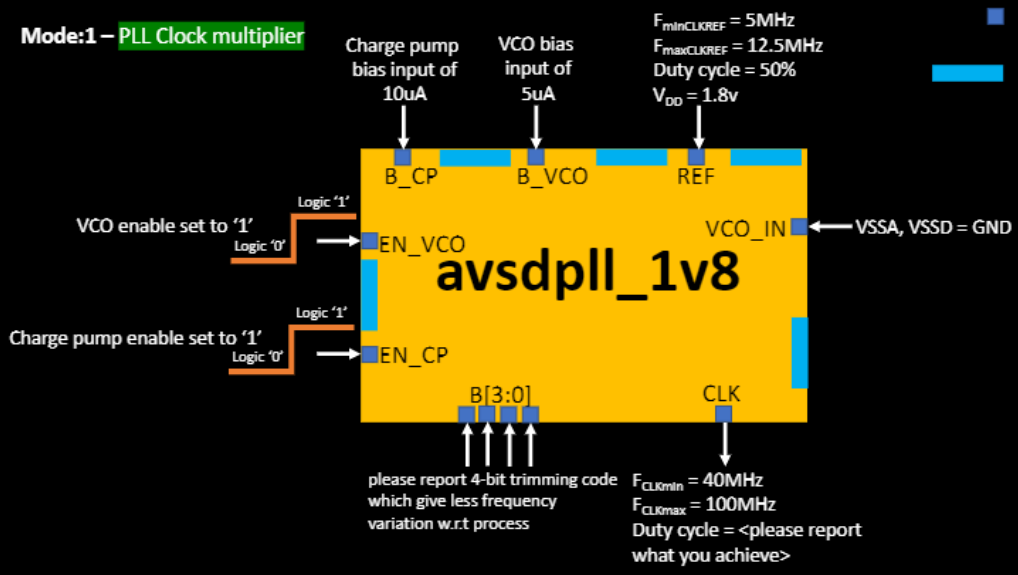
Signal pins – 0.34um x 0.34um

VDDA, VDDD, VSSA, VSSD pins
3um x 0.34um

https://www.vlsisystemdesign.com/

avsdpll_1v8 operating modes

Mode:1 – PLL Clock multiplier



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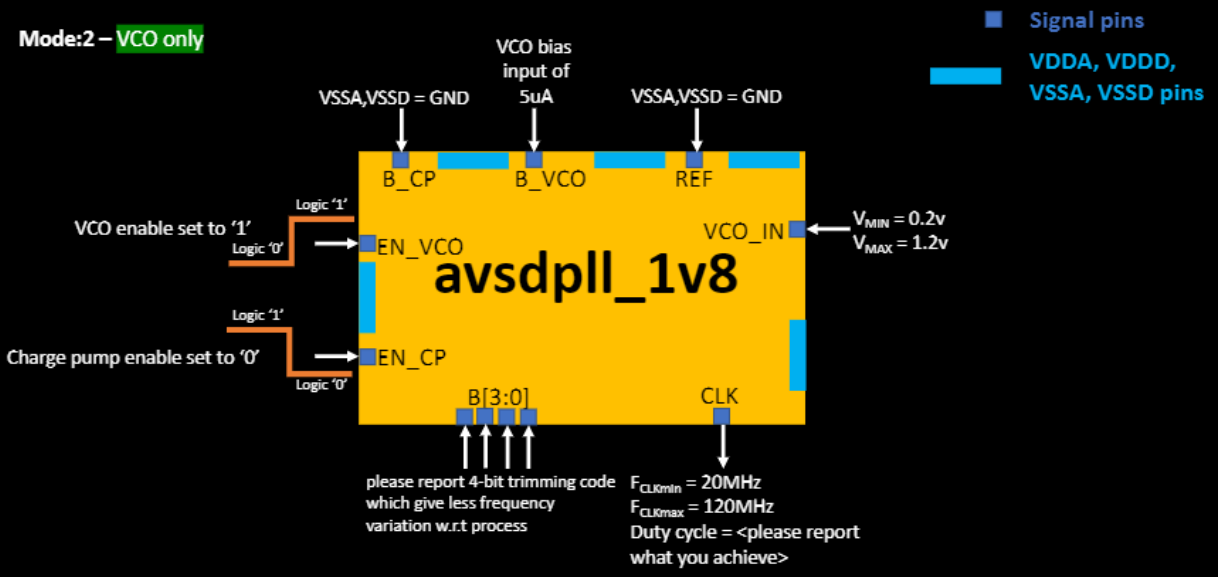
avsdpll_1v8 operating modes



avsdpll_1v8 plots and values needed

1) Jitter(RMS) at input F_{REFCLK} of 10MHz in PLL mode (expected = 30ps) – Post tape-out

2) F_{CLK} vs VCO at T=-40C, +27C, +150C with VDD = 1.8v and recommended trimming bit code B[3:0]

3) F_{CLK} vs VCO at T=+27C, VDD = 1.8v and B[3:0] = 4'b0000 to 4'b1111

4) F_{CLK} vs VDD at T=-40C, +27C, +150C with VCO = 0.2v and recommended trimming bit code B[3:0]

avsdpll_1v8 plots and values needed

5) F_{CLK} vs T (-40C to 160C) at VDD = 1.6v, 1.8v, 1.98v with VCO = 0.2v and recommended trimming bit code B[3:0]

6) IDDA vs VCO at T=+27C, VDD = 1.8v and B[3:0] = 4'b0000 to 4'b1111 (VCO mode)

7) IDDD vs VCO at T=+27C, VDD = 1.8v and B[3:0] = 4'b0000 to 4'b1111 (VCO mode)

8) Duty cycle vs VDDR[1.6V to 2V] at F_{CLKREF} = 10MHz and recommended trimming bit code B[3:0] (PLL mode)