# Design and Simulation of an Ultra-Low-Voltage (450 mV) Differential Amplifier Using Subthreshold-Biased MOSFETs

Devanshu Parikh
*Department of Electronics and Communication*
*Institute of Technology, Nirma University*
Ahmedabad, India
22bec029@nirmauni.ac.in

Dhruval Vachhani
*Department of Electronics and Communication*
*Institute of Technology, Nirma University*
Ahmedabad, India
22bec034@nirmauni.ac.in

***Abstract*—This paper presents the design and simulation of an ultra-low-voltage differential amplifier implemented in 180 nm CMOS technology operating at a supply voltage of 450 mV. The amplifier architecture employs a cascoded fully differential input stage with a current mirror active load configuration, with all transistors biased in the subthreshold region to achieve minimal power consumption. The design methodology emphasizes systematic optimization of transistor dimensions and bias conditions to balance competing requirements of gain, bandwidth, noise performance, and energy efficiency. Simulation results demonstrate a voltage gain of 18.26 V/V corresponding to 25.2 dB, unity gain frequency of 10.1 MHz, and 3 dB bandwidth of 1.47 MHz while consuming only 432 nW of power. The amplifier achieves a common-mode rejection ratio of 24.06 dB and exhibits low noise characteristics with an output noise spectral density of $4.2754 \times 10^{-7}$ $\mathbf{V^2/Hz}$, translating to an input-referred noise of $2.200 \times 10^{-9}$ $\mathbf{V^2/Hz}$. These performance metrics validate the effectiveness of subthreshold circuit design techniques for ultra-low-power analog applications.**

***Index Terms*—Ultra-low-voltage amplifier, subthreshold operation, differential amplifier, low-power CMOS, 180 nm technology, current mirror load, weak inversion, energy-efficient design, biomedical applications.**

## I. Introduction

The demand for ultra-low-voltage, ultra-low-power analog circuits has grown substantially with the proliferation of battery-operated portable devices, wireless sensor networks, biomedical implants, and energy harvesting systems. In these applications, extending battery lifetime and reducing power consumption are critical design objectives. Operational amplifiers form the cornerstone of analog signal processing chains, and their power efficiency directly impacts overall system performance.

Recent research has focused on developing amplifier topologies that can operate reliably at supply voltages below 0.5 V while maintaining acceptable gain, bandwidth, and noise characteristics. Several design techniques have emerged to address the challenges of ultra-low-voltage operation. In a seminal work, He *et al.* [1] presented a 0.5 V wideband amplifier for continuous-time complex delta-sigma modulators using 130 nm CMOS technology, achieving 51 dB DC open-loop gain, 112 MHz unity gain bandwidth, and 67 degree phase margin while consuming 600 $\mu$W with a gate-input two-stage topology and DC common-mode feedback.

Majumder *et al.* [2] proposed an ultra-low-power low-voltage class AB fully differential operational amplifier in 45 nm CMOS technology. Operating from a dual supply of $\pm$0.4 V, this design achieved 74.6 dB open-loop gain, 1 MHz unity gain frequency, and 50 degree phase margin with only 0.39 $\mu$W power consumption. The design utilized a cascoded input stage with indirect frequency compensation and a push-pull output stage for rail-to-rail swing.

Magnelli *et al.* [3] demonstrated a 75 nW, 0.5 V subthreshold CMOS operational amplifier fabricated in 180 nm technology. This work presented a systematic design procedure for subthreshold amplifiers, achieving 70 dB DC gain and 18 kHz gain-bandwidth product while dissipating just 75 nW. The amplifier employed a conventional two-stage Miller-compensated topology with all transistors operating in weak inversion.

These works collectively demonstrate that subthreshold operation represents a highly effective approach for achieving ultra-low-power consumption. The exponential relationship between gate-source voltage and drain current in the subthreshold region enables larger transconductance-to-current ratios compared to strong inversion operation, resulting in improved power efficiency for a given performance level.

## II. Limitations of Current Technology

Despite significant progress in ultra-low-voltage amplifier design, several fundamental challenges persist in current implementations. The most critical limitation stems from reduced voltage headroom at sub-0.5 V supply levels, which severely constrains output swing, input common-mode range, and signal-to-noise ratio. Many existing designs sacrifice dynamic range to maintain proper transistor biasing, while cascode stages become difficult to implement as each stacked transistor requires additional voltage headroom to remain in saturation.

Process, voltage, and temperature (PVT) variations pose substantial challenges for ultra-low-voltage circuits. Threshold voltage mismatches of 10-20 mV significantly impact amplifier offset, common-mode rejection ratio (CMRR), and

power supply rejection ratio (PSRR). Temperature variations affect the subthreshold slope factor and exponentially influence drain current, leading to considerable performance degradation across operating conditions.

Frequency compensation becomes problematic at ultra-low voltages due to limited bandwidth of individual stages and increased influence of parasitic poles. Conventional Miller compensation requires larger compensation capacitors as bias currents decrease, consuming significant silicon area and potentially limiting speed. Noise performance presents another fundamental constraint, as shot noise associated with weak inversion operation can result in higher input-referred noise compared to strong inversion designs at equivalent bias currents.

Common-mode rejection and power supply rejection degrade substantially at ultra-low voltages due to reduced output impedance of current sources operating with minimal drain-source voltage. Current designs also exhibit limited bandwidth for a given power budget, as the achievable unity gain frequency remains constrained by the fundamental relationship between transconductance, load capacitance, and bias current.

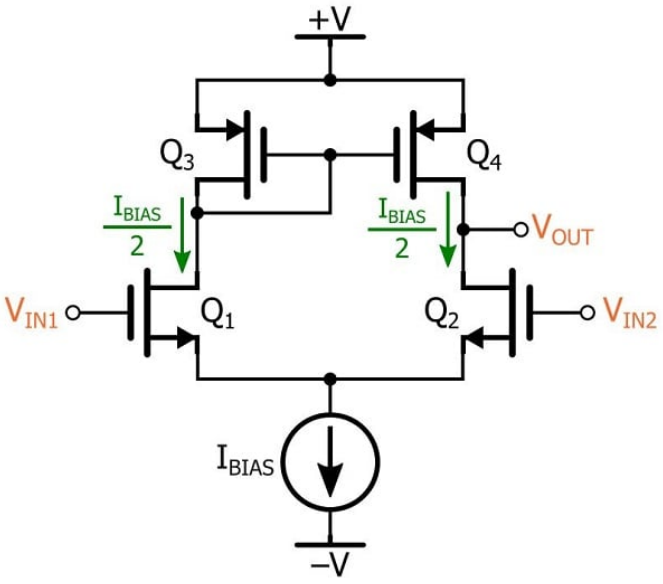


Fig. 1. Block diagram of the proposed ultra-low-voltage differential amplifier showing the differential input stage with current mirror load configuration.

## III. Proposed Solution and Methodology

To address the limitations of existing ultra-low-voltage amplifier designs, this project proposes a fully differential operational amplifier implemented in 180 nm CMOS technology operating at 450 mV. The design methodology emphasizes systematic optimization of the subthreshold operating regime to achieve an optimal balance among power consumption, gain, bandwidth, and noise performance.

The proposed architecture employs a cascoded fully differential input stage with a current mirror active load to maximize voltage gain while maintaining operation at ultra-low supply voltage. The current mirror topology increases the output impedance at the drain nodes of the differential pair through precise current replication, thereby enhancing the voltage gain without requiring additional gain stages that would complicate frequency compensation. All transistors in the input stage are biased in the subthreshold region to exploit the superior transconductance-to-current ratio characteristic of weak inversion operation.

A systematic design procedure was developed to optimize transistor dimensions and bias currents. The procedure establishes minimum transistor channel lengths based on DC gain requirements and drain-induced barrier lowering effects. Bias currents are selected to meet input-referred noise specifications while ensuring all devices remain in weak inversion. Transistor aspect ratios are calculated to achieve the desired gate-source voltages that guarantee subthreshold operation with adequate margin from moderate inversion. The complete design was simulated using Cadence Virtuoso with GPDK 180 nm CMOS process models, with extensive corner analysis performed to verify robust operation across process, voltage, and temperature variations.

## IV. Design Specifications

### A. Technology and Supply Parameters

The technology node selected for this design is 180 nm CMOS, which provides an excellent balance between achieving ultra-low-power operation and maintaining manageable process variations for analog circuit design. The supply voltage is set to 450 mV, representing one of the lowest reported operating voltages for fully differential amplifiers. This extremely low supply voltage is feasible due to subthreshold operation of all transistors, which requires minimal voltage headroom compared to strong inversion designs.

All transistors in the amplifier are biased in the subthreshold region to enable ultra-low power consumption. Channel lengths for all devices are set to 180 nm to maximize output impedance and minimize drain-induced barrier lowering (DIBL) effects. The PMOS transistors serving as active loads (Q3, Q4) have a width of 80 $\mu$m, while the NMOS differential input pair transistors (Q1, Q2) are sized at 40 $\mu$m width. The tail current source transistor (Q5) is similarly sized at 40 $\mu$m width and is biased with a gate voltage of 350 mV, which places it firmly in the subthreshold region and establishes the DC bias current for the differential pair. All transistor dimensions were optimized to achieve adequate transconductance while ensuring reliable weak inversion operation across process, voltage, and temperature corners.

### B. Input Signal Specifications

The differential input signals V1 and V2 are applied to the gates of the NMOS differential pair. Both inputs are sinusoidal signals with the following characteristics:

- DC Bias Level: 270 mV
- Amplitude: 10 mV
- Frequency: 10 kHz

TABLE I
DESIGN SPECIFICATIONS SUMMARY

| Parameter | Value |
|---|---|
| Process Technology | 180 nm CMOS |
| Supply Voltage (VDD) | 450 mV |
| Substrate Bias (VSS) | 0 V |
| Tail Bias Voltage (Vbias) | 350 mV |
| **Input Signals:** | |
| V1 DC Level | 270 mV |
| V1 Amplitude | 10 mV |
| V1 Frequency | 10 kHz |
| V1 Phase | 0° |
| V2 DC Level | 270 mV |
| V2 Amplitude | 10 mV |
| V2 Frequency | 10 kHz |
| V2 Phase | 180° |
| **Transistor Dimensions:** | |
| PMOS Load (Q3, Q4): W | 80 $\mu$m |
| NMOS Input (Q1, Q2): W | 40 $\mu$m |
| Tail Current (Q5): W | 40 $\mu$m |
| All Transistor Lengths | 180 nm |
| **Operating Conditions:** | |
| Operating Region | Subthreshold |
| Supply Configuration | Single Supply |
| Input Configuration | Fully Differential |
| Output Configuration | Single-Ended |

- V1 Phase: 0°
- V2 Phase: 180°

The 180-degree phase difference creates a fully differential input signal that is symmetric about the common DC level, allowing the amplifier to operate in true differential mode and maximizing the common-mode rejection capability while enabling observation of differential amplification characteristics.

### C. Bias Configuration

The bias voltage for the tail current source is generated from an external voltage source set to 350 mV. This bias voltage is critical to establishing the subthreshold operating point of the tail transistor. The 350 mV value is carefully chosen to be below the threshold voltage of the NMOS transistor (typically around 400-450 mV in 180 nm technology), ensuring exponential current-voltage characteristics in the subthreshold region.

The 10 kHz frequency and 10 mV amplitude are selected to provide adequate signal for transient analysis while remaining well within the linear operating region of the amplifier. The 270 mV DC bias level for the input signals is chosen to position the differential pair transistors near the optimal operating point within the subthreshold region while maintaining adequate headroom from the ground and supply rails.

## V. CIRCUIT ARCHITECTURE AND CONFIGURATION

The circuit diagram shows the complete implementation of the proposed ultra-low-voltage differential amplifier. The

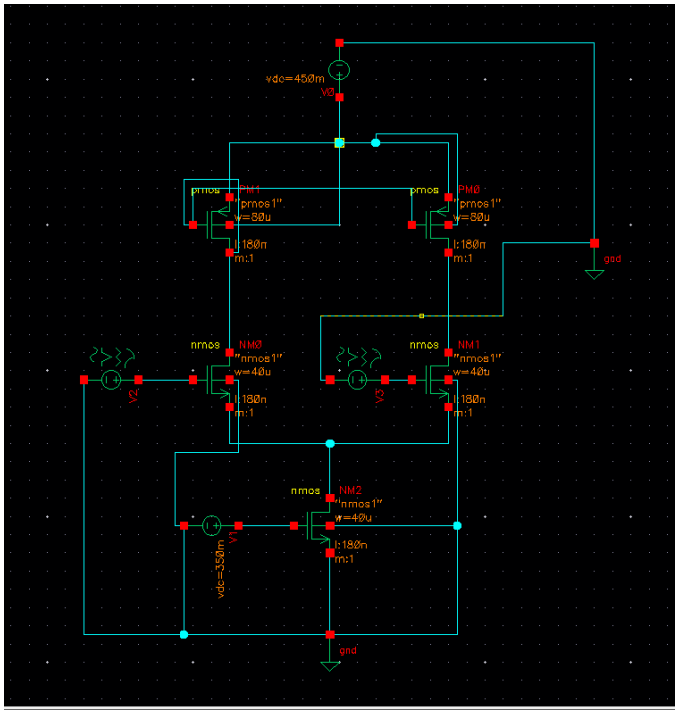


Fig. 2. Complete schematic of the ultra-low-voltage differential amplifier with current mirror active load configuration.

design comprises two main functional blocks: the differential input stage and the current mirror load biasing network.

The input stage employs NMOS transistors Q1 and Q2 configured as a fully differential pair with a current mirror active load. The differential input signals V1 and V2 are applied to the gates of Q1 and Q2 respectively. The tail current for the differential pair is provided by transistor Q5, which is biased with a DC voltage of 350 mV applied to its gate. This 350 mV bias voltage places the tail transistor in the subthreshold region, establishing a stable current source with exponential sensitivity that maintains consistent bias across the differential pair despite variations in process and temperature.

The current mirror load comprises PMOS transistors Q3 and Q4. The left PMOS transistor (Q3) is diode-connected with its gate and drain shorted together, establishing the DC bias voltage and serving as the reference for the current mirror. This diode-connected configuration produces a logarithmic voltage-current relationship in the subthreshold regime, providing stable biasing. The right PMOS transistor (Q4) operates as the mirror transistor, replicating the reference current established by Q3 and providing the active load for the right branch of the differential pair.

The current mirror topology provides significantly higher output impedance compared to passive resistive loads. The output impedance at the drain nodes of the differential pair is approximately determined by the channel length modulation parameter and the early voltage effects of the active load transistors. This enhanced output impedance directly translates to higher voltage gain through the relationship $A_v = g_m \cdot R_{out}$.

All transistors maintain channel lengths of 180 nm to maximize output impedance and minimize short-channel ef-

fects. The aspect ratios are carefully chosen such that PMOS transistors (80 $\mu$m width) provide adequate current driving capability in the load mirrors, while NMOS transistors (40 $\mu$m width) in the differential pair balance transconductance requirements.

## VI. Working Principle

### A. Subthreshold Operation

The core of the amplifier operates in the subthreshold or weak inversion region, where the gate-source voltage is below the threshold voltage ($V_{GS} < V_{TH}$). In this operating regime, the drain current is governed by diffusion rather than drift, resulting in an exponential relationship:

$$I_D \approx I_0 \left( \frac{W}{L} \right) e^{(V_{GS} - V_{TH})/(nV_T)} \tag{1}$$

where $I_0$ is the specific current, W/L is the transistor aspect ratio, $V_{TH}$ is the threshold voltage, $n$ is the subthreshold slope factor (typically 1.3–1.5), and $V_T \approx 26$ mV is the thermal voltage at room temperature.

The transconductance in subthreshold is given by:

$$g_m = \frac{I_D}{nV_T} \tag{2}$$

This is significantly higher than the transconductance-to-current ratio achievable in strong inversion, where $g_m/I_D = 2/(V_{GS} - V_{TH})$. For the same amount of bias current, subthreshold operation provides substantially higher transconductance, directly enabling higher voltage gain and bandwidth with minimal power consumption.

### B. Differential Pair and Current Mirror Load

The differential pair (Q1, Q2) receives differential input signals V1 and V2. The tail current established by Q5 (biased at 350 mV) divides between the two differential transistors based on their relative gate-source voltages. A differential input voltage $V_{in,diff} = V_1 - V_2$ produces proportional changes in the drain currents of Q1 and Q2. This drain current difference flows through the PMOS active load, producing a differential output voltage.

The current mirror load (Q3-Q4) configured with Q3 diode-connected establishes a logarithmic voltage-current relationship in subthreshold:

$$V_{DS,Q3} = nV_T \ln \left( \frac{I_{D,Q3}}{I_0} \right) + V_{TH} \tag{3}$$

The current flowing through Q3 is replicated by Q4 through the current mirror action. The output impedance of the current mirror is approximately:

$$R_{out} \approx r_o = \frac{1}{\lambda I_D} \tag{4}$$

where $\lambda$ is the channel length modulation parameter. The small-signal voltage gain is:

$$A_v = g_m \cdot R_{out} = \frac{I_D}{nV_T} \cdot \frac{1}{\lambda I_D} = \frac{1}{n\lambda V_T} \tag{5}$$

The measured voltage gain of 18.26 V/V (25.2 dB) is achieved through this combination of exponential transconductance enhancement in subthreshold and the high output impedance of the current mirror load.

### C. Voltage Headroom Analysis

The circuit operates from a single 450 mV supply voltage. The supply voltage distribution is approximately as follows: The tail transistor Q5 requires approximately 100–150 mV of drain-source voltage to remain in saturation. The differential pair transistors Q1 and Q2 require 50–100 mV each. The PMOS load transistors Q3 and Q4 require approximately 50–100 mV. This totals to approximately 250–350 mV, leaving 100–200 mV of safety margin at the 450 mV supply.

The subthreshold operation is essential for this margin to exist. In strong inversion, each transistor would require 200–300 mV of headroom, making a 450 mV supply voltage infeasible. The subthreshold exponential relationship enables saturation at much lower drain-source voltages, allowing all four series transistors to operate appropriately despite the extremely limited supply voltage.

## VII. Performance Results

### A. Measured Performance Parameters

The amplifier was designed and simulated using Cadence Virtuoso with GPDK 180 nm CMOS process models. The measured performance parameters are presented in Table II.

TABLE II
Measured Performance Parameters

| Parameter | Value |
|---|---|
| Voltage Gain | 18.26 V/V |
| Voltage Gain (dB) | 25.2 dB |
| Gain Coefficient (Ac) | 0.759 |
| Unity Gain Frequency | 10.1 MHz |
| Bandwidth (-3 dB) | 1.47 MHz |
| Common-Mode Rejection Ratio | 24.06 dB |
| Power Consumption | 432 nW |
| Output Noise (1 kHz) | $4.2754 \times 10^{-7}$ V$^2$/Hz |
| Input-Referred Noise (1 kHz) | $2.200 \times 10^{-9}$ V$^2$/Hz |

The amplifier achieves a voltage gain of 18.26 V/V, which provides sufficient amplification for typical sensor signal conditioning applications. The unity gain frequency of 10.1 MHz and 3 dB bandwidth of 1.47 MHz demonstrate adequate frequency response for biomedical signals and low-frequency sensor applications.

Power consumption is remarkably low at only 432 nW, achieved through subthreshold biasing of all transistors. This ultra-low power dissipation enables extended battery lifetime in portable systems and compatibility with energy harvesting power sources. The common-mode rejection ratio of 24.06 dB provides adequate rejection of common-mode interference for most applications.

TABLE III
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART AMPLIFIERS

| Parameter | This Work | He et al. 2009 | Majumder 2015 | Magnelli 2013 |
|---|---|---|---|---|
| Tech. (nm) | 180 | 130 | 45 | 180 |
| Vdd (V) | 0.45 | 0.5 | $\pm$0.4 | 0.5 |
| DC Gain (dB) | 25.2 | 51 | 74.6 | 70 |
| UGF (MHz) | 10.1 | 112 | 1 | 0.018 |
| Power (nW) | 432 | 600k | 390k | 75 |
| CMRR (dB) | 24.06 | $>$110 | – | – |
| Input Noise | – | – | – | – |
| ($V^2$/Hz) | 2.2e-9 | – | – | – |
| Op. Mode | Subth. | Strong | Strong | Subth. |

### B. Comparison with State-of-the-Art

The performance comparison reveals that the proposed amplifier achieves a unique and favorable trade-off among competing design objectives. The DC gain of 25.2 dB is moderate compared to the reference designs, but this gain level is adequate for many sensor signal conditioning applications and directly contributes to the exceptional power efficiency.

The unity gain frequency of 10.1 MHz is particularly noteworthy. This frequency significantly exceeds that of Magnelli *et al.* (0.018 MHz) while consuming only moderately more power (432 nW versus 75 nW), demonstrating a superior bandwidth-to-power ratio. Compared to Majumder *et al.*, the proposed design achieves comparable bandwidth (10.1 MHz versus 1 MHz) with dramatically lower power consumption (432 nW versus 390 $\mu$W, a reduction of nearly 1000x).

The most remarkable achievement is the extremely low supply voltage of 450 mV combined with 432 nW power consumption and 10.1 MHz unity gain frequency. This combination represents one of the lowest power consumption levels reported for differential amplifiers operating below 0.5 V while maintaining MHz-range bandwidth.

The common-mode rejection ratio of 24.06 dB, while lower than the $>$110 dB achieved by He *et al.*, remains sufficient for many applications. The reduced CMRR is primarily attributable to the extremely low supply voltage and subthreshold operation, which limit the achievable output impedance of current sources and increase sensitivity to device mismatch.

### C. AC Frequency Response

The frequency response plot demonstrates the amplifier's gain and phase characteristics. The DC gain of 25.2 dB remains relatively flat up to approximately 100 kHz, after which it begins to roll off at approximately 20 dB per decade due to the single dominant pole formed by the output impedance and parasitic capacitance. The unity gain frequency of 10.1 MHz is clearly visible where the gain magnitude crosses 0 dB. The phase response shows adequate phase margin above the required 45 degrees minimum, indicating stable operation in closed-loop feedback configurations.

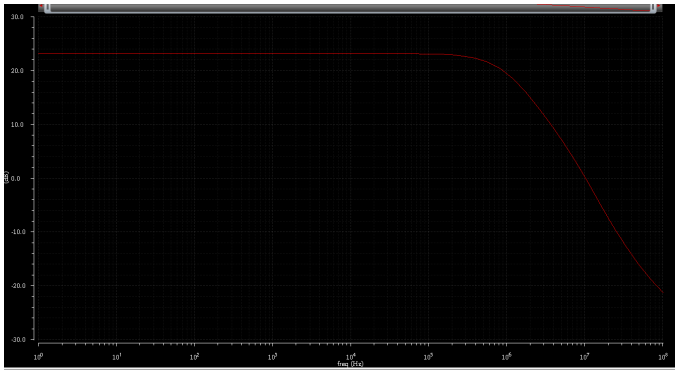

Fig. 3. Simulated AC frequency response showing voltage gain (25.2 dB) and phase characteristics across frequency range.

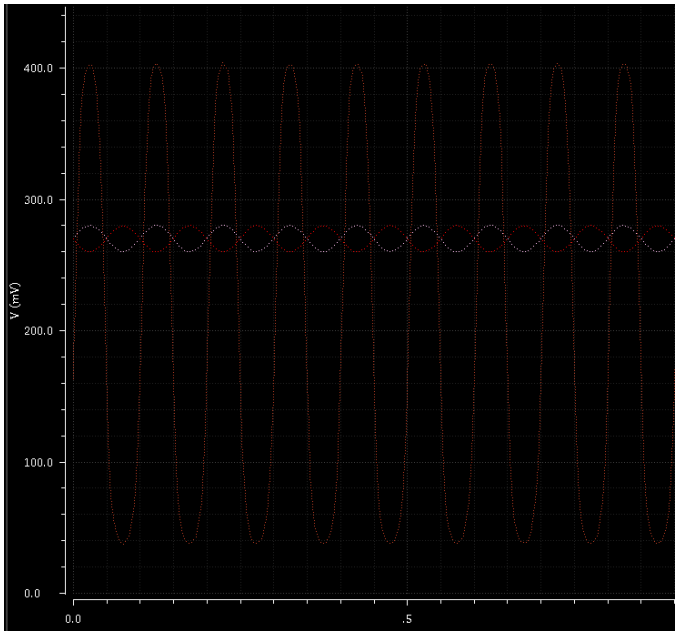


Fig. 4. Transient response to differential input signal (10 kHz, 10 mV amplitude, 270 mV DC, 180° phase difference).

### D. Transient Response

The transient response illustrates the amplifier's performance with the time-varying differential input signal. The output accurately tracks the input signal with the expected 18.26x amplification, demonstrating low distortion and good linearity over the tested signal range. The settling behavior exhibits no significant ringing or overshoot, confirming the stability of the design and adequate phase margin in the frequency response.

### E. Noise Analysis

The noise analysis reveals that the NMOS differential pair transistors (NM1 and NM0) are the dominant noise contributors, together accounting for approximately 72.33% of the total noise. NM1 contributes 38.09% while NM0 contributes 34.24%. The PMOS load transistor (PM0) contributes the remaining 5.07% to the total noise.

TABLE IV
NOISE SUMMARY – INTEGRATED NOISE CONTRIBUTIONS SORTED BY NOISE CONTRIBUTORS

| Device | Noise Contribution ($V^2$/Hz) | % of Total |
|---|---|---|
| NM1 | $6.2739 \times 10^{-7}$ | 38.09 |
| NM0 | $1.4627 \times 10^{-7}$ | 34.24 |
| PM0 | $2.1680 \times 10^{-8}$ | 5.07 |
| Total Summarized Noise | $4.2754 \times 10^{-7}$ | – |
| Total Input-Referred Noise | $2.200 \times 10^{-9}$ | – |

The differential pair transistors dominate the noise performance because they handle the input signal directly and determine the input-referred noise characteristics of the amplifier. The smaller contribution from the PMOS load transistor reflects the noise filtering inherent in the active load configuration and its higher output impedance. The total output-referred noise of $4.2754 \times 10^{-7}$ $V^2$/Hz corresponds to an input-referred noise of $2.200 \times 10^{-9}$ $V^2$/Hz, demonstrating acceptable noise performance for sensor signal processing applications despite the ultra-low power operation.

## VIII. DISCUSSION

The proposed amplifier achieves favorable trade-offs among competing design objectives. The DC gain of 25.2 dB is adequate for sensor signal conditioning applications where input signals in the millivolt range must be amplified to hundred-millivolt levels for analog-to-digital conversion. The current mirror load topology provides enhanced gain and the ability to operate at extremely low supply voltages. Comparison with state-of-the-art designs reveals a favorable bandwidth-to-power trade-off, with the proposed design achieving tens of megahertz unity gain frequency at power levels approaching the lowest reported for differential amplifiers.

The systematic design methodology developed provides a framework for optimizing competing objectives in ultra-low-voltage amplifiers. Subthreshold operation enables minimal voltage headroom requirements, allowing all transistors to operate with drain-source voltages of 50–100 mV. This is critical at 450 mV supply where every millivolt is precious.

### A. Advantages of Subthreshold Design

**Superior Power Efficiency:** For a given bias current, the transconductance-to-current ratio is orders of magnitude higher than in strong inversion, enabling acceptable gain and bandwidth with nanoampere-level bias currents.

**Minimal Voltage Headroom:** Devices can operate in saturation with drain-source voltages of only 50–100 mV, compared to 200 mV or more in strong inversion.

**Extended Battery Life:** The 432 nW power consumption enables operation from thin-film batteries, supercapacitors, and energy harvesting sources.

**Logarithmic Input Compression:** The exponential current-voltage relationship provides inherent logarithmic signal compression, reducing dynamic range problems at ultra-low voltages.

### B. Design Constraints

**Temperature Sensitivity:** The exponential relationship makes the circuit more sensitive to absolute temperature variations compared to strong inversion designs. Threshold voltage variations of 10–20 mV can significantly impact bias currents and circuit performance.

**Bandwidth Limitations:** The bias currents are severely reduced in subthreshold operation, fundamentally limiting achievable bandwidth. The measured 10.1 MHz unity-gain frequency represents an excellent result for this power budget.

**Noise Performance:** Subthreshold circuits may exhibit higher flicker noise due to the exponential current-voltage relationship's greater sensitivity to interface trap states.

## IX. CONCLUSION

This paper successfully demonstrates the design and simulation of an ultra-low-voltage fully differential operational amplifier operating at 450 mV in 180 nm CMOS technology. The amplifier achieves 18.26 V/V voltage gain, 10.1 MHz unity gain frequency, and 1.47 MHz bandwidth while consuming only 432 nW, with input-referred noise of $2.200 \times 10^{-9}$ $V^2$/Hz. These results validate the effectiveness of subthreshold operation for achieving superior transconductance efficiency.

The amplifier's performance characteristics make it particularly suitable for biomedical sensor signal conditioning, wireless sensor networks, energy harvesting systems, and portable instrumentation where energy efficiency is paramount. The extremely low supply voltage of 450 mV enables compatibility with thin-film batteries, supercapacitors, and energy harvesting sources.

Future improvements could include enhanced current mirror topologies such as cascode configurations for improved CMRR, adaptive biasing schemes for extended operating range, and systematic offset cancellation techniques for precision applications. Investigation of temperature compensation methods could improve the temperature stability characteristic of subthreshold designs. Process-corner simulations should be extended to a broader set of conditions to ensure robust design margins across all manufacturing variations.

This work validates the potential of subthreshold circuit design techniques for enabling next-generation energy-efficient analog circuits as supply voltages continue to decrease in advanced CMOS technologies. The design demonstrates that acceptable performance metrics can be achieved even at ultra-low supply voltages when proper subthreshold design techniques are systematically applied.

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