University of Texas, Dallas
Department of Electrical and Computer Engineering

CE/EEDG 6325: VLSI Design

ARITHMETIC LOGIC UNIT OPERATIONS

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DESCRIPTION

The project is to design and simulate arithmetic logic unit operations. The *input1* and *input2* are two 32-bits inputs. The 32-bits output *out* stores the result of the performed operation. The 1-bit output Cout stores the carry and borrow outputs for addition and subtraction operations. The 4-bit sel line decides the operation to be performed.

The following operations are designed in this ALU

1.Addition

2.Subtraction

3.Logical AND

4. Logical OR

5. Division

6. Comparison and Equality

7.Logical XOR

VERILOG CODE

```
module PROJECT_1_A (input1, input2, reset, clk, sel, out, c_out);
input [31:0] input1, input2;
input reset;
input clk;
input[3:0] sel;
output[31:0] out;
output c_out;
reg[31:0] out;
reg c_out;
always@(posedge clk)
```

```
begin
//Implementing D-FlipFlop. If the reset signal is 1,c_out will be reset
if(reset)
{out,c_out} = 33'b0;
else
begin
  case(sel)
    // Arithmetic Addition
              4'b0000: begin {c_out,out} = input1 + input2; end
    // Arithmetic Subtraction
              4'b0001: begin {c_out,out} = input1 - input2; end
    //Logical AND Operation. 'c_out' is not used so it is initialised as 0
              4'b0010: begin out = input1 & input2; c_out = 1'b0; end
    //Logical OR Operation. 'c_out' is not used so it is initialised as 0
              4'b0011: begin out = input1 | input2; c_out = 1'b0; end
    // Arithmetic Division
              4'b0100: begin {c_out,out} = input1 / input2; end
    // Comparison Operations where 'out' is not used to initialised to 16'd0
              4'b0101: begin c_out = (input1>input2) ? 1'b1:1'b0; out = 16'd0;  end
              4'b0110: begin c_out = (input1<input2) ? 1'b1:1'b0; out = 16'd0;  end
              4'b0111: begin c_out = (input1==input2) ? 1'b1:1'b0; out = 16'd0; end
    //Logical XOR Operation. 'c_out' is not used so it is initialised as 0
              default : begin out = input1 ^ input2; c_out = 1'b0; end
  endcase
end
end
Endmodule
```

TESTBENCH

```
module PROJECT_1_TB;
reg[31:0] input1,input2;
reg clk,reset;
reg[3:0] sel;
wire[31:0] out;
wire c_out;

integer i;
  PROJECT_1_A DUT(input1,input2,reset,clk,sel,out,c_out);
          initial begin


    #0          input1 = 32'b11111111111111111111111111111111;
                input2 = 32'b11111000011111111111111111111111;
    #0 sel =  4'b0000;
    reset = 0;
    clk =0;
  end
  always begin
    #5 clk = !clk;
  end
  always@(posedge clk)
    begin
             for(i = 0; i <= 16 ; i =  i+1)
               begin
                       #20; sel = sel + 4'b0001;
               end
    end

Endmodule
```

SIMULATION WAVEFORM

Addition

input 1: 11111111111111111111111111111111

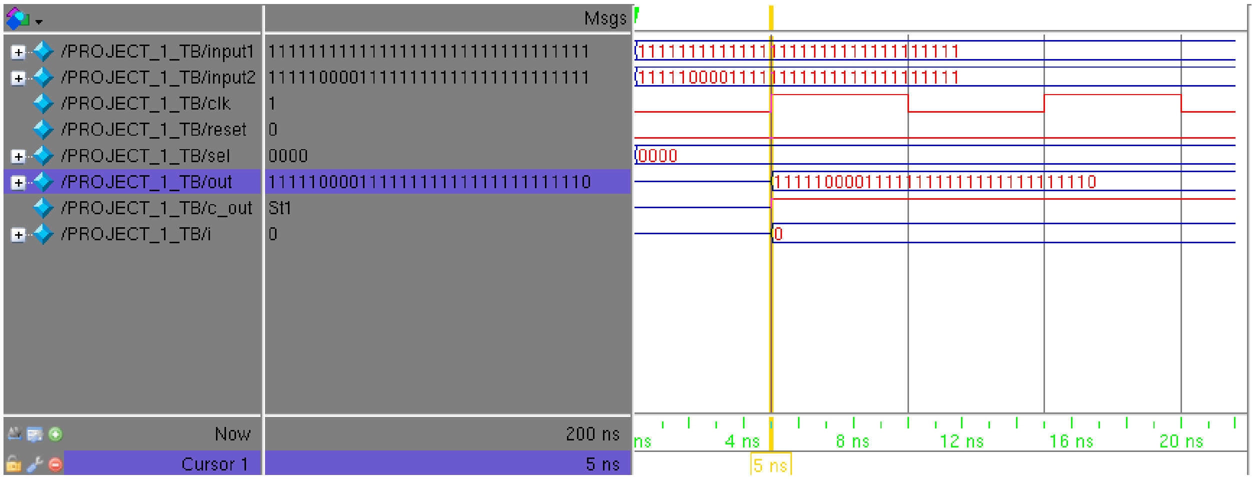
input 2:11111000011111111111111111111111

sel: (0000)

reset : 0

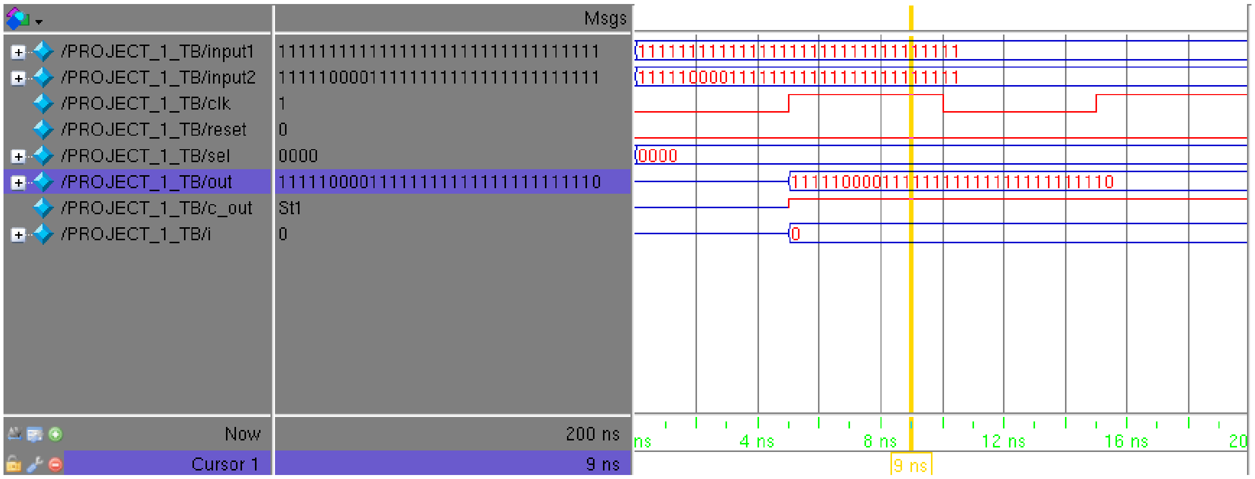
clk : 1

out :input1+input2= 11111000011111111111111111111110



```
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0000
/PROJECT_1_TB/out      11111000011111111111111111111110
/PROJECT_1_TB/c_out    St1
/PROJECT_1_TB/i        0
Now                    200 ns
Cursor 1               5 ns
```

Behavioural Code Simulation



```
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0000
/PROJECT_1_TB/out      11111000011111111111111111111110
/PROJECT_1_TB/c_out    St1
/PROJECT_1_TB/i        0
Now                    200 ns
Cursor 1               9 ns
```

Mapped Code Simulation

Subtraction

input 1: 11111111111111111111111111111111

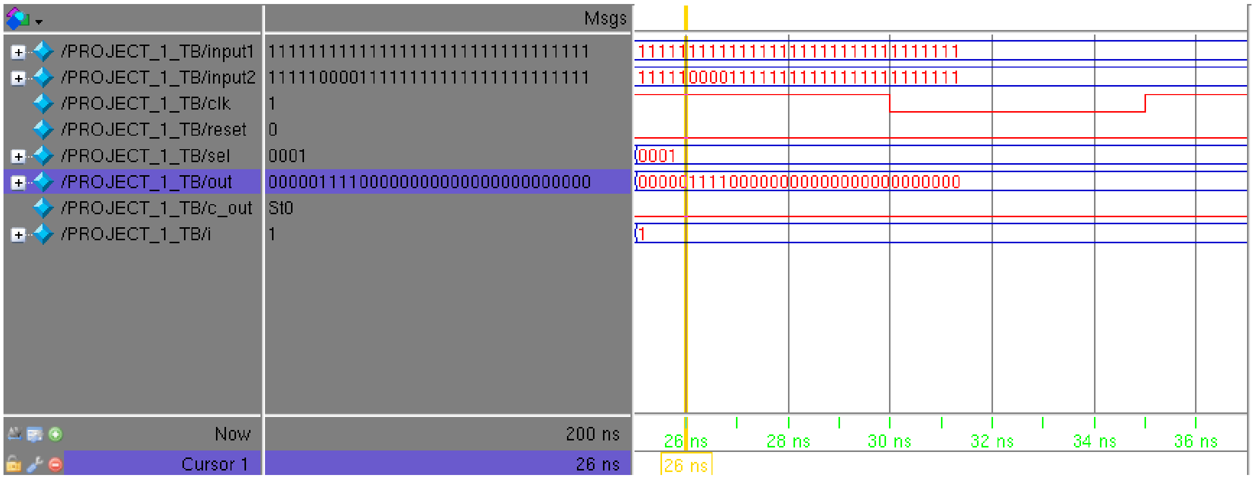
input 2:11111000011111111111111111111111

sel: (0001)

reset : 0

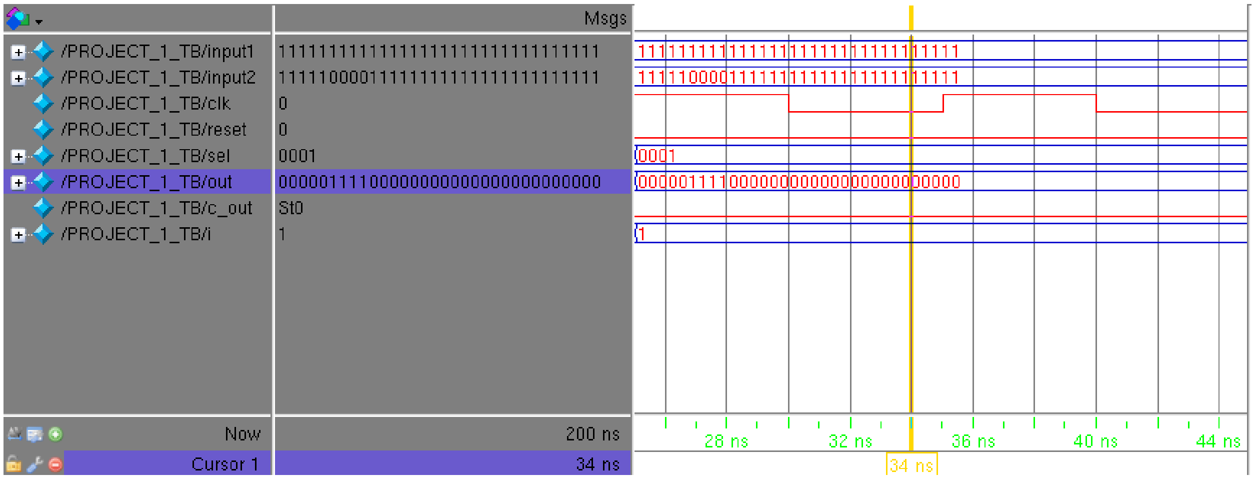
clk : 1

out :input1-input2= 00000111100000000000000000000000



```
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0001
/PROJECT_1_TB/out      00000111100000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        1
Now                    200 ns
Cursor 1               26 ns
```

Behavioural Code Simulation



```
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      0
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0001
/PROJECT_1_TB/out      00000111100000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        1
Now                    200 ns
Cursor 1               34 ns
```

Mapped Code Simulation

Logical AND

input 1: 11111111111111111111111111111111

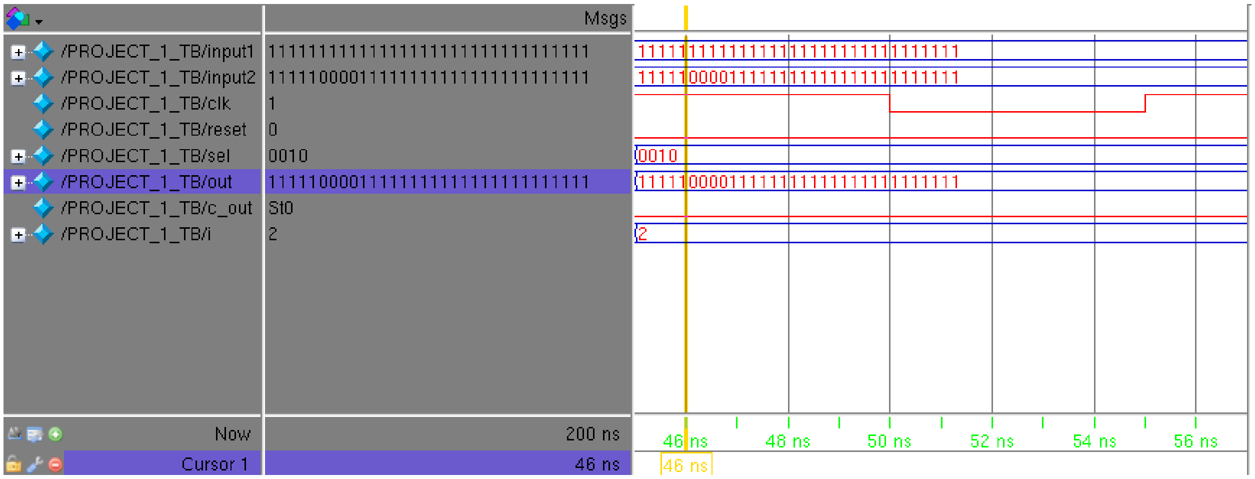
input 2:11111000001111111111111111111111

sel: (0010)

reset : 0

clk : 1

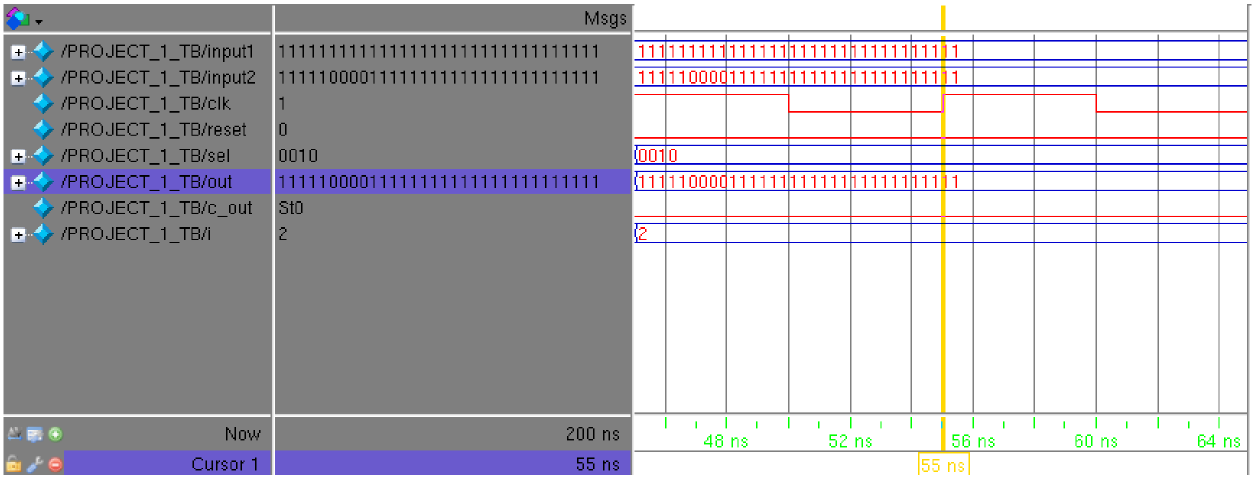
out :input1&input2= 11111000001111111111111111111111



```
                     Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000001111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0010
/PROJECT_1_TB/out      11111000001111111111111111111111
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        2

Now                    200 ns
Cursor 1               46 ns
```

Behavioural Code Simulation



```
                     Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000001111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0010
/PROJECT_1_TB/out      11111000001111111111111111111111
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        2

Now                    200 ns
Cursor 1               55 ns
```

Mapped Code Simulation

Logical OR

input 1: 11111111111111111111111111111111

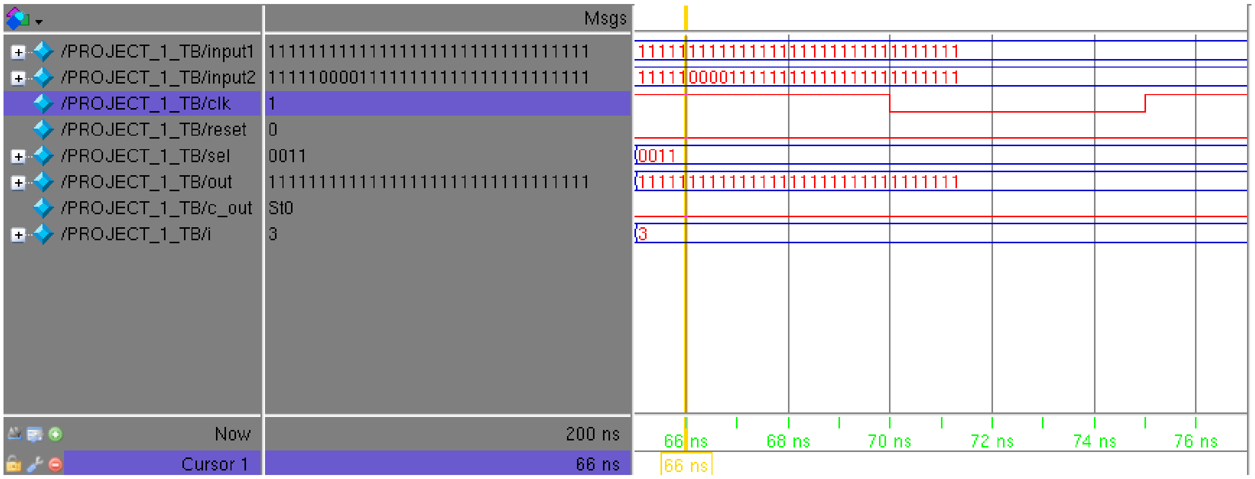
input 2:11111000011111111111111111111111

sel: (0011)

reset : 0

clk : 1

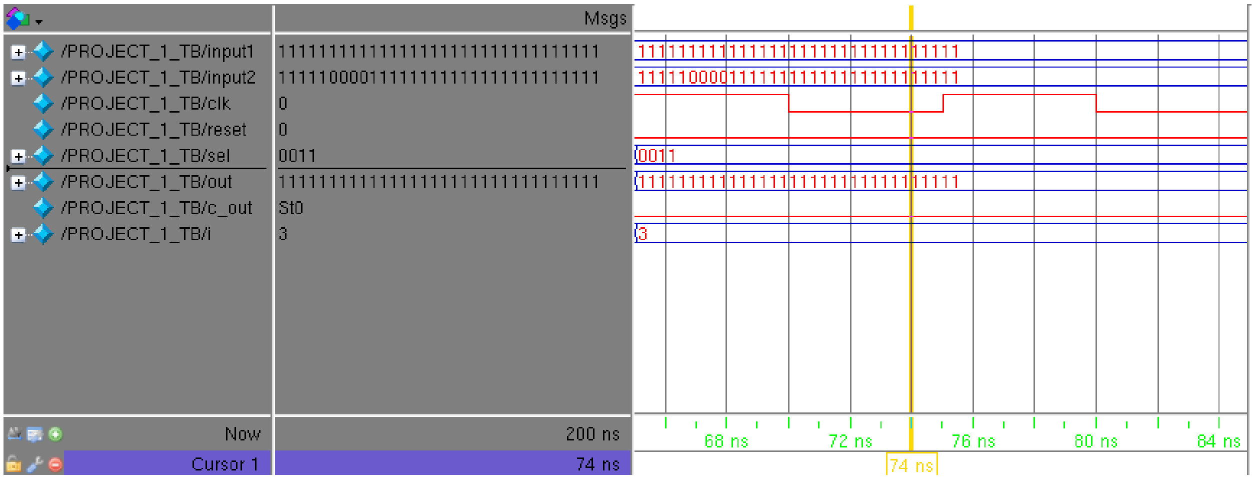
out :input1|input2= 11111111111111111111111111111111



```
                         Msgs
/PROJECT_1_TB/input1    11111111111111111111111111111111
/PROJECT_1_TB/input2    11111000011111111111111111111111
/PROJECT_1_TB/clk       1
/PROJECT_1_TB/reset     0
/PROJECT_1_TB/sel       0011
/PROJECT_1_TB/out       11111111111111111111111111111111
/PROJECT_1_TB/c_out     St0
/PROJECT_1_TB/i         3

Now                     200 ns
Cursor 1                66 ns
```

Behavioural Code Simulation



```
                         Msgs
/PROJECT_1_TB/input1    11111111111111111111111111111111
/PROJECT_1_TB/input2    11111000011111111111111111111111
/PROJECT_1_TB/clk       0
/PROJECT_1_TB/reset     0
/PROJECT_1_TB/sel       0011
/PROJECT_1_TB/out       11111111111111111111111111111111
/PROJECT_1_TB/c_out     St0
/PROJECT_1_TB/i         3

Now                     200 ns
Cursor 1                74 ns
```

Mapped Code Simulation

Division

input 1: 11111111111111111111111111111111

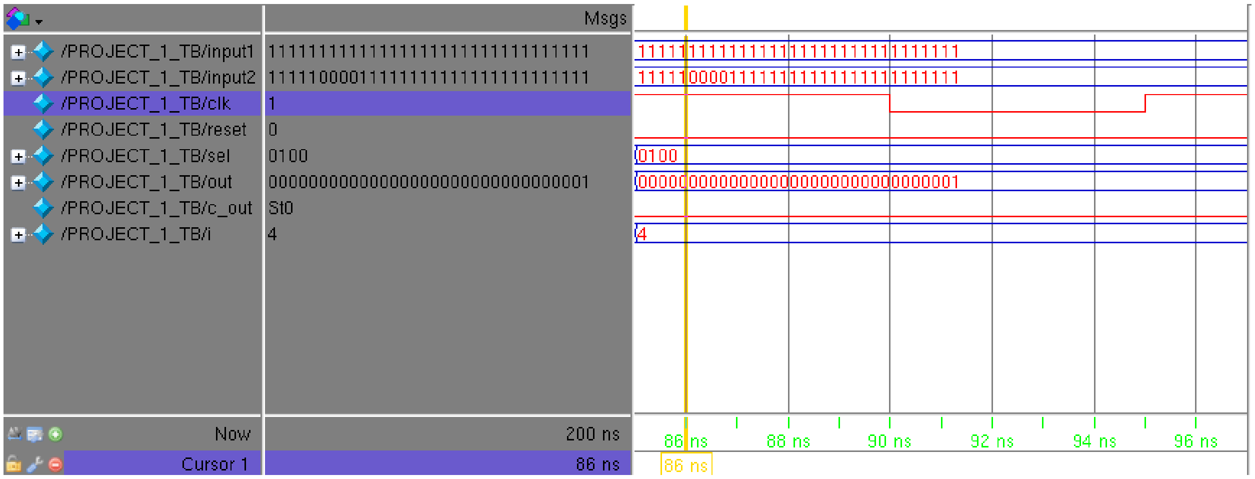
input 2:11111000011111111111111111111111

sel: (0100)

reset : 0

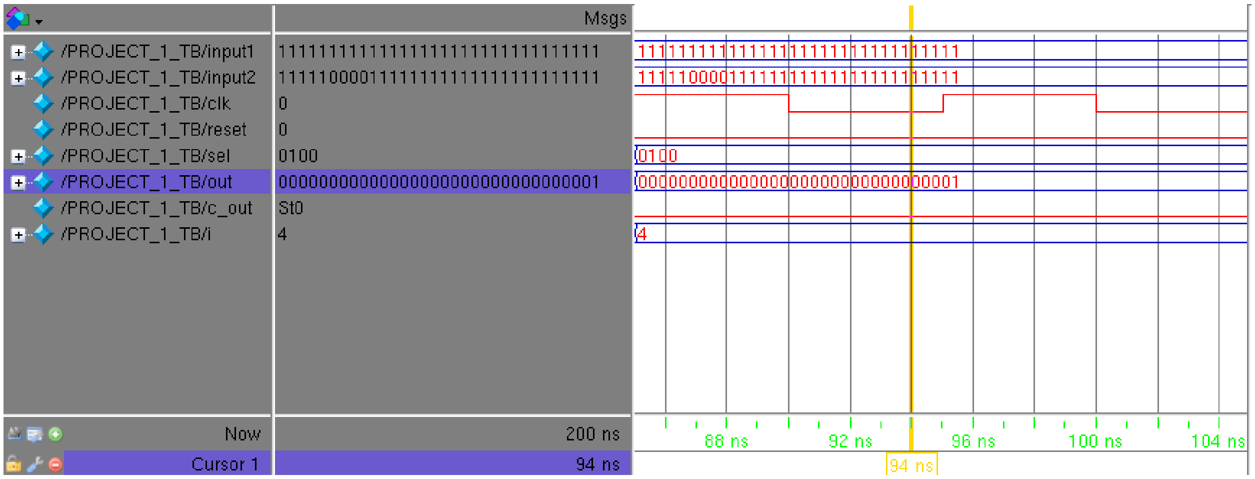
clk : 1

out :input1/input2= 00000000000000000000000000000001



```
/PROJECT_1_TB/input1    11111111111111111111111111111111
/PROJECT_1_TB/input2    11111000011111111111111111111111
/PROJECT_1_TB/clk       1
/PROJECT_1_TB/reset     0
/PROJECT_1_TB/sel       0100
/PROJECT_1_TB/out       00000000000000000000000000000001
/PROJECT_1_TB/c_out     St0
/PROJECT_1_TB/i         4
Now                     200 ns
Cursor 1                86 ns
```

Behavioural Code Simulation



```
/PROJECT_1_TB/input1    11111111111111111111111111111111
/PROJECT_1_TB/input2    11111000011111111111111111111111
/PROJECT_1_TB/clk       0
/PROJECT_1_TB/reset     0
/PROJECT_1_TB/sel       0100
/PROJECT_1_TB/out       00000000000000000000000000000001
/PROJECT_1_TB/c_out     St0
/PROJECT_1_TB/i         4
Now                     200 ns
Cursor 1                94 ns
```

Mapped Code Simulation

Comparison Operations

Greater:

input 1: 11111111111111111111111111111111

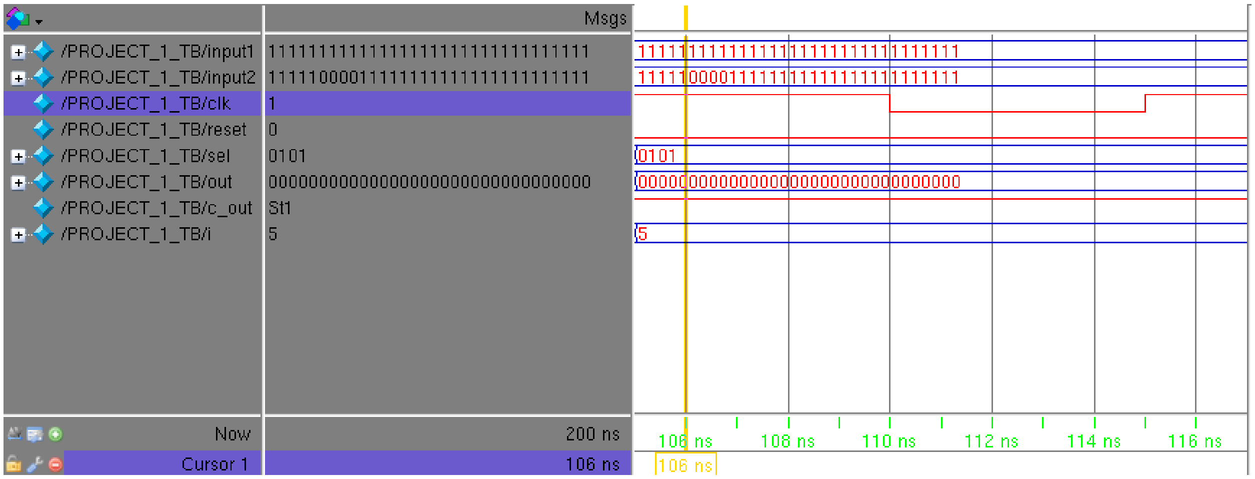
input 2:11111000011111111111111111111111

sel: (0101)

reset : 0

clk : 1

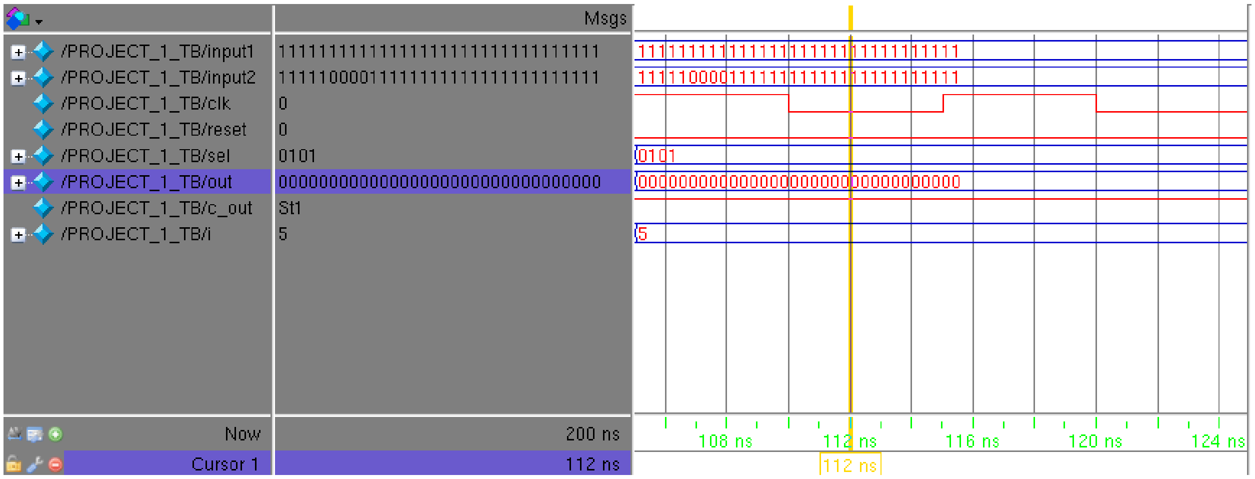
out :input1>input2= 00000000000000000000000000000000



```
                                  Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0101
/PROJECT_1_TB/out      00000000000000000000000000000000
/PROJECT_1_TB/c_out    St1
/PROJECT_1_TB/i        5

                 Now                          200 ns
            Cursor 1                          106 ns
```

Behavioural Code Simulation



```
                                  Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      0
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0101
/PROJECT_1_TB/out      00000000000000000000000000000000
/PROJECT_1_TB/c_out    St1
/PROJECT_1_TB/i        5

                 Now                          200 ns
            Cursor 1                          112 ns
```

Mapped Code Simulation

Lesser

input 1: 11111111111111111111111111111111

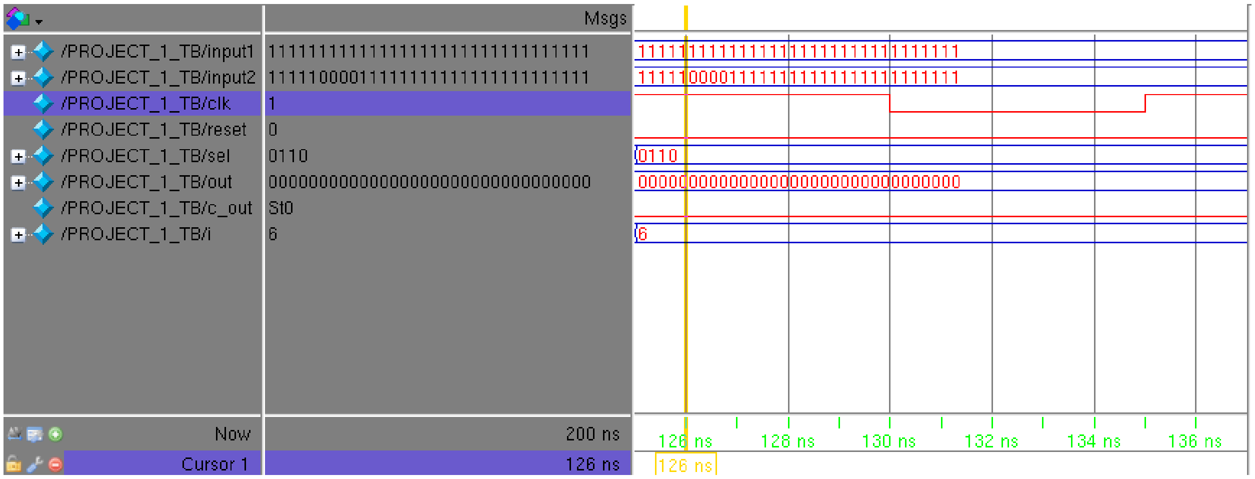
input 2:11111000011111111111111111111111

sel: (0110)

reset : 0

clk : 1

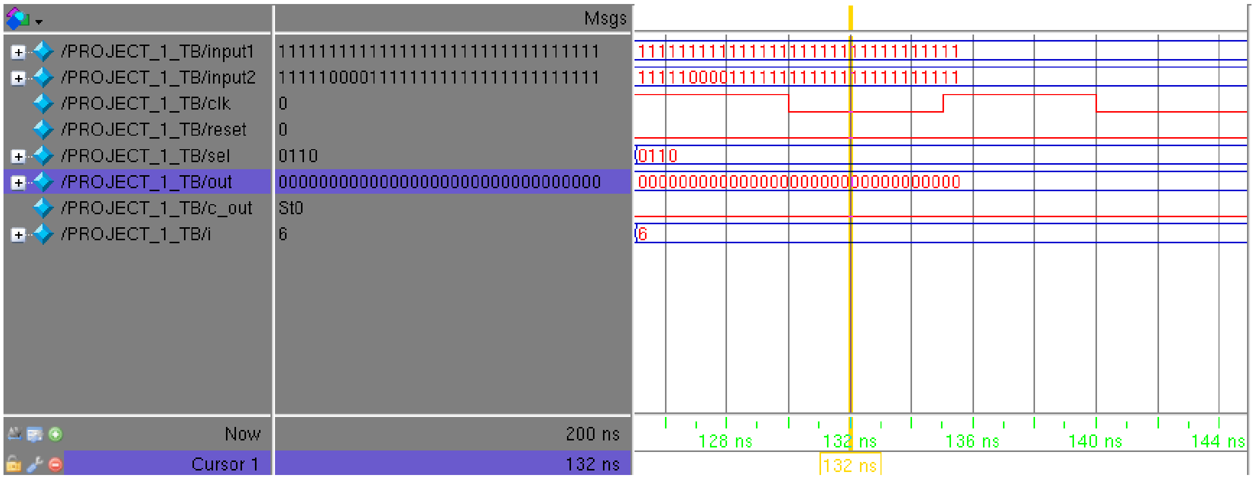
out :input1<input2= 00000000000000000000000000000000



```
                                            Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0110
/PROJECT_1_TB/out      00000000000000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        6

Now                    200 ns
Cursor 1               126 ns
```

Behavioural Code Simulation



```
                                            Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      0
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0110
/PROJECT_1_TB/out      00000000000000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        6

Now                    200 ns
Cursor 1               132 ns
```

Mapped Code Simulation

Equality

input 1: 11111111111111111111111111111111

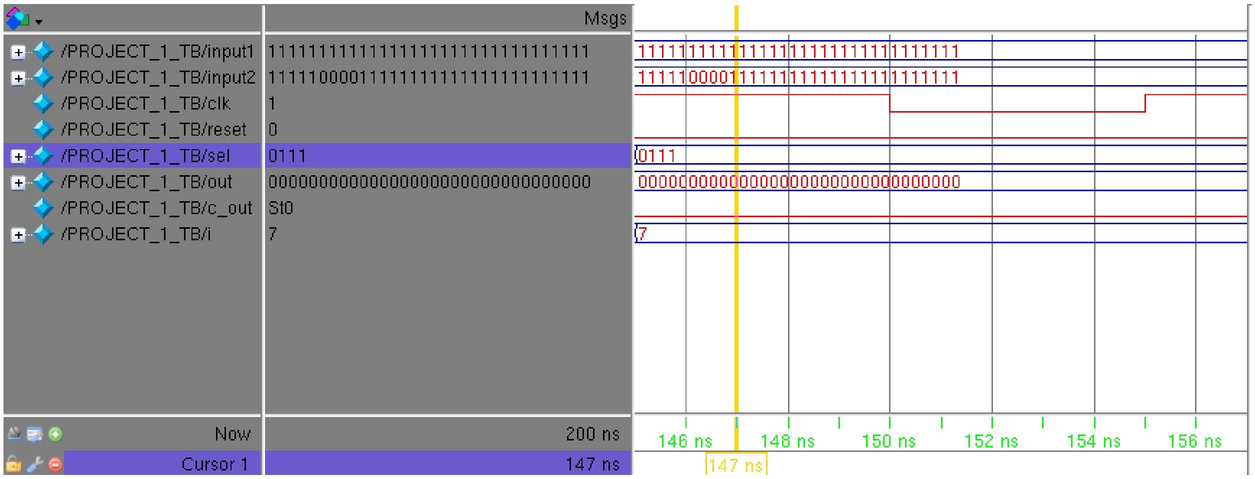
input 2:11111000011111111111111111111111

sel: (0111)

reset : 0

clk : 1

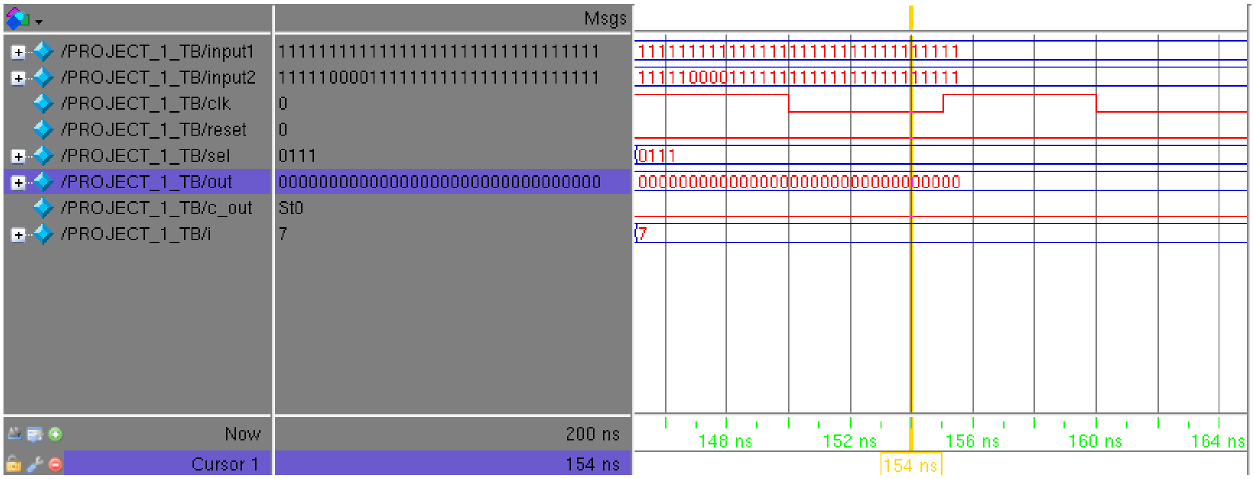
out :input1=input2= 00000000000000000000000000000000



```
                                    Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0111
/PROJECT_1_TB/out      00000000000000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        7

Now                    200 ns
Cursor 1               147 ns
```

Behavioural Code Simulation



```
                                    Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      0
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      0111
/PROJECT_1_TB/out      00000000000000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        7

Now                    200 ns
Cursor 1               154 ns
```

Mapped Code Simulation

Logical XOR

input 1: 11111111111111111111111111111111

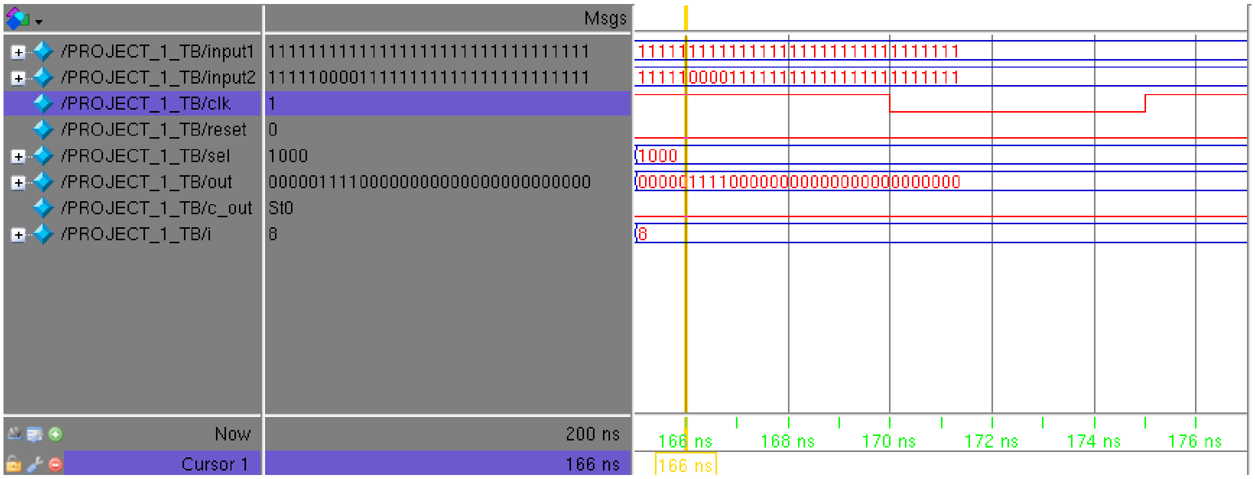
input 2:11111000011111111111111111111111

sel: (1000)

reset : 0

clk : 1

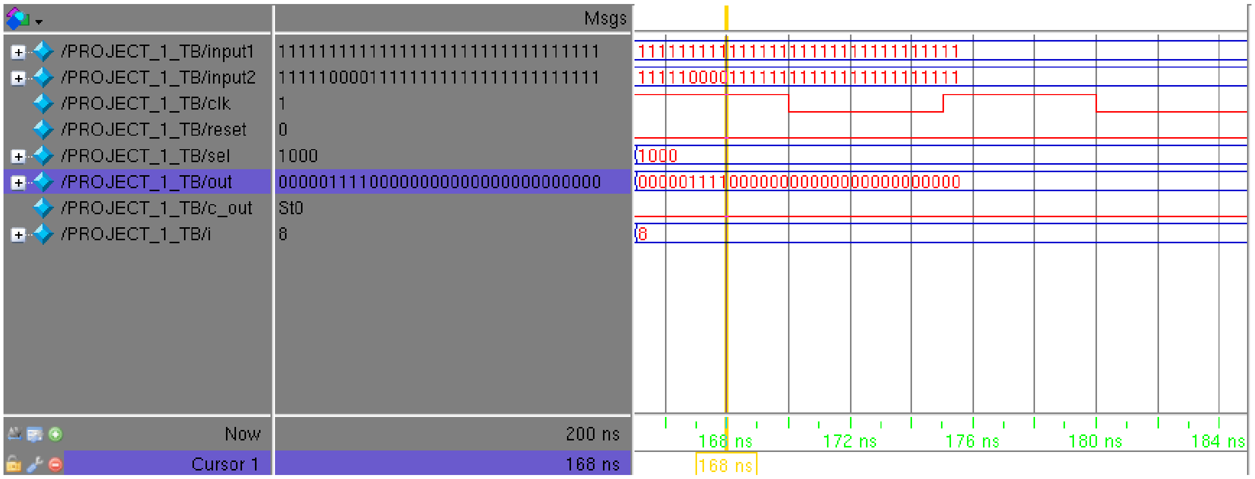
out :input1^input2= 00000111100000000000000000000000



```
                              Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      1000
/PROJECT_1_TB/out      00000111100000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        8

Now                    200 ns
Cursor 1               166 ns
```

Behavioural Code Simulation



```
                              Msgs
/PROJECT_1_TB/input1   11111111111111111111111111111111
/PROJECT_1_TB/input2   11111000011111111111111111111111
/PROJECT_1_TB/clk      1
/PROJECT_1_TB/reset    0
/PROJECT_1_TB/sel      1000
/PROJECT_1_TB/out      00000111100000000000000000000000
/PROJECT_1_TB/c_out    St0
/PROJECT_1_TB/i        8

Now                    200 ns
Cursor 1               168 ns
```

Mapped Code Simulation

CELL REPORT

```
Information: Updating graph... (UID-83)

****************************************
Report : cell
Design : PROJECT_1_A
Version: L-2016.03-SP3
Date   : Sun Sep 12 21:45:36 2021
****************************************

Attributes:
    b - black box (unknown)
    h - hierarchical
    n - noncombinational
    r - removable
    u - contains unmapped logic

Cell                      Reference       Library              Area  Attributes
-----------------------------------------------------------------------------
C16                       nand2           library          1.000000
C19                       nand2           library          1.000000
C23                       nand2           library          1.000000
C32                       nand2           library          1.000000
C42                       nand2           library          1.000000
C45                       nand2           library          1.000000
C313                      nand2           library          1.000000
C314                      nand2           library          1.000000
C315                      nand2           library          1.000000
C316                      nand2           library          1.000000
C317                      nand2           library          1.000000
C318                      nand2           library          1.000000
C319                      nand2           library          1.000000
C320                      nand2           library          1.000000
```

```
C321             nand2      library     1.000000
C322             nand2      library     1.000000
C323             nand2      library     1.000000
C324             nand2      library     1.000000
C325             nand2      library     1.000000

out_reg[0]       dff        library     7.000000  n
out_reg[1]       dff        library     7.000000  n
out_reg[2]       dff        library     7.000000  n
out_reg[3]       dff        library     7.000000  n
out_reg[4]       dff        library     7.000000  n
out_reg[5]       dff        library     7.000000  n
out_reg[6]       dff        library     7.000000  n
out_reg[7]       dff        library     7.000000  n
out_reg[8]       dff        library     7.000000  n
out_reg[9]       dff        library     7.000000  n
out_reg[10]      dff        library     7.000000  n
out_reg[11]      dff        library     7.000000  n
out_reg[12]      dff        library     7.000000  n
out_reg[13]      dff        library     7.000000  n
out_reg[14]      dff        library     7.000000  n
out_reg[15]      dff        library     7.000000  n
out_reg[16]      dff        library     7.000000  n
out_reg[17]      dff        library     7.000000  n
out_reg[18]      dff        library     7.000000  n
out_reg[19]      dff        library     7.000000  n
out_reg[20]      dff        library     7.000000  n
out_reg[21]      dff        library     7.000000  n
out_reg[22]      dff        library     7.000000  n
out_reg[23]      dff        library     7.000000  n
out_reg[24]      dff        library     7.000000  n
out_reg[25]      dff        library     7.000000  n
out_reg[26]      dff        library     7.000000  n
out_reg[27]      dff        library     7.000000  n
out_reg[28]      dff        library     7.000000  n
```

```
out_reg[29]         dff         library      7.000000  n
out_reg[30]         dff         library      7.000000  n
out_reg[31]         dff         library      7.000000  n

-----------------------------------------------------------------------------
Total 4278 cells                            7303.000000
```