University of Texas, Dallas
Department of Electrical and Computer Engineering

CE/EEDG 6325: VLSI Design

INVERTER DESIGN AND LAYOUT

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Analysis of Inverter

Energy : -1.602 *fJ*
Delay : 183 *ps*
EDP : 1.943 e^-23 *Js*
Area : 32.5e^-24sq.m

HSPICE TEST SETUP FILE

```
$transistor model
.include
"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "inverter_1.pex.netlist"

.option post run lvl=5

xi GND! OUT VDD! IN inverter_1

vdd VDD! GND! 1.2v
vin IN GND! pwl(0ns 1.2v 1ns 1.2v 1.007ns 0v 6ns 0v 6.007ns 1.2v 12ns 1.2v)
cout OUT GND! 70f

$transient analysis
.tr 100ps 12ns
$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp
$.tr 100ps 12ns sweep WP 1u 9u 0.5u

.measure tran trise trig v(IN) val=0.6v fall=1 targ v(OUT) val=0.6v rise=1 $measure tlh at 0.6v
.measure tran tfall trig v(IN) val=0.6v rise=1 targ v(OUT) val=0.6v fall=1 $measure tpl at 0.6v
.measure tavg param = '(trise+tfall)/2' $calculate average delay
.measure tdiff param='abs(trise-tfall)' $calculate delay difference
.measure delay param='max(trise,tfall)' $calculate worst case delay

$ method 1
.measure tran iavg avg i(vdd) from=0 to=10n $average current in one clock cycle
.measure energy param='1.2*iavg*10n' $calculate energy in one clock cycle
.measure edp1 param='abs(delay*energy)'

.end
```

Energy Delay Product:

Minimized EDP is defined as the product of energy and worst-case delay. That is,

$$EDP = Energy * worst\ case\ Delay$$

Given: Cload = 70fF and VDD= 1.2 V where Energy can be calculated as,

Esupply = Cload $*$ Vdd^2

Theoretical calculation*:*

Esupply = Cload $*$ Vdd^2

$$Esupply = (70 * 10-15 * 1.2^2)$$

$$= 100.8\ fJ$$

From SPICE Setup file:

a) Energy in one clock cycle can be calculated as:

$$Energy = 1.2 * iavg * 10n$$

$$=1.2 * (0.885 * 10-5) * 10 * 10-9$$

$$=106.2\ fJ$$

b)Worst case Delay can be calculated as:

Delay = max(trise,tfall)

= max(178ps, 183ps)

=183ps

$$Minimized\ EDP = (106.2 * 10-15) * (183 * 10-12)$$

$$=1.9434 * 10-23\ J$$

OUTPUT WAVEFORM :

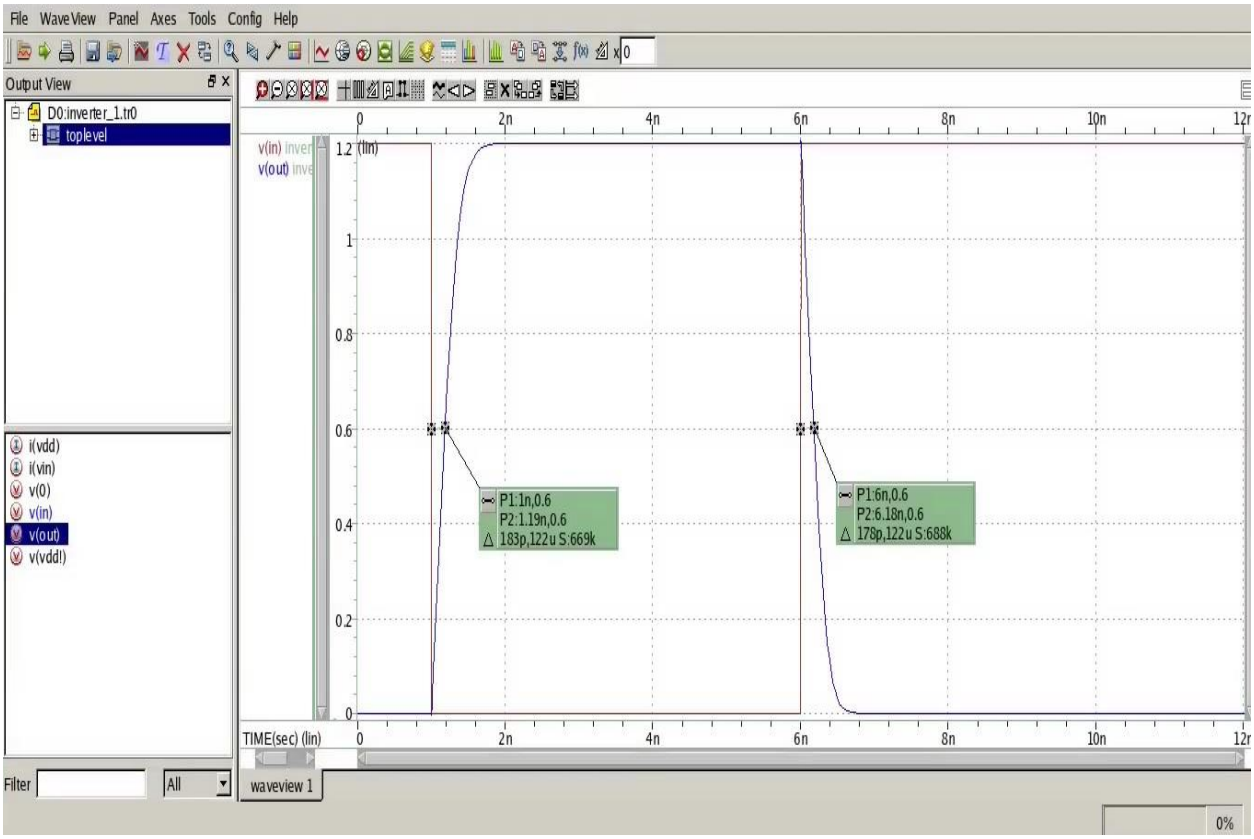

Figure 1: Output waveform showing tLH and tHL

Rising time (trise/tLH) = 178 ps
Falling time(tfall/tHL) = 183 ps
Delay difference between tPLH and tPHL (tdiff) = 5ps

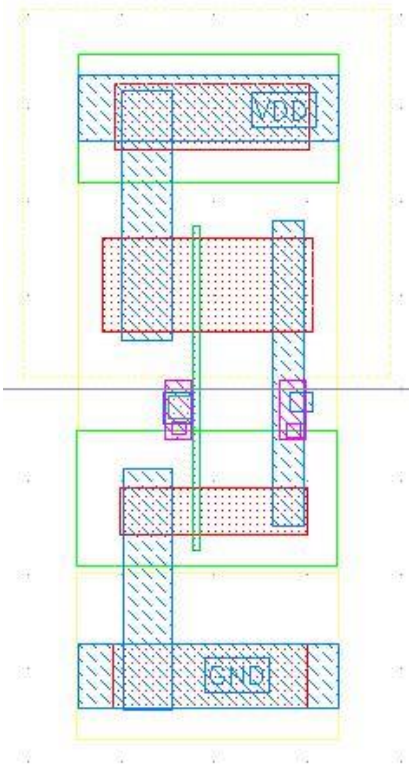

Fig 1 : Inverter Layout

Figure 2: Inverter Layout with measurements represented in ruler

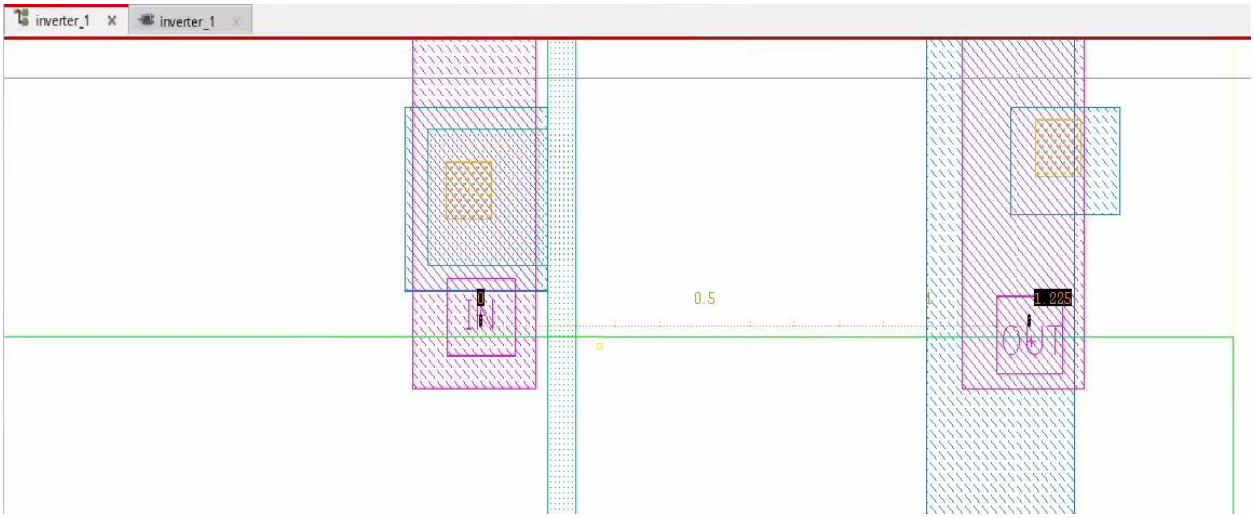

Figure 3 ; Pin pitching Distance