

University of Texas, Dallas
Department of Electrical and Computer Engineering
CE/EEDG 6325: VLSI Design
D FlipFlop

Submitted by
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Times of D FlipFlop

Parameter	Passing 1	Passing 0
Tsu_dd	39.85ps	29.85ps
Tsu_opt	82.85ps	82.85ps
Thold	29.85ps	39.85ps
Tclk>Q	234.5ps	241.5ps
tD	317ps	324ps

Analysis of D FlipFlop

Height : 7.942um
Width : 8.5um
Area : 67.507um

Introduction :

We have designed a schematic for D-Flip-Flop and applied Dual Euler Trail (DET). After obtaining DET, we designed a layout with 2 diffusion breaks and characterized the D-Flip-Flop. The D Flip-flop has three inputs:

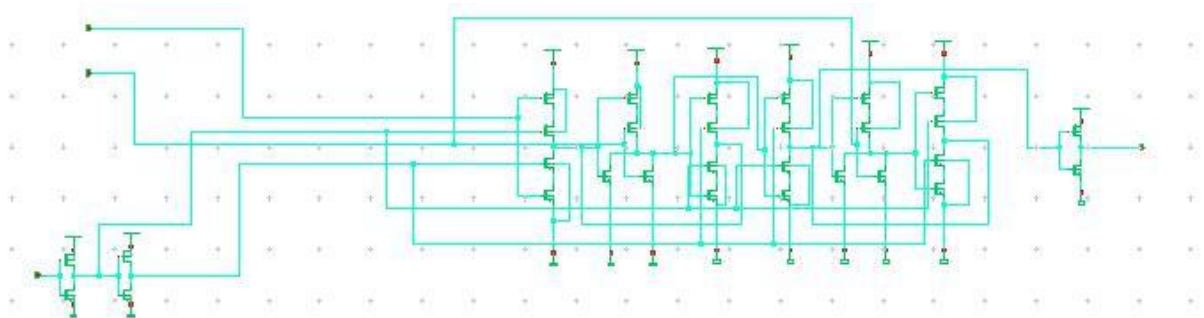
- a) D
 - b) CLK
 - c) Reset (R) and
- one output:
- a) Q

We have calculated T_{su_dd} , T_{su_opt} , T_{hold} , $T_{clk \rightarrow Q}$ and t_D for passing '0' and passing '1' conditions of the flip-flop using a rising edge clock.

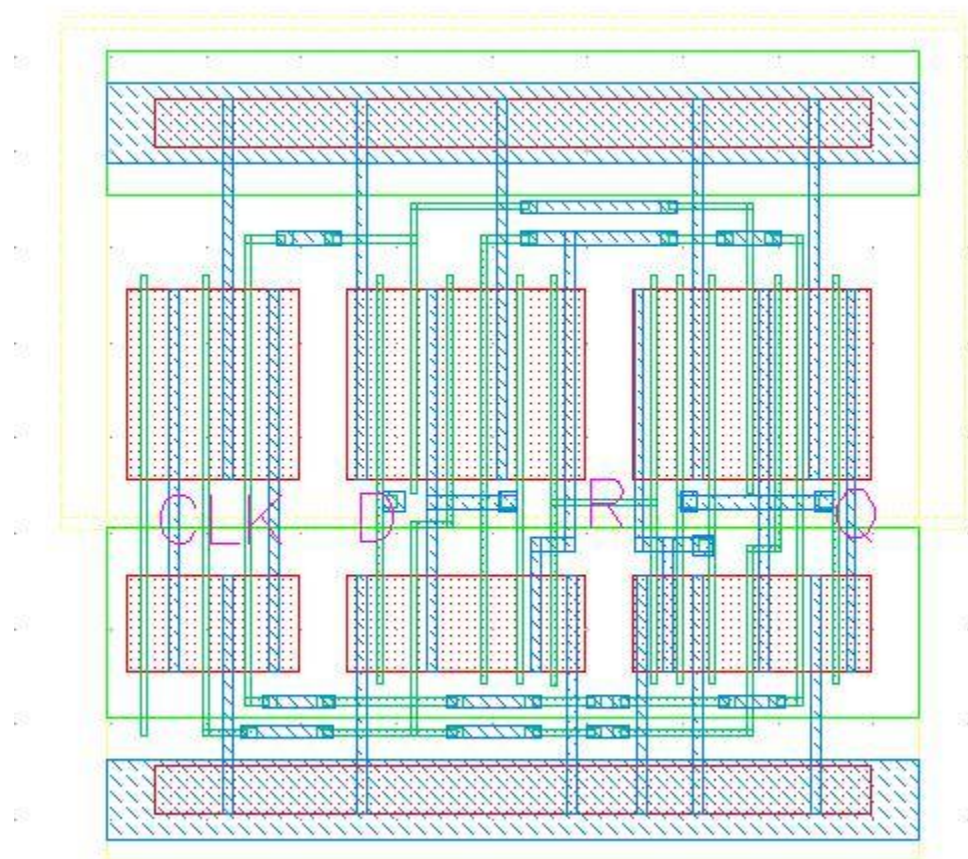
Steps to find the time of D-FF

- a) SetupTime(T_{su}) : Time Duration that an input signal D must be present and stable before capturing edge to get a valid logic value at the Output.
- b) DropDead Setup Time(T_{su_dd}) : Absolute minimum time required for the input signal D to arrive before triggering clock edge such that input signal is captured at the output.
- c) Clock to Q time($T_{clk \rightarrow q}$) : Time taken for the output Q to take a value after the capturing edge.
- d) Delay Time(t_D): Time taken by input signal to appear at output.
$$t_D = T_{su_dd} + T_{clk \rightarrow q}$$
- e) Hold Time ; Minimum time measured from triggering edge for which the input must be stable to get the valid output.
$$T_{su_dd}(1) = T_{hold}(0) \text{ and Viceversa}$$
- f) Optimum Setup Time(T_{su_opt}) ; Time for which t_D is minimum and can be obtained by using T_{su} and t_D .

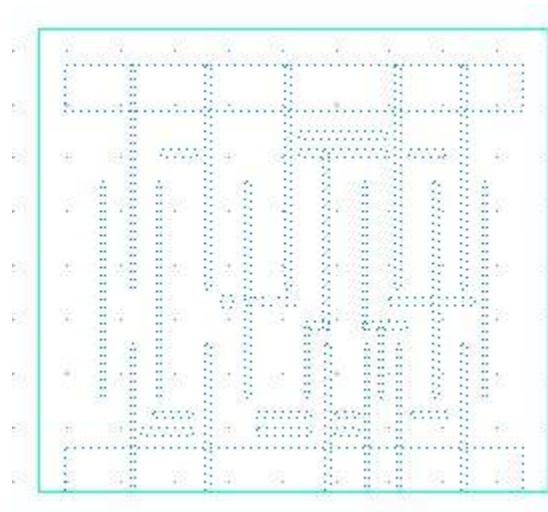
Schematic



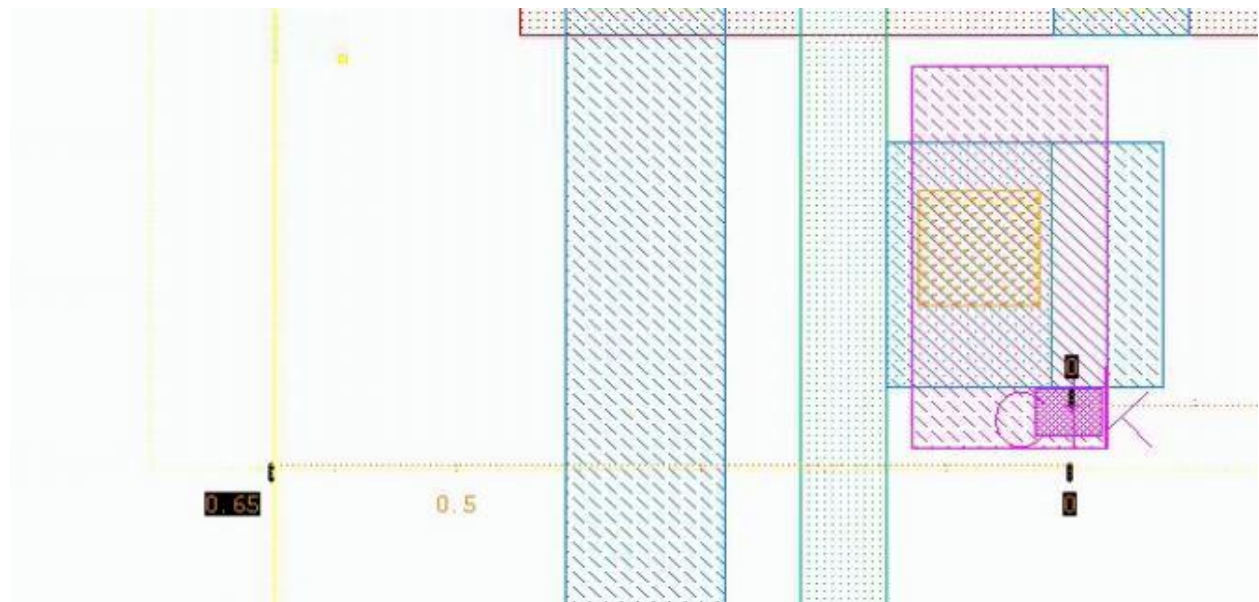
Layout



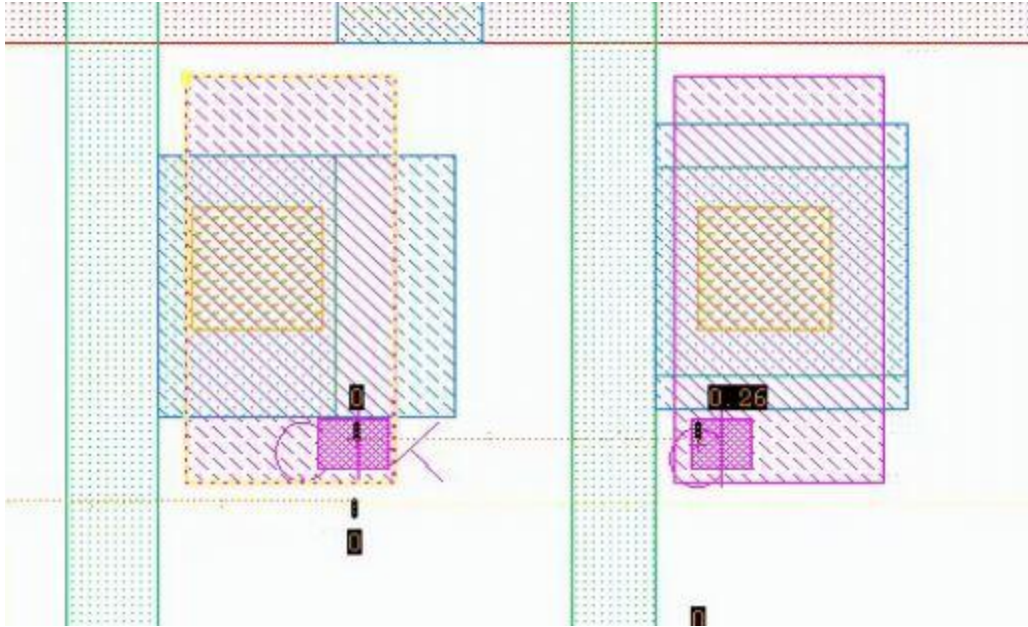
Abstract View



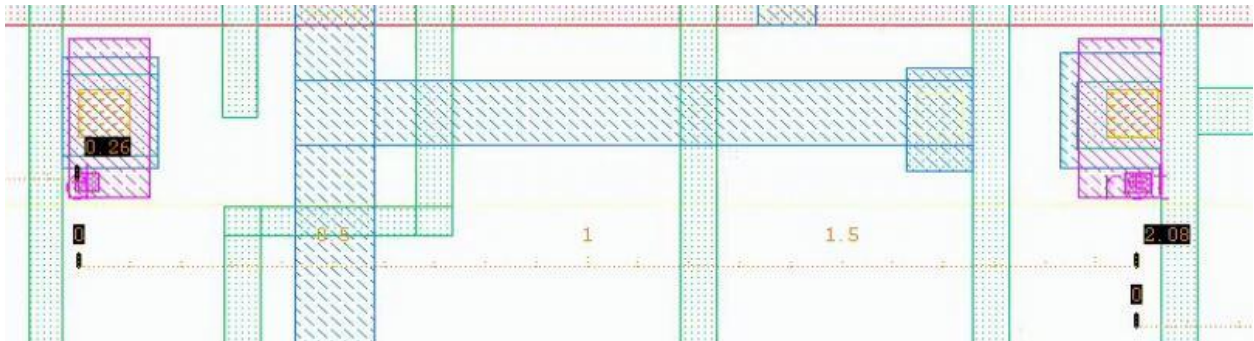
Distance of Pin Grid



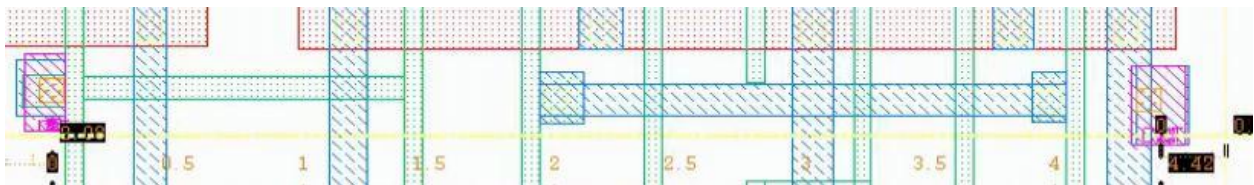
Distance between Right offset and Clk



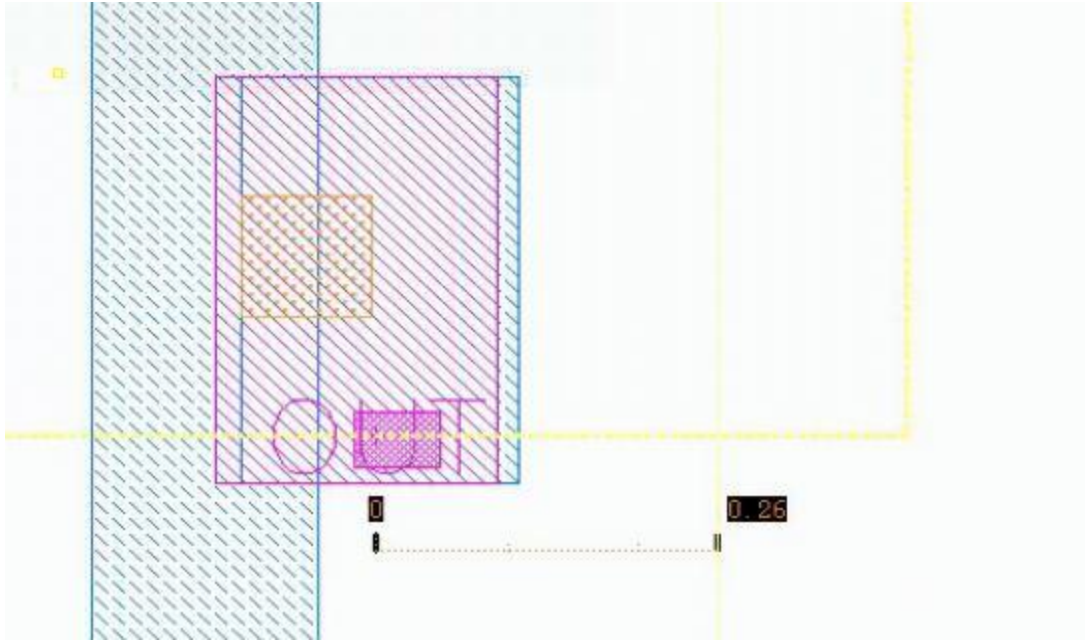
Distance between Clk and D



Distance between D and R



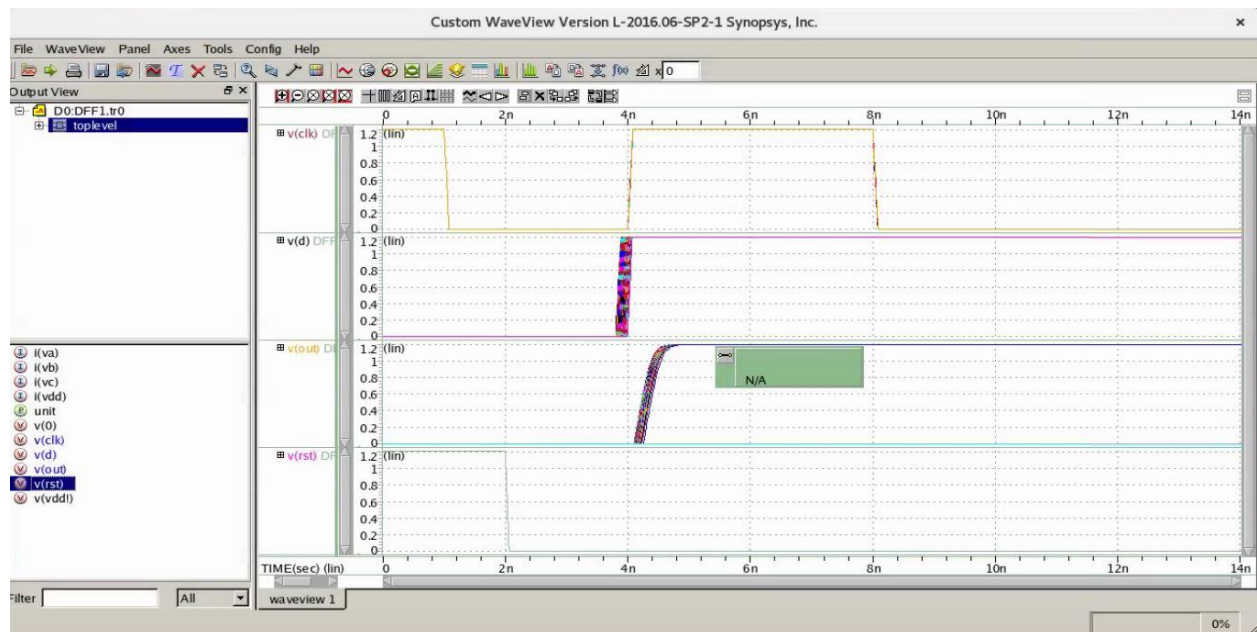
Distance between R and Out



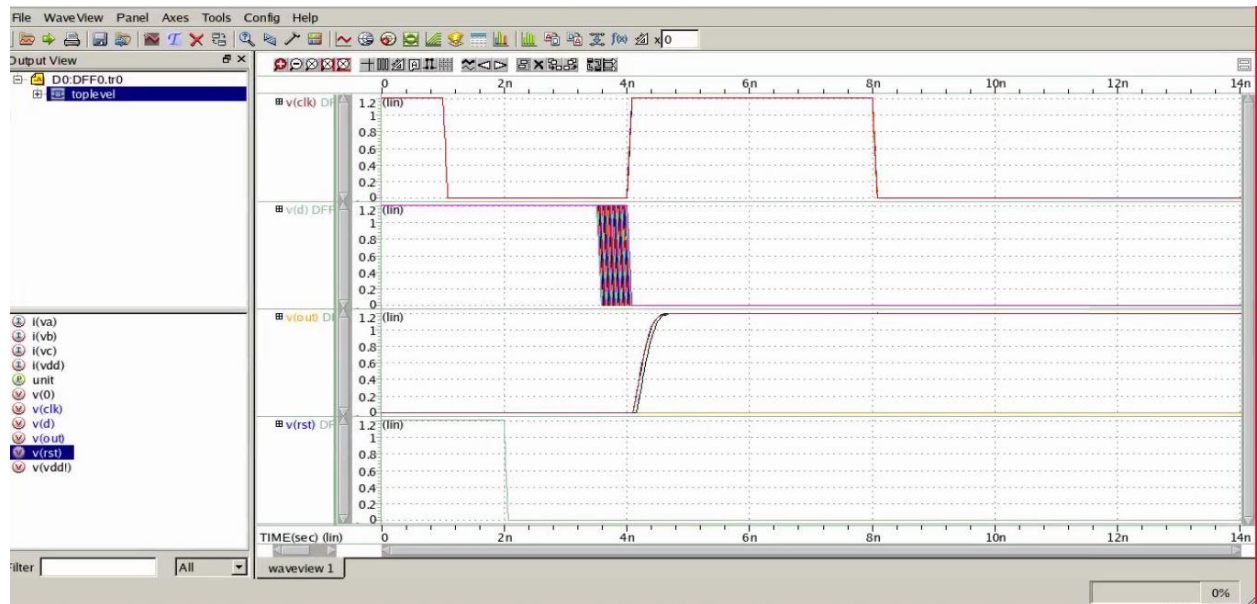
Distance between Out and Offset

Waveforms

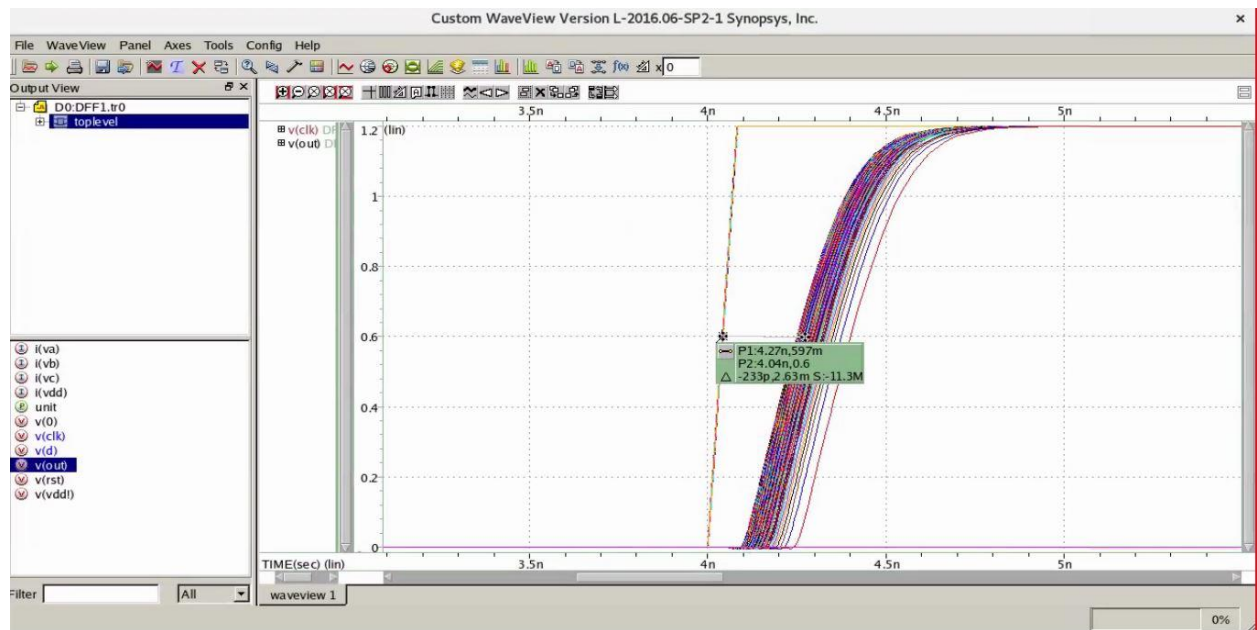
Passing 1 :



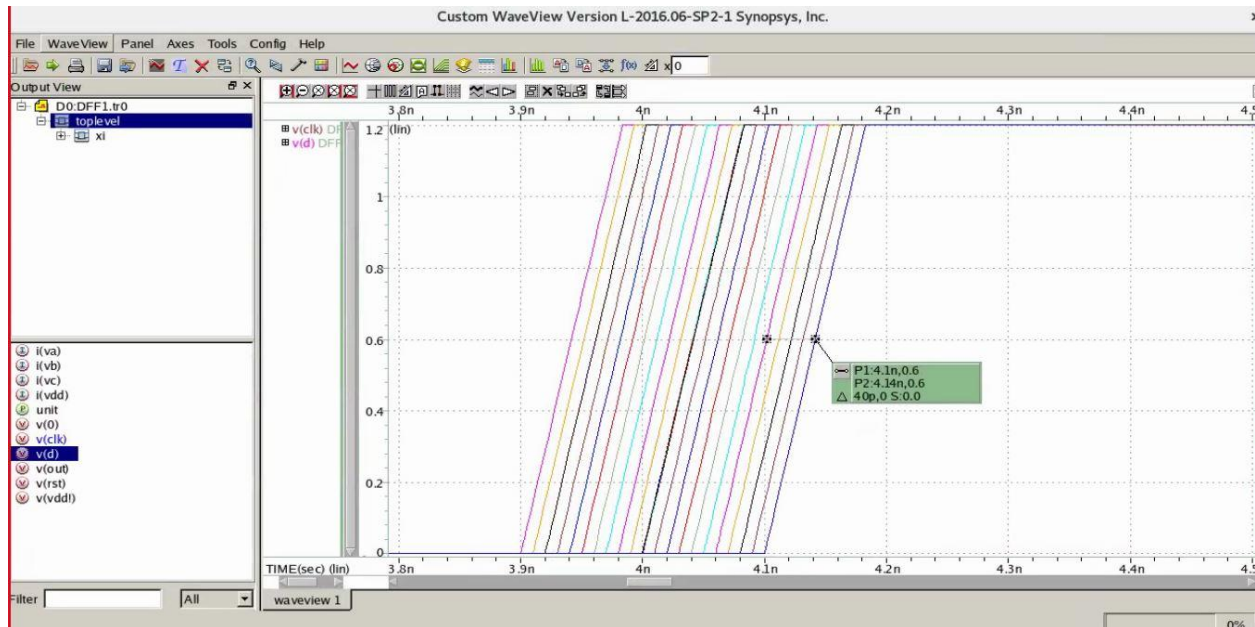
Passing '0'



Opt time vs Clk



Setup time



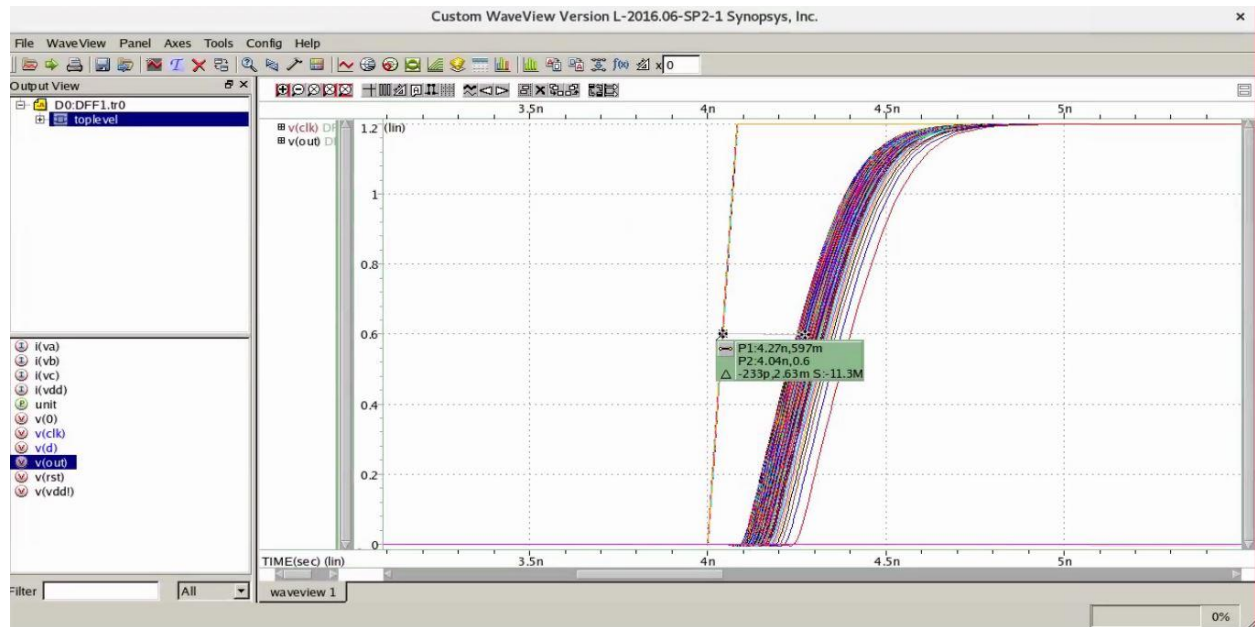
Minimal Time opt

Activities Text Editor Wed 00:32

DFF1.mt0 ~/cad/spice/DFF/Result_3 Save

DFF1.sp				DFF1.mt0
3.910e-09	8.985e-11	2.279e-10	3.177e-10	
	25.0000	1		
3.911e-09	8.885e-11	2.287e-10	3.176e-10	
	25.0000	1		
3.912e-09	8.785e-11	2.296e-10	3.175e-10	
	25.0000	1		
3.913e-09	8.685e-11	2.307e-10	3.175e-10	
	25.0000	1		
3.914e-09	8.585e-11	2.316e-10	3.174e-10	
	25.0000	1		
3.915e-09	8.485e-11	2.325e-10	3.174e-10	
	25.0000	1		
3.916e-09	8.385e-11	2.336e-10	3.174e-10	
	25.0000	1		
3.917e-09	8.285e-11	2.345e-10	3.173e-10	
	25.0000	1		
3.918e-09	8.185e-11	2.356e-10	3.174e-10	
	25.0000	1		
3.919e-09	8.085e-11	2.366e-10	3.175e-10	
	25.0000	1		
3.920e-09	7.985e-11	2.376e-10	3.174e-10	
	25.0000	1		
3.921e-09	7.885e-11	2.386e-10	3.174e-10	
	25.0000	1		
3.922e-09	7.785e-11	2.396e-10	3.175e-10	
	25.0000	1		
3.923e-09	7.685e-11	2.407e-10	3.176e-10	
	25.0000	1		
3.924e-09	7.585e-11	2.418e-10	3.176e-10	
	25.0000	1		
3.925e-09	7.485e-11	2.428e-10	3.176e-10	
	25.0000	1		

Plain Text Tab Width: 8 Ln 239, Col 2 INS



Spice testing Setup File

For Passing '1'

\$transistor model

.include

"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "DFlipFlop.pex.sp"

.option post runlvl=5

xi GND! OUT VDD! CLK D RST DFlipFlop

vdd VDD! GND! 1.2v

va CLK GND! pwl(0ns 1.2v 1ns 1.2v 1.083ns 0v 4ns 0v 4.083ns 1.2v 8ns 1.2v 8.083ns 0v 12ns 0v 12.083ns 0v 14ns 0v)

vb D GND! pwl(0ns 0v 'unit' 0v 'unit' + 83.3ps' 1.2v)

vc RST GND! pwl(0ns 1.2v 2ns 1.2v 2.0625ns 0v 3ns 0v 3.0625ns 0v 14ns 0v)

cout OUT GND! 50f

\$transient analysis

.tran 0.001ns 14ns sweep unit 3.8ns 3.99ns 1ps

.measure t_su trig v(D) val=0.6 rise=1 targ v(CLK) val=0.6 rise = 1

.measure clk_Qt trig v(CLK) val=0.6 rise = 1 targ v(OUT) val=0.6 rise=1

.measure tdelay param='t_su + clk_Qt'

.end

For Passing '0'

\$transistor model

.include

"/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"

.include "DFlipFlop.pex.sp"

.option post runlvl=5

xi GND! OUT VDD! CLK D RST DFlipFlop

vdd VDD! GND! 1.2v

va CLK GND! pwl(0ns 1.2v 1ns 1.2v 1.083ns 0v 4ns 0v 4.083ns 1.2v 8ns 1.2v 8.083ns 0v 12ns 0v 12.083ns 0v 14ns 0v)

vb D GND! pwl(0ns 1.2v 'unit' 1.2v 'unit + 83.3ps' 0v)

vc RST GND! pwl(0ns 1.2v 2ns 1.2v 2.0625ns 0v 3ns 0v 3.0625ns 0v 14ns 0v)

cout OUT GND! 50f

\$transient analysis

.tran 0.001ns 14ns sweep unit 3.5ns 4ns 10ps

.measure t_su trig v(D) val=0.6 fall=1 targ v(CLK) val=0.6 rise = 1

.measure clk_Qt trig v(CLK) val=0.6 rise = 1 targ v(OUT) val=0.6 fall=1

.measure tdelay param='t_su + clk_Qt'

.end