BMS COLLEGE OF ENGINEERING, B'lore-19

(Autonomous Institution under VTU & affiliated to VTU, Belgaum)

DEPARTMENT OF ELECTRONICS &COMMUNICATION ENGG.,

LABORATORY MANUAL

SEMESTER: 5

SUBJECT: COMMUNICATION THEORY-1

SUB-CODE: 16EC5DCCT1

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Subject: COMMUNICATION THEORY-1 **Subject Code: 16EC5DCCT1**

List of Experiments:

	Part -1 Preliminary Experiments.
01	Design and testing of 2nd order Butter worth Low Pass and High pass filter.
02	Design and testing of 2nd order Butter worth Band Pass and Band elimination filter.
03	Design and testing of class C tuned amplifier.
04	Design and testing of generation and detection of AM wave using transistor.
05	Generation of DSBSC wave using ring modulator.
06	FM generation using 8038.
07	Design and testing of Mixer.
08	Design and testing of generation and detection of PAM.
	Part -2 Open Ended Experiments. **(Using Matlab / Simulink to conduct the following experiments)**
01	Generation of SSB Wave.
02	Generation of VSB Wave.
03	Sampling of band limited signal.
04	Time division multiplexing and de multiplexing.

Extra :- Sampling Theorem verification

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EXP NO: 1

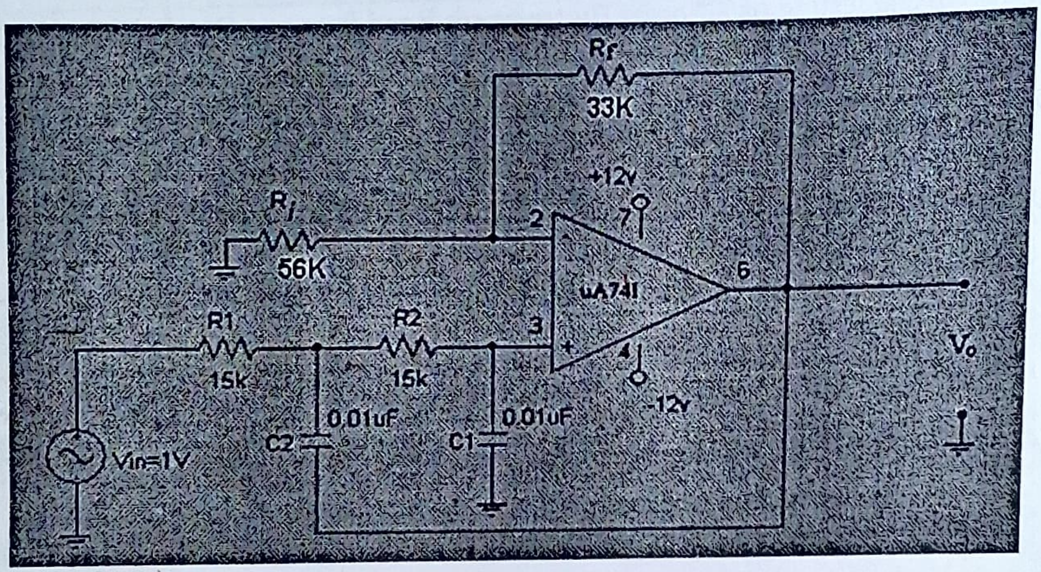
SECOND ORDER ACTIVE FILTERS

A. LOW PASS FILTER:

AIM: To design a second order Low pass Butterworth filter for a cutoff frequency of 1 KHz and to draw its frequency response. Calculate there from the cut-off frequency and Roll-off factor.

APPARATUS REQUIRED: Op-amp (μA741), Resistors 33KΩ, 56KΩ, 15KΩ 2 no's, Ceramic (Disk) Capacitors 0.01μF 2nos, Power supply, Signal generator, CRO Connecting wires etc.

CIRCUIT DIAGRAM:



$f_c = \frac{1}{2\pi CR}$ and K =1.5858

DESIGN:

Gain: **$K = (1+R_f/R_i) = 1.5858$;** Cut-off Frequency: $f_c = 1/(2\pi CR)$

Given $f_c = 1$ KHz; Let $C_1 = C_2 = C = 0.01\mu f$

Then $R_1 = R_2 = R = 1/2\pi f_c C = 1/(2\pi \times 1K \times 0.01\mu f) = 15.9$ KΩ (Remember $1/2\pi = 0.159$)

Use $R_1 = R_2 = \mathbf{R} = $ **(12+ 3.9KΩ)** Series combination

The pass band voltage gain, $K = 1.5858 \Rightarrow R_f/R_i = 0.5858$ or $R_f = 0.5858\, R_i$

Without losing high input impedance advantage, use R_i = 56K and R_f = 32.8K
Use nearest available single values: R_i=56 KΩ, R_f= 33 KΩ

PROCEDURE:

1. Make the connections as shown in the circuit diagram.

   Apply the sinusoidal I/P signal of amplitude 1V, (P-P) or any other convenient value (See if you can apply (24×0.9)/1.5858 = 13.6V PP) with a frequency less than $\frac{1}{10}f_c$ so that the O/P is undistorted and measure the O/P voltage (P – P). Record this as V_{Max}.

2. Keeping the input signal amplitude constant, increase the frequency until the O/P voltage reduces to **0.707V_{Max}**.The frequency at which this happens is your **f_c**, the filter cutoff frequency.

3. Keeping the I/P signal amplitude constant, measure and record at least 6 readings below and 6 readings above the cutoff frequency and one reading at the cut off frequency.(**Note:** Whenever you change the frequency button /setting, you should check and adjust the I/P to its previous constant value)

4. Plot the graph of Gain in dB V/S frequency on a semi-log graph paper.

5. Identify the 3dB point on your graph and identify the cut off frequency.

6. Increase the frequency to f_1 = 10f_c. Increase I/P signal amplitude also so as to be able to observe some O/P on the CRO. Measure the O/P when there is no distortion.(V_{01})

7. Increase the frequency to f_2=20fc. Maintaining same I/P amplitude, measure the O/P voltage (V_{02})

8. Compute Roll–Off factor of the filter using:Roll – off Factor = $20\log\left(\frac{V_{02}}{V_{01}}\right)$dB / Octave

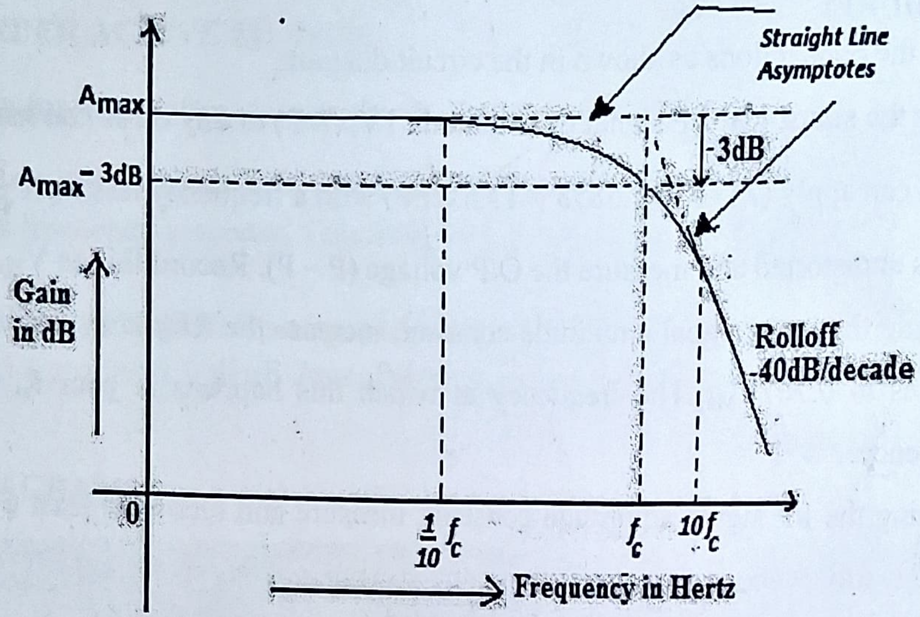
   {Gain in dB at f_1 is M_1=20log (V_{01}/V_i) dB, at f_2 it is M_2=20 log (V_{02}/V_i) dB; Change in magnitude as the frequency is increased is $M_2 - M_1$ = 20 log (V_{02}/V_{01}) dB. This is the Roll – off factor. The answer is in dB/Octave because the two frequencies selected are in the ratio of 1:2. To convert the answer to dB / Decade, multiply the answer obtained in dB / Octave by (20/6) because 20n dB / Decade = 6n dB/Octave}

9. Alternatively, measure v_{01} at f_c/10 and v_{02} at 10f_c. Roll-off factor is given by

   Roll-off factor = 20log (v_{02}/v_{01}) dB/decade

2

EXPECTED FREQUENCY RESPONSE GRAPH:



TABULAR COLUMN:

V_i = …… *Volts*, Constant.

Frequency in Hz	Output V_0, in Volts	$M = 20 \log (V_0/V_i)$ in dB

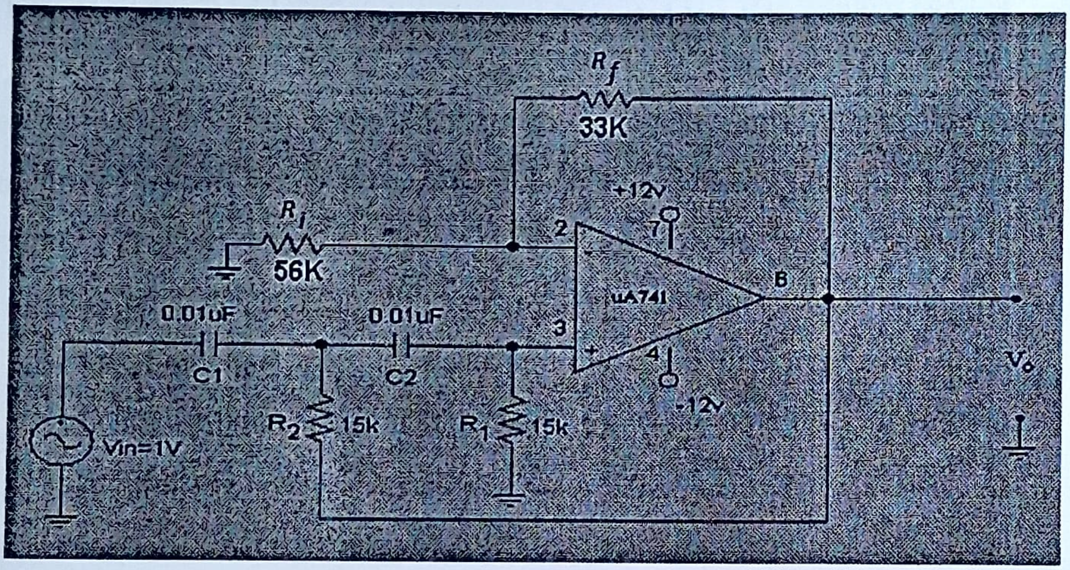
RESULT: -Record and comment on the results obtained.

B.HIGH PASS FILTER

AIM: To design a second order High pass Butter worth filterfor a cutoff frequency 1 KHz and to draw its frequency response. Calculate there from the cut-off frequency and Roll-off factor.

APPARATUS REQUIRED: Op-amp (μA741), Resistors 33KΩ, 56KΩ, 15KΩ 2nos, Capacitors 0.01μF 2nos, Power supply, Signal generator, CRO, Connecting wires and Spring board.

CIRCUIT DIAGRAM:



Using these values we get $f_c = \frac{1}{2\pi CR}$ and K =1.5858

DESIGN:

Gain, K = **$(1+R_f/R_i)$ = 1.5858** and Cut-off Frequency, fc=**$1/(2\pi CR)$**

Given f_c= 1 KHz; Let $C1=C_2=0.01\mu f$

Then $R_1=R_2=R = 1/2\pi f_c C=1/(2\pi\times 1K\times 0.01\mu f) = 15.9$ KΩ

Use $R_1=R_2=$ **(12KΩ + 3.9KΩ)** Series combination or use **R = 15KΩ** (Nearest single component)

The pass band voltage gain, K = 1.5858 $\Rightarrow R_f/R_i=0.5858$ or **$R_f= 0.5858\ R_i$**

Without losing high input impedance advantage, use R_i= 56K and R_f = 32.8K
Use nearest available single values: R_i= 56 KΩ , R_f= 33 KΩ

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PROCEDURE:

1. Make the connections as shown in the circuit diagram.
2. Apply sinusoidal I/P signal of amplitude 1V, (P-P) or any other convenient value with frequency >$10f_c$(Around 13.6V, why?) such that the O/P is undistorted and measure the O/P voltage (P – P). Record this as $\mathbf{V_{Max}}$.
3. Keeping the input signal amplitude constant, decrease the frequency until the O/P voltage reduces to $\mathbf{0.707V_{Max}}$.The frequency at which this happens is your f_c, the filter cutoff frequency.
4. Keeping the I/P signal amplitude constant at a convenient value, measure and record at least 6 readings below and 6 readings above the cutoff frequency and one reading at the cut off frequency.(**Note:** Whenever you change the frequency button /setting, you should check and adjust the I/P to its previous constant value)
5. Plot the graph of Gain in dB V/S frequency on a semi log graph paper.
6. Identify the 3dB point on your graph and identify the cut off frequency.
7. **Decrease the frequency to** $\mathbf{f_1 = \frac{1}{10} f_c}$ **.** Increase I/P signal amplitude also, so as to be able to observe some O/P on the CRO. Measure the O/P when there is no distortion.($\mathbf{V_{01}}$)
8. **Decrease the frequency to** $f_2 = \frac{1}{20} f_c$. Maintaining same I/P amplitude, measure the O/P voltage ($\mathbf{V_{02}}$)
9. Compute the **Roll – Off factor** of your filter using the formula:

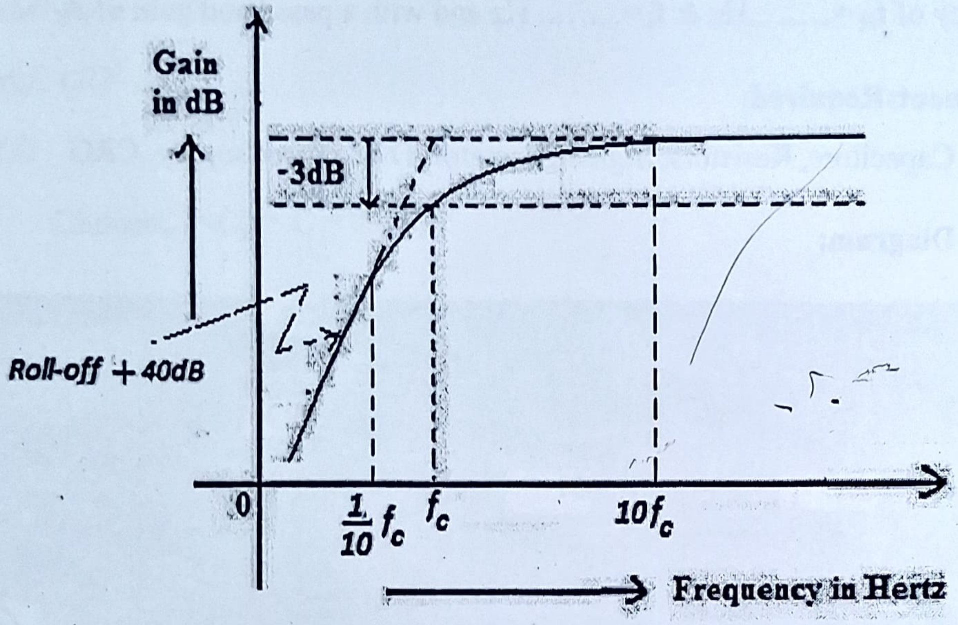
   $$\text{Roll} - \text{off Factor} = 20\log\left(\frac{V_{01}}{V_{02}}\right)\ \text{dB / Octave.}$$

{Gain in dB at $\mathbf{f_1}$ is $\mathbf{M_1=20\log(V_{01}/V_i)}$ **dB**, at $\mathbf{f_2}$ it is $\mathbf{M_2=20\log(V_{02}/V_i)}$ **dB**; Change in magnitude as the frequency is decreased is $\mathbf{M_1 - M_2 = 20\log(V_{01}/V_{02})}$ **dB**. This is the Roll – off factor. The answer is in **dB/Octave** because **the two frequencies Selected are in the ratio 1:2. To convert the answer to dB/Decade, multiply the answer obtained in dB / Octave by (20/6)}**

10. Alternatively, measure v_{o1} at $f_c/10$ and v_{o2} at $10f_c$. Roll-off factor is given by

Roll-off factor = 20log (v_{o2}/v_{o1}) dB/decade

EXPECTED FREQUENCY RESPONSE GRAPH:



TABULAR COLUMN:

V_i = ... Volts, Constant.

Frequency in Hz	Output V_0, in Volts	M=20 log (V_0/V_i) in dB

RESULT: -Record and comment on the results obtained.

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EXP NO: 2

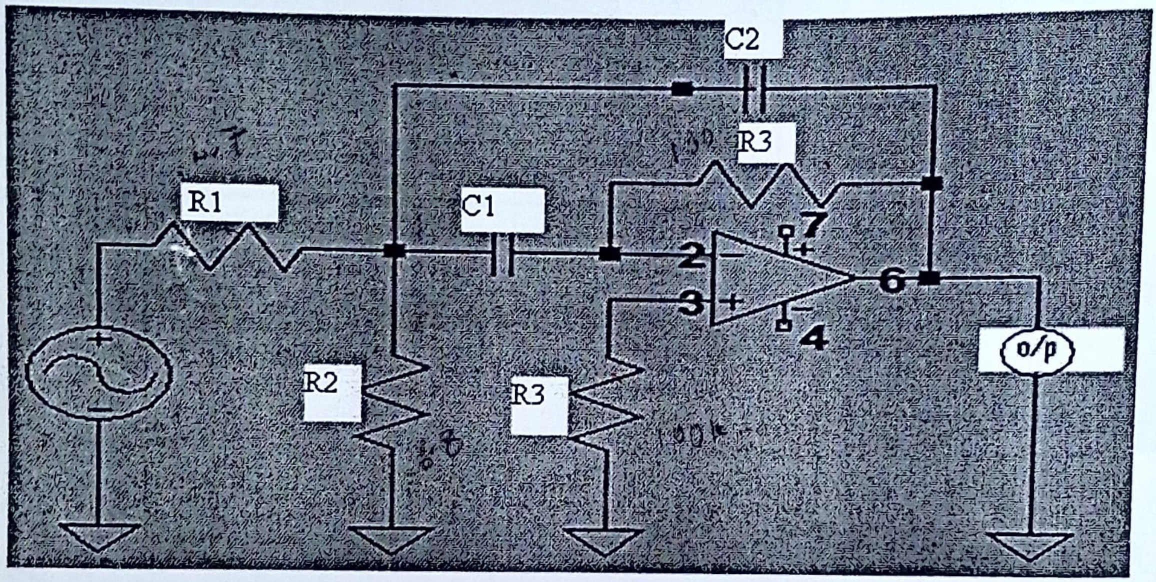
A. SECOND ORDER ACTIVE BAND PASS FILTER

Aim: To design a second order wideband pass filter and band reject filter with a cutoff frequency of f_H =........Hz & f_L=........ Hz and with a pass band gain of A_f=1.586.

ComponentsRequired:

IC-741, Capacitors, Resistors, Signal generator, Dual power supply, CRO

Circuit Diagram:



$R_1 = 4.7k$

$R_2 = 5.6k$

$R_3 = 100k$

Fig: Circuit Diagram

Design:

Band pass filters are of two types depending upon the Quality Factor 'Q'.

If Q <1, it is a wide band pass filter.

If Q >1, it is a narrow band pass filter. Let f_H=7 kHz and f_L=3 kHz,

Design: Design the band pass filter of cut off frequency f_c of 1 kHz $Q=3$ and $A_f=10$

Choose the values of C1 and C2 first and then calculate the values of R1, R2 and R3 from the equation.

$R1=Q/2\pi f_c C A_f$

$R2=Q/2\pi f_c C(2Q^2-A_f)$

$R3=Q/\pi f_c C$

Choose $C1=C2=C=0.01\ \mu F$

R1$=3/(2\pi)(10^3)(10^{-8})(10)$

$=4.77$ (Use 4.7 kΩ)

R2 $=3/(2\pi)(10^3)(10^{-8})[2(3)^2-10]$

$=5.97$ (Use 6.2 kΩ)

R3$=3/(\pi)(10^3)(10^{-8})$

$=95.5$ (Use 100 kΩ)

Procedure:

1. Make the connections as shown in the circuit diagram.
2. Set the input amplitude in the signal generator to 2Vp-p.
3. Vary the frequency of the signal generator in steps from 100 Hz to 100 kHz and note down the corresponding peak to peak output voltage at pin no. 6 with the help of CRO.
4. Tabulate the readings and plot a graph of gain in dB v/s frequency (use semi log graph).

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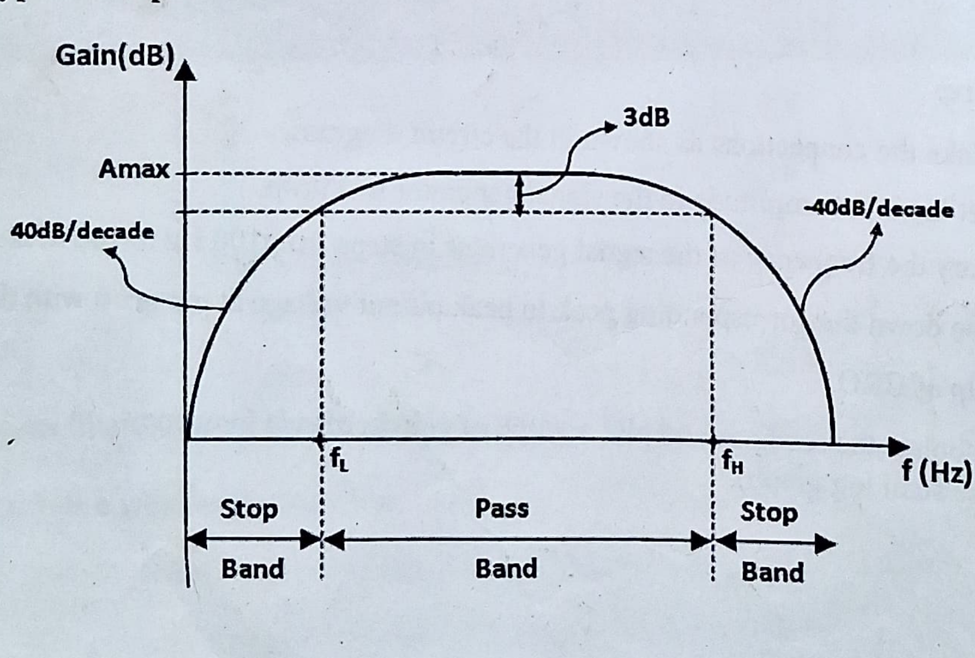
Tabular Column:

V in = 2 V p-p

Frequency (Hz)	Vo(Vp-p)	GainMagnitude = |Vo/ Vin|	Gain(dB) = 20 log |Vo/Vin|

Typical Graph:



Result: The second order band pass filter has been realized.

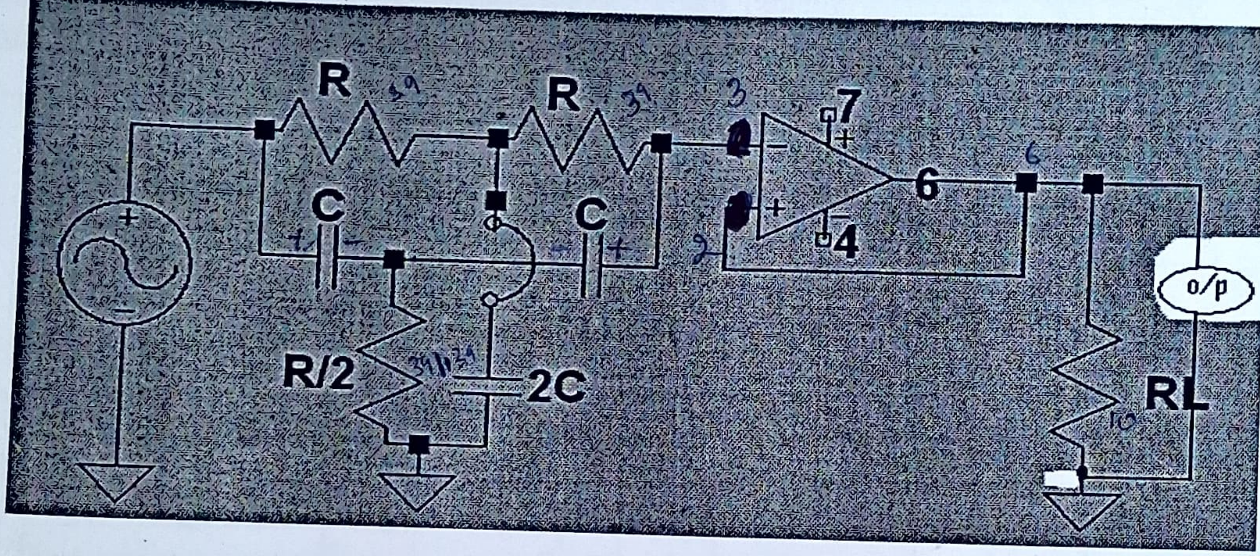
B. SECOND ORDER ACTIVE BAND ELIMINATION FILTER

Aim: To design a second order band reject filter with a cut off frequency of f_C=........ Hz

Components Required:

IC-A741, Capacitors, Resistors, Signal generator, Dual power supply, CRO

Circuit Diagram:



Band pass filters are of two types depending upon the Quality Factor 'Q'.

IfQ <1, itis a wide band reject filter.

IfQ >1, itis a narrow band reject filter.

Design: Design a 60 Hz active notch filter.

Given f_N = 60 Hz,

WKT R =1/2πf_NC,

Choose a value of C≤1μF.f_N=1/2πRC

Let C=0.068 μF

R = 1/ (2π) (60) (68) (10^{-9}) = 39.01 kΩ

Use 39 kΩ for R/2 parallel two 39 kΩ Resisters:

For the 2C component parallel two 0.068μF

R = 39K , 33

R_L = 10K or 1KΩ

C = 0.068 μF

2C = 0.136 μF

R/2 = 15KΩ

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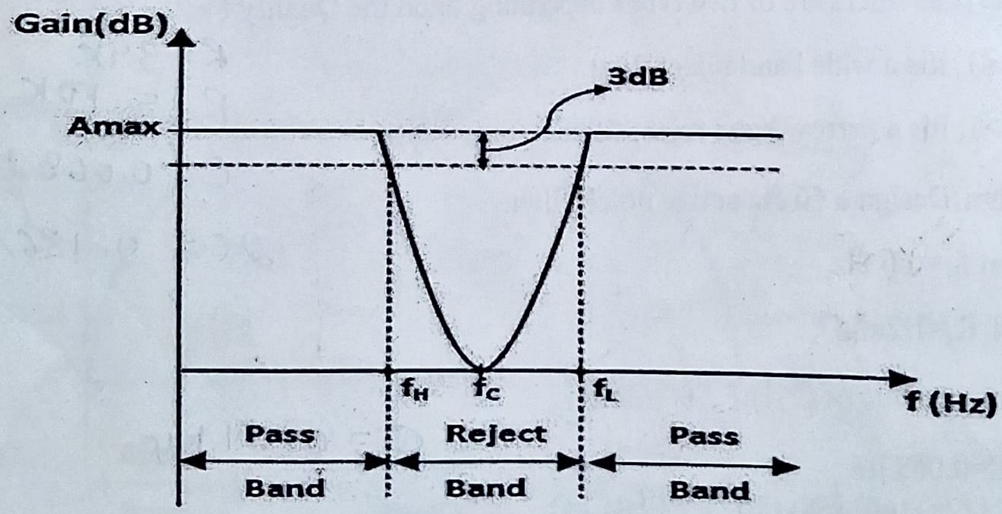
Procedure:

1. Make the connections as shown in the circuit diagram.
2. Set the input amplitude in the signal generator to 2Vp-p.
3. Vary the frequency of the signal generator in steps from100 Hz to 100 kHz and note down the corresponding peak to peak output voltage a tpin no. 6 with the help of CRO.
4. Tabulate the readings and plot a graph of gain in dB v/s frequency (use semi log Graph).

Tabular Column in =2 Vp-p

Frequency (Hz)	Vo(Vp-p)	GainMagnitude = |Vo/ Vin|	Gain(dB) = 20 log |Vo/ Vin|

Typical Graph:



Result: The second order band pass filter has been realized.

EXP NO: 3

DESIGN AND TESTING OF CLASS C TUNED AMPLIFIER

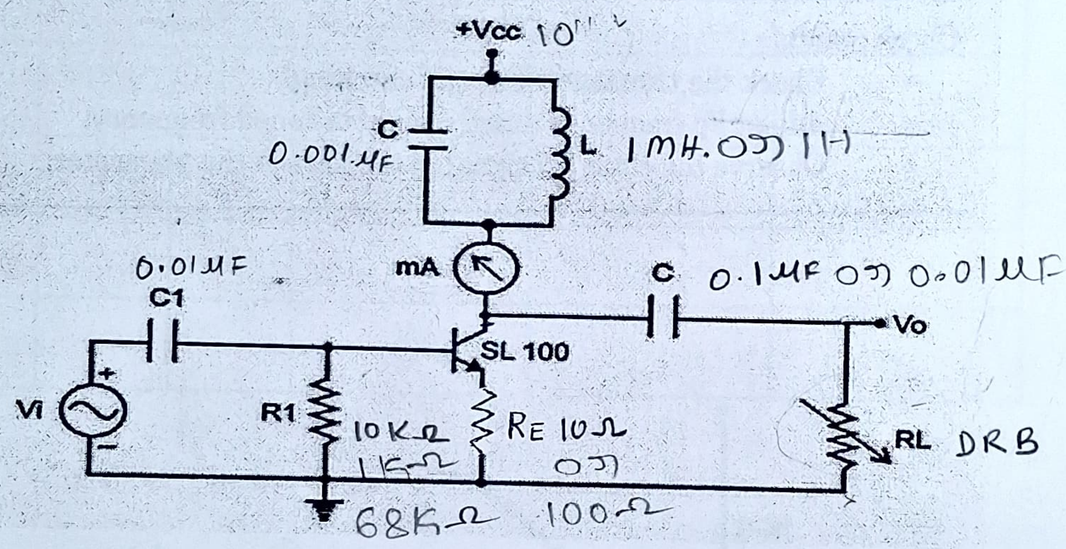
AIM: Study and Design ofa Class C tuned Amplifier at Centre frequency.

PREREQUISITE: -Knowledge of class C Amplifier, Tuned Amplifiers, etc.

APPARATUS: Class C Tuned amplifier kit, CRO, function generator, power supply.

CIRCUIT DIAGRAM: -

Class-C Tuned Amplifier



PROCEDURE:

1. Connections are made as shown in the circuit diagram.
2. Adjust the input frequency of the signal to get the maximum output at the load.
3. For the applied DC voltage adjust the amplitude of sine wave signal so that the output signal peak to peak amplitude is twice of the DC voltage(without any distortion)
4. Vary the load resistance R_L around 10 KW.
5. Note V_O, V_{DC}, I_C and R_L to find P_{AC} and P_{DC} hence the efficiency.
   (Note: While measuring V_O short the Ammeter connection)

7

Design:-

Specification:

Frequency $f = 150$ KHz, $t = 6.66$ usec

$R_1C_1 >> t$, i.e, $R_1C_1 = 100\,t$

Choose $C_1 = 0.01\mu f$, the $R_1 = 66.6\ K\Omega$.Select $R_1 = 68\ K\Omega$ (std value)

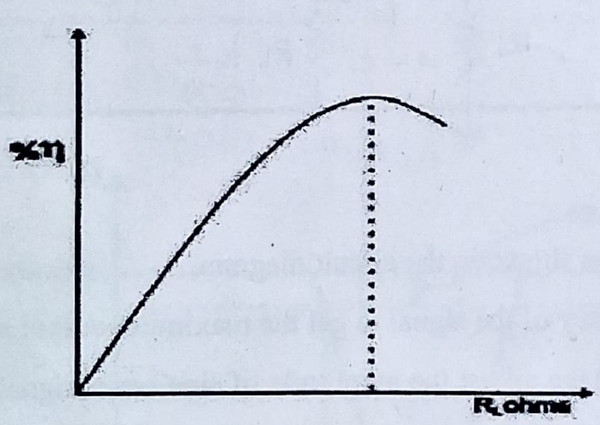
Tank ckt: $f = \dfrac{1}{2\pi\sqrt{LC}} = 150KHz$

If $C = 0.001\mu f$, then $L = 1.125$ mH ~1mH. Then $F_{actual} = 159$ KHz.

$$\boxed{R1 = 68K\Omega,\ C1 = 0.01\mu f,\ C = 0.001\mu f,\ L = 1mH}$$

Check points: -

- Check the transistor (See self checking)
- Adjust i/p frequency exactly equal to tuned frequency.
- Observe the clamped signal at the base of the transistor.



Observation table:

$Pdc = \frac{Vdc^2}{RL}$

R_L (Ohms)	Vo (Volts)	V_{DC} (Volts)	I_C (mA)	$P_{ac}=Vo^2/8R_L$ (mW)	$P_{dc}=V_{DC}I_C$ (mW)	$\eta = P_{ac}/P_{dc}$

CONCLUSION:

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EXP NO: 4

Amplitude modulation using transistor (Generation and detection)

AM USING TRANSISTOR

AIM: To conduct an experiment to generate an AM signal using transistors& to find its modulation Index. Also demodulate the AM signal using diode envelope detector circuit.

APPARATUS REQUIRED: Transistor SL100, Resistors10Ω, 10KΩ, 150KΩ, Capacitors 0.1µF(3nos), 0.01µF, 0.001µF, 470 pF, Discrete Inductance 100 µH, AFT, Diode 0A79, Two Signal generators, Dual Trace CRO.

CIRCUIT DIAGRAM:

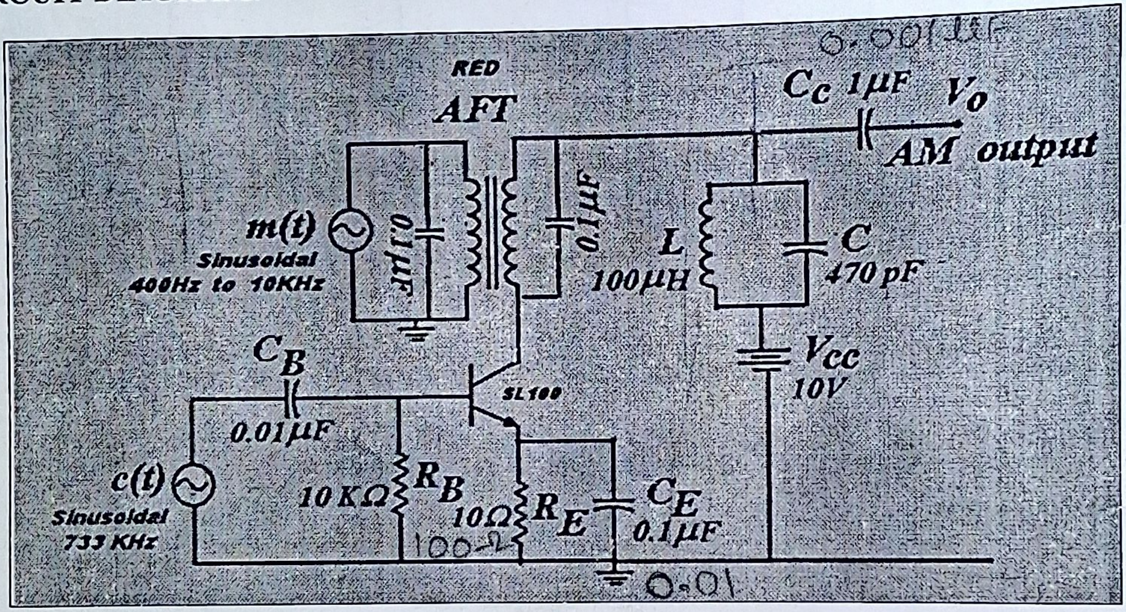


Fig 1: Transistor AM generator (Collector Modulator).

DESIGN:

Tank Circuit: Let the Carrier frequency be 700 KHz.

With **L = 100µH**, we have from $f_t = \frac{1}{2\pi\sqrt{LC}}$; C=515.94 pF;

Nearest available is 470 pF. **Use C= 470pF**

The new tank frequency is f_t= 733.4 KHz $\Rightarrow T_c=(1/f_t) = 1.36$ µs

$R_B.C_B >> T_c \Rightarrow$ with R_B=10KΩ, we can use C_B=0.01µF

R_E = 10 Ω (Arbitrary, may be for the purpose of displaying emitter voltage

70×10^{-12} $70 \times 10^{-6} \times 10^{-6}$

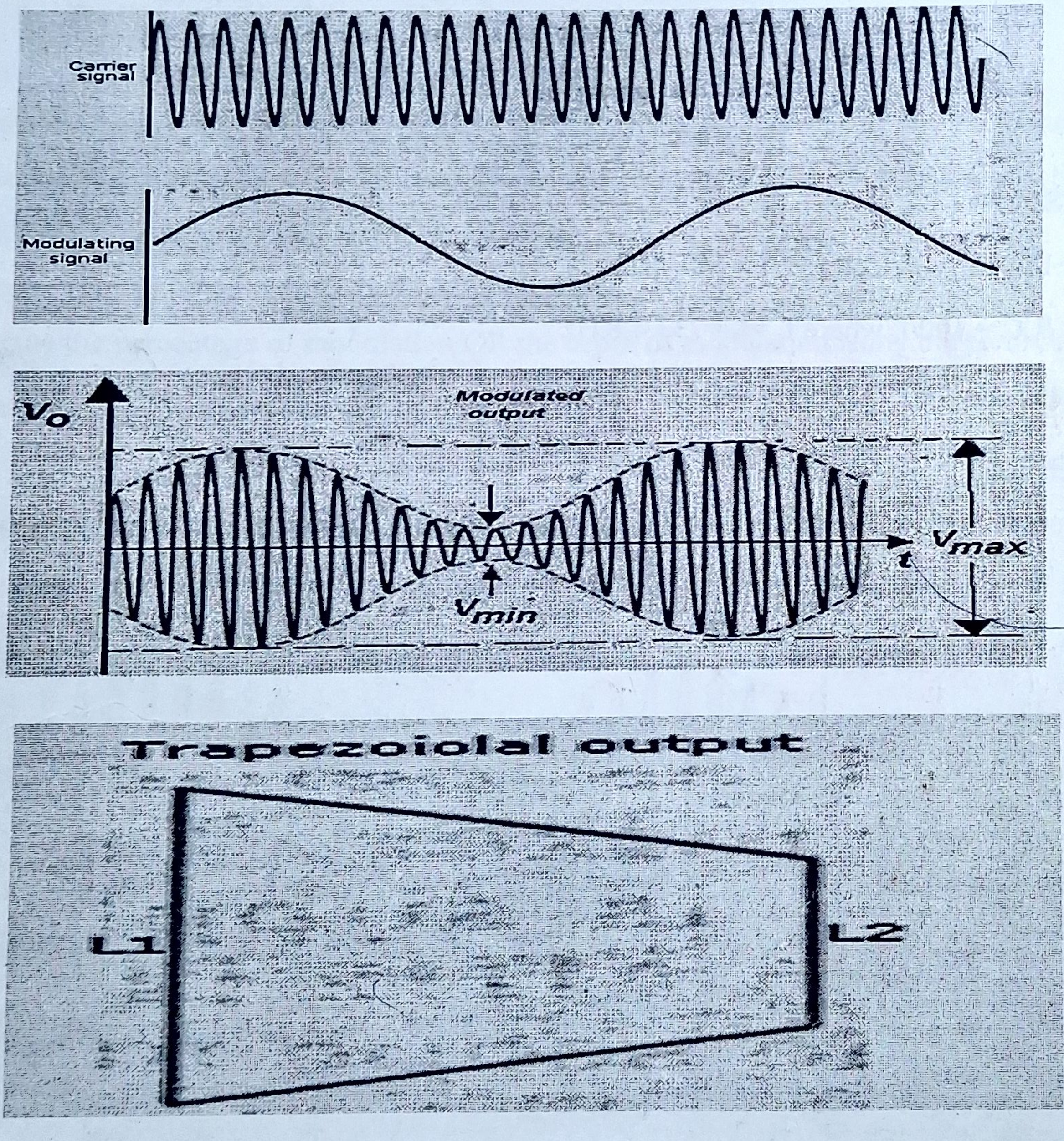
0.000070

Wave form to illustrate class C operation)

C_E =0.1μF for effectively bypassing R_E at f_t

For 100% modulation, maximum voltage that appears across collector and base of the transistor = $4V_{cc}$.This voltage shall not exceed $V_{CBO\ Max}$ specified by the manufacturer. For SL100 transistor, $V_{CBO\ Max}$ = 45 V ⇒Vcc<11.25 V. We use **Vcc = 10 V**

WAVE FORM



Expected output wave forms

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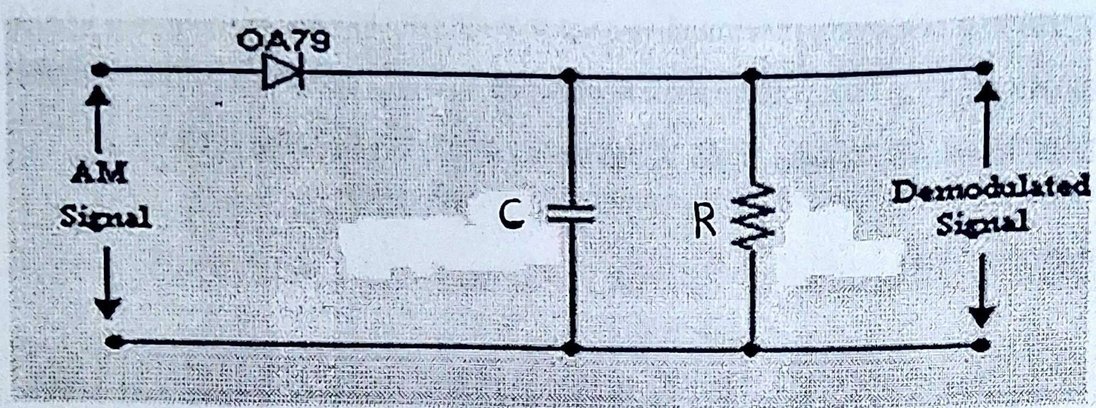
DEMODULATION CIRCUIT:



Demodulator using Diode Envelope detector.

DESIGN:

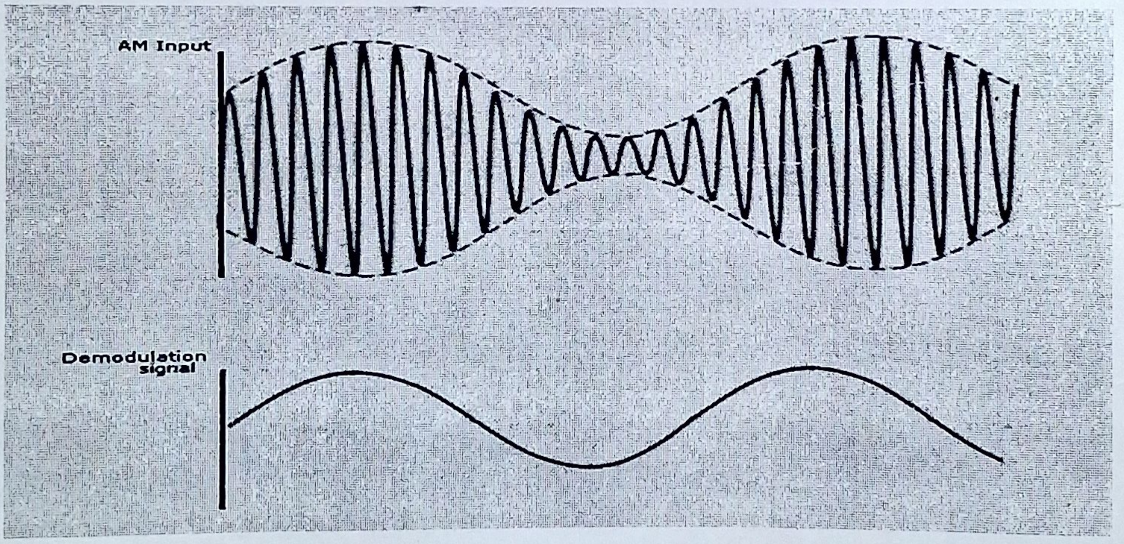
For Envelope detector: $1/f_c < RC < 1/f_m$

Let R C = $100/f_c$ where $f_c = f_t$ =733.4 KHz

Then R C =$100/733.4\times10^3$ = 0.136 mS.

Choose C = 0.001µf, then R= 136.35 KΩ.

Select R = 150 KΩ (Nearest available higher value)



Detector output wave form

PROCEURE:

1. Make the connections shown in the circuit diagram.(Fig 1)
2. Switch on the Carrier signal generator connected to the base i/p and adjust the frequency in the range of 730 KHz to 740 KHz so as to get a maximum undistorted output.
3. Increase i/p signal level until the o/p remains undistorted.
4. Now switch on modulating signal generator connected to the input of the audio frequency transformer. Observe the AM output on the CRO.
5. As you vary m(t), the depth of modulation also varies.
6. If the output wave form is not satisfactory, slightly reduce magnitude of c(t) and adjust.
7. By connecting two capacitors across primary and secondary of the AFT, you can bypass the RF signal and get an improved waveform.
8. Measure V_{max} and V_{min} as indicated on the diagram.
9. Compute the percentage of modulation OR the depth of modulation using the formula:

$$m = \frac{V_{max}-V_{min}}{V_{max}+V_{min}} \times 100\ \%$$

10. Feed m(t) to channel A (or X input) and c(t) to channel B (or Y input) and press the XY mode button. You will see a trapezoidal pattern. As shown in the diagram.
11. Measure L1 and L2 as indicated. Compute Modulation Index using the formula:

$$m = \frac{L_1-L_2}{L_1+L_2} \times 100\ \%$$

If you interchange the inputs to the CRO, the trapezoidal pattern would be rotated by 90^0

12. Make the detector circuit connections as shown in the diagram. (Fig 3)
13. Observe the o/p on the CRO and record the nature of the o/p.
14. Connect resistors of 47K, 68K, 100K 180K and 220K in place of 150K. Observe what happens as you vary the time constant R C

(W)

TABULAR COLUMN

Sl. No.	Vcc	V_{Max}	V_{Min}	m
1	4V			
2	6V			
3	8V			
4	10V			

Vcc = 10V (Constant)

Sl. No.	V_m (P-P)	V_{Max}	V_{Min}	m
1				
2				
3				
4				

Vm = 5V (P-P) Constant

Sl. No.	Vcc	V_{Max}	V_{Min}	m
1	4V			
2	6V			
3	8V			
4	10V			

RESULTS: Write your observations on the behavior of the modulator and demodulator circuits.

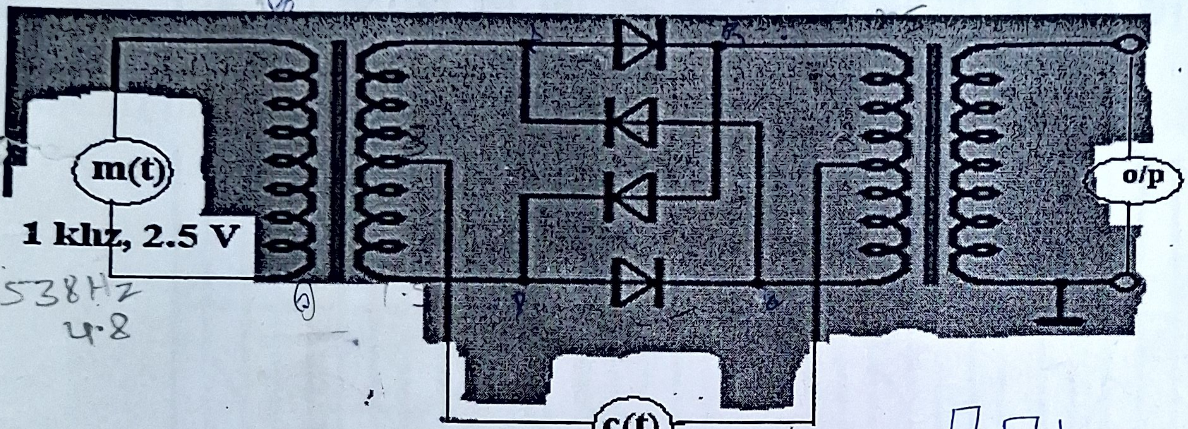
EXP NO: 5

Double Sideband Suppressed carrier Modulation (DSBSC)

AIM: To generate a double side band suppressed carrier Modulated wave, using discrete Devices and to study the input and output wave form.

APPARATUS REQUIRED: Audio Frequency Transformer (AFT) 02 Nos., Diode 0A79 04 No's, Signal generators, Dual Trace CRO.

CIRCUIT DIAGRAM:



538Hz
4.8

20 khz 5 V

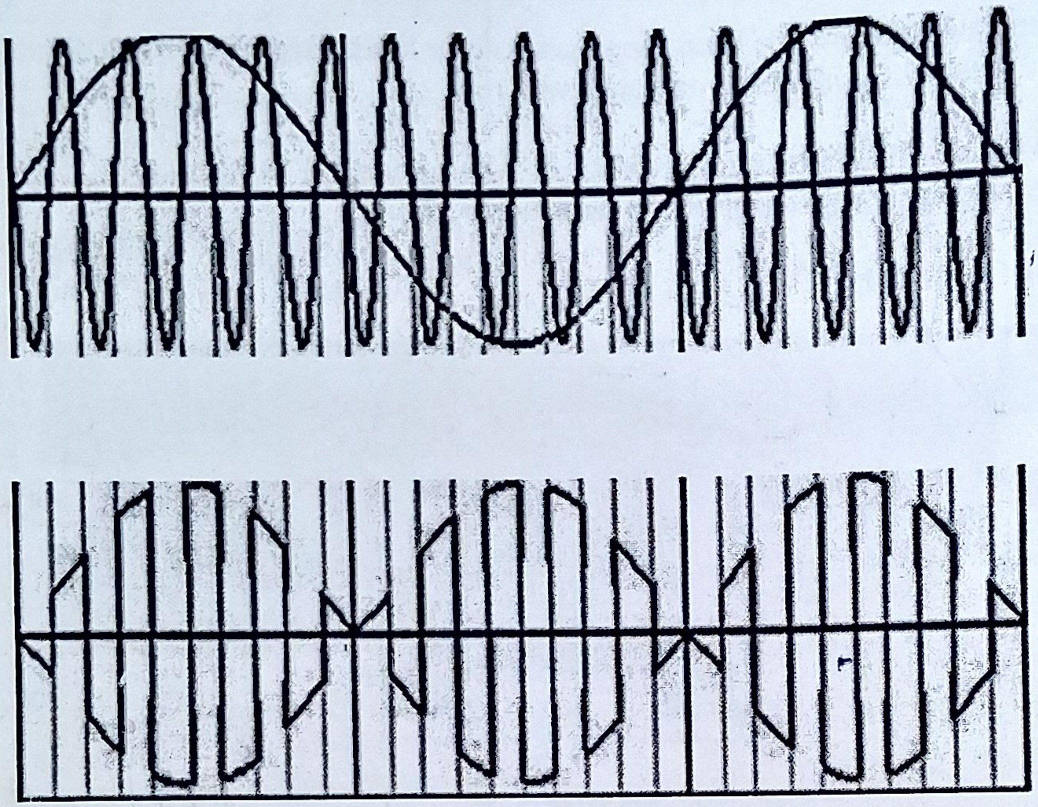
17.7KHz
2.12V

PROCEURE:

1. Connections are made as shown in the circuit diagram.
2. Connect the AF generator and carrier signal generator as shown.
3. Select the amplitude of modulating signal Vm =1 V Peak to peak, with frequency of 500 Hz and select the carrier signal of amplitude VC =3V Peak to peak and frequency of 10 Khz.
4. Observe the DSBSC wave form on CRO. Observe the Phase change at zero crossing of envelop. Study the variations by changing signal amplitudes and frequencies.

4

OUTPUT WAVE FORM



RESULTS:

EXP NO: 6

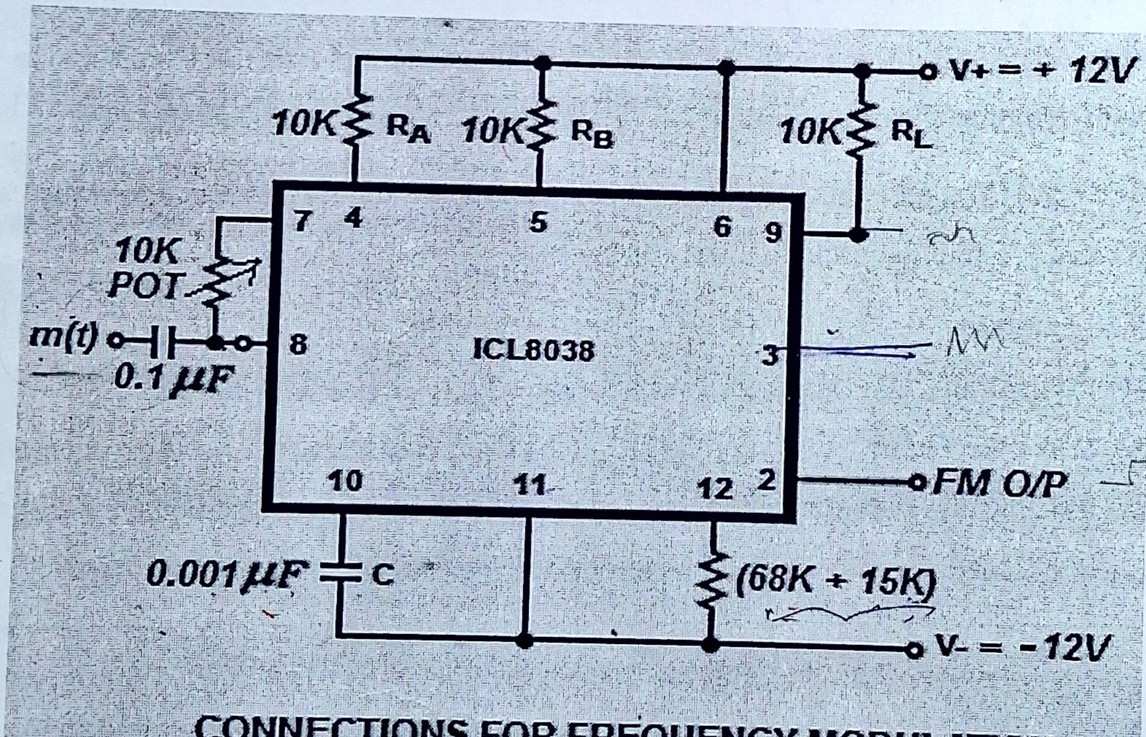
FM GENERATION USING I C 8038

AIM: To design & conduct an experiment to generate FM wave using IC 8038& to find the parameters the modulation index β, the bandwidth of operation B_T& maximum frequency deviation δ.

DESIGN: Rest frequency is given by $f_c = \frac{1}{RC}$;where C = C1 and R = R1 || R2

For the values indicated on the circuit diagram, f_c = 200 KHz

CIRCUIT DIAGRAM:



CONNECTIONS FOR FREQUENCY MODULATION

V, 6.

(12)

PROCEDURE:

Part A: Deviation Sensitivity

The Deviation Sensitivity is the amount of frequency deviation of the carrier for every volt of amplitude change in the modulating signal. In the case of the circuit above, the XR2206 is configured to vary the carrier frequency away from the rest frequency inversely to the applied voltage. Follow the steps below to determine the Deviation Sensitivity in Hz per Volt.

1. Make the connections as shown in the diagram.
2. Connect a 12 V power supply to the Modulator as indicated and apply power.
3. Connect another DC power supply in place of the Modulating Signal. Set the power supply to 0V DC. (This provides No Modulation at this point.)
4. Connect the Oscilloscope to the Modulated Output pin and adjust R3 until a sine wave with minimum distortion is seen.
5. The signal you are seeing at this point is the un-modulated Rest Frequency of the carrier. Record it's amplitude and frequency below:

   Rest frequency:____________________ Amplitude:____________________ Vpp

   Are the measured and calculated values the same?
6. Modulate the carrier by varying the DC voltage and measuring the resulting frequency of the Modulated wave form on the scope. Fill in the table below then graph the result. From the graph the inverse of the slope is the frequency sensitivity in Hz/V.

DC Bias Voltage	+ 3 Volts	+ 2 Volts	+ 1 Volt	- 1 Volt	- 2 Volts	- 3 Volts
Modulated Output Frequency						

7. From your table calculate the Deviation Sensitivity (k) of the Modulator and compare to the slope of the graph. $k = \frac{\Delta f}{\Delta V}$

8. Set up the display so that it is similar to the diagram shown below.

   From your scope display, determine the frequency deviation that is occurring. Use this

Procedure:

Measure the time for the shortest cycle being displayed: ______________

Invert the time to get the maximum frequency of the carrier :______________(Max)

Measure the time for the longest cycle being displayed: ____________

Invert the time to get the minimum frequency of the carrier :______________(Min)

Subtract Maximum Frequency from Minimum Frequency = Frequency Swing

____

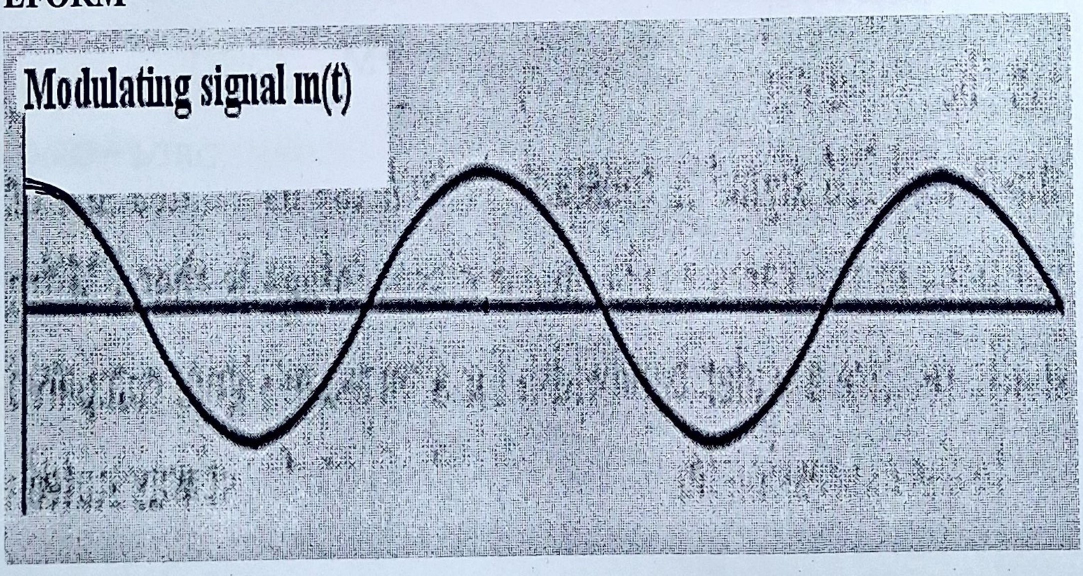
Divide the Frequency Swing by 2 to get the Peak Deviation: ______________

Calculate the frequency sensitivity from $\Delta f = kV_m$

$\Delta f = f_{max} - f_{min}$.

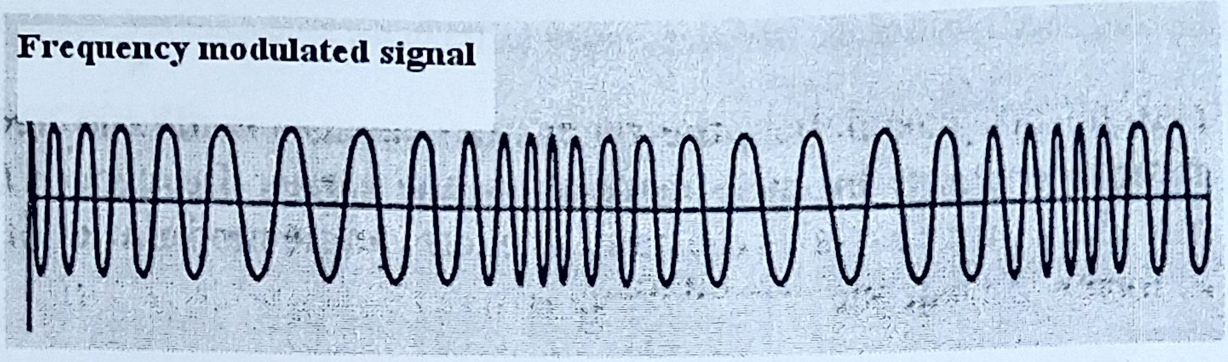
Calculate the Modulation Index, $\beta = \Delta f / f_m$

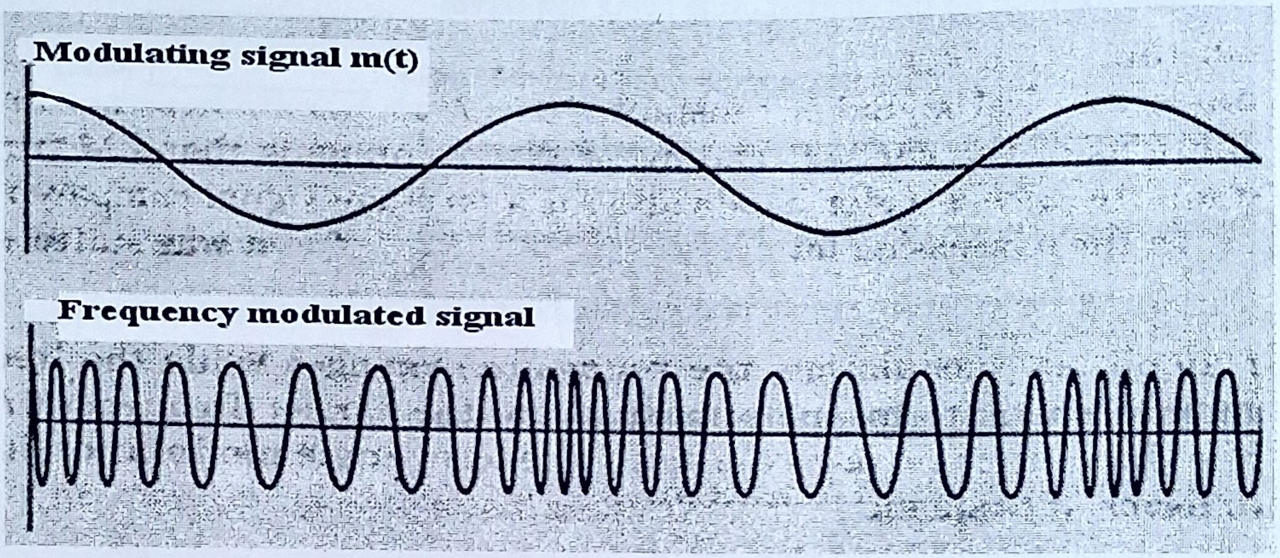
WAVEFORM



BW:

(13)

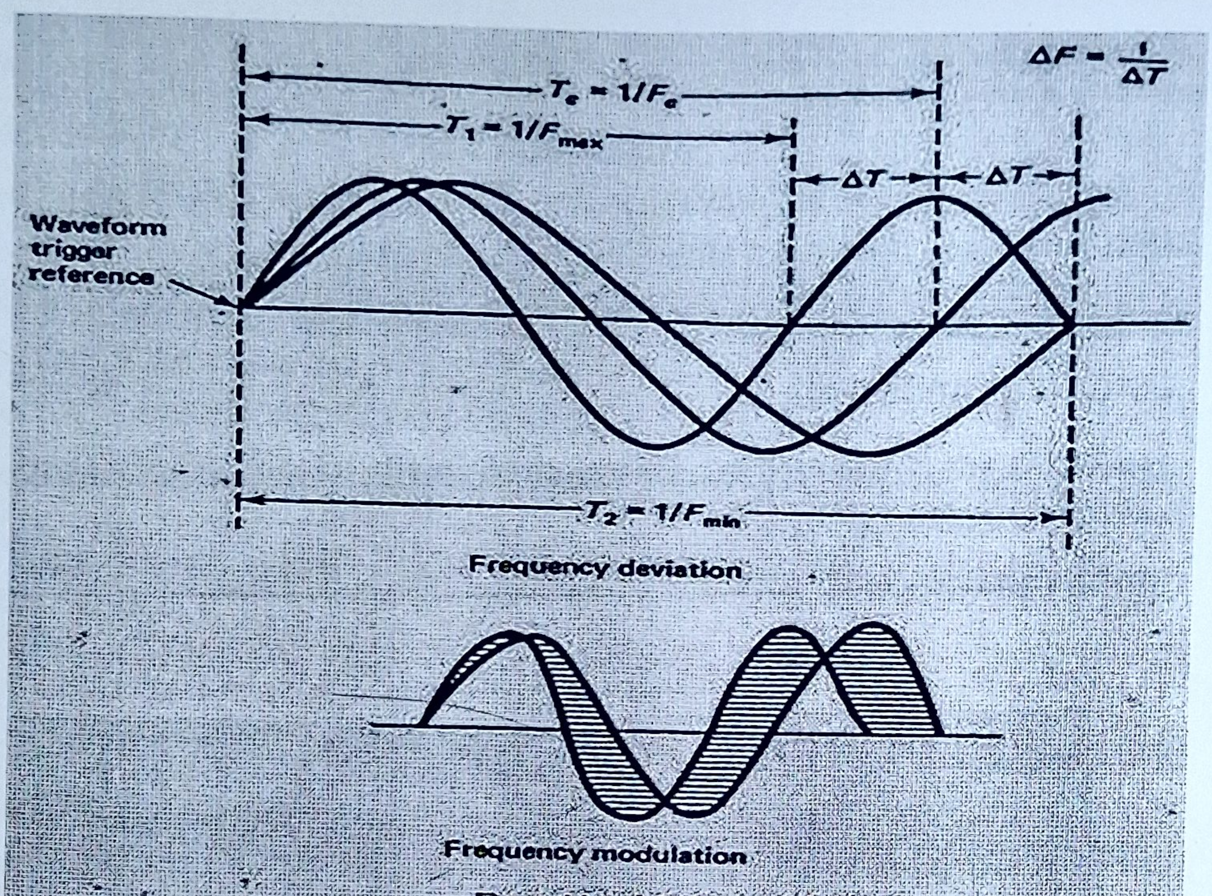




Wave forms of FM

$f_{max} = \frac{1}{T}$ $\boxed{|\Delta f|}$

f_{min}



Practical Wave forms

ACTIVITY: Another circuit is shown for FM generation using ICL8038.

The carrier frequency depends on R_A, R_B and C.

If $R_A=R_B=R$ then

$f=0.33/RC = 1/3RC$

Thus for f = 33 KHz =0.001μfwe get R = 10K. Take R_L = 10K.

Verify the performance of the circuit.

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EXP NO: 7

MIXER CIRCUIT

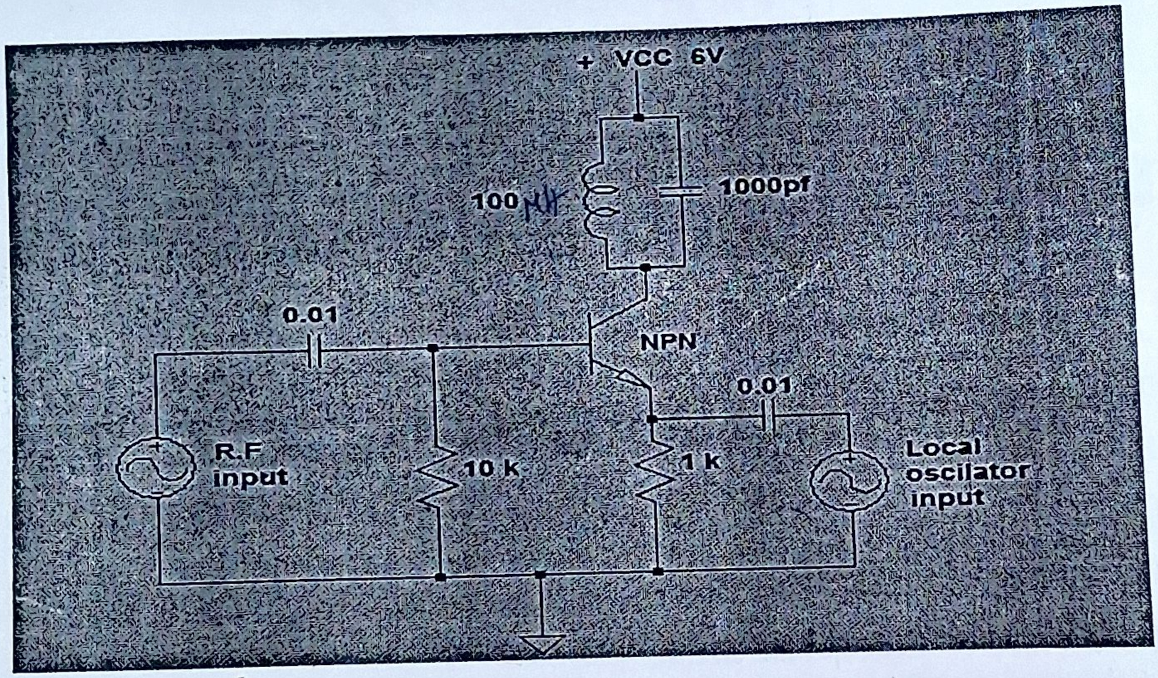
AIM: To design an IF amplifier/ Mixer Circuit and study its operation

Design BJT Mixer

APPARATUS REQUIRED:

Transistor SL 100, Resistor 390 KΩ, 150 KΩ, 680 Ω, 10 KΩ, 0.01µf 2nos, RF Signal generators 2nos, CRO.

CIRCUIT DIAGRAM:



DESIGN: Given: RF Transistor BF 194for which the working $h_{FE} = 150$. For designing of a mixer we need to choose non – linear region of operation (Why?). (See the transfer characteristics shown).

Choose near cutoff operation by selecting the base current to be < 10 μA.

Thus Let $V_{cc} = 6V$; $I_B = 5\mu A \Rightarrow I_C = 0.75\ mA \approx I_E$.

Let $R_E = 1k\Omega \Rightarrow V_E = I_E R_E = 0.51V \Rightarrow V_B = V_{BE} + V_E = 1.11V$ ($V_{BE} = 0.6V$ Si Transistor)

Let $R_2 = 10\ K\Omega \Rightarrow I_2 =$ Current through $R_2 = 1.11V/10K\Omega = 7.4\mu A$

I_1=Current through $R_1 = IB + I_2 = 12.4\ \mu A$;

V_1 = Voltage across $R_1 = V_{cc} - V_B = 4.89\ V$;

$R_1 = V_1/I_1 = 4.89V/12.4\mu A = 394.35\ K\Omega$. Use $R_1 = 390\ K\Omega$

Use $C_c = 0.01\ \mu F$ coupling capacitors for both RF I/P and Local OSC I/P

PROCEDURE:

1. Make the connections as shown in circuit diagram.
2. Set Vcc = 6V.
3. Set the amplitude of 2 V in both the signal generator.
4. One input was kept at 0 Hz and the other was varied to get maximum output.
5. The frequencies were adjusted such that their sum was equal to the tuned frequencies of the LC tank circuit.
6. The readings were tabulated.
7. The experiment was repeated by adjusting the frequencies such that their difference Was equal to the tuned frequencies.

FRF	700 KHz	1.2 MHz	1.5 MHz	2.0 MHz	2.5 MHz
FLO=FRF – 455 (UP Conversion)					
FLO=FRF + 455 (Down Conversion)					

RESULT:

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EXP NO: 8

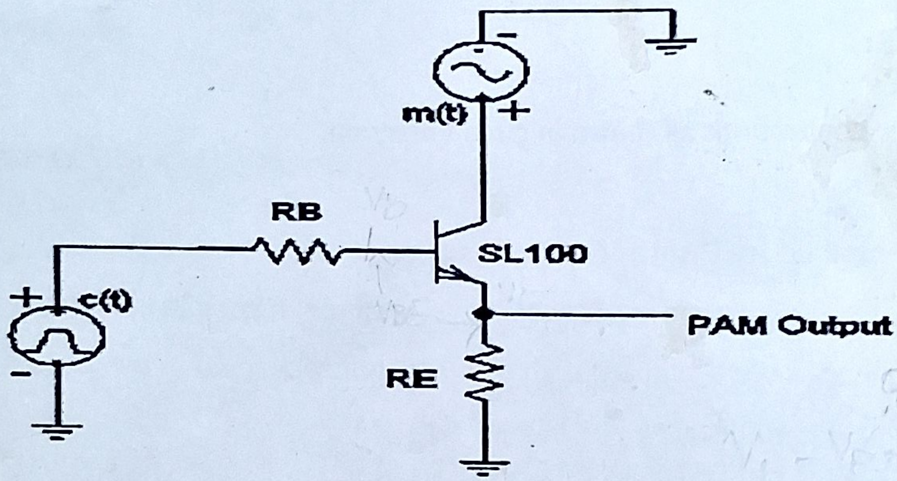
PULSE AMPLITUDE MODULATION (PAM) ANDDETECTION

Aim: To generate PAM signal, de modulate it and to verify sampling theorem.

Components: Transistor (SL100), Resistors, Capacitors, CRO, Signal generators.

Modulation

Circuit diagram:



Design:

$R_B=10\ R_C$ $\quad R_C \approx R_E$

$\therefore R_B=10\ R_E$

Let $R_E=1k\Omega$ $\quad \therefore R_B=10\ k\Omega$.

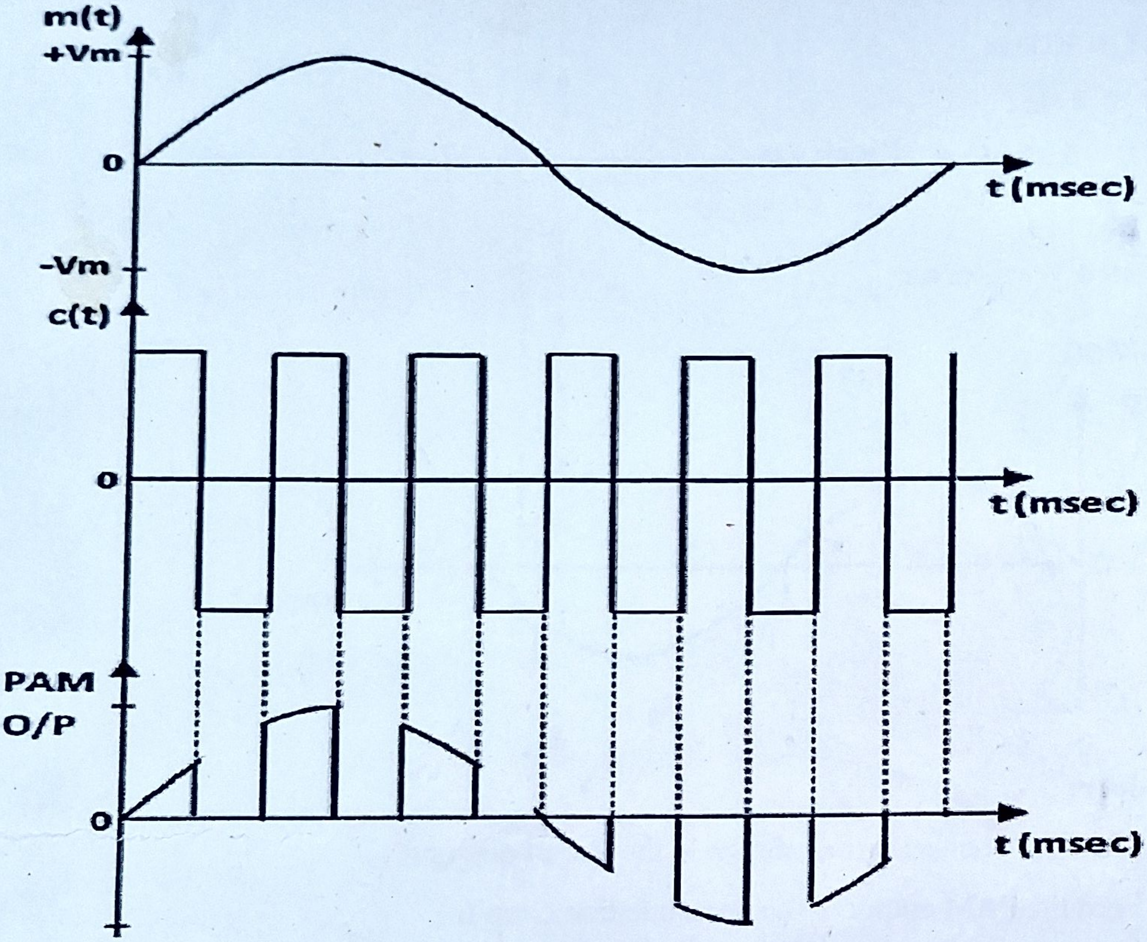
Procedure:

1. Make the connections as shown in the circuit diagram.
2. Set the carrier amplitude & frequency greater than modulating signal.

   m (t): fm=500 Hz to 2 KHz, Vm=1.5 Vpp

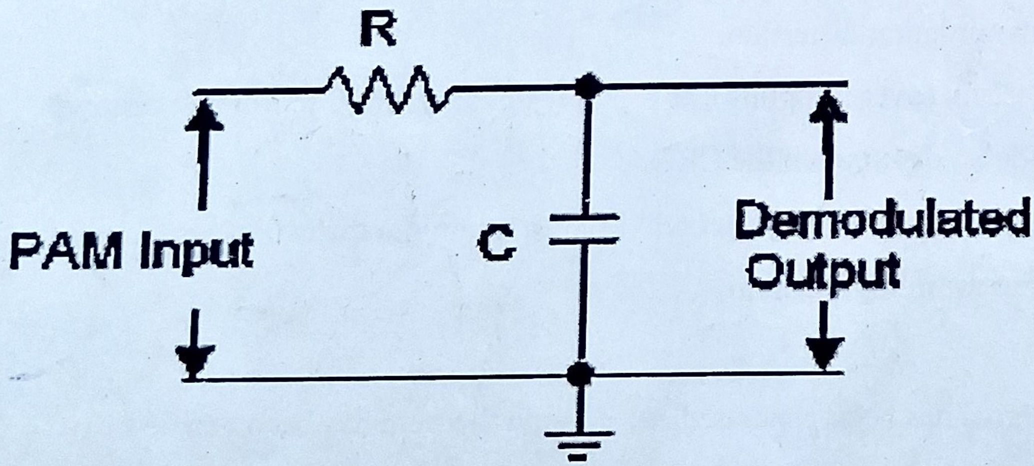
   c(t): fc=10 KHz to 100 KHz, Vc=10-15 Vpp
3. Observe the PAM output on the CRO.

Expected Waveforms:



B). Demodulation

Circuit Diagram:



(16)

- TDM
- Sampling

Design:

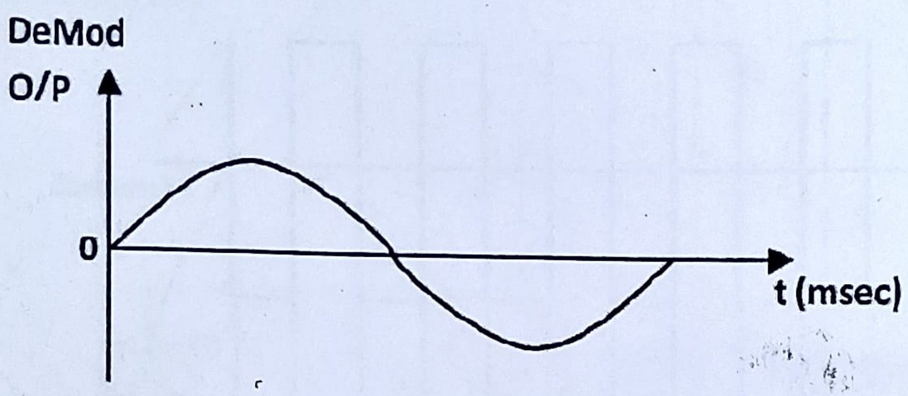
$1/f_m >> RC >> 1/f_c$

Let $f_c = 50$ kHz,

$RC >> 1/f_c$;

Let $C = 0.01\ \mu F$ & $R = 10\ K\Omega$

Expected Waveform:



Procedure:

1. Make the connections as shown in the circuit diagram.
2. Feed the PAM output to the demodulation circuit.
3. **To verify sampling theorem:**
   The sampling theorem states that if the sampling rate in any system exceeds twice the Maximum signal frequency, then the original signal can be reconstructed in receiver side With minimum distortion.
4. Keep fc > 2 fm (over sampling), fc = 2fm (right sampling), fc < 2fm& observe the demodulated output on the CRO.
5. Observe that demodulated output will be with minimum distortion for fc > 2 fm. This verifies sampling theorem.

Result: PAM signal has been generated & sampling theorem has been verified.

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