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1.

a. LDI R1, label in machine code is 1010 001 001100101
1010 for LDI opcode
001 for binary of decimal 1 of R1
001100101 for the decimal difference between the instruction memory address (x31A1) and the label memory address (x3246) converted to binary. The offset of the label from the program counter.
b. Transfers the value stored at the memory address x3246 which is stored in *label* to R1.
c.
I could not understand what this question wanted. I assume it wants me to copy the FSM control signals for the instruction from the provided PDF but if this is not correct, I do not intend to plagiarize.
1. ADDR1MUX selects PC
2. ADDR2MUX selects SEXT(IR[8:0])
3. MARMUX selects ADDR ADD
4. Gate.MARMUX
5. LD.MAR
6. MEM.EN/R
a. Wait for R
7. MDRMUX selects Memory
8. LD.MDR
9. Gate.MDR
10. LD.MAR
11. MEM.EN/R
12. MDRMUX selects Memory (the MDRMUX is not shown in the simplified datapath)
13. LD.MDR
14. Gate.MDR (the MDR Gate is not shown in the simplified datapath)
15. DRMUX selects IR[11:9] (not shown in the simplified datapath)
16. LD.REG

2.

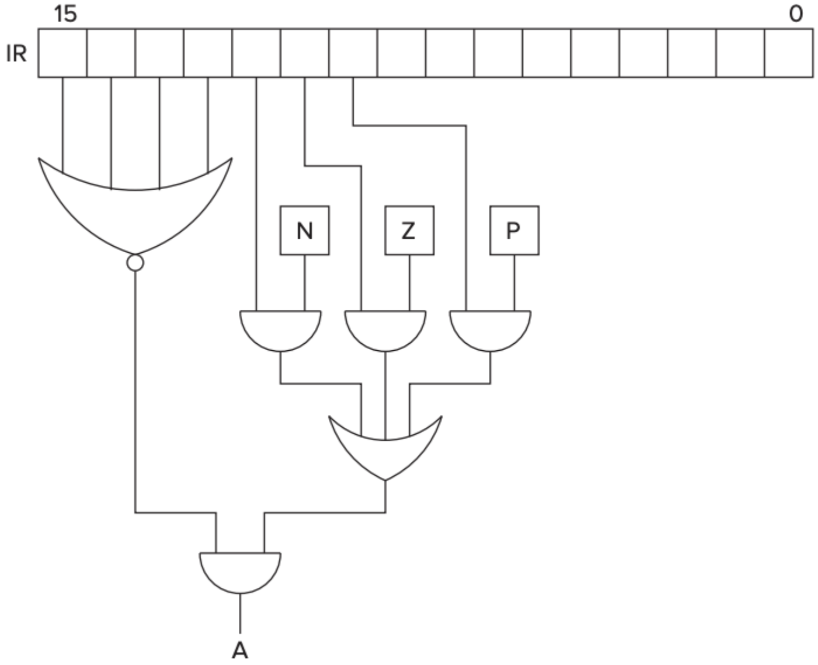
a. STR R0, R6, x0 in machine code is 0111 000 110 000000
0111 for STR opcode
000 for binary of decimal 0 of R0
110 for binary of decimal 6 of R6
000000 for binary of decimal 0 offset
b. Transfers the value stored in R0 to the memory address stored in R6
c. I could not understand what this question wanted. I assume it wants me to copy the FSM control signals for the instruction from the provided PDF but if this is not correct, I do not intend to plagiarize.
1. SR1MUX selects IR[8:6]

2. ADDR1MUX selects SR1OUT
3. ADDR2MUX selects SEXT(IR[5:0])
4. MARMUX selects ADDR ADD
5. Gate.MARMUX
6. LD.MAR
7. SR1MUX selects IR[11:9] (not shown in the simplified datapath)
8. ALUK selects Pass Through
9. Gate.ALU
10. MDRMUX selects Bus
11. LD.MDR
12. MEM.EN/W

3.

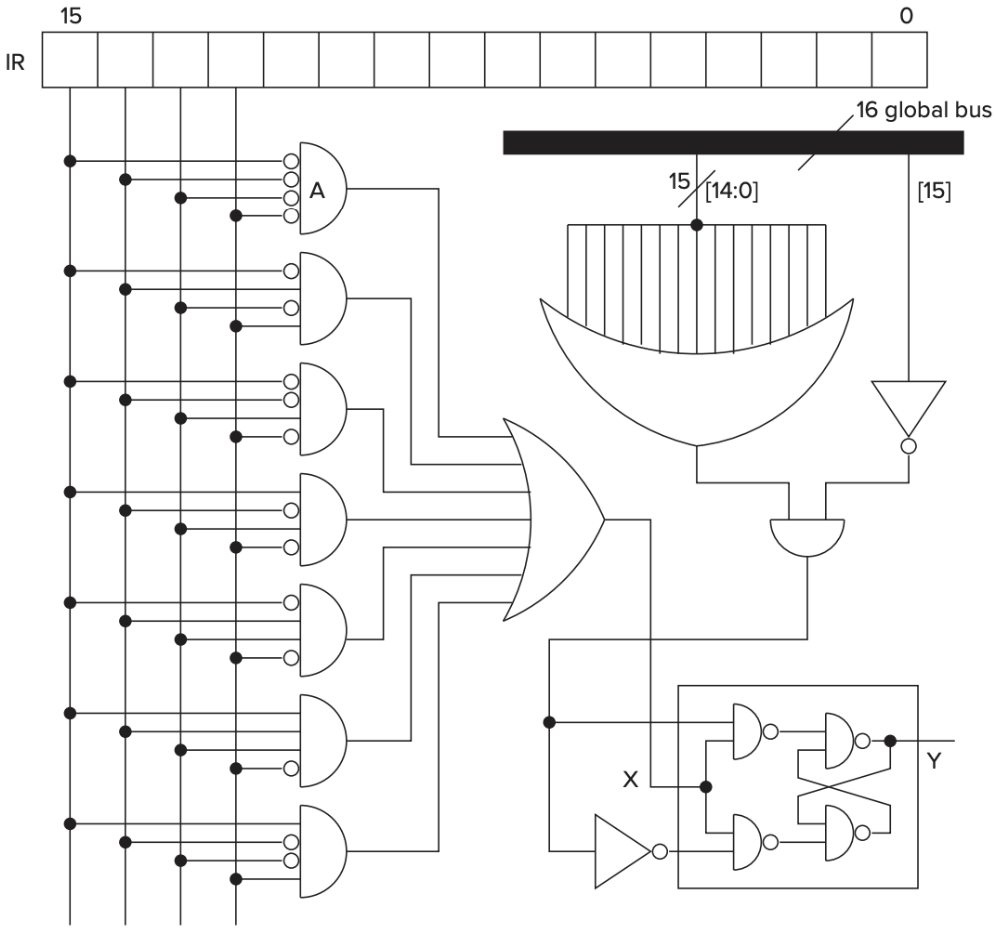
a. BRzp label in machine code is 0000 011 100000001
0000 for BR opcode
011 for n, z, p (no n, yes z, yes p)
100000001 for the decimal difference between the instruction memory address (x35D0) and the label memory address (x35D0) converted to binary. The offset of the label from the program counter.
b. Branch to label if the most recent operation resulted in a zero or positive
c. I could not understand what this question wanted. I assume it wants me to copy the FSM control signals for the instruction from the provided PDF but if this is not correct, I do not intend to plagiarize.
1. ADDR1MUX selects PC
2. ADDR2MUX selects SEXT(IR[8:0])
3. PCMUX selects ADDR ADD
4. LD.PC iff (N.n + Z.z + P.p)

5.40 The following logic diagram shows part of the control structure of the LC-3 machine. What is the purpose of the signal labeled A?



The signal A determines whether the program should branch or not.

5.41 A part of the implementation of the LC-3 architecture is shown in the following diagram.
a. What information does Y provide?
Y is the P condition code.
b. The signal X is the control signal that gates the gated D latch. Is there an error in the logic that produces X?
No, signal X produces 1.



5.42 The LC-3 macho-company has decided to use opcode 1101 to implement a new instruction. They need your help to pick the most useful one from the following:

a. MOVE Ri, Rj; The contents of Rj are copied into Ri.
b. NAND Ri, Rj, Rk; Ri is the bit-wise NAND of Rj, Rk
c. SHFL Ri, Rj, #2; The contents of Rj are shifted left 2 bits and stored into Ri.
d. MUL Ri, Rj, Rk; Ri is the product of 2’s complement integers in Rj, Rk.

Justify your answer.
I would pick c because this instruction has the most use cases. This instruction can support arithmetic operations like addition, subtraction, and multiplication by shifting bits which is very versatile compared to the other instructions.