Optimised Arithmetic logic unit with carry look ahead generation

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INTRODUCTION

An arithmetic logic unit acts as the basic building blocks or cell of a central processing unit of a computer. And it is a digital circuit comprised of the basic electronics components, which is used to perform various function of arithmetic and logic and integral operations further the purpose of this work is to propose the design of an 4-bit ALU . Thus, the functionalities of the ALU in this study consist of following main functions like addition also subtraction, increment, decrement, AND, OR, NOT, XOR, NOR also two complement generation multiplication. And the functions with the adder in the airthemetic logic unit are implemented using a Carry Look Ahead adder joined by a ripple carry approach. The proposed ALU can be designed by using verilog or VHDL.

WHAT IS AN ALU?

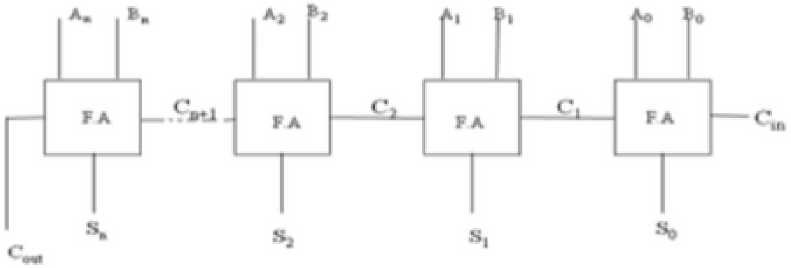
Instead of having individual registers performing the microoperations directly, computer systems employ a number of storage registers connected to a common operational unit called an arithmetic logic unit, abbrevited ALU. To perform a microoperations ,the contents of specified registers are placed in the inputs of the common ALU. The ALU performs an operation and the result of the operation is then transferred to a destination register .

WHAT ARE ADDERS AND IN SPECIFIC CARRY LOOK AHEAD ADDERS

A digital computer must contain circuits which can perform arithmetic operations such as addition, subtraction, multiplication, and division. Among these, addition and subtraction are the basic operations whereas multiplication and division are the repeated addition and subtraction respectively.

To perform these operations 'Adder circuits' are implemented using basic logic gates. Adder circuits are evolved as Half-adder, Full-adder, Ripple-carry Adder, and Carry Look-ahead Adder.

Among these **Carry Look-ahead Adder is the faster adder circuit.** It reduces the propagation delay, which occurs during addition, by using more complex hardware circuitry. It is designed by transforming the ripple-carry Adder circuit such that the carry logic of the adder is changed into two-level logic



Ripple carry adder

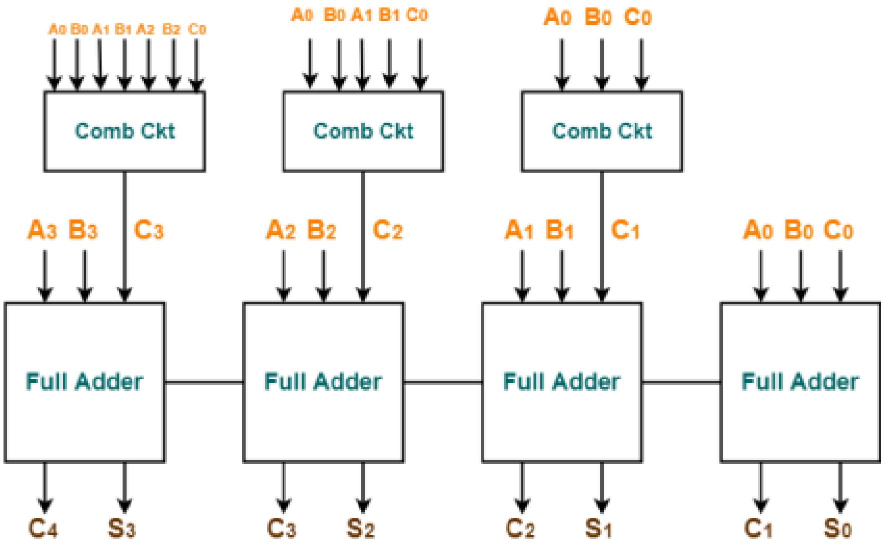
DIFFERENT COMPONENTS OF AN ALU, THEIR PROBLEMS AND SOLUTION

1) ADDERS

Various adder circuits are used in other Arithmetic logic unit which is used to perform the addition operations , also conventional ripple-carry adders have been used while designing logical circuits but it has been seen that when two individual operands are applied as input to adder, it takes less time before giving out the valid output result. This happens because each full adder in the combination introduces a certain delay. If one full adder introduce a delay of time ‘t’ then for an ‘n’ bit circuit the total delay after which Cout is obtained is ‘(n-1)t’. The delay incurred depends on the size of the operands. Thus when higher bit number is used the delay becomes highly unacceptable.

In digital adders the speed of addition is limited by the time required to propagate the carry signal towards the adder also in an elementary adder the generation of sum for each bit position takes places in a sequentially only after the preceding bit position has been summed and a carry is propagated in to the ascending next position

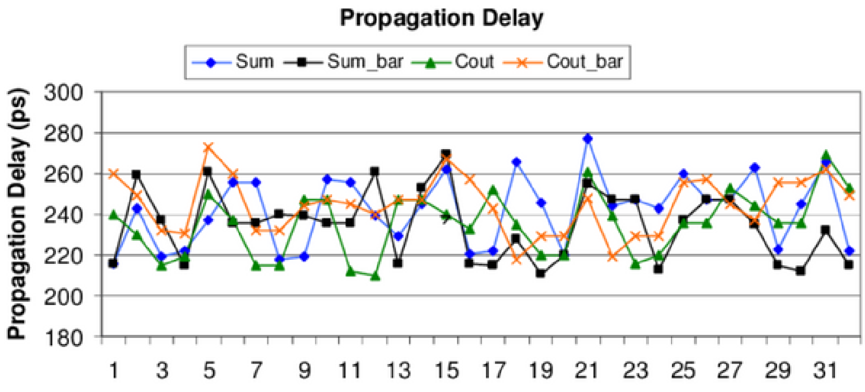
A carry look-ahead helps us in eliminating the delay caused by the propagation of the Carry signal in a binary adder thus; the delay caused in the addition operation is because of the carry signal.



Carry Look Ahead Adder

2.)SUBTRACTOR

We construct the subtract or circuit by implementing the carry look-ahead adder and an inverter. For an n-bit number a complement 2N is what the two’s complement means. The result obtained after we subtract the number by 2N also the two’s complement exhibits the behaviour of the negative to be in use of the original number.



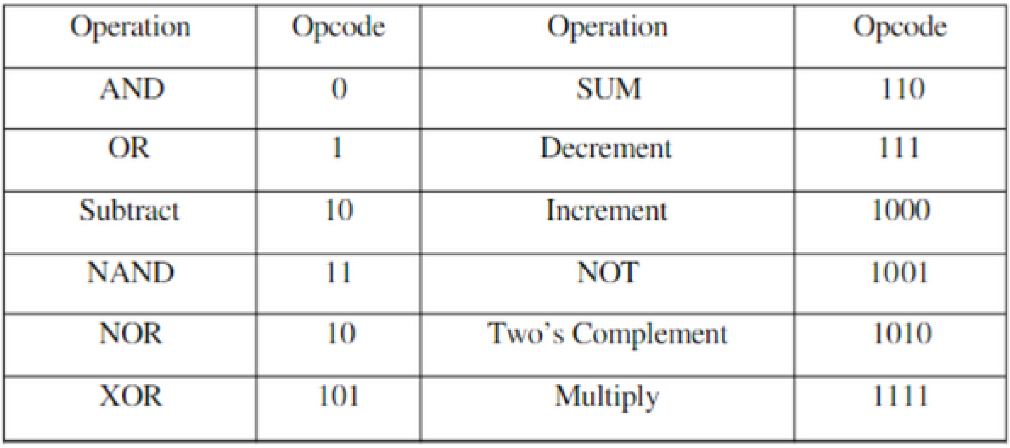
3.)INCREMENT AND UNIT DECREMENT

The incrementer and decrement units are built using the adder and subtractor units. For increment one of the addends is given the input value logic ‘1’. For decrement unit the subtrahend of the subtractor is provided with logic ‘1’ value.

Two’s complement generation:

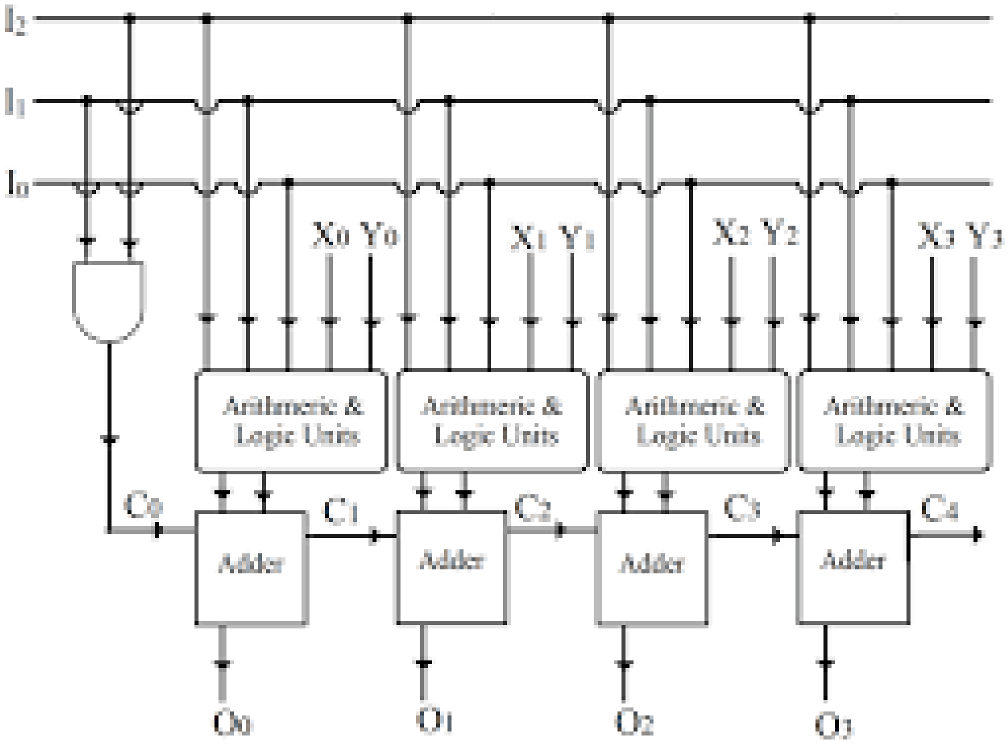
The Two’s complement generator circuit is achieved by using an inverter and also an incremental thus; the input operands is passed by an inverter which inverts its digit also the output of the inverter is as input to the incremental. The incremented add as logic 1 to the inverted bits. Therefore, the output generated is the two’s complement of the input bit.

The multiplexer is used to select the output. All operations are performed in a single cycle but only the required operation is selected by the multiplexer.

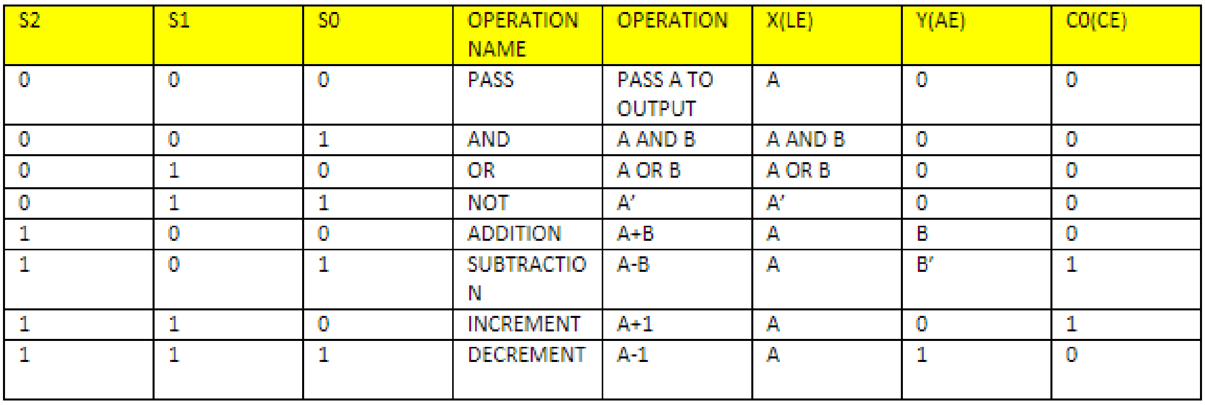


Operation	Opcode	Operation	Opcode
AND	0	SUM	110
OR	1	Decrement	111
Subtract	10	Increment	1000
NAND	11	NOT	1001
NOR	10	Two’s Complement	1010
XOR	101	Multiply	1111

CONVENTIONAL ALU SCHEMATIC



ALL FUNCTION TABLE



S2	S1	S0	OPERATION NAME	OPERATION	X(LE)	Y(AE)	C0(CE)
0	0	0	PASS	PASS A TO OUTPUT	A	0	0
0	0	1	AND	A AND B	A AND B	0	0
0	1	0	OR	A OR B	A OR B	0	0
0	1	1	NOT	A’	A’	0	0
1	0	0	ADDITION	A+B	A	B	0
1	0	1	SUBTRACTION	A-B	A	B’	1
1	1	0	INCREMENT	A+1	A	0	1
1	1	1	DECREMENT	A-1	A	1	0

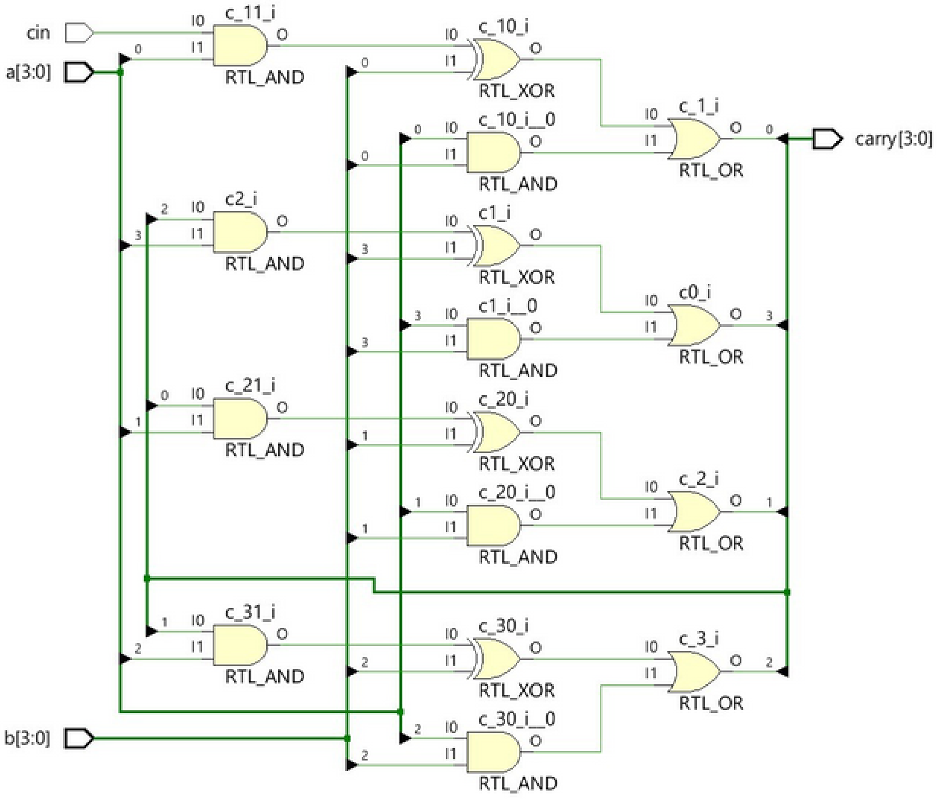
Verilog Code:

We implemented the design of ALU with CLA using Verilog language.

The Code and the testbench can be accesed using this link:

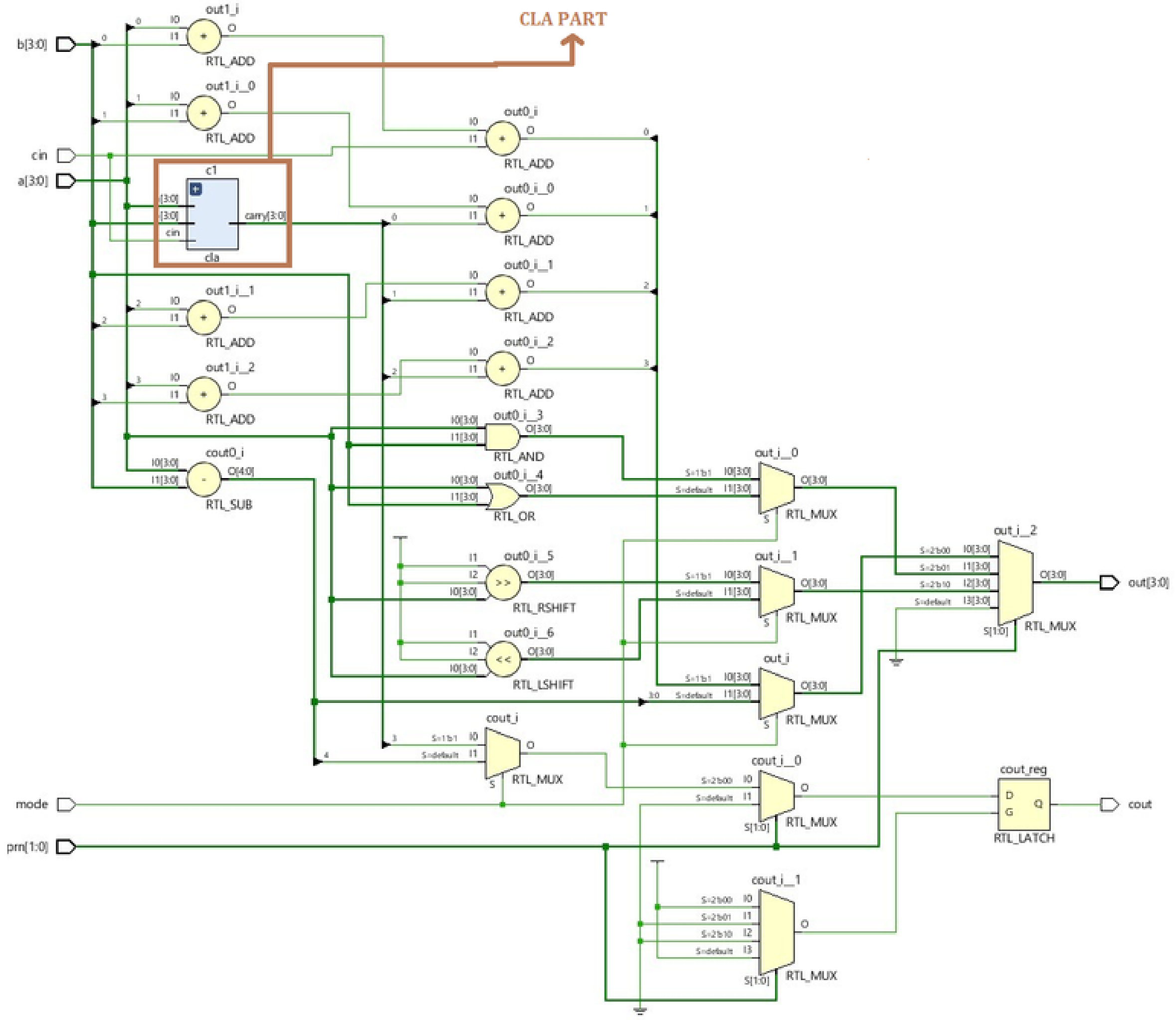
LINK FOR CODE: CLICK HERE
LINK FOR TEST BENCH: CLICK HERE
LINK FOR SIMULATION: CLICK HERE

CLA DESIGN



The following is the schematic of CLA as received after we coded the CLA on vivado using verilog

ALU WITH CLA SCHEMATIC



The following is the schematic of CLA as received after we coded the CLA on vivado using verilog

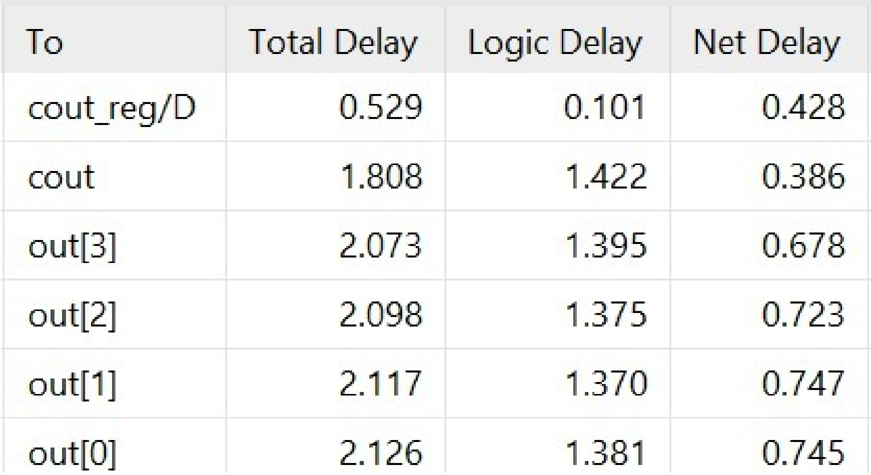
ADVANTAGES:

Following are the advantages of using ALU With CLA

- Speed:

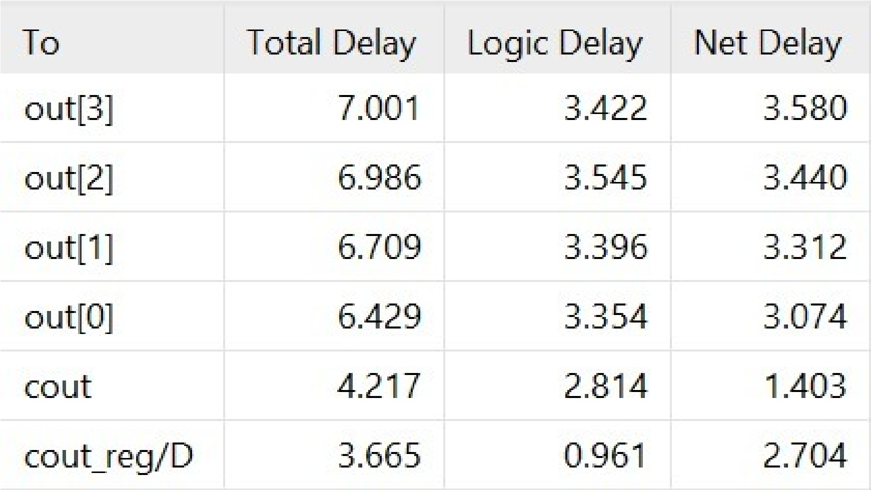
The speed of Alu with CLA is much faster than that of Alu without CLA as CLA predicts the carry for the next process and hence eliminates the time of waiting for the carry and hence speed ups the process.

The following is the time comparison between Alu with Cla and Alu without cla done using vivado



To	Total Delay	Logic Delay	Net Delay
cout_reg/D	0.529	0.101	0.428
cout	1.808	1.422	0.386
out[3]	2.073	1.395	0.678
out[2]	2.098	1.375	0.723
out[1]	2.117	1.370	0.747
out[0]	2.126	1.381	0.745

Time in nano seconds for each output for ALU with CLA



To	Total Delay	Logic Delay	Net Delay
out[3]	7.001	3.422	3.580
out[2]	6.986	3.545	3.440
out[1]	6.709	3.396	3.312
out[0]	6.429	3.354	3.074
cout	4.217	2.814	1.403
cout_reg/D	3.665	0.961	2.704

Time in nano seconds for each output for ALU without CLA

DISADVANTAGES:

Following are the disadvantages of using ALU With CLA

- Complexity:

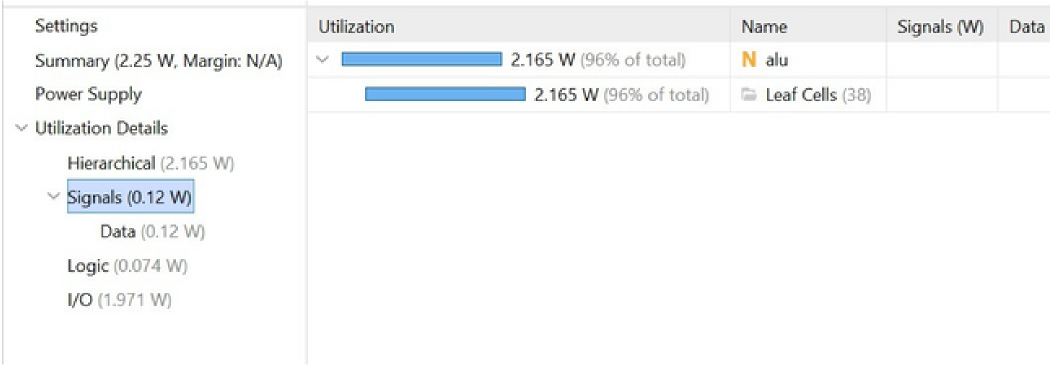
The complexity of the ALU with CLA is very high hence it is very difficult to implement.

- Power Consumption:

As additional gates are required for the implementation of CLA, The power consumption of ALU with CLA is higher than the power required for ALU without CLA.

One thing to be noted here is that the power consumption is lesser in case of CLA than in ripple carry adder or sparse adder

Following is the power consumption analysis performed on vivado on ALU with CLA.



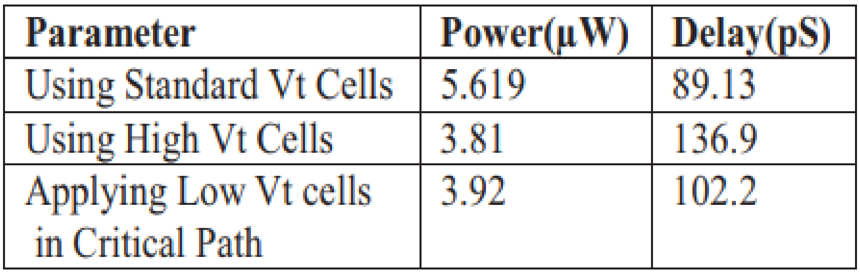
- Settings
- Summary (2.25 W, Margin: N/A)
- Power Supply
- Utilization Details
  - Hierarchical (2.165 W)
  - Signals (0.12 W)
    - Data (0.12 W)
  - Logic (0.074 W)
  - I/O (1.971 W)

Utilization	Name	Signals (W)	Data
2.165 W (96% of total)	alu		
2.165 W (96% of total)	Leaf Cells (38)		

NOTE: We performed the power analysis on ALU without CLA too and it came out to be **1.914 W**

FUTURE SCOPE:

In future in order to make the ALU using CLA more efficient we need to reduce the power losses. To reduce power we can use high Vt cells are used in the P-MOSFET’s of Logic gates, and to reduce delay standard Vt cells are used in logic gates of critical path.



Parameter	Power(µW)	Delay(pS)
Using Standard Vt Cells	5.619	89.13
Using High Vt Cells	3.81	136.9
Applying Low Vt cells in Critical Path	3.92	102.2

CONCLUSION

The main goal of our project is to reduce delay. The key element in the 4-bit ALU is the 4-bit Carry look ahead adder. to reduce delay standard Vt Cells are used in logic gates of critical path. This will reduce the delay in the circuit , which will make our circuit more efficient.

REFERENCES

Following are the references we used for performing our project work:

- https://www.researchgate.net/figure/Propagation-Delay-of-the-Full-Adder_fig4_220863085

- U. Sreenivasulu & T.Venkta Sridhar, Implementation of a four bit ALU using Low Power and Area efficient Carry select Adder, International Conference on Electronics and Communication Engineering, 20th May 2012, Bangalore.

- https://www.researchgate.net/publication/273163416_Implementation_of_an_Arithmetic_Logic_Using_Area_Efficient_Carry_Lookahead_Adder