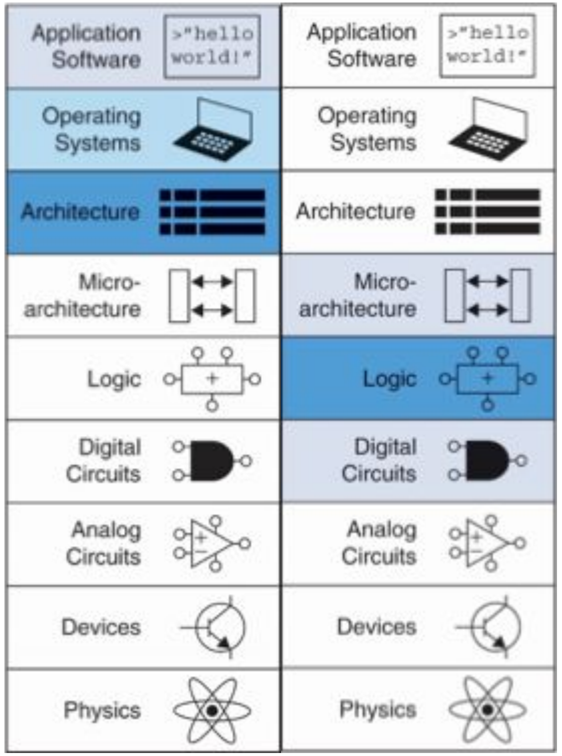
COSC175 (Systems I): Computer Organization & Design

Professor Lillian Pentecost
Fall 2024

Warm-Up October 1 (spooky!!)

- Where we were
  - FSMs, sequential logic
- Where we are going
  - Responding to feedback about workload
  - Our first computer processor!
  - Introducing remaining building blocks
  - Introducing the guts of the ALU (Arithmetic Logical Unit)
- Logistics, Reminders
  - TA help 7-9PM on Sundays, Tuesdays, Thursdays in C107
  - LP Office hours M 9-10:30AM, Th 2:30-4PM
  - Weekly Exercises Due Friday 5PM (CYOA)
  - Pre-Lab for tomorrow (DDCA Review 1.4.6, Read 5.2.2)
- Textbook Tags: 2.8, 5.2 (5.2.4), DiveIntoSystems 5.5



Responding to Feedback; Course Workload

- *Reducing* # of mandatory-to-hand-in weekly exercises
    - (all listed are still useful study tools, looking ahead to midterm exam)
- *Increasing Clarity* around time + effort expectations in upcoming labs
    - *& reducing length of labs, including expectations for testing as appropriate*
- A quick discussion around *debugging strategies*; work smarter, not longer
    - SystemVerilog "from scratch" is prone to many errors, even for experts; start from a provided example, and incorporate desired features and ideas <u>***incrementally***</u> so you can always pinpoint issues quickly; use testbenches crafted for each case you care about before deployment
    - If an exercise or idea is feeling unreasonable, take a step a away, scale back to a textbook example or simpler version first, and you will ultimately save yourself time

Our First Hardware Architecture

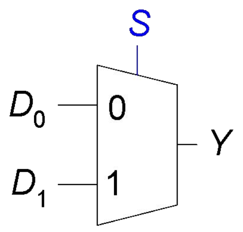
- 3 important blocks for now
    - **ALU** (Arithmetic Logical Unit, does the computation)
    - **Registers** (specific little chunks of memory, hold convenient and/or important bits)
    - **Memory** (one big blob of extra bits we can grab information from)
- We will also have a block for “control” → given an instruction, it gets the right data and sends it to the right place

Building Blocks: Multiplexer (Mux)

Selects between one of *N* inputs to connect to output

Select input is **log$_2$*N* bits** – control input

Example: 2:1 Mux

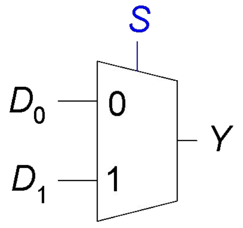


S	D_1	D_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

S	Y
0	D_0
1	D_1

2:1 Multiplexer Implementations

Desired Behavior



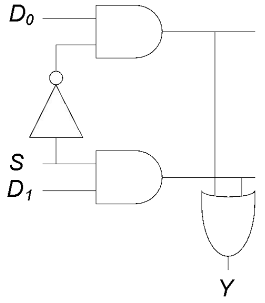
S	D_1	D_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

S	Y
0	D_0
1	D_1

Familiar, reasonable design: with Logic Gates

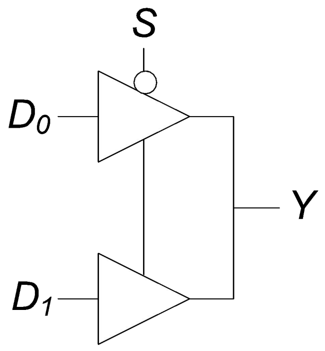
Y \ S \ D_0D_1	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$Y = D_0\overline{S} + D_1S$

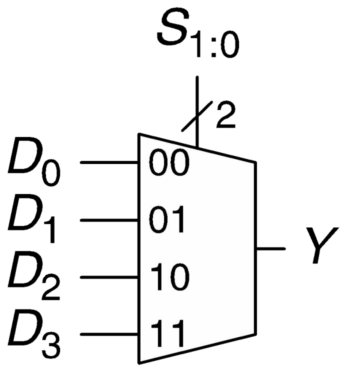


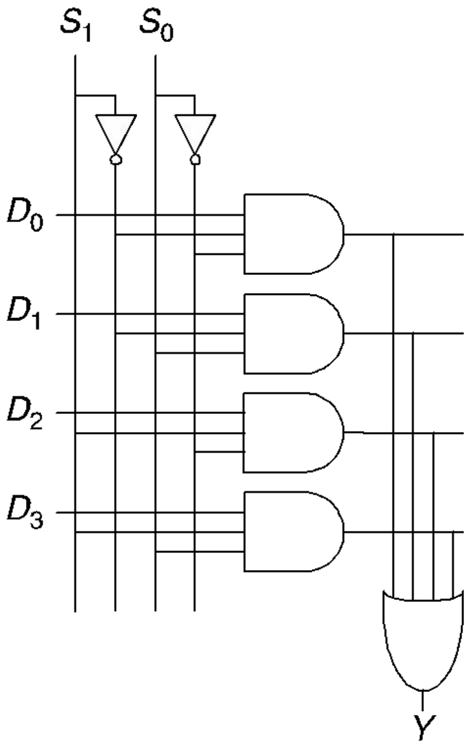
Simpler: with Tristates

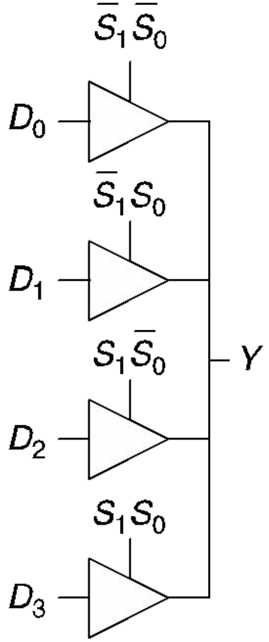
- Two tristates
- Turn on exactly one to select the appropriate input



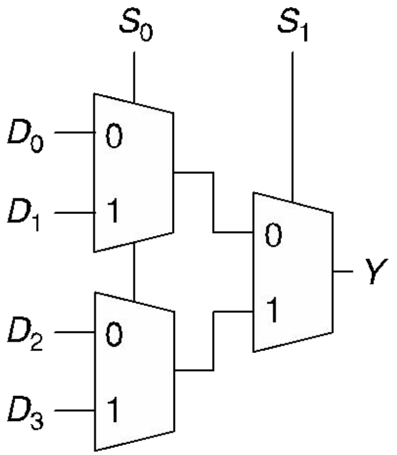
4:1 Multiplexer Implementations







Hierarchical

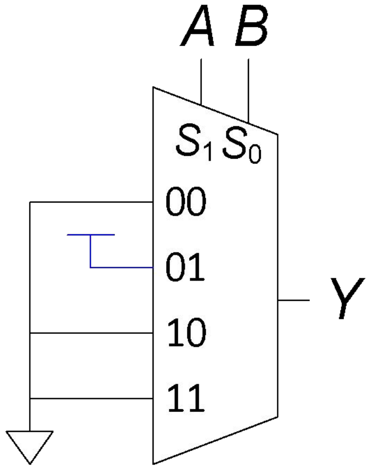


Logic using Multiplexers

Example:
“Hardcode” a MUX to produce desired output (Y) for given input combinations

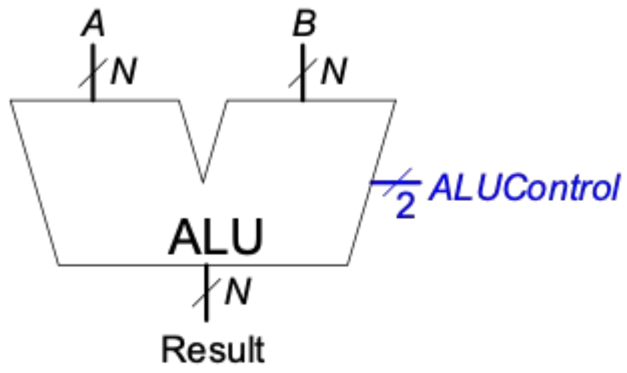
Essentially, a ***look-up-table*** encoding a boolean equation

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0



ALU: Arithmetic Logic Unit

$ALUControl_{1:0}$	**Function**
00	Add
01	Subtract
10	AND
11	OR



Example: Perform *A* OR *B*

$ALUControl_{1:0}$ = 11

Result* = *A* OR *B

ALU: Arithmetic Logic Unit

$ALUControl_{1:0}$	Function
00	Add
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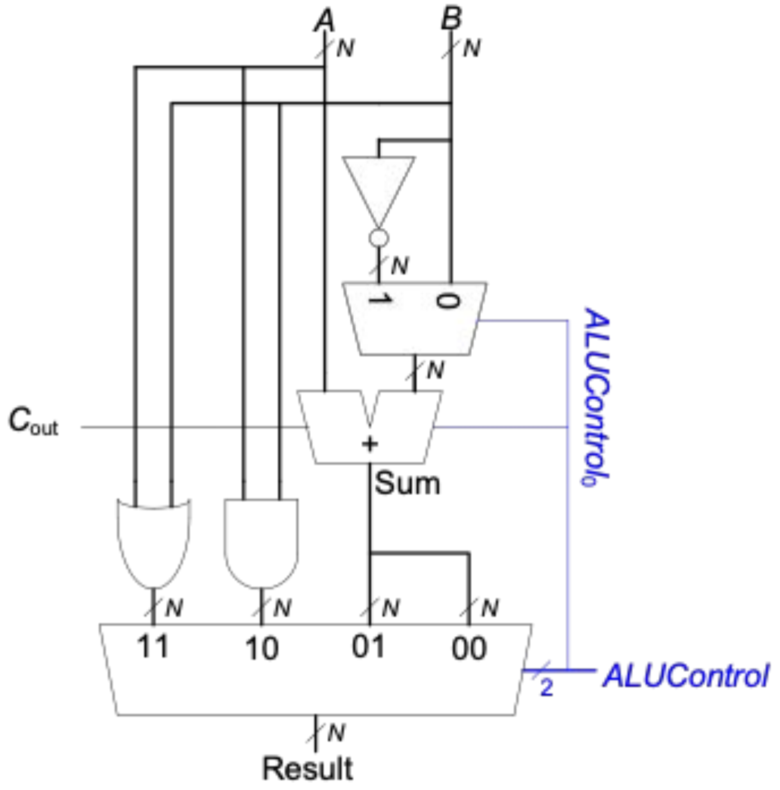
10	AND
11	OR

Example: Perform *A* OR *B*

$ALUControl_{1:0}$ = 11

Mux selects output of OR gate as *Result*, so:

Result* = *A* OR *B



ALU: Arithmetic Logic Unit

$\text{ALUControl}_{1:0}$	Function
00	Add
01	Subtract
10	AND
11	OR

Example: Perform *A* + *B*

$ALUControl_{1:0}$ = 00

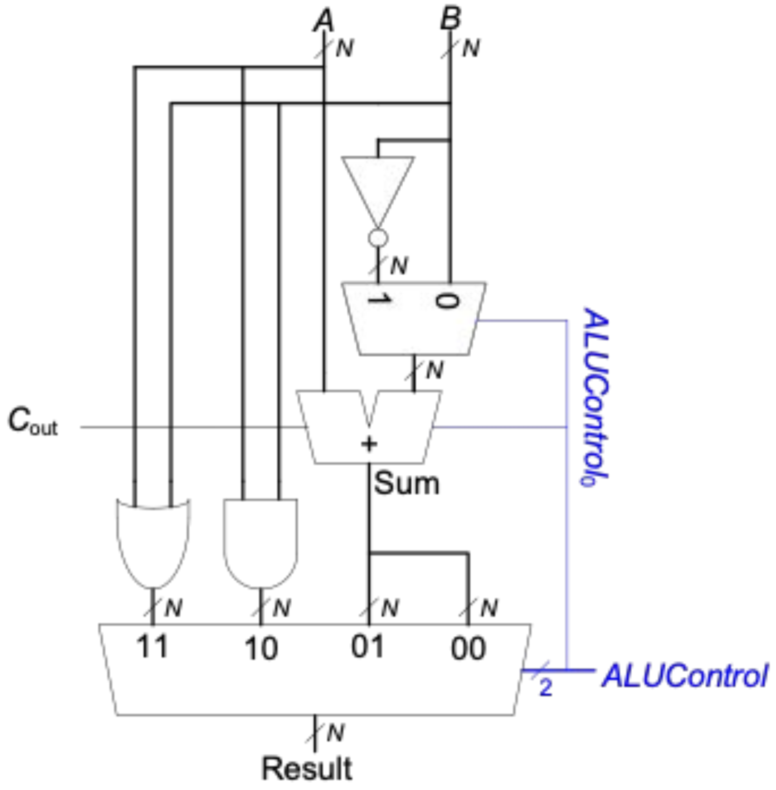
$ALUControl_0$ = 0, so:

C_{in} to adder = 0

2nd input to adder is *B*

Mux selects *Sum* as *Result*, so

Result* = *A* + *B



Wrap-Up October 1

SCAN ME

- Coming up next!
  - ***Building the components we need for general-purpose computing!***
- Logistics, Reminders
  - Evening help sessions 7-9PM on Sundays, Tuesdays, Thursdays in C107
  - Weekly Exercises Due Friday 5PM
  - **Stay up to date with readings!**
  - Lab 0, 1, Weekly Exercises 0 Feedback is posted via Moodle, reach out to **me** with questions
  - Pre-Lab for tomorrow (building an ALU, split over two weeks!)
- FEEDBACK
  - https://forms.gle/5Aafcm3iJthX78jx6