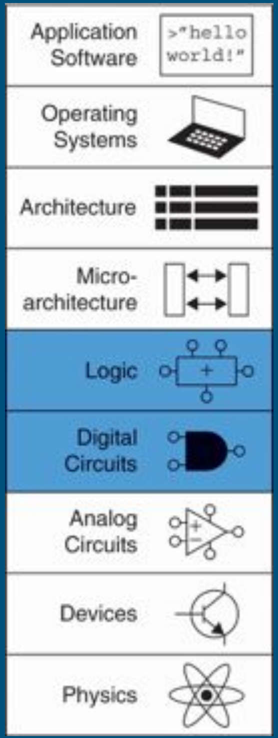
COSC175 (Systems I): Computer Organization & Design

Professor Lillian Pentecost
Fall 2024

Warm-Up September 10

- Where we were
  - Syllabus questions
  - More gates, boolean expressions
  - Introducing ***combinational logic***
  - Tools and techniques for constructing and simplifying our circuits
- Where we are going
  - Picking up with ***simplifying*** boolean equations and ***proving*** equality
  - Hardware Description Languages (HDLs) to preview tomorrow's lab!
- Logistics, Reminders
  - Evening help sessions 7-9PM on Sundays, Tuesdays, Thursdays in C107
  - Weekly Exercises Due Friday 5PM
  - Pre-Lab for tomorrow, Lab 1 meeting – time for hardware prototyping!!
  - **LAB SECTION 02: PLEASE PLEASE SWITCH LAB TIME IF YOU CAN**
    - **It'll be a better, cozier experience for you, and will improve my life and the TAs' lives**
- Textbook Tags: 2.3, 4.1



Syllabus Annotation – Closing the loop!

- I'm looking for ***your*** thoughts and questions on our syllabus
- I answered your questions at THIS GOOGLE DOC

- Some common themes in the doc and discussions are:
    a. What's up with the random partners?
    b. What does collaboration mean or look like?
    c. How to use the textbook?

Simplification!!

- There are ***axioms*** and ***theorems*** of Boolean Algebra that you can apply to your equations to simplify them
- The ***Dual*** simply replaces * with + and 0 with 1!

Number	Axiom	Dual	Name
A1	B = 0 if B ≠ 1	B = 1 if B ≠ 0	Binary Field
A2	$\overline{0}$ = 1	$\overline{1}$ = 0	NOT
A3	0 • 0 = 0	1 + 1 = 1	AND/OR
A4	1 • 1 = 1	0 + 0 = 0	AND/OR
A5	0 • 1 = 1 • 0 = 0	1 + 0 = 0 + 1 = 1	AND/OR

Simplification!!

- Boolean Theorems of one Variable:

Number	Theorem	Dual	Name
T1	$B \bullet 1 = B$	$B + 0 = B$	Identity
T2	$B \bullet 0 = 0$	$B + 1 = 1$	Null Element
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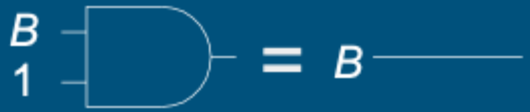

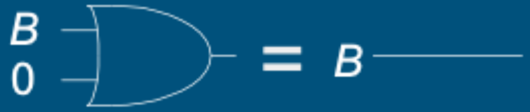

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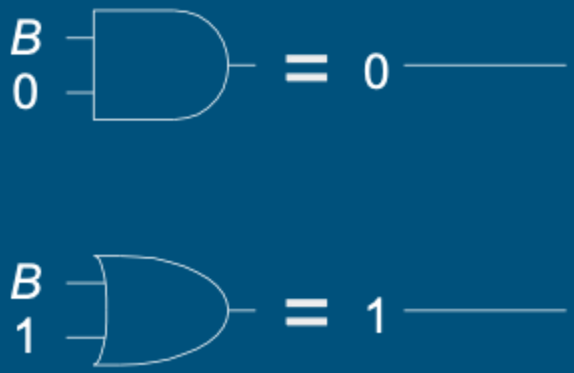

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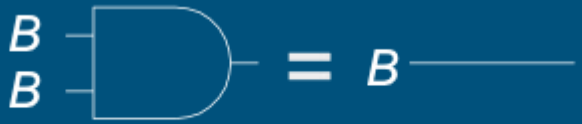

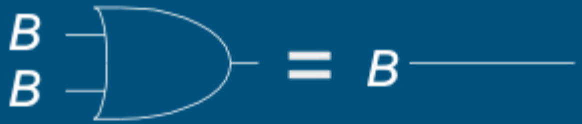

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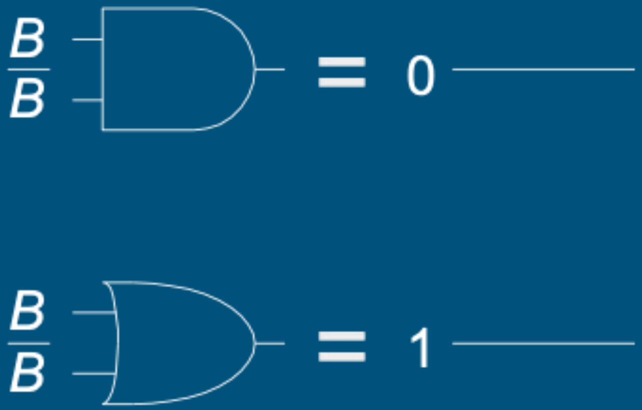

How do we ***prove a theorem***?

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- **Method 1: Perfect Induction**
  - I.e., exhaustively list every input value; if two expressions produce the same output for every possible input, they are equivalent
  - I.e., use a truth table
- **Method 2: Use other theorems and axioms to make two sides of an equation look like one another**
  - Iterative simplification, reformulation

Boolean Theorems of Multiple Variables

#	Theorem	Dual	Name
T6	B•C = C•B	B+C = C+B	Commutativity
T7	(B•C) • D = B • (C•D)	(B + C) + D = B + (C + D)	Associativity
T8	B • (C + D) = (B•C) + (B•D)	B + (C•D) = (B+C) (B+D)	Distributivity
T9	B • (B+C) = B	B + (B•C) = B	Covering
T10	(B•C) + (B•C) = B	(B+C) • (B+C) = B	Combining
T11	(B•C) + (B•D) + (C•D) = (B•C) + (B•D)	(B+C) • (B+D) • (C+D) = (B+C) • (B+D)	Consensus

Warning: T8' differs from traditional algebra:
OR (+) distributes over AND (•)

Prove a Theorem: Example

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T7	$(B \bullet C) \bullet D = B \bullet (C \bullet D)$	$(B + C) + D = B + (C + D)$	Associativity
T8	$B \bullet (C + D) = (B \bullet C) + (B \bullet D)$	$B + (C \bullet D) = (B+C)\ (B+D)$	Distributivity
T9	$B \bullet (B+C) = B$	$B + (B \bullet C) = B$	Covering
T10	$(B \bullet C) + (B \bullet \overline{C}) = B$	$(B+C) \bullet (B+\overline{C}) = B$	Combining
T11	$(B \bullet C) + (\overline{B} \bullet D) + (C \bullet D) =$ $(B \bullet C) + (\overline{B} \bullet D)$	$(B+C) \bullet (\overline{B}+D) \bullet (C+D) =$ $(B+C) \bullet (\overline{B}+D)$	Consensus
T12	$\overline{B \bullet C \bullet D \ldots} = \overline{B}+\overline{C}+\overline{D} \ldots$	$\overline{B+C+D \ldots} = \overline{B} \bullet \overline{C} \bullet \overline{D} \ldots$	De Morgan's

Combining

Method 1: show with a truth table

Method 2: Use other axioms & theorems

Prove a Theorem: Example

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Combining

$B \bullet C + B \bullet \overline{C}$	$= B \bullet (C+\overline{C})$	T8: Distributivity
	$= B \bullet (1)$	T5': Complements
	$= B$	T1: Identity

One more theorem! An extra useful one

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De Morgan's Theorem: *The* ***complement*** *of the* ***product*** *is the* ***sum*** *of the* ***complements****.*

Dual:

The ***complement*** *of the* ***sum*** *is the* ***product*** *of the* ***complements****.*

Method 1: show with a truth table

Draw the gates, and know the appropriate substitutions!

If it helps to remember:
"Break the line, change the sign"

Check-In Activity ***in pairs, on notecard***:

A. Prove T9 (***covering***) theorem using each method (TT, other theorems)

B. Simplify the following expressions into ***two or fewer terms***, each with ***two or fewer literals***, then check your work with a truth table:

a. $Y = AC + BC + ABC$

b. $Y = \bar{A}\bar{B} + \bar{A}B\bar{C} + \overline{(A + \bar{C})}$

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Hardware Description Languages (HDLs)

- To deploy & test our hardware designs in this course, we will learn some **SystemVerilog**, a prominent and industry-preferred HDL
- We will use SystemVerilog to describe HW that we can then ***simulate***, or even ***synthesize*** into a deployable + testable circuit diagram
- There is one ***IMPORTANT thing to remember*** before we start this journey:
  - When writing SystemVerilog, you should be thinking about the **hardware** the HDL should produce, then write the appropriate description or procedure that implies that hardware.
  - **Beware** of treating HDL like software – you cannot write SystemVerilog like you write code, and you cannot write it without thinking of the hardware.

Example Module


```
module example(input  logic a, b, c,
               output logic y);
  // module body goes here
  assign y = ~a & ~b & ~c | a & ~b & ~c | a & ~b &  c;
endmodule
```

- **module/endmodule**: required to begin/end module
- **example**: name of the module
- Operators:
  - ~: NOT
  - &: AND
  - |: OR
- SystemVerilog is **case sensitive:** “reset” and “Reset” are not the same signal.
- No names that start with numbers (e.g., “3and” is an invalid name)
- Whitespace is ignored, *// for single line comment* **/* for multiline comment */**

Wrap-Up September 10

- Coming up next!
  - Bigger, better, multi-component designs → **doing actual computation**
- Logistics, Reminders
  - *Weekly Exercises* due Friday
  - Complete Pre-Lab (Read DDCA 4.1 + setting up GitLab) before tomorrow
  - Weekly reading, Lab 1 released later today
  - **LAB SECTION 02: PLEASE PLEASE SWITCH IF YOU CAN**
    - **It'll be a better, cozier experience for you, and will improve my life and the TAs' lives**
- FEEDBACK
  - https://forms.gle/5Aafcm3iJthX78jx6

SCAN ME