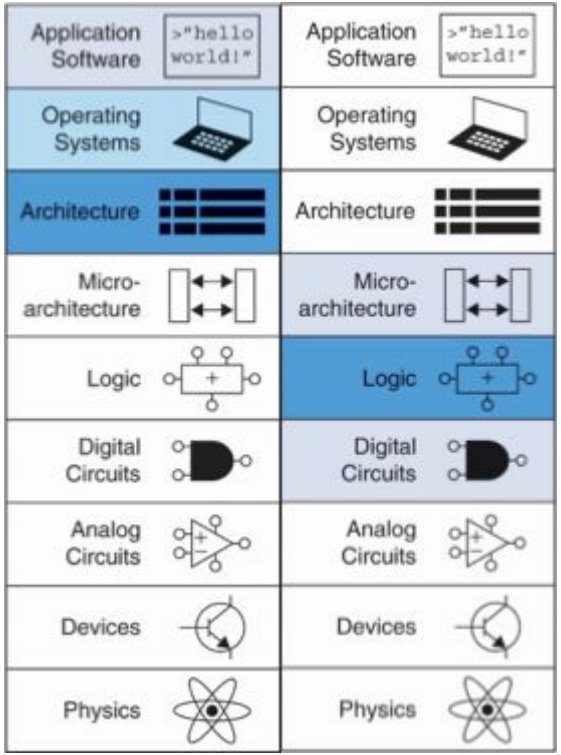
COSC175 (Systems I): Computer Organization & Design

Professor Lillian Pentecost
Fall 2024

Warm-Up October 3

- Where we were
  - Introducing our first higher-level processor picture
  - More building blocks! MUXes and ALUs
- Where we are going
  - Activities based on observed questions + requests
- Logistics, Reminders
  - TA help 7-9PM on Sundays, Tuesdays, Thursdays in C107
  - LP Office hours M 9-10:30AM, Th 2:30-4PM
  - Weekly Exercises Due Friday 5PM (CYOA)
  - ***<u>Midterm Exam Announcement: Tuesday EVENING on October 22</u>***
    - ***<u>Pruyne Lecture hall, 2 hr exam, in the range of 6-9:30PM</u>***
    - ***<u>Open notes/textbook, more details to be provided next week</u>***
    - ***<u>NO lecture on October 22, no pre-lab for October 23</u>***
- Textbook Tags: 2.8, 5.2 (5.2.4), DiveIntoSystems 5.5

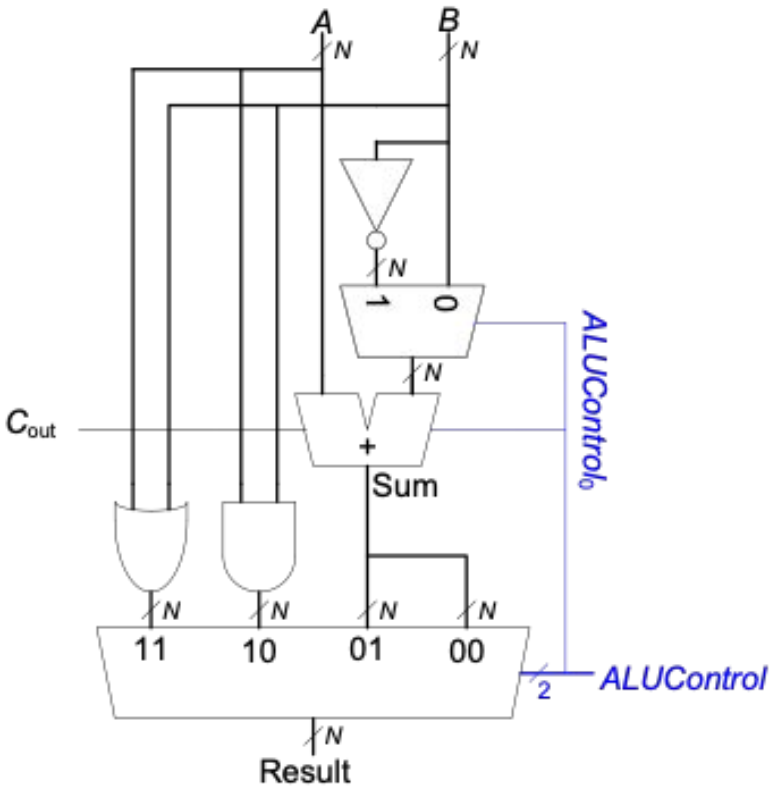


Check-In Activity: based on lab + feedback questions!

- Start by assigning **group roles!**
  - ***Ambassador, Recorder, Sketcher, and Executive***
- Parts ***do not need to be completed in order*** – decide as a group which part sounds more interesting and useful to start with!
- Hand in recorder's notes at the end of class (either on paper or via email)

ALU: Arithmetic Logic Unit

$ALUControl_{1:0}$	Function
00	Add
01	Subtract
10	AND
11	OR



Example: Perform *A* + *B*

$ALUControl_{1:0}$ = 00

$ALUControl_0$ = 0, so:

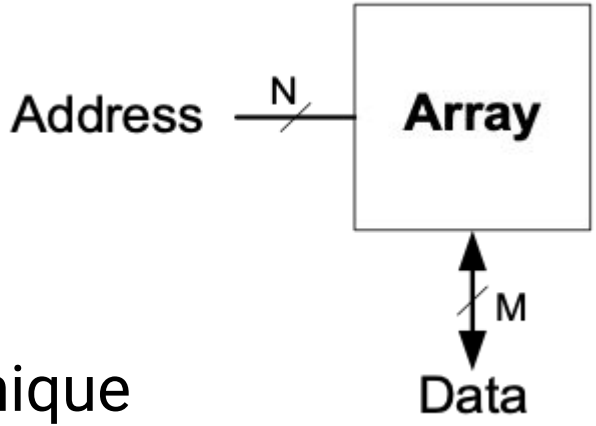
C_{in} to adder = 0

2nd input to adder is *B*

Mux selects *Sum* as *Result*, so

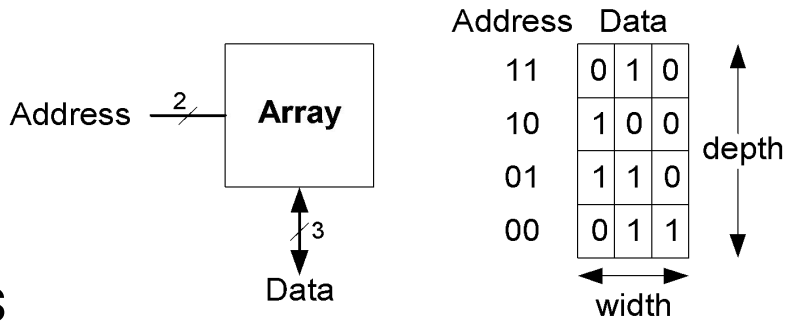
Result* = *A* + *B

Memory Arrays



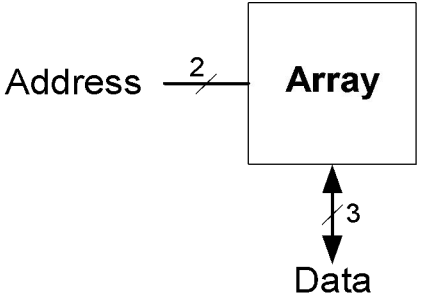
- Efficiently store large amounts of data
- *M*-bit data value read/written at each unique *N*-bit address
- 3 common types:
  - Dynamic random access memory (DRAM)
  - Static random access memory (SRAM)
  - Read only memory (ROM)

Memory Arrays



- 2-dimensional array of bit cells
- Each bit cell stores one bit
- *N* address bits and *M* data bits:
  - 2^N rows and *M* columns
  - **Depth:** number of rows (number of words)
  - **Width:** number of columns (size of word)
  - **Array size:** depth × width = $2^N \times M$

Memory Array Example



Address	Data		
11	0	1	0
10	1	0	0
01	1	1	0
00	0	1	1

depth

width

- **2^2 × 3-bit** array
- **Number of words:** 4
- **Word size:** 3-bits
- For example, the 3-bit word stored at address 10 is 100

Wrap-Up October 3

- Coming up next!
  - Memory Arrays (one of our last building blocks!)
- Logistics, Reminders
  - Evening help sessions 7-9PM on Sundays, Tuesdays, Thursdays in C107
  - Weekly Exercises Due Friday 5PM
  - Lab 0, 1, Weekly Exercises 0 Feedback is posted via Moodle, reach out to **me** with questions
  - Lab 4 Report (First & Second Stage) due October 17
    - Complete First stage, Part 2 diagram as pre-lab for next Wednesday
    - Spend time now to get comfortable with testing!!
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- FEEDBACK
  - https://forms.gle/5Aafcm3iJthX78jx6

SCAN ME