Carleton University

Department of Systems and Computer Engineering

SYSC 3006 (Computer Organization) Fall 2020

Lab / Assignment 1 – Answering file

Student Name: Youssef Ibrahim

Question 1 [0.3-mark]

What is the minimum ROM Address Bit Width needed to implement Table 1, and why?
Answer in this space:

The minimum ROM Address Bit Width needed to implement Table 1 is 3-bits. Since $2^m \geq$ number of states (8), m is the minimum Address Bit Width (3), $2^3 = 8$.

Question 2 [0.3-mark]

What is the minimum ROM Data Bit Width needed to implement Table 1, and why?
Answer in this space:

The minimum ROM Data Bit Width needed to implement Table 1 is 6-bits. Since to store the outputs we need 3 bits, and to store the next state we need another 3 bits, (3+3=6).

Question 3 [0.6-mark]

Fill in the following table; it is the content of your FSM ROM that you are going to implement.

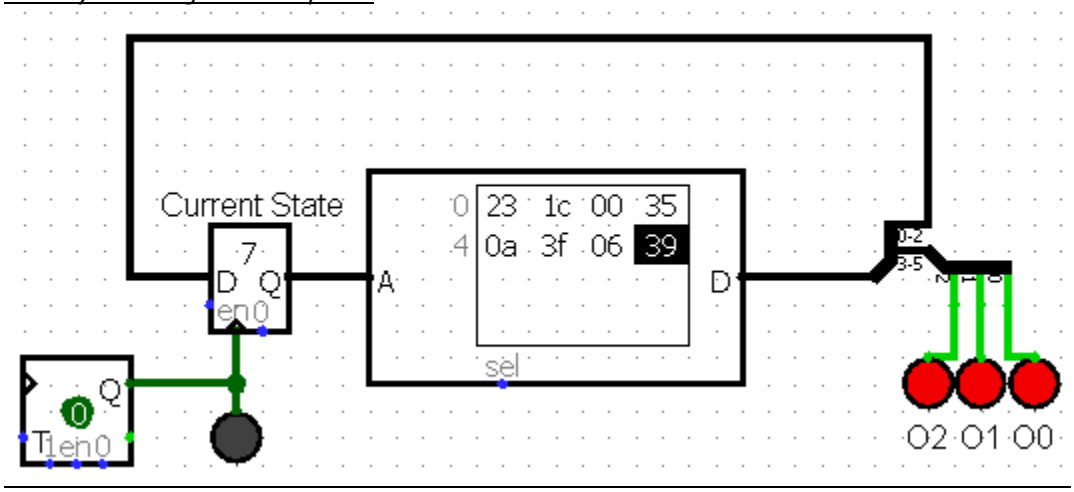
Address	DATA content (binary)	DATA content (Hex)
0b000 (0)	100011	23
0b001 (1)	011100	1C
0b010 (2)	000000	00
0b011 (3)	110101	35
0b100 (4)	001010	0A
0b101 (5)	111111	3F
0b110 (6)	000110	06
0b111 (7)	111001	39

Table 2 - Lab1 ROM content

Question 4

4.1 [0.3-mark] Show here a screenshot of your final Logisim circuit for your implementation.

Insert your image in this space:

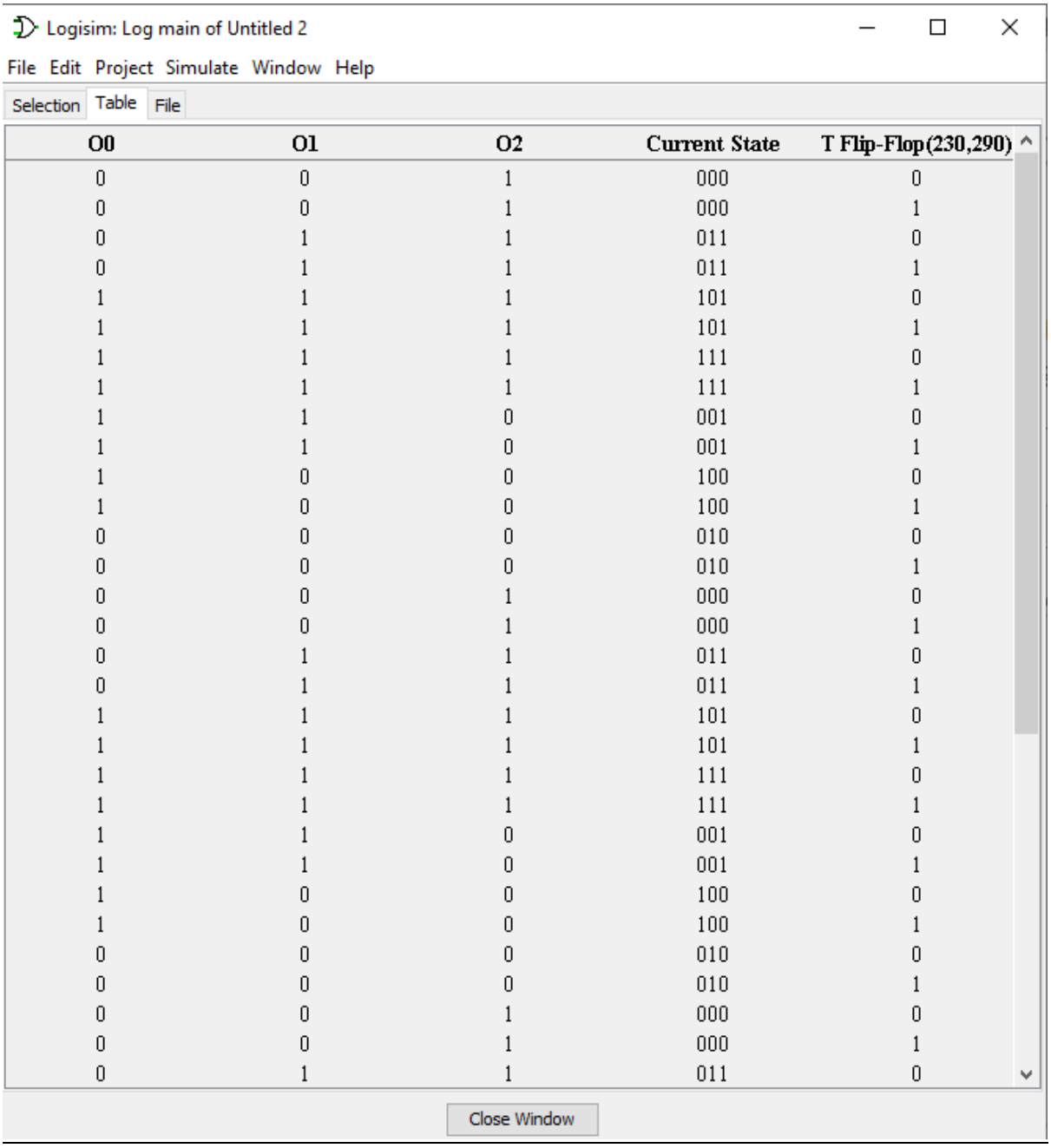


4.2 [0.3-mark] A short description of how the component attributes have been configured to meet the lab requirements.

Answer here:

- A ROM was configured to have an Address Bit Width = 3 to cover the minimum number of states (8), and Data Bit Width = 6-bits Since to store the outputs we need 3 bits, and to store the next state we need another 3 bits.
- A Register (Current State) was configured to have 3-bits since for the Register to be connected successfully to the ROM we must make sure that the Data Bits from the Register equals to the Address Bit Width of the ROM.
- 2 splitters were used, the first splitter input was connected to the output of the ROM and was configured for Fan Out = 2 and Bit Width In = 6, branch 0-2 of the splitter was connected to the input of the Register while the 3-5 branch was connected the second splitter. The second splitter was configured to have a Fan Out = 3 and Bit Width In = 3, Each branch of the second splitter was connected to different LED (O2 & 01 & 00).

4.3 [1.2-mark] Including this document, submit your Logisim lab1 file circuit (.circ) in a zip folder. Also insert below a screenshot of your Log table (0.5-mark for the Log table and 1.5-mark for a circuit working properly and respecting the design specifications described in this statement).
Insert your image in this space:



O0	O1	O2	Current State	T Flip-Flop(230,290)
0	0	1	000	0
0	0	1	000	1
0	1	1	011	0
0	1	1	011	1
1	1	1	101	0
1	1	1	101	1
1	1	1	111	0
1	1	1	111	1
1	1	0	001	0
1	1	0	001	1
1	0	0	100	0
1	0	0	100	1
0	0	0	010	0
0	0	0	010	1
0	0	1	000	0
0	0	1	000	1
0	1	1	011	0
0	1	1	011	1
1	1	1	101	0
1	1	1	101	1
1	1	1	111	0
1	1	1	111	1
1	1	0	001	0
1	1	0	001	1
1	0	0	100	0
1	0	0	100	1
0	0	0	010	0
0	0	0	010	1
0	0	1	000	0
0	0	1	000	1
0	1	1	011	0

Now save this document as PDF and do not forget to include your .circ file with your submission!

Submission deadline

Must be submitter on cuLearn, locate (Assignment 1 submission) and follow instructions, submission exact deadline (date and time) is displayed clearly with the Assignment 1 submission on cuLearn.

Note: If you have any question please ask them during your TA online live session. Do not wait till the deadline to ask questions as there in no warranty you will get answered before the deadline.

Good Luck