EE5003 Project Report

Device Modeling of Oxide Semiconductor Based Thin Film Transistors (TFTs)

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ABSTRACT

Extremely scaled amorphous InGaZnO thin film transistors (a-IGZO TFTs) can meet the increasing demand of high-density and low-power in emerging memory design. Traditional multiple trapping and release (MTR) carrier transport and effective mobility model with arbitrary energy distribution of traps in a-IGZO TFTs compact model are done for long channel a-IGZO TFTs, however, leading to error for scaled devices. To address this, a carrier transport physics-based compact model is proposed accounting for the effect of scaling on the device and material properties. Particularly, it is achieved with corrected hopping and percolation models derived using saturation transition function introduced by MIT virtual source model. Effective mobility, contact resistance and defects determine the performance for sub-micron and deep sub-micron scaled a-IGZO device. Final projections of transfer characteristics, output characteristic and transconductance are in excellent agreement with experiments, when considering extreme-scaling induced severe short channel and contact effect, such as drain-induced barrier lowing (DIBL) and effective mobility degradation due to source and drain series resistance. According to our compact model, a group of short-channel a-IGZO TFTs can be packaged into manager library in Cadence Virtuoso using Verilog-A language, contributing to future flexible logic circuit design. It also indicates a great potential for a-IGZO-based 3D logic-in-memory system that can broaden Moore's law.

Key Words: a-IGZO TFTs; multiple trapping and release (MTR); contact effect; drain-induced barrier lowing (DIBL); effective mobility degradation; 3D logic-in-memory system

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CHAPTER 1 INTRODUCTION

1.1 Research Background

As approaching the end of Moore’s law, the transistor gate length has scaled to less than 20 nm. More Moore's and More than Moore's has become the top priority of scientists' research. 3D nano-scaled integrated systems based on stacked layer structure is obviously a potential solution. By developing semiconductors with high electron mobility channel material system and good integration compatibility as the interlayer, monolithic 3D integration of the system can be realized eventually to integrate emerging memory, logic devices, RF devices, sensors, etc., connected together to achieve system-level chip performance.

Faster operation speed is required to enhance transistors performance. Extensive research efforts have been made to use high mobility channel materials to further push the device performance for future high performance and low power logic applications as well as ultra-high frequency RF applications. Lower power consumption means emerging memories are also required to develop. To achieve this goal, researchers have made major efforts to develop solid-state devices, including non-volatile memory resistors, to simulate biological synaptic behavior. The rapid development of intelligent tasks such as artificial intelligence, big data analysis, autonomous driving, voice and image recognition has put forward higher requirements for computing speed and energy consumption.

Higher device density is based on the novel system integration platform. Nowadays, pathways for extending Moore's law beyond device dimension downscaling are highly desired, e.g. three dimensional integration techniques. However, as the most widely used monolithic integration compatible channel materials, hydrogenated amorphous silicon (a-Si:H) and low-temperature polysilicon (LTPS) cannot meet the increasing demand on device performance due to poor mobility or large device to device variation. Benefiting from their amorphous nature and bonding structure,

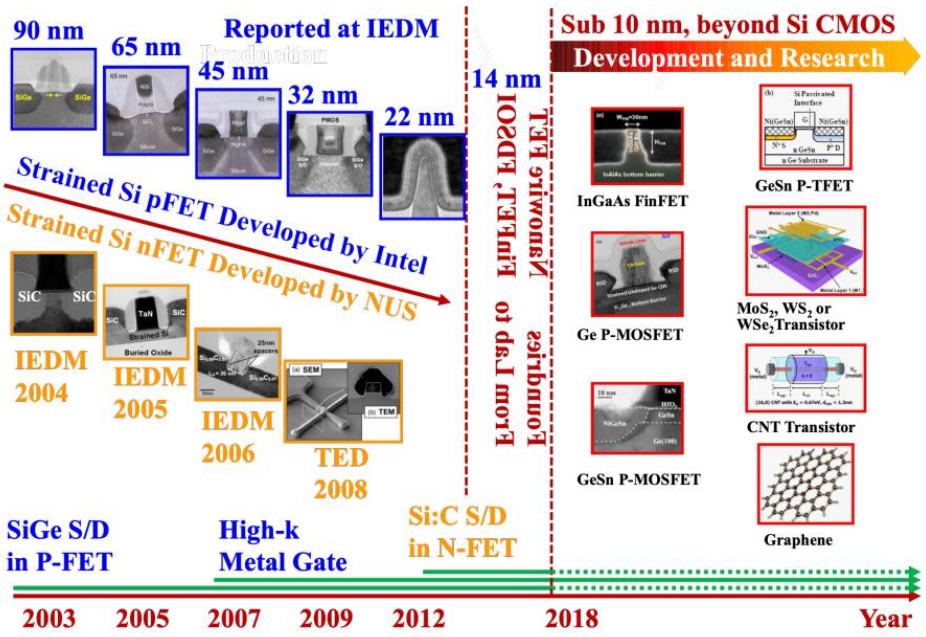

Fig. 1.1.1 Development of Moore's law and novel nano-scale devices.

amorphous oxide semiconductors have advantages including low process temperature, moderate mobility, and decent large size uniformity, showing a great potential to be a key enabler in future monolithic three dimension (3D) integrated nanoelectronic and photonic systems. In addition, with excellent flexibility and high transparancy, amorphous oxide semiconductors, e.g. Indium-Gallium-Zinc-Oxide and Zinc-Oxide, have been widely used in applications ranging from large size flat panel displays to flexible portable devices.

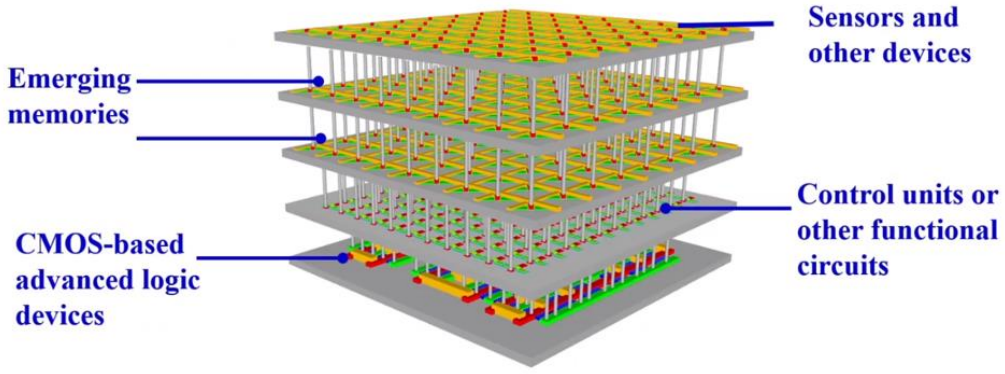

Fig. 1.1.2 3D stacked transistors structure for sensing-memorizing-computing integration.

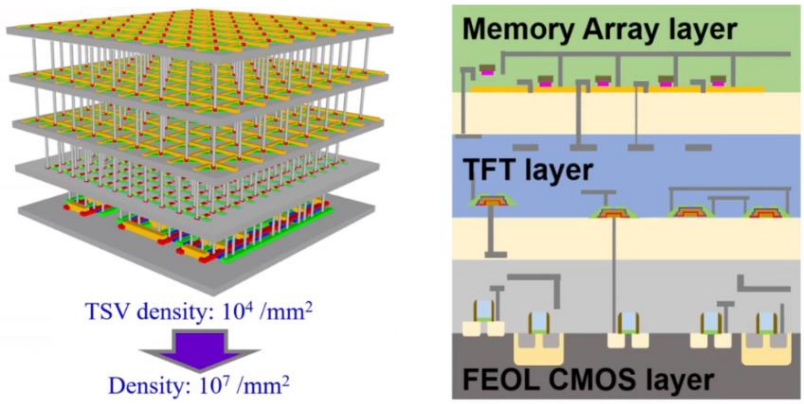

Fig. 1.1.3 IGZO TFTs show great integration density for logic-in-memory structure.

The reasons why IGZO TFTs have great potential to the future 3D monolithic integration are demonstrated following.

First of all, amorphous oxide semiconductors can be deposited directly on the amorphous layer such as SiO_2 and SiN which are widely used in BEOL with large scale and cost effectiveness.

Besides, mobilities are in the range of 10 to 100 cm2/V.s, much higher than that of a-Si (~1cm2/V.s). Simultaneously, the off-state current of IGZO TFTs is even smaller than both a-Si and polysilicon TFTs.

Additionally, the temperature for both materials deposition and device fabrication can be less than 450. Layer by layer deposition and device fabrication can be realized.

Eventually, it can flexible number of layers and have the pretty low cost.

1.2 Project Objective

The purpose of this project is to build a suitable compact model that can fit with the experimental data with reasonable device parameters, which means this model holds on the similar important parameters compared with the device fabricated in cleanroom, such as threshold voltage, subthreshold swing, DIBL coefficient, effective carrier mobility, etc. Simultaneously, this model can also reflect some electrical characteristic corresponding to the carrier transport behavior of fabricated device.

The potential research direction of this project is to build the SPICE model and

package into the manager library in Cadence Virtuoso, so that can contribute to NMOS logic circuit design or analog circuit simulation using amplifiers. Then further research will aim at the compact model of sub-100nm channel length IGZO TFTs, which has great potential to 3D monolithic integration for stacked transistor technology and logic-in-memory circuit.

1.3 Main Work

In this project, first of all, I reviewed device physics of ultra-scaled thin film transistors and then spent much time learning basic knowledge of amorphous metal oxide semiconductor material theory and relating carrier transport for thin film transistors with amorphous material channel by doing literature review.

Then I learned the methodology of device modeling and explore how to build a compact model for the IGZO-based transistors gradually, which considers the different carrier transport in the channel, short channel effect and the effect of source and drain series resistance. In addition, on thing that is pretty significant is to find the proper mathematical processing or create the transition function to unify the splitting analytical model separated by the different operation mode of the transistor. For example, to find the new way that can combine the subthreshold model and above threshold model to a unified one, as well as make the model illustrating transistors operating at linear region and saturation region, respectively, become a completely new one by building the proper transition function.

By using suitable iteration and fitting algorithm, the simulated results based on the analytical model can be able to fit with the experimental data with reasonable device parameters.

CHAPTER 2 FUNDAMENTALS

2.1 Amorphous Semiconductor Material Theory

2.1.1 Wavefunction of Electron in Disordered System

Amorphous material means that the atoms in the material no longer have obvious periodic arrangement, while show the properties of both short-range order and long-range disorder. Short-range order means that around an atom, the arrangement of several atoms bonded to it still exhibits structural characteristics, which is similar to crystalline materials. Long-range disorder means that from the macroscopic point of view of the whole material, the arrangement of atoms is disordered, and the distribution of chemical bonds appears as a random network.

In the field of thin film transistors, two commonly used amorphous materials are amorphous silicon (a-Si) thin film materials and amorphous InGaZnO (a-IGZO) thin film materials. Amorphous silicon is a kind of covalent compound in which each silicon atom forms a covalent bond with an adjacent silicon atom. However, IGZO is an ionic compound material obtained by simultaneously doping two elements, In and Ga, into ZnO thin film.

In 1958, physicist P. W. Anderson published his famous results in the field of amorphous semiconductors. Fig. 2.1.1 shows the one-dimensional amorphous potential field and the distribution model of the electronic energy state used by Anderson when feasting on the electronic energy state in the amorphous solid.

As can be seen from Fig. 2.1.1, the model assumes that the arrangement of lattice atoms is still periodic, but the potential field around the atoms has a certain distribution on the basis of a certain average value, and the distribution width is V_0. Under this action, the intrinsic state wave function of the electron obtained by solving the Schrödinger equation will no longer be a Bloch function (wavefunction that satisfies Bloch's theorem), but there are two intrinsic states wavefunction, which are called extended states wavefunction and localized states wavefunction.

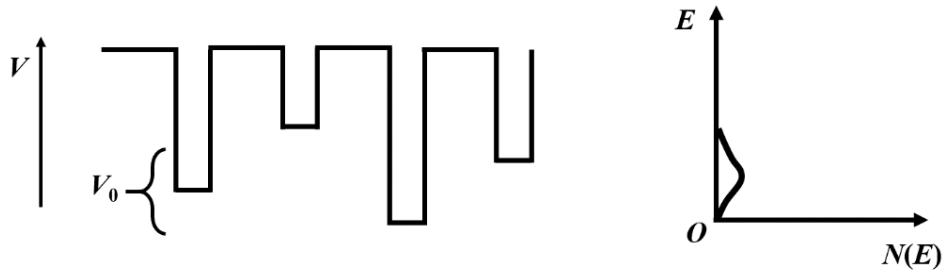

Fig. 2.1.1 Distribution model of 1D amorphous potential field and electron states.

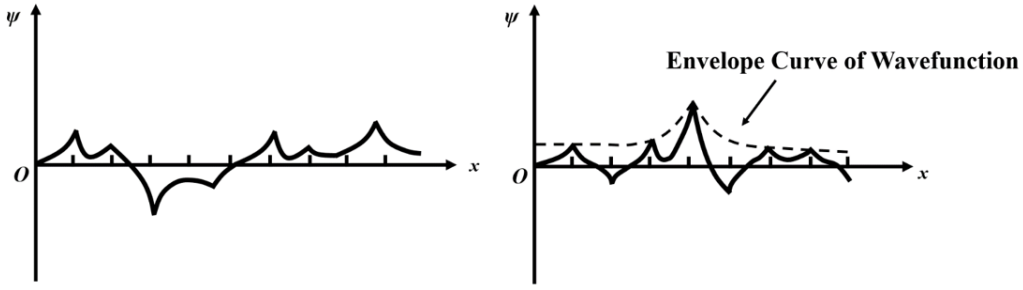

Fig. 2.1.2 Wavefunction of electrons in amorphous solid states.

2.1.2 Mobility Edge

After Anderson proposed the local state theory, N. F. Mott developed the concept of mobility edge on this basis. Mott believes that the electrons in the amorphous solid are not all localized at the same time, but the localization of the electron energy lift first occurs in the energy region of the shadow as shown in Fig. 2.1.3. The localized electronic energy states are called tailed states. The energy state between E_C and $E_{C'}$ is called the extended state. As the degree of amorphization of the material increases, the energy separation between E_C and $E_{C'}$ gradually decreases. If the degree of amorphization of the material is so high that the electronic energy states in it are all localized, E_C and $E_{C'}$ coincide. In these two split amorphous materials, the energy boundary between the extended state and the tailed state is called the mobility edge. The mobility edge is a fundamental concept in the physics of amorphous semiconductors.

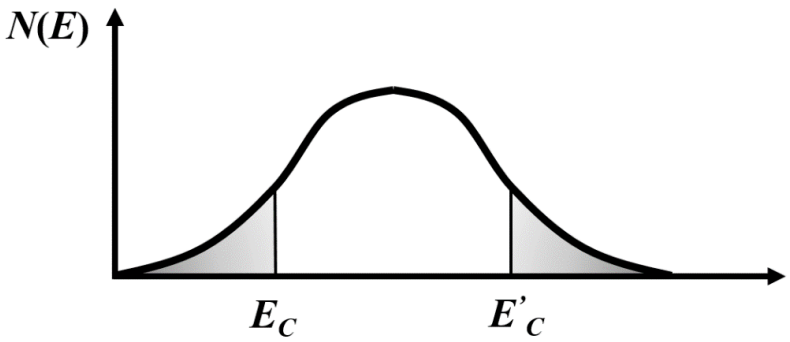

Fig. 2.1.3 Electron states in amorphous material.

2.1.3 Energy Band Structure and Theory

The earliest proposed band structure of amorphous semiconductor materials is shown in Fig .2.1.4, which is called CFO model. This model assumes that the band structures of amorphous and crystalline semiconductor materials are similar. Both two types of material have conduction band, valence band, and forbidden band between them. However, the difference is that in amorphous materials, due to the amorphization of the structure, the energy state of electrons appears in the bandgap, which is called tail states. CFO model believes that the tail states at the bottom of the conduction band are electron acceptor states, while the tail states at the top of the valence band are electron donor states or hole acceptor states.

CFO model also considers that the tail states at the bottom of the conduction band and the top of the valence band overlap each other at the center of the bandgap. The Fermi level is pinned in this overlapping region. According to this model, when a kind of material is irradiated with photons of energy less than its bandgap, the photons are absorbed. The reason is that when the energy of the photon is equivalent to that of an electron in the defect state, the energy of the photon is absorbed by the electron, and the electron undergoes a transition after absorbing the energy. But experiments have found that many amorphous materials are transparent to infrared even visible light. This shows that the defect states in the bandgap of amorphous semiconductor materials do not spread over the entire band gap energy range as thought in the CFO model. Based on this, some researchers propose a model as shown in Fig. 2.1.4. The basic structure

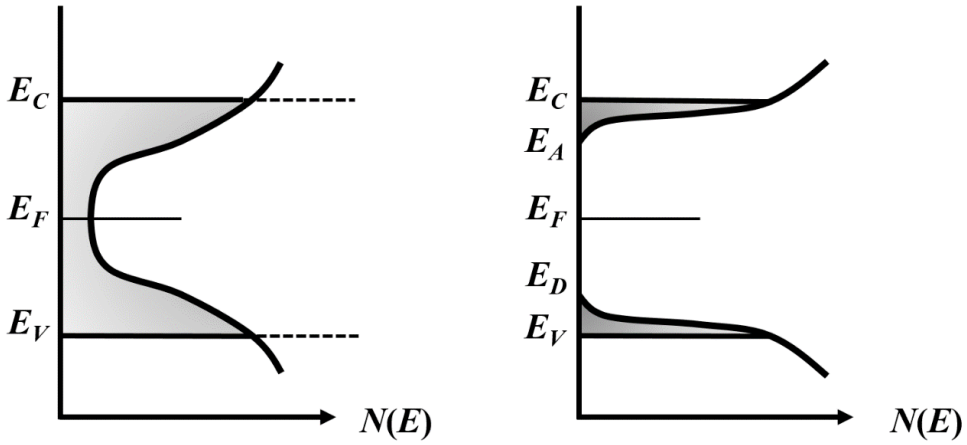

Fig. 2.1.4 CFO model and CFO-like model.

of this model is similar to the CFO model, except that the tail states of electrons in the forbidden band only exist in part of the energy range of the bottom of the conduction band and the top of the valence band, distributed from E_A to E_C at the bottom of the conduction band and E_V at the top of the valence band to E_B energy range. Obviously, this model believes that the defect states in amorphous materials all originate from the band tails caused by the amorphization of the material structure, and the Fermi level is pinned at the center of the bandgap. This also deviates from the distribution of defect states in real amorphous materials.

At present, the general understanding of the band structure of amorphous materials is the model shown in Fig .2.1.5. The model believes that in amorphous semiconductor materials, in addition to structural amorphization, there are other structural defects. These structural defects also introduce electronic energy states in the forbidden band. The difference is that the level tails introduced by these structural defects are deep levels. These deep levels are closer to the center of the forbidden band relative to the band tail states. Deep energy levels also have donor and acceptor states. The donor state of an electron is an energy position below the Fermi level, and the acceptor state is an energy position above the Fermi level. For some amorphous semiconductor materials, the donor and acceptor states of the deep level may overlap at the center of the band gap. This suggests that the deep energy levels at the overlapping positions can be either donor or acceptor states.

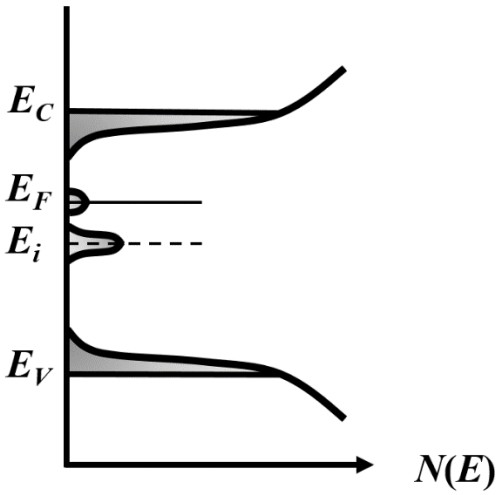

Fig. 2.1.5 Energy band model of amorphous semiconductor material involving in deep states.

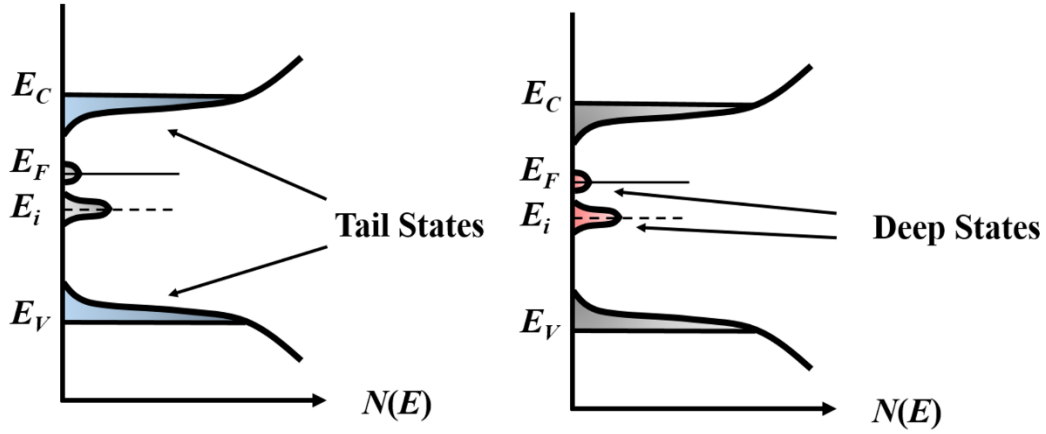

Fig. 2.1.6 Distribution of tail states and deep states in energy band.

2.1.4 Disordered System Conduction Theory

The states of electrons in amorphous materials can be roughly divided into two categories: one type of electrons is located in an extended state, and under the action of an external bias voltage or temperature, its behavior is similar to that of conducting electrons in crystalline materials. Another type of electrons are located in defect states. These two states of electrons determine the conductivity properties of amorphous semiconductor materials.

The electrons in the extended state, in the non-degenerate case, have a concentration distribution that satisfies the Boltzmann equation.

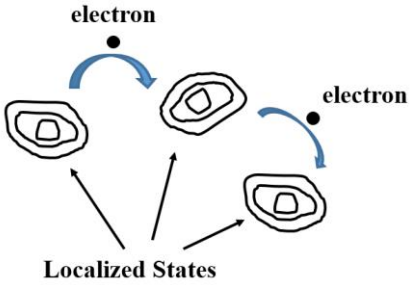

Fig. 2.1.7 Electron hopping process between localized states.

Electrons in the band tail state can jump from one localized state to another under the action of an external bias voltage or temperature, forming another conduction mechanism, as shown in Fig. 2.1.7.

2.2 Fundamentals of InGaZnO Thin Film Transistor

2.2.1 IGZO Material Properties

Amorphous metal oxide IGZO is an ionic compound material composed of In_2O_3, Ga_2O_3 and ZnO, and the bandgap width is about 3.5eV. It is an N-type semiconductor material. The In^{3+} ions in In_2O_3 can form a 5*s* electron orbital at the microscopic level, which can greatly improve the transport speed of carriers, thus improving the electron mobility. Ga_2O_3 has extremely strong ionic bonds, which can strongly inhibit the generation of O^{2-} vacancies. The divalent Zn in ZnO can form a very stable tetrahedral structure, which can make the metal oxide IGZO form a stable amorphous structure. In view of the above factors, metal oxide IGZO is more suitable for making thin film transistors with high mobility.

2.2.2 IGZO TFTs Structure

For the structure of the thin film transistor, when the gate is located above the semiconductor active layer, and the source and drain are located below the semiconductor active layer, it is called a top-gate structure. On the contrary, when the gate is located under the semiconductor active layer, and the source and drain are located above the active layer, it is called a bottom gate structure.

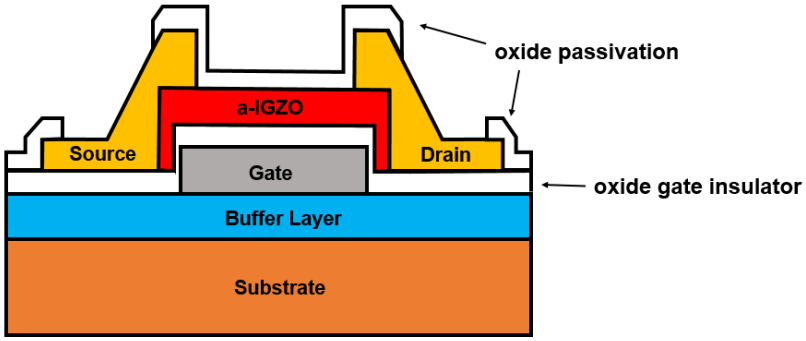

Fig. 2.2.1 Bottom gate structure of IGZO TFTs.

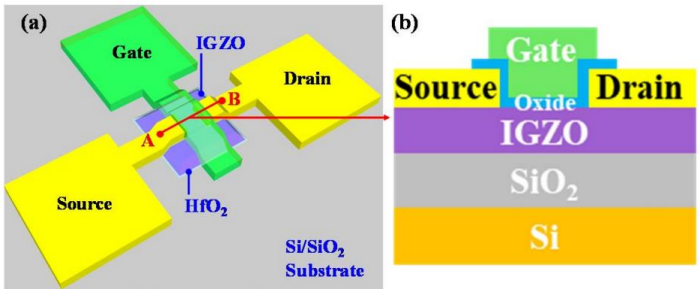

Fig. 2.2.2 Top Gate Structure of IGZO TFTs.

For IGZO TFTs with bottom gate structure, there is a large overlapping area between the gate and the source/drain. On the one hand, there are considerable overlapping capacitances C_{gs} and C_{gd}. At submicron, deep submicron and even nanometer scales, the effect of the overlapping region on the effective channel length cannot be ignored. However, with the top-gate TFT, the gate and source/drain overlap region is very small, the overlap capacitance is small, and the short-channel effect is effectively suppressed.

2.2.3 Operation Mode of IGZO TFTs

For IGZO TFTs, due to the low intrinsic carrier concentration and large number of defects in the amorphous semiconductor thin film material, it is very difficult to form a channel at the interface between the active layer and the gate dielectric layer through the minority in the amorphous thin film. In addition, the intrinsic IGZO material is n-type semiconductor as opposed to the conventional inversion mode of silicon-based MOSFETs, and the channel of IGZO TFT is formed by the accumulation of majority

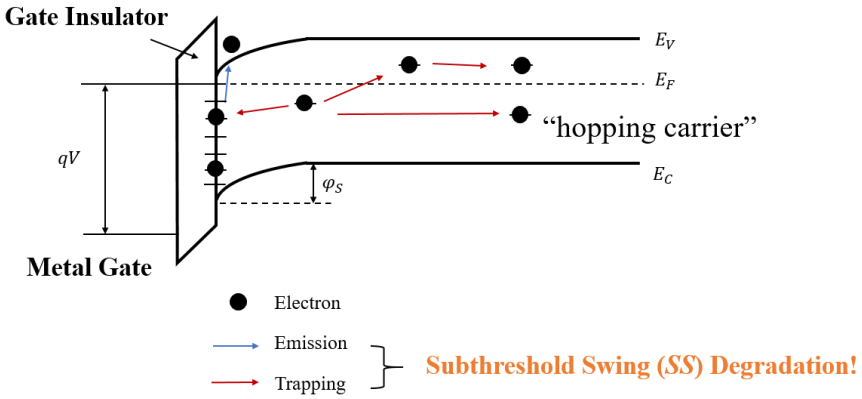

Fig. 2.2.3 Energy band of hopping current conduction mechanism.

(electrons). For enhanced IGZO TFTs, when the gate is positively biased, electrons in the IGZO film will gradually accumulate on the side of the film close to the dielectric layer, thereby forming an electron channel connecting the source and drain. When the gate is negatively biased, the IGZO TFT is turned off. For depleted IGZO TFTs, when no gate bias is applied, electrons in the IGZO film have accumulated on the side of the film close to the dielectric layer, TFT is under the on state. The negative gate bias can make accumulated channel electrons gradually decrease until the TFT is turned off.

In addition, in the process of loading the gate voltage, in addition to forming a part of the carriers of the free electron channel, there is also a part of the electrons attracted by the gate voltage trapped by the defects in the IGZO thin film material near the interface. Under the action of the drain voltage, these trapped carriers participate in conduction through the hopping mechanism, as shown in Fig 2.2.3.

2.3 Threshold Voltage Shift Effect

2.3.1 Drain-Induced Barrier Lowing (DIBL) Effect

For a long channel device with a low V_{DS}, a high barrier can prevent drain current flowing from drain region to source region.

For a device especially the short channel device with a high V_{DS}, the space charge region around drain region and around source region can affect each other and make the height of barrier lower so that drain current will dramatically increase eventually.

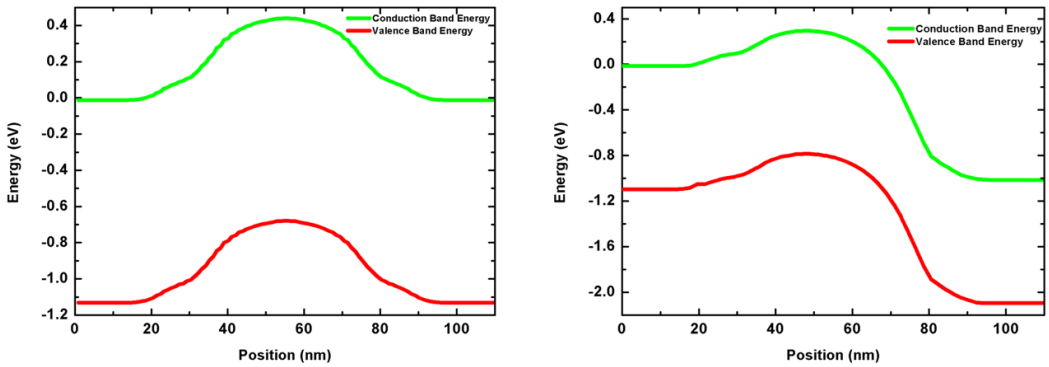

Fig. 2.3.1 Energy band of DIBL effect simulated in Silvaco TCAD.

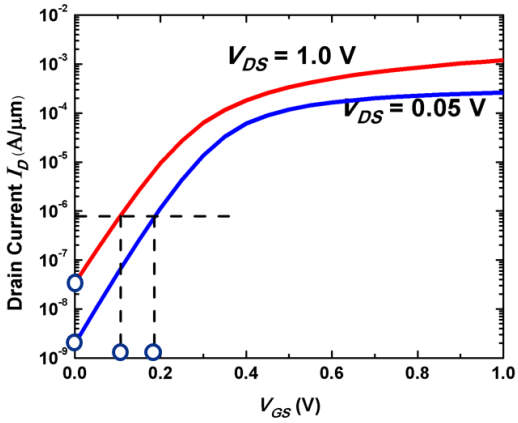

Fig. 2.3.2 DIBL coefficient calculation method through transfer characteristic curve in log-scale.

Simulation results of DIBL effect in Silvaco TCAD are shown in Fig. 2.3.1.

DIBL effect can make the threshold voltage of MOSFET decrease and influence on its performance even make its voltage gain lower. The DIBL coefficient can be obtained from the difference between the threshold voltage at a high drain-source voltage value (e.g., 1V) and that at a low value (e.g., 0.05V) as Fig. 2.3.2 shown.

2.3.2 Trap Effect

Fig. 2.3.3 shows the effect of TFT gate bias on interface state filling. A large number of dangling bonds exist at the interface between the active layer material and the GI layer, and these dangling bonds are the recombination centers of carriers. Typically, the

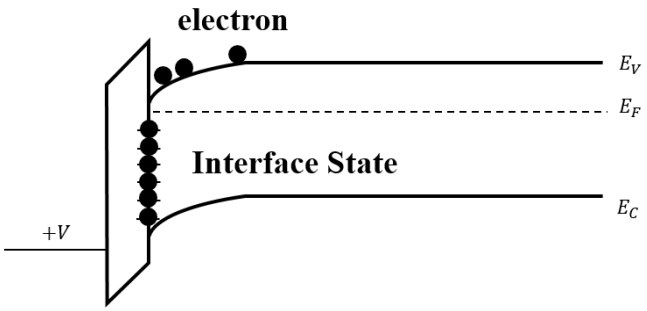

Fig. 2.3.3 The condition of interface states affected by the gate bias.

interface states below the Fermi level are filled with electrons, while the interface states above the Fermi level are empty. No matter how the gate voltage of the TFT is changed or how the energy band of the semiconductor is bent, some electrons will always be trapped in the interface state. Electrons in the interface state can change the surface potential of one side of the semiconductor material, resulting in non-ideal characteristics of the transfer characteristic of the TFT.

In addition, when the positive gate bias of the IGZO TFT is large, the electrons at the interface between the active layer and the GI layer will tunnel into the GI layer under the action of a strong electric field. Because the GI layer is an amorphous material, there are usually a large number of structural defects. The number of defects depends on the quality of the film, and the quality of the film depends on the process conditions when the film is deposited. These structural defects in the film can be effective recombination centers for charge carriers, and electrons trapped in the GI layer are usually difficult to be released. These trapped electrons will have the same effect as the interface fixed charge, causing the transfer characteristic curve of the TFT to shift.

2.3.3 Positive Bias Threshold Instability (PBTI)

IGZO TFT is an n-type thin film transistor. When the gate is included in a positive bias voltage, the electrons in the film will be attracted to the interface near the IGZO and GI. The negative charge at the interface causes the transfer characteristic curve of the device to move toward the direction of the positive gate voltage.

2.3.4 Negative Bias Threshold Instability (NBTI)

When negative bias is applied to the gate of IGZO TFT, electrons at the interface are repelled into the interior of the IGZO film, and holes are attracted by the negative gate bias. However, due to the high concentration of electrons in the IGZO film, the hole concentration is very small, and only a small amount of holes can be attracted to the interface near the IGZO and GI layers by the negative bias loaded by the gate, and can be absorbed by the interface. The number of holes trapped at the donor level at the ion is very small. The shift of the transfer characteristic curve of IGZO TFT to the negative gate voltage direction caused by this is also small. Therefore, the gate voltage reliability of depletion-mode IGZO TFT is stronger than that of enhancement-type IGZO TFT. However, when the IGZO TFT is exposed to light, this negative gate voltage drift becomes very obvious.

2.4 Device Fabrication

The device fabrication started with deposition of 15 nm-thick α-IGZO on a SiO_2/Si substrate by radio frequency sputtering at room temperature. After that, a bilayer structure with 10 nm Ti and 30 nm Au was deposited and lifted off as the source/drain. Mesa formation was performed by a wet etch process using hydrogen chloride acid. This was followed by the deposition of HfO_2 using ALD at a temperature of 300 K. After that, the gate region was defined using electron beam lithography and Ti/Al were deposited and lifted off as the gate contact metal. Finally, a PMA process was performed in N_2 ambient at 300 K for 20 minutes. Three different L_{CH} of 1 μm, 500 nm and 200 nm are formed short-channel a-IGZO TFT devices, respectively. All electrical measurements were carried out using a Keithley 4200 Semiconductor Characterization System (SCS) Semiconductor Parameter Analyzer.

CHAPTER 3 LITERATURE REVIEW

3.1 Multiple Trapping and Release (MTR) Transport Mechanism

For amorphous metal oxides, organic and polymer thin film transistors, carrier transport is always described as the basic Multiple Trapping and Release (MTR) model. The concept of band mobility is introduced to illustrate the process that charges are assumed to be trapped in a manifold of states and thermally excited to extended states where they have some mobility value. However, the drawback of basic MTR model is some details of the charges behavior that move in extended states are negligible. Crucially, the complicated interaction between the trapped and extended state carriers is significant to determine the effective mobility under near all conditions.

Xiao et al. [1] expanded the MTR model to involve these effects and demonstrated a new type of scattering mechanism, which is called trapped carrier (TC) scattering. Different from common impurity scattering and carrier-carrier scattering, TC scattering includes the scattering of carriers that move in extended states by carriers that are trapped and essentially immobile. The high degree of spatial overlap between these types of carriers makes this a particularly effective and important scattering mechanism in TFTs. Our work can be considered as the natural extension of the long-serving MTR model for TFTs based on disordered semiconductors. It is a substantial extension, which includes the use of the Boltzmann transport equation (BTE) and considers all relevant scattering mechanisms. It also includes the effects of screening which is particularly important in such trap-influenced materials. We note that the trap density of states (DOS) is influenced by the stoichiometry of the semiconductor. In particular, oxygen vacancies

influence the mobility, as has been shown by work of R. Martinset al. [2] and H. Hosono et al. [3]

Once a charged carrier is trapped in a trap in the semiconductor, the trap can be regarded as a charged (or ionized) scattering center, since the carrier release and trap rate is much lower than the scattering rate. The total trapped carrier density consists of

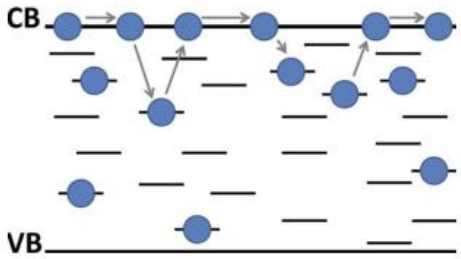

Fig. 3.1.1 Schematic view of the MTR-transport mechanism. A charge carrier (filled circle) from the conduction band is trapped into a localized site in the gap. After a thermal excitation, it can return in the extended state where it is free to move. The transport takes place by means of MTR events.

two components: carriers trapped at the interface between the semiconductor and the gate insulator and carriers trapped in the semiconductor. The carriers trapped at the interface can also impact the charge transport. [4]

In addition to the trapped carrier scattering (which is a Coulomb scattering mechanism), the electron–phonon interaction also can influence the transport in the band. Certain lattice vibration modes—phonons—can effectively scatter charges even in amorphous oxide thin films. Longitudinal Optical (Polar Optical) Phonon Scattering and Surface Optical Phonon Scattering. The details of the former is that A strong Coulomb potential is caused by the movement of the different atoms in optical vibrations (atoms moving against each other) in polar semiconductors. This Coulomb interaction effectively modifies the dielectric function by the dispersion of the long wave length LO mode. This mode of phonon is a very effective scattering mechanism for electrons in polar semiconductors, including oxide semiconductors. For the latter, High-k dielectrics such as HfO_2 in close proximity with a conducting surface channel in a semiconductor leads to enhanced surface optical (SO) scattering due to remote optical phonon coupling between electrons in the semiconductor channel and polar vibrations in the dielectric. For thin film semiconductors, this SO-phonon scattering should exist too.

The multiple trap and release (MTR) model has been widely applied to analyze transport in thin film semiconductor system since the defects play an important role in

carrier transport. The MTR effective mobility is the band mobility multiplied by the fraction of carriers (free carriers) in the band.

Here, $\mu_{band} = \frac{q\tau}{m^*}$ is mobility of carriers in the band.

According to Matthiessen's rule, the total band mobility arises from the combination of several scattering mechanisms such as trapped carrier Coulomb scattering and various phonon scattering etc. is given by where μ_{tc} is the trapped carrier mobility, and the μ_{ph} is the mobility limited by different phonon interaction mechanisms.

3.2 Field Effect Mobility Model in Oxide Semiconductor Thin Film Transistors with Arbitrary Energy Distribution of Traps

Ling Li et al. [5] elaborated a unified physical model of mobility in oxide semiconductors with arbitrary energy distribution of traps based on the multiple trapping and release theory, the VRH theory is not involved in this model. Even so, the hopping like charge transport and band like transport can be described consistently.

In crystalline field-effect transistors above threshold, nearly all the charge induced in the channel appears in the conduction band, yielding a clear threshold and full band mobility. In real defective channel TFTs, however, much of the induced charge is trapped at localized mid-gap (deep) or shallow (tail) states degrading the subthreshold slope, mobility, and threshold sharpness [6]. Therefore, the voltage-dependent effective mobility for long defective channel TFTs could be expressed as follows.

$$\mu_{eff} = \mu_n \frac{n_{free}}{n_{induced}} = \mu_n \frac{n_{free}}{n_{free} + n_{trap}} \quad (1)$$

where, μn, ni, and nf are the band mobility, the sheet density of total induced electrons, and the sheet density of the free electrons at conduction band, respectively.

In the case of amorphous-channel TFTs such as a-Si:H and oxide TFTs, the density of acceptor-like defect states (g(E)) could be assumed to be approximately exponential with energy (E) as follows.

$$g(E) = g_{t0} \exp\left(\frac{E - E_C}{kT_t}\right) + g_{d0} \exp\left(\frac{E - E_C}{kT_d}\right) \quad (2)$$

Where E_C and $T_{t/d}$ are the conduction band energy and the characteristic temperatures

of the tail and deep states, respectively.

From the above assumption and in the accumulation mode, the free-electron sheet density (n_{free}) induced in the channel at a gate bias (V_G) is known to have a power-law relation with gate bias as follows.

$$n_{free\_above} \propto (V_{GS} - V_{th})^{\alpha+1} \tag{3}$$

$$n_{free\_below} \propto K_b(V_{GS} - V_{FB})^{\beta+1} \tag{4}$$

α and β are two fitted coefficient that indicate the characteristic temperature of tail states and deep states, as expressed as follows.

$$\alpha = 2\left(\frac{T_t}{T} - 1\right) \tag{5}$$

$$\beta = 2\left(\frac{T_d}{T} - 1\right) \tag{6}$$

$$\mu_{eff\_above} = \mu_n \frac{n_{free}}{n_{induced}} = \mu_n \frac{\frac{C_{ox} \cdot K_a(V_{GS} - V_{th})^{\alpha+1}}{\mu_n \cdot q}}{\frac{\int_{V_{th}}^{V_{GS}} C_{ox}\, dV_{GS}}{q}} = K_a(V_{GS} - V_{th})^{\alpha} \tag{7}$$

Similarly,

$$\mu_{eff\_above} = \mu_n \frac{n_{free}}{n_{induced}} = \mu_n \frac{\frac{C_{ox} \cdot K_b(V_{GS} - V_{th})^{\alpha+1}}{\mu_n \cdot q}}{\frac{\int_{V_{FB}}^{V_{GS}} C_{ox}\, dV_{GS}}{q}} = K_b(V_{GS} - V_{FB})^{\beta} \tag{8}$$

Interestingly, although VRH theory is not included in this model, the gate voltage dependence of the field effect mobility predicted by (7) and (8) agrees with the results developed by VRH theory [7]. However, it also reveals the transition from hoping-like transport to band like transport.

However, for short-channel device, contact effect can bring effective mobility degradation. Contact resistance should be considered in above threshold region and (7) should be corrected according to the definition of effect of source and drain series resistance.

CHAPTER 4 ANALYTICAL MODEL

4.1. Voltage Dependent Above Threshold Current Model

Derivation from the physical insight of direct current, the drain current of IGZO TFTs can be described as:

$$I_D = \frac{Q_{free}}{t} = \frac{Q_{free} \cdot v}{L} \tag{9}$$

For the active layer is very thin, according to 1-D Poisson's equation shown in (11), doing mathematic manipulation as descripted in (11), final drain current can be obtained from (11).

$$\int_0^L I_{D\_above}\,(V_{GS}, V_{DS})dx$$

$$= \frac{Q_{free\_above}}{L} \cdot \mu_{contact}(V_{GS}) \cdot F_{sat}(V_{GS}, V_{DS})$$

$$\cdot \int_0^{V_{DS}-I_D R_{SD}(V_{GS})} dV_{CH} \tag{10}$$

Q_{free_above} can be described as (11) according to the definition of effective mobility. [8]

$$Q_{free\_above} = W \cdot L \cdot \frac{C_{ox} \cdot K_a (V_{GS} - V_{ths})^{\alpha+1}}{\mu_n} \tag{11}$$

Here, $\mu_{contact}$ is the effective mobility in short-channel device considering the contact effect, it is a key parameter that is a function of gate voltage. [9] Besides, when considering the interface traps, the component V_{th} in the original expression should be corrected to $V_{th} + q\varphi_S$, symbolled as V_{ths}, which represents a new threshold voltage definition based on the surface potential.

$$\mu_{contact}(V_{GS}) = \frac{\mu_{eff\_above}(V_{GS})}{1 + \mu_{eff}(V_{GS}) \cdot \frac{W}{L} \cdot \int_{V_{th}+q\varphi_S}^{V_{GS}} C_{ox}\, dV_{GS} \cdot R_{SD}(V_{GS})} \tag{12}$$

Also, for short-channel device, it is essential to pay attention to short channel effect, indicating threshold voltage roll off, subthreshold swing and DIBL effect. So, the corrected threshold voltage based surface potential can be derived as follow.

$$V_{ths} = V_{ths0} - \delta \Delta V_{DS} \tag{13}$$

Where V_{ths0} is the threshold voltage at a low drain voltage based surface potential and δ is DIBL coefficient.

As Silicon MIT Virtual Source Model illustrated, [10] for ultra-scaled channel length MOSFET, the transition function $F_{sat}(V_{GS}, V_{DS})$ is given as

$$F_{sat}(V_{GS}, V_{DS}) = \frac{(V_{DS} - I_D R_{SD}(V_{GS}))/V_{Dsat}}{\left(1 + \left(\frac{V_{DS} - I_D R_{SD}(V_{GS})}{V_{Dsat}}\right)^{\theta}\right)^{\frac{1}{\theta}}} \tag{14}$$

$$V_{Dsat} = V_{GS} - V_{ths} \tag{15}$$

Here, θ is so-called saturation coefficient, which is a fitted parameter, V_{Dsat} is the critical saturation voltage of IGZO TFTs, and the expression $V_{DS} - I_D R_{SD}(V_{GS})$ characterizes the actual voltage dropped to the channel region when considering the source and drain series resistance.

However, for amorphous oxide semiconductor TFTs, the transverse electrical field will increase with a larger drain voltage, leading to the fact that electrons localized in traps would be activated, and enhance the hopping current. Also, the drain current would increase permanently. Therefore, a new transition function $F_{sat}(V_{GS}, V_{DS})$ considering the enhancement effect of hopping current can be modulated as (11) expressed. H is the hopping enhancement modulation function that required to be fitted as a function of voltage as well. Also, θ in (14) is also divided into two saturation coefficient θ_1 and θ_2 for a-IGZO device, in order to make an more accurate modulation modeling the quasi-saturation effect in amorphous channel material transistors.

$$F_{sat}(V_{GS}, V_{DS}) = H(V_{GS}, V_{DS}) \cdot \frac{(V_{DS} - I_D R_{SD}(V_{GS}))/V_{Dsat}}{\left(1 + \left(\frac{V_{DS} - I_D R_{SD}(V_{GS})}{V_{Dsat}}\right)^{\theta_1}\right)^{\frac{1}{\theta_2}}} \tag{16}$$

4.2. Voltage Dependent Below Threshold Current Model

Due to the localized states in defective channel material, the diffusion process is very difficult for carriers to achieve successfully, the dominant current is also drift current in

subthreshold region, which is mainly determined by the effective mobility.

As the analysis based on the experimental data and mathematic manipulation, the source and drain series resistance can be negligible for subthreshold current model, for the parasitic resistance can be viewed as the total resistance numerically.

Similarly,

$$\int_0^L I_{D\_below}\,(V_{GS}, V_{DS})dx = \frac{Q_{free\_below}}{L} \cdot \mu_{eff\_below}(V_{GS}) \cdot \int_0^{V_{DS}} dV_{CH} \quad (17)$$

Q_{free_above} can be also expressed as (11) according to the definition of effective mobility. [11]

$$Q_{free\_below} = W \cdot L \cdot \frac{C_{ox} \cdot K_b (V_{GS} - V_{FBS})^{\beta+1}}{\mu_n} \quad (18)$$

In the same way, when considering the interface traps, the component V_{th} in the original expression should be corrected to $V_{FB} + q\varphi_S$, symbolled as V_{FBS}, which represents a new flat band voltage definition based on the surface potential.

4.3 Unified Analytical Current versus Voltage Model

After deriving the drain current versus voltage expression in both above threshold region and subthreshold region, and unified analytical model can be obtained by using the reciprocal demonstration to keep a good transition. Also, the gate leakage current still should to be considered in the final compact model. In this project, this part is not mainly mentioned and summarized to the future work.

The unified analytical model is descripted according to (19).

$$I_D = I_{leakage}(V_{GS}, V_{DS}) + \left(\frac{1}{I_{D\_sub}(V_{GS}, V_{DS})} + \frac{1}{I_{D\_above}(V_{GS}, V_{DS})}\right)^{-1} \quad (19)$$

CHAPTER 5 METHOD & ANALYSIS

5.1 DIBL Coefficient Extraction

As mentioned before, drain induced barrier lowering (DIBL) is a short-channel effect in MOSFETs referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. In a classic planar field effect transistor with a long channel, the bottleneck in channel formation occurs far enough from the drain contact that it is electrostatically shielded from the drain by the combination of the substrate and gate, and so classically the threshold voltage is independent of drain voltage. In short-channel devices, however, this is no longer true: The drain is close enough to gate the channel, and so a high drain voltage can open the bottleneck and turn on the transistor prematurely. According to (20), DIBL coefficient can be calculated by the threshold voltage change with the drain voltage.

$$\delta = \frac{\Delta V_{th}}{\Delta V_{DS}} \tag{20}$$

In addition, constant current method is also used to extract threshold voltage of IGZO TFTs. The constant current method can be expressed as (21). [5]

$$V_{th} = V_{GS}|_{\frac{W}{L}\times 10\ \mathrm{n}A} \tag{21}$$

TABLE I

EXTRACTION RESULTS OF THRESHOLD VOLTAGE AND DIBL COEFFICIENT

	L_{CH}=1μm	L_{CH}=500nm	L_{CH}=200nm
V_{th0} (expt. V_{DS}=0.1V) (V)	-2.09	-2.26	-2.76
V_{th_DIBL} (expt. V_{DS}=1V) (V)	-2.40	-2.36	-2.77
δ (mV/V)	13	110	344

5.2 Levenberg-Marquardt (LM) Algorithm

The Levenberg-Marquardt (LM) algorithm is one of the optimization algorithms. Simultaneously, it has the advantages of both gradient descent method and Gauss-Newton iteration method.

The LM algorithm can be understood as the combination of Gauss-Newton algorithm and gradient descent method. According to (22) gradient descent method, the gradient information of the current position is given, that is the first derivative of the loss equation with respect to the variable. The Newton method gives the Hessian matrix, that is, the second derivative of the loss equation with respect to the variable, as described in (23).

$$x_{k+1} = x_k - \alpha g_k \tag{22}$$

$$x_{k+1} = x_k - {H_k}^{-1} g_k{}' \tag{23}$$

However, although the Newton method has a fast convergence speed, it needs to calculate the Hessian matrix. For high-dimensional problems, the calculation of the second derivative will be very complicated. So we have the Gauss-Newton iterative algorithm. The Gauss-Newton algorithm does not directly calculate the Hessian matrix, but fits the Hessian matrix through the Jacobian matrix, as described in (24).

$$H \approx J^T J \tag{24}$$

However, by fitting the Hessian matrix with the Jacobian matrix, the calculated result is not necessarily invertible. Therefore, on this basis, it is necessary to introduce an identity matrix, which is described in (25).

$$H \approx J^T J + \mu I \tag{25}$$

This gives the LM algorithm mentioned in (26). It can be seen that when μ is close to 0, the algorithm approximates the Gauss-Newton algorithm, while when μ is large, the algorithm approximates the gradient descent method.

$$x_{k+1} = x_k - (J^T J + \mu I)^{-1} g_k \tag{26}$$

Table II lists several algorithms and comparisons among them.

TABLE II

COMPARISON BETWEEN DIFFERENT MATHEMATIC ITERATION ALGORITHM

Algorithms	Update Rules	Convergence	Computation Complexity
EBP algorithm	$\omega_{k+1} = \omega_k - \alpha g_k$	Stable, slow	Gradient
Newton algorithm	$\omega_{k+1} = \omega_k - H_k^{-1} g_k$	Unstable, slow	Gradient and Hessian
Gauss-Newton algorithn	$\omega_{k+1} = \omega_k - \left(J_k^T J_k\right)^{-1} J_k e_k$	Unstable, fast	Jacobian
Levenberg-Marquart algorithm	$\omega_{k+1} = \omega_k - \left(J_k^T J_k + \mu I\right)^{-1} J_k e_k$	Stable, fast	Jacobian
NBN algorithm	$\omega_{k+1} = \omega_k - Q_k^{-1} g_k$	Stable, fast	Quasi Hessian

5.3 Contact Resistance Extraction

Long channel transistors have been very useful for understanding and modeling the physical properties of the transistor channel, but for 3D monolithic integration, the required IGZO thin film transistor channel length is limited to sub-micron, deep sub-micron even nano-scale. When scaling down the transistor channel length, other physical effects such as injection processes, interface traps between metal electrode and semiconductor, and variations or imperfections introduced by the technology process have to be considered. These factors are usually collected under the name of "contact effects", as shown in Fig .5.3.1.

The studies on amorphous and polycrystalline silicon [11], [12] and also on organic semiconductors [13], [14] lead to a common shared point: Contact resistances in high-mobility and short channel TFTs seriously affect the transistor performance. In general, the "parasitic" voltage drop at the contacts reduces the effective bias voltage applied to the intrinsic drain to source channel and consequently reduces the device current. Therefore, source and drain parasitic resistances R_S and R_D give rise to an apparent field-effect mobility μ_{FE}, which is lower than the actual one. The impact of the contact resistance is more relevant at large carrier mobility and small channel length, where the contact resistance may become comparable to, or even larger than the channel resistance.

Extraction of contact resistance (R_{SD}) in short channel device is significant owing to

non-ideal ohmic contact between the source/drain electrode and semiconductor material channel. As what have mentioned above, although the contact resistance can be neglected in long channel devices for the channel resistance composes almost total resistance of the device, the impact of contact resistance can be more serious in short channel devices and cause both mobility degradation and current reduction. In order to examine the effect of contact resistance on the short channel IGZO TFTs, conventional method of extracting total resistance is used. For extraction of contact resistance, also called source and drain series resistance, transfer length method (TLM) is used in this work. The total resistance R_{TOT} is determined by:

$$R_{TOT}=r_{ch}L+R_{SD}$$

Here r_{ch} is the channel resistance per channel length unit of IGZO and R_{SD} is the series resistance of source and drain.

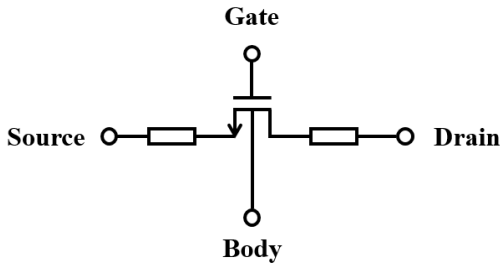

Fig. 5.3.1 Schematic view of source and drain series resistance.

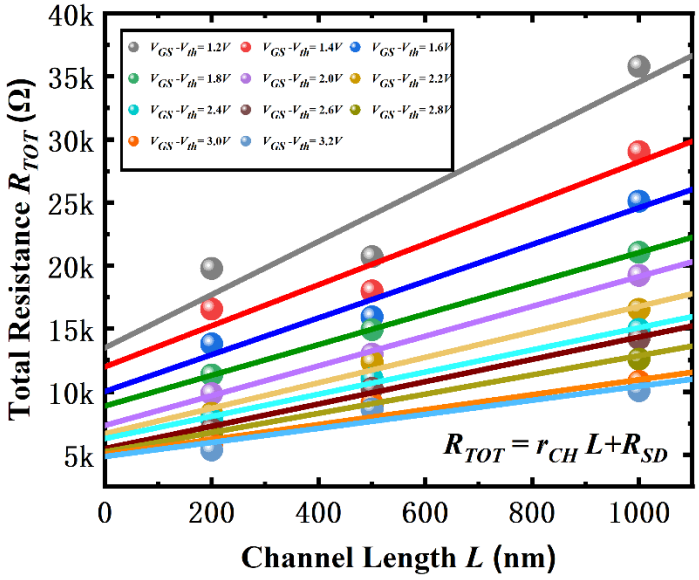

Fig. 5.3.2 Contact resistance extraction by using transfer length method (TLM).

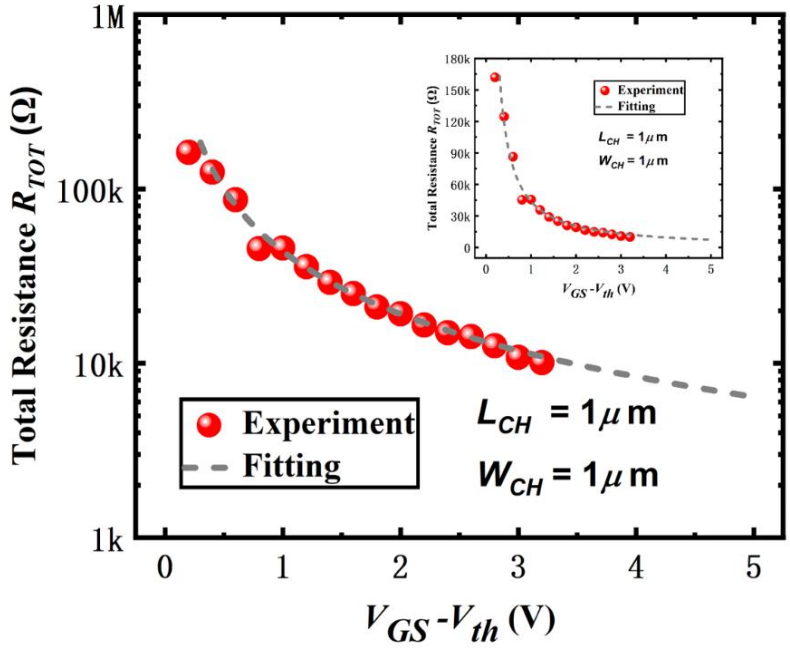

Fig. 5.3.3 The function of total resistance vs driving voltage for IGZO TFT with L_{CH}=1μm.

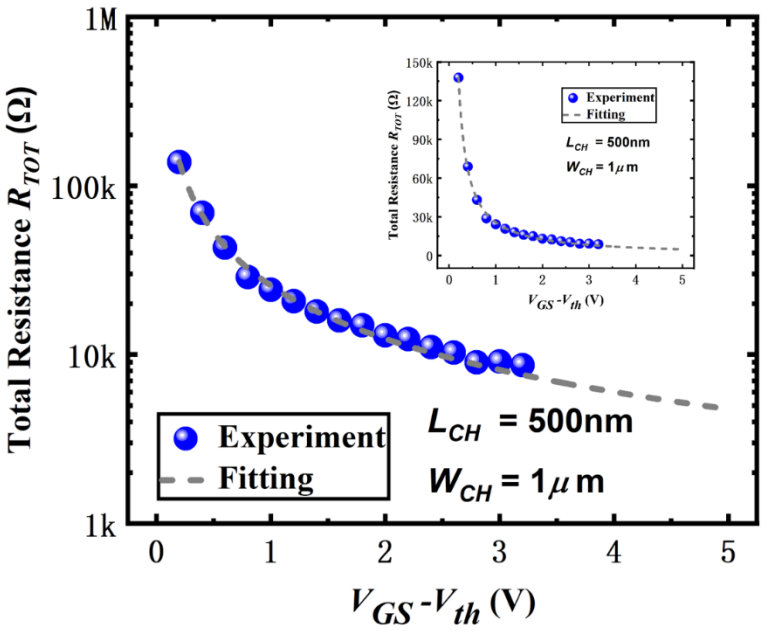

Fig. 5.3.4 The function of total resistance vs driving voltage for IGZO TFT with L_{CH}=500nm.

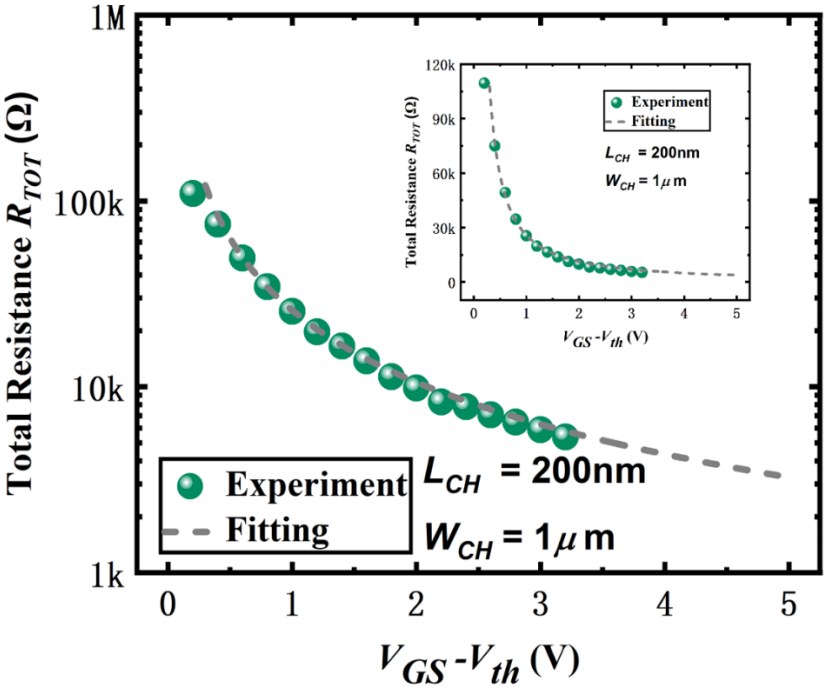

Fig. 5.3.5 The function of total resistance vs driving voltage for IGZO TFT with L_{CH}=200nm.

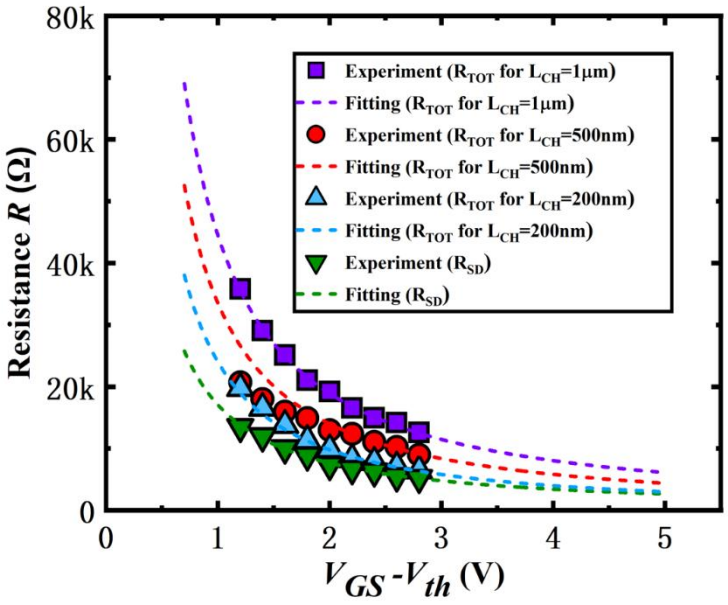

Fig. 5.3.6 Comparison of all resistance for IGZO TFTs with different channel length.

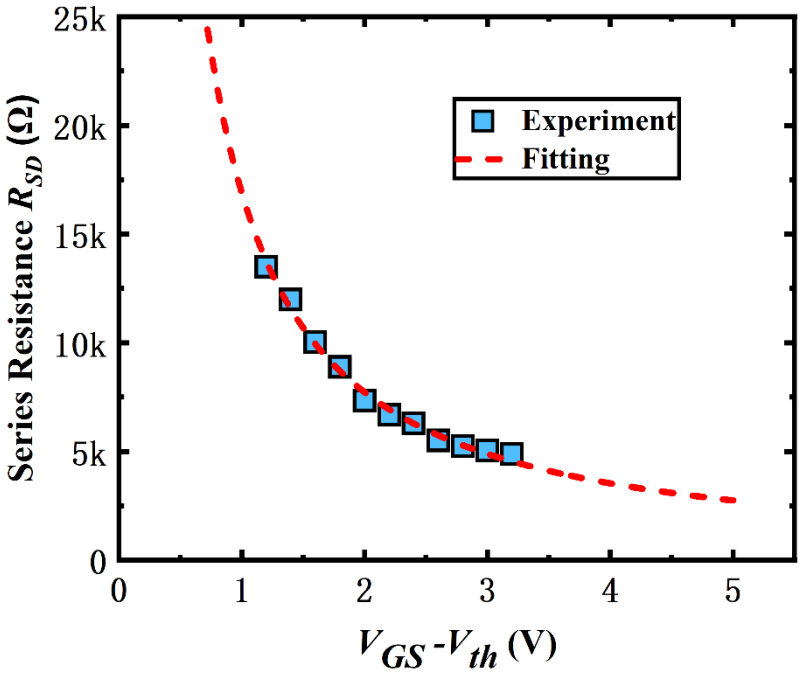

Fig. 5.3.7 Source and drain resistance extraction and fitted function.

TABLE III

EXTRACTION RESULTS OF SOURCE AND DRAIN SERIES RESISTANCE

Fitted Parameter	Value
A	16.88
n	1.13

We can use fitting equation (27) to extract the fitted parameter and then obtain the relationship between contact resistance and gate driving voltage.

Table III shows the extraction results of this step.

$$R_{SD} = \frac{A}{(V_{GS} - V_{th})^n} \tag{27}$$

5.4 Effective Mobility Extraction

It is believed that the field effect mobility should increase with increasing gate-induced charge carrier concentration and increasing temperature in disordered semiconductors [15], [16]. This phenomenon is a consequence of thermally activated hopping [17], where the carriers hop between localized states with the assistance of thermal energy [18]. An increase in carrier concentration raises the Fermi level and suppresses the average barrier height for energetic uphill jump, resulting in higher field-effect mobility [19]. Contrary to theory, several teams had observed degradation in mobility at a certain high voltage after initially increasing mobility [15], [20]. They attributed this abnormal behavior to contact resistance or increased interface scattering as gate voltage increases [21].

For the extraction of effective mobility, Hoffman's method can be used as (28) descripted. To notice that the drain voltage should be small enough to convince a low-field effect mobility.

$$\mu_{eff} = \frac{L}{W}\frac{I_D}{C_{ox}(V_{GS} - V_{on})V_{DS}} \tag{28}$$

Here V_{on} represents V_{ths} and V_{FBS} in above and below threshold voltage region, respectively when considering about the effect of interface trap.

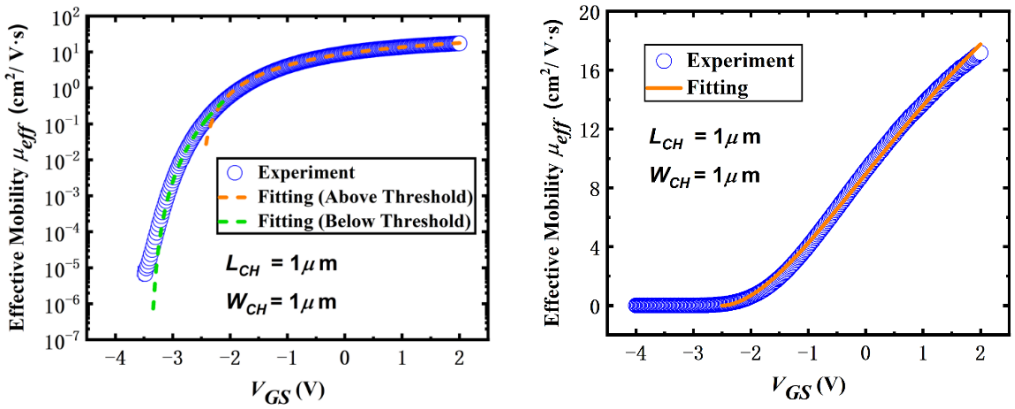

Fig. 5.4.1 Effective mobility extraction and fitted function when considering contact effect for IGZO TFTs with L_{CH}=1μm.

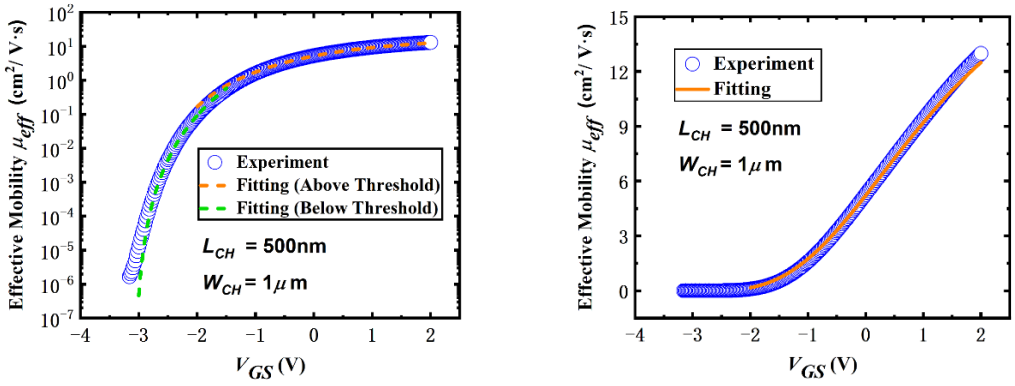

Fig. 5.4.2 Effective mobility extraction and fitted function when considering contact effect for IGZO TFTs with L_{CH}=500nm.

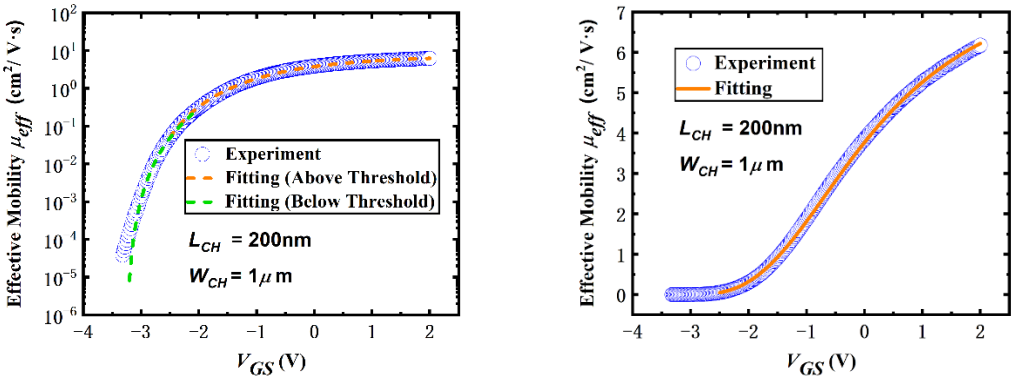

Fig. 5.4.3 Effective mobility extraction and fitted function when considering contact effect for IGZO TFTs with L_{CH}=200nm.

TABLE IV

EXTRACTION RESULTS OF EFFECTIVE CARRIER MOBILITY

Fitted Parameter	L_{CH}=1μm	L_{CH}=500nm	L_{CH}=200nm
K_a	1.394	0.431	1.031
α (T_t)	1.769 (565 K)	3.026 (754 K)	2.358 (301 K)
K_b	0.138	0.081	0.205
β (T_d)	3.453 (818 K)	4.877 (1763 K)	3.060 (759 K)
V_{fbs} (V)	-3.61	-3.32	-3.13

CHAPTER 6 RESULTS AND DISCUSSION

6.1 Transfer Characteristic Curve

From transfer characteristic curve, it is clear that the curve can be divided into subthreshold region, above threshold region and leakage current region. Furthermore, above threshold region can be separated into linear region and saturation region.

Fig. 6.1.1 to Fig. 6.1.3 all show comparison of transfer characteristic curve between fabricated device and the compact model in this work, it is so obvious that the fitting results have an excellent agreement between the measured data and analytical compact model in both subthreshold and above threshold region.

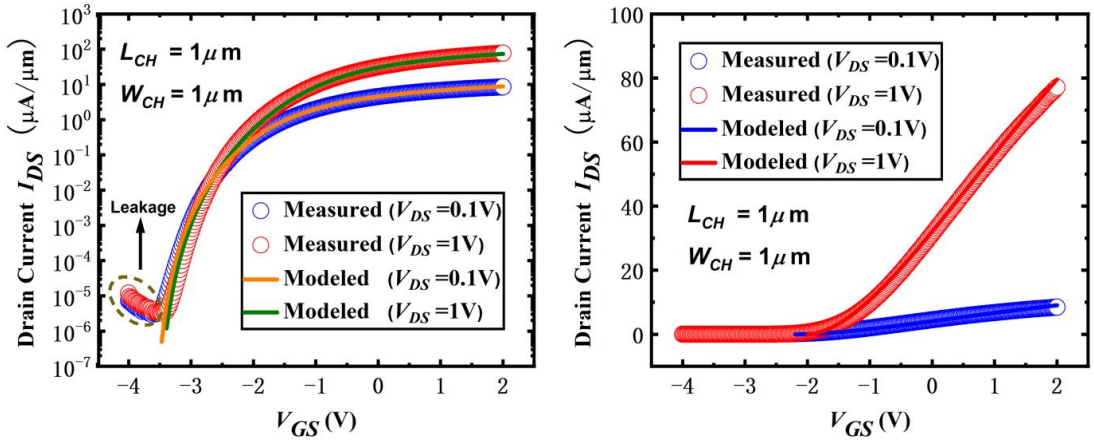

Fig. 6.1.1 Comparison of transfer characteristic curve between experimental data and our unified compact model for IGZO TFTs with L_{CH}=1μm.

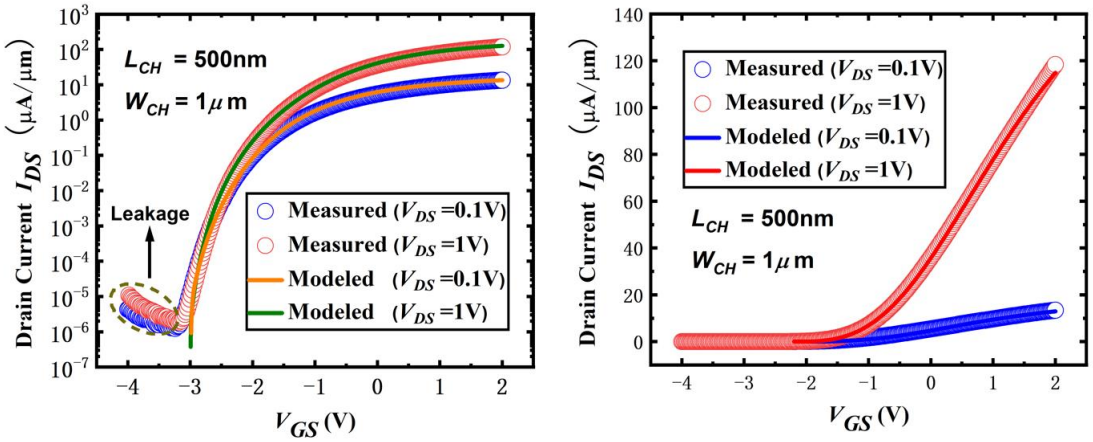

Fig. 6.1.2 Comparison of transfer characteristic curve between experimental data and our unified compact model for IGZO TFTs with L_{CH}=500nm.

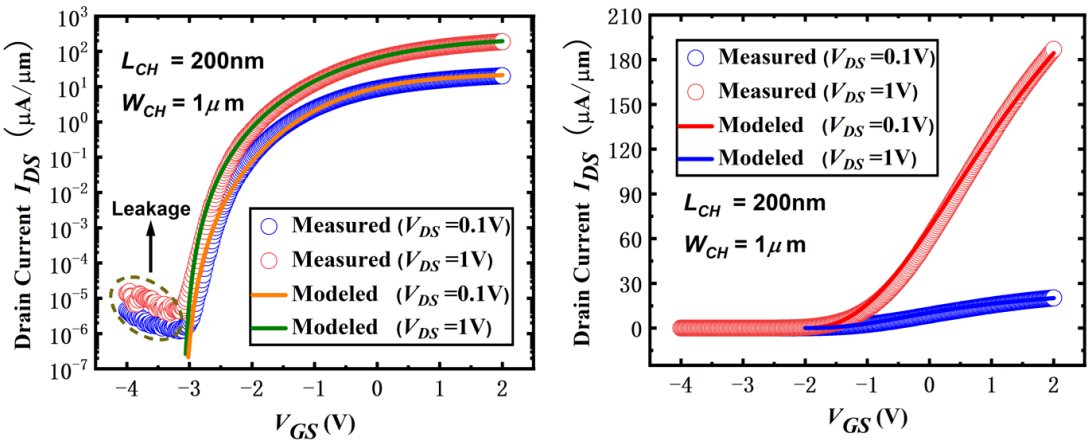

Fig. 6.1.3 Comparison of transfer characteristic curve between experimental data and our unified compact model for IGZO TFTs with L_{CH}=200nm.

6.2 Transconductance

Transconductance is one of the most important parameters of MOSFET, which is used to describe the ability of gate voltage to control drain current. Also, it indicates the electrical characteristic relating the current through the output of one device to the voltage across the input of itself. The maximum transconductance can be calculated as the maximum derivative of the I_D-V_G curve. Through (29), g_m can be obtained automatically through the inner calculation tool of Origin Pro.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{29}$$

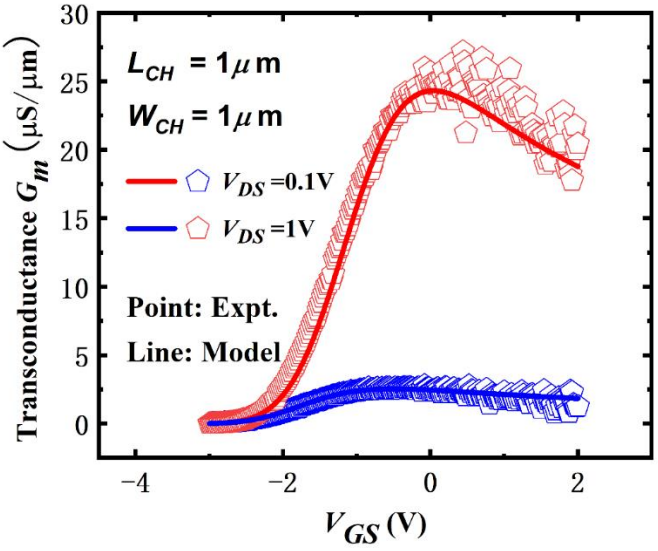

Fig. 6.2.1 Comparison of transconductance between experimental data and our compact model for IGZO TFTs with L_{CH}=1μm.

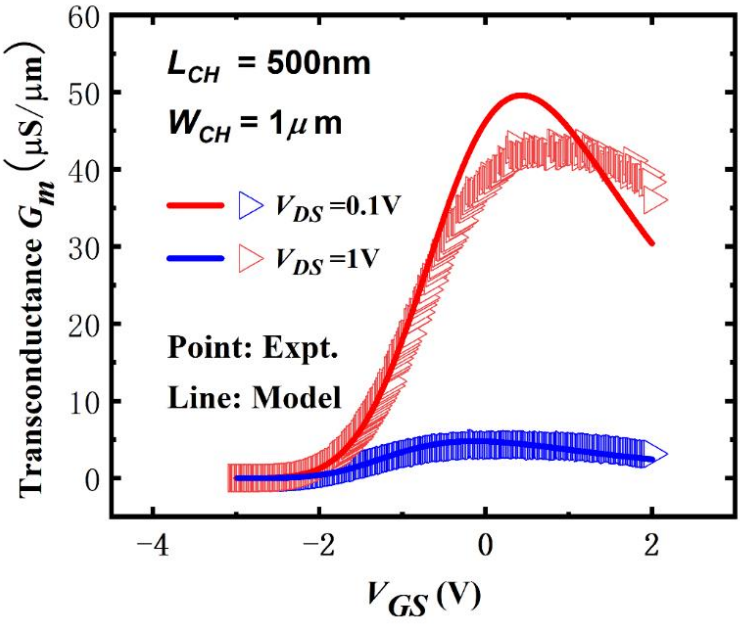

Fig. 6.2.2 Comparison of transconductance between experimental data and our compact model for IGZO TFTs with L_{CH}=500nm.

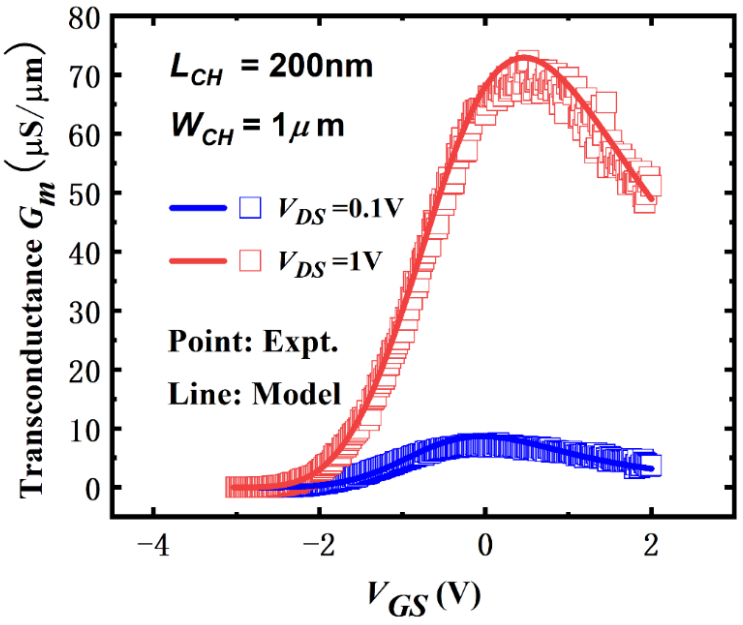

Fig. 6.2.3 Comparison of transconductance between experimental data and our compact model for IGZO TFTs with L_{CH}=200nm.

TABLE V

COMPARISON OF MAXIMUM TRANSCONDUCTANCE BETWEEN EXPERIMENT AND COMPACT MODEL

	L_{CH}=1μm	L_{CH}=500nm	L_{CH}=200nm
Gm, max (expt. V_{DS}=0.1V) (μS/μm)	2.62	4.53	7.36
Gm, max (model V_{DS}=0.1V) (μS/μm)	2.59	4.79	8.69
Relative Error (model. V_{DS}=0.1V)	1.15 %	5.74 %	18.07 %
Gm, max (expt. V_{DS}=1V) (μS/μm)	27.17	42.81	72.35
Gm, max (model V_{DS}=1V) (μS/μm)	24.82	49.59	72.89
Relative Error (model. V_{DS}=1V)	8.65 %	15.84 %	0.75 %

Fig. 6.2.1 to Fig. 6.2.3 all show comparison of transconductance between fabricated device and the compact model in this work, it is also apparent that the fitting results have a great agreement between the measured data and analytical compact model after doing mathematical differential manipulation.

6.3 Output Characteristic Curve

From output characteristic curve, it is clear to observe so-called quasi-saturated effect. That is because both channel length modulation effect and hopping current enhancement, which means carriers in trap states are thermally activated by increasing transverse electrical field gradually.

Similarly, Fig. 6.3.1 to Fig. 6.3.3 all show comparison of output characteristic curve between fabricated device and the compact model in this work, it is clear that the fitting results have an excellent agreement between the measured data and analytical compact model in both subthreshold and above threshold region.

Table I shows the results of fitted parameters that characterize transition between linear region and saturation region in our compact model.

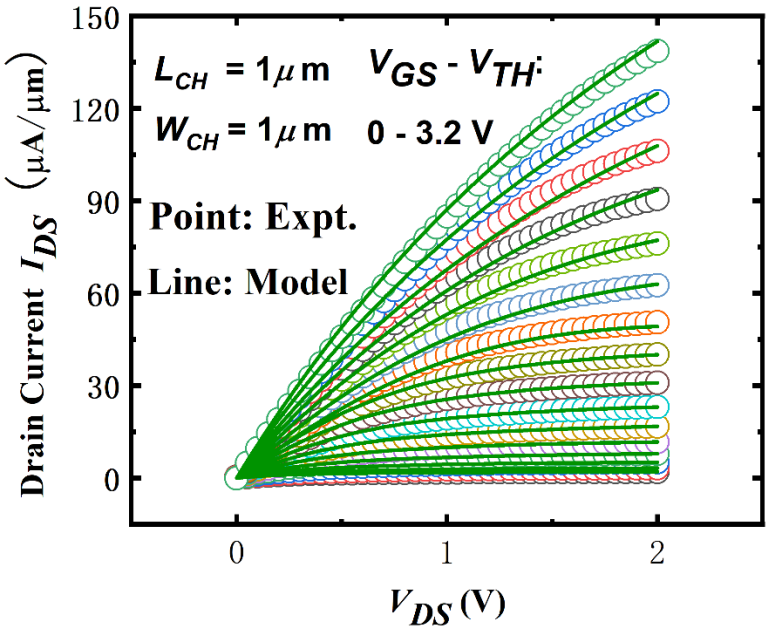

Fig. 6.3.1 Comparison of output characteristic curve between experimental data and our unified compact model for IGZO TFTs with L_{CH}=1μm.

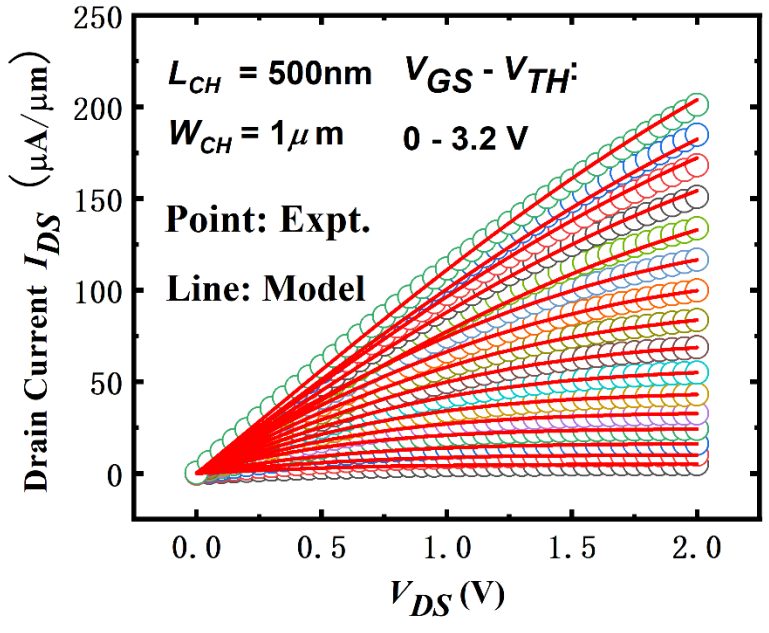

Fig. 6.3.2 Comparison of output characteristic curve between experimental data and our unified compact model for IGZO TFTs with L_{CH}=500nm.

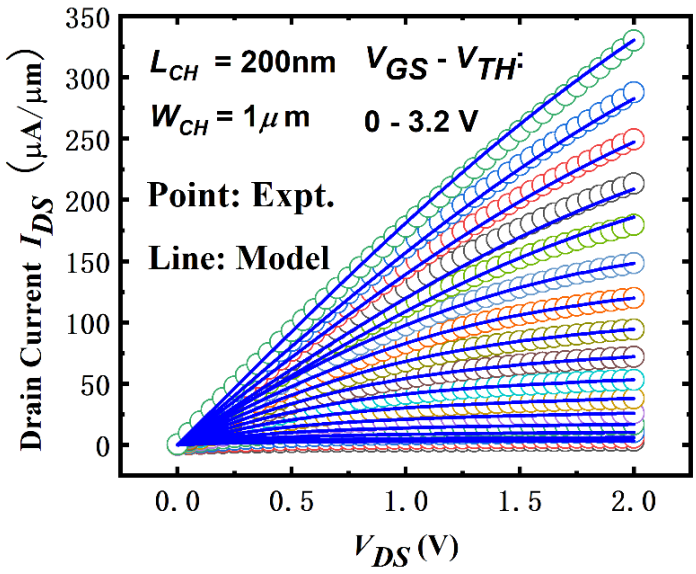

Fig. 6.3.3 Comparison of output characteristic curve between experimental data and our unified compact model for IGZO TFTs with L_{CH}=200nm.

6.4 DIBL Coefficient Variation

Similarly, the final results of DIBL coefficient have a good agreement between the fabricated device and our compact model, which indicates the modeling results for device target are pretty excellent as well as the results of characteristic curve fitting.

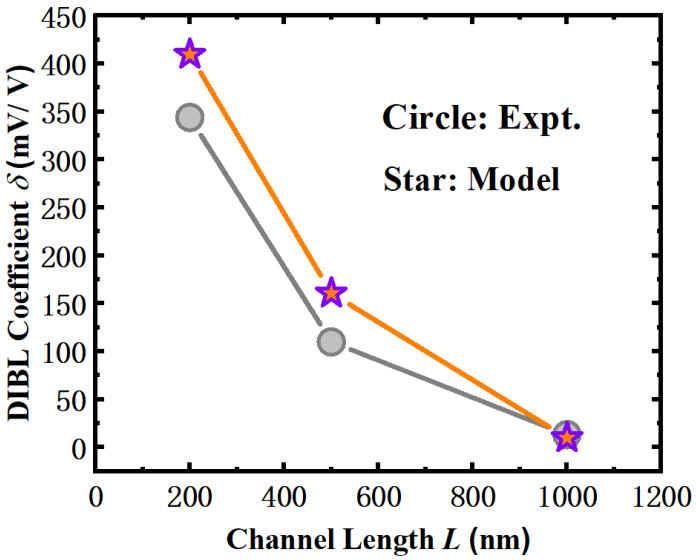

Fig. 6.4.1 Comparison of DIBL coefficient variation between experiment and compact model.

CHAPTER 7 CONCLUSION

In this project, a compact model for a-IGZO TFTs at sub-micron and deep sub-micron scales is successfully developed with the considering of drain-induced barrier (DIBL) effect, contact effects and interface traps on multiple trapping and release (MTR) carrier transport. Incorporating of short channel effect, contact resistance, effective mobility are both verified by experimental results under different channel length. Meanwhile, characteristic curves and significant device targets between experiment and compact model have an excellent agreement which highlights the effectivity of our compact model. Furthermore, it enables an accurate prediction and benchmark for flexible and logic circuit design, even presents a great potential as a practical tool to evaluate the future a-IGZO based 3D monolithic integration technology and logic-in-memory IC design.

CHAPTER 8 FUTURE WORK

8.1 Gate Leakage Current model

Gate induced drain leakage (GIDL) effect is that when the device is operating at off state, the gate is loaded with a negative bias, and the drain is loaded with a larger positive bias. On the one hand, the heavily doped region of the drain and pn junction formed by the substrate are in a reverse bias state. When the drain voltage is larger, a wider depletion region is formed around the drain region. On the other hand, when the absolute value of the negative gate bias voltage is large, the value of the two-dimensional superimposed potential near the drain is very large, which causes the electrons to undergo inter-band tunneling as shown on the right side of the figure, that is, the valence band Under the action of the strong electric field near the drain, the electrons in the ion tunnel directly from the valence band to the conduction band of the drain region with the assistance of the defect state, forming a GIDL current.

$$E_S = \frac{V_{DG} - E_g/q}{k \cdot T_{ox}} \tag{30}$$

Where E_S is the vertical electrical field at the semiconductor surface, k is the ratio between the permittivity of drain material and that of gate dielectric. [22]

$$I_{GIDL} = A \cdot E_S \cdot \exp\left(-\frac{B}{E_S}\right) \tag{31}$$

$$B = \frac{\pi \cdot m^{*\frac{1}{2}} \cdot E_g^{\frac{2}{3}}}{2\sqrt{2} \cdot q \cdot h} \tag{32}$$

Here A is a pre-exponential constant and B is 21.3 MV/cm (assume $m^* = 0.2m_0$ for silicon)

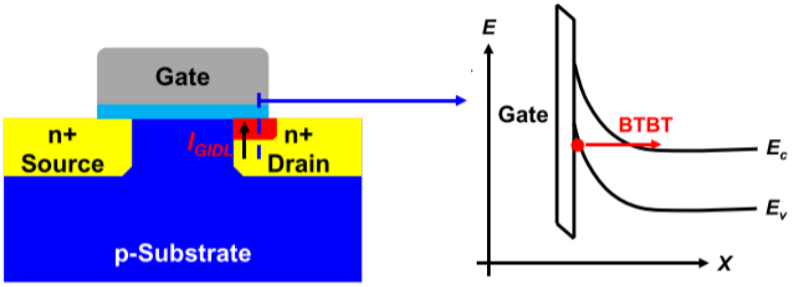

Fig. 8.1.1 Device and energy band structure of GIDL current.

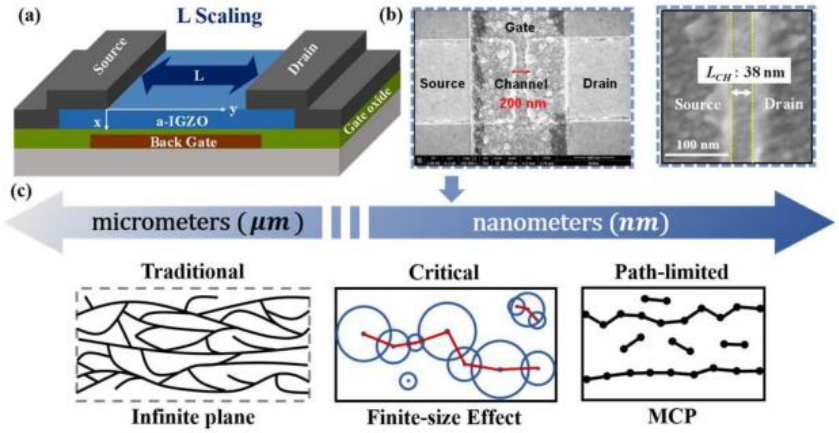

Fig. 8.2.1 (a) Schematic for a-IGZO TFT at nanoscale with bottom gate. (b) SEM images of the fabricated a-IGZO TFTs with the channel length at 200 nm and 38 nm, which used 10 nm HfO2 as the gate dielectric. (c) Schematic of the transition from traditional to critical and path-limited conduction as the channel length scaling. Critical transport is to introduce the relationship between the percolation threshold and the channel length into traditional PM. MCP conduction is suitable for ultra-scaled channel, and exhibits a path-limited feature and power-law T-dependence.

8.2 IGZO Compact Model in Nano-scale

As the size of TFT is reduced to nanometer scale, the influence of channel length on the percolation threshold can no longer be ignored. Therefore, based on the traditional percolation mechanism (PM), our model takes the finite-size effect into account properly. The channel length dependent characteristics are introduced into the variable range hopping (VRH) and percolation through the critical concentration. Regarding ultra-scaling effects, path-limited transport is supposed to dominate instead of spatial-energy coupling contribution. For a single percolation channel, the minimal number of concatenative bonds is 2L/α, as the boundary condition (BC). Therefore, a path-limited mobility is proposed, where α is much smaller for multiple channels. Particularly, this mobility shows a Mott-like T-dependence at the extreme point and power-law T-dependence otherwise. [23]

Fig. 8.2.1 represents the scaling down process from micron-scale to nano-scale clearly.

8.3 Computer Interpretation of IGZO Compact Model

After having established an accurate analytical model for the TFT, computer implementation for circuit simulation is not always easy. Several considerations including speed, convergence and even the way of translating different form of equations into computer language should be taken into consideration in this step. For a-Si TFTs, several SPICE models have been developed. Specifically, the model developed by Rensselaer Polytechnic Institute, also known as the RPI model, has become a commercialized standard supported by many simulation platforms including SmartSpice, HSPICE and Spectre, etc. However, CAD of organic and metal-oxide TFTs is yet to become a standard due to the rapid and ongoing evolution in materials and device structures. In fact, and as mentioned previously, there is a quest for unifying the TFT model to meet simulation requirements of TFTs with ever changing structures and materials. It is important to understand the benefits and drawbacks of SPICE and Verilog-A, while developing a device model to be used in further circuit simulation and system design. [24]

TABLE VI
COMPARISON BETWEEN DIFFERENT MODEL LANGUAGES

	SPICE	Spectre CMI	Verilog-AMS
Language	C/Fortan	C	Verilog
Language level	Low	Low	High
Easy to use	No	NO	Yes
Efficiency & Speed	High	High	Low
Complexity	High	High	Low
Simulator information needed for developers	Simulation algorithm & limitations	Simulator limitation on equations	None
Users	Spice developers	CAD engineers, Cadence Programmers	End users

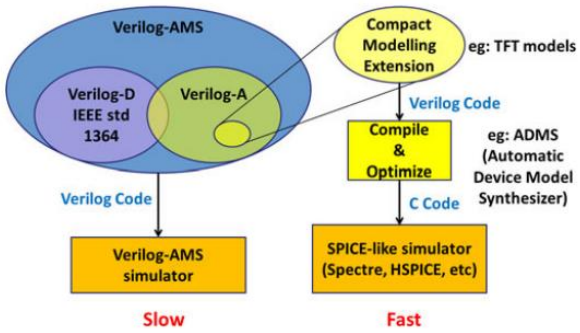

Fig. 8.3.1 Circuit design and simulation flow in Cadence Design Environment.

The short channel a-IGZO compact model can be packaged into manager library in Cadence Virtuoso described by Verilog-A language, and make future circuit simulation and design. For example, due to the flexibility and transparency properties of amorphous oxide semiconductor material, it can be used to design flexible circuit and display arrays. Also, the moderate transconductance shows a good possibility for a-IGZO device to be used in analog integrated circuit design such as single amplifier optimization. Meanwhile, it has a good potential for 3D monolithic integration as the interlayer, which would make great contributions to future logic-in-memory circuit.

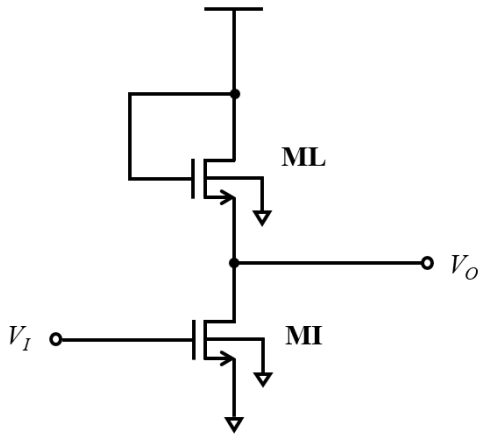

Fig. 8.3.2 Schematic of IGZO TFT NMOS inverter.

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