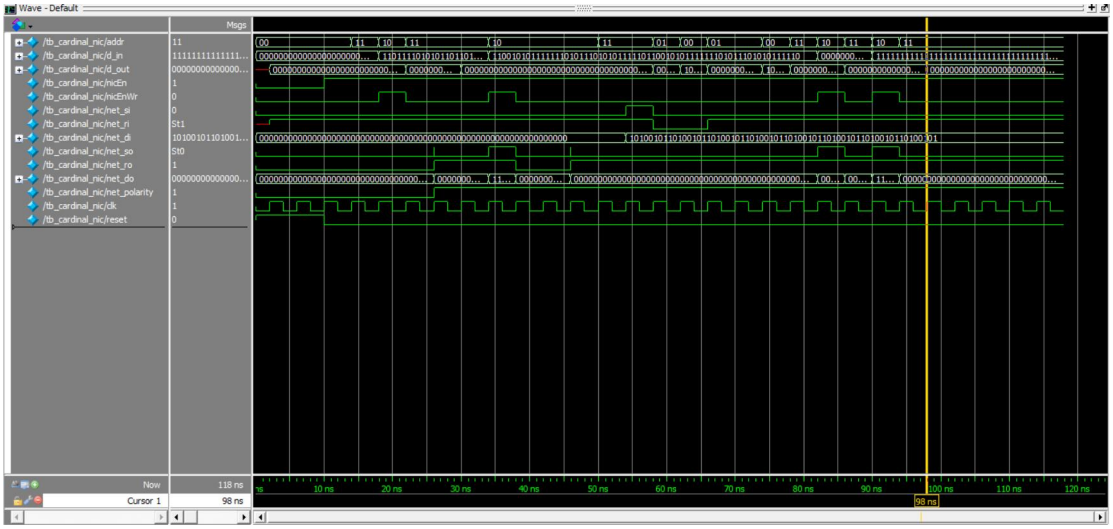
Project Phase1 NIC Report

Waveform:



Test case reset: 0 ns - 14 ns

net_ri is high and the NIC has cleared its buffers。

Test case NIC-Router handshake (non-blocking): 14 ns - 38ns

At 14 ns, initial output status is read (expected to be 0).
A store to the output buffer occurs around 18 ns.
Status is checked by 22 ns.
With net_ro and net_polarity asserted, the packet is sent by 26–30 ns.
Final output status verification is done around 34 ns.

Test case NIC-Router handshake (blocking): 38 ns - 58ns

A packet is stored into the output buffer at 38 ns.
Router is kept not ready (blocking) until around 46 ns.
Once net_ro is asserted at 46 ns, the packet is sent by 50 ns.
Output status is verified around 54 ns.

Test case processor load operation (buffer available): 58 ns - 78 ns

At 58 ns, a packet is sent from the router (via net_si).
Input status is read around 62 ns (should be high).
The packet is read from the input buffer around 66 ns, which clears the flag.
Status is rechecked around 70 ns.

Test case processor load operation (buffer unavailable): 78 ns - 90 ns

With no new packet arriving, input status is read between 78 ns and 90 ns.
The data read is undefined or retains the previous value.

Test case processor store operation (buffer available): 90 ns - 104 ns

At 90 ns, output status is verified.

A store occurs at 94 ns with a new packet.

Output status is read again around 98 ns.

Test case processor store operation (buffer available): 104 ns - 118 ns

An attempt to store a new packet is made at 104 ns while the output buffer is still full.

Output status is checked around 108 ns and remains 1, confirming that the write is ignored.