

LogiCORE IP Endpoint Block Plus v1.15 for PCI Express

User Guide

UG341 June 22, 2011



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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/23/06	1.1	Initial Xilinx release.
2/15/07	2.0	Update core to version 1.2; Xilinx tools 9.1i.
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About This Guide

This user guide describes the function and operation of the Endpoint Block Plus for PCI Express® (PCIe®) core, including how to design, customize, and implement the core.

Contents

This guide contains these chapters and appendices:

- [Chapter 1, Introduction](#), describes the core and related information, including recommended design experience, additional resources, technical support, and submitting feedback to Xilinx.
- [Chapter 2, Core Overview](#), describes the main components of the Block Plus core architecture.
- [Chapter 3, Quick Start Example Design](#), provides instructions for quickly generating, simulating, and implementing the example design using the demonstration test bench.
- [Chapter 4, Generating and Customizing the Core](#), describes how to use the graphical user interface to configure the Endpoint Block Plus using the CORE Generator™ software.
- [Chapter 5, Designing with the Core](#), provides instructions on how to design a device using the Endpoint Block Plus core.
- [Chapter 6, Core Constraints](#), discusses the required and optional constraints for the Endpoint Block Plus core.
- [Chapter 7, Hardware Verification](#), provides information on PCI Express systems tested by Xilinx.
- [Chapter 8, FPGA Configuration](#), describes FPGA configuration requirements.
- [Chapter 9, Known Restrictions](#), details known issues related to the integrated block and the transceivers.
- [Appendix A, Programmed Input Output Example Design](#), describes the Programmed Input Output (PIO) example design for use with the core.
- [Appendix B, Root Port Model Test Bench](#), describes the test bench environment, which provides a test program interface for use with the PIO example design.
- [Appendix C, Migration Considerations](#), defines the differences in behaviors and options between the Block Plus and the Endpoint for PCI Express (versions 3.5 and earlier).
- [Appendix D, Additional Design Considerations](#), defines additional considerations when implementing the example design.

Additional Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website at:

<http://www.xilinx.com/support>

For a glossary of technical terms used in Xilinx documentation, see:

http://www.xilinx.com/support/documentation/sw_manuals/glossary.pdf.

List of Acronyms

This section defines the acronyms used in this document.

Acronym	Definition
ASPM	Active State Power Management
BAR	Base Address Register
CMIO	Configuration Mapped Input Output
CRC	Cyclic Redundancy Check
DLLP	Data Link Layer Packet
DSN	Device Serial Number
DWORD, DW	Doubleword (four bytes)
ECRC	End-to-end CRC
LCRC	Link CRC
LTSSM	Link Training and Status State Machine
MMIO	Memory Mapped Input Output
MSI	Message Signaled Interrupt
PCI	Peripheral Component Interconnect
PIO	Programmed Input Output
PM	Power Management
PPM	Programmed Power Management
QWORD, QW	Quadword (eight bytes)
RCB	Read Completion Boundary
TL	Transaction Layer
TLP	Transaction Layer Packet
TPI	Test Programming Interface
UCF	User Constraints File

Introduction

This chapter introduces the Endpoint Block Plus for PCI Express® and provides related information including system requirements, recommended design experience, additional core resources, technical support, and submitting feedback to Xilinx.

About the Core

The Endpoint Block Plus for PCIe® solution from Xilinx is a reliable, high-bandwidth, scalable serial interconnect building block for use with the Virtex®-5 LXT, SXT, FXT, and TXT FPGA architecture. The core instantiates the Virtex-5 FPGA Integrated Block for PCI Express found in Virtex-5 LXT, SXT, FXT, and TXT families, and supports both Verilog-HDL and VHDL.

The Endpoint Block Plus core is a Xilinx® LogiCORE™ IP core, included in the latest IP Update on the Xilinx IP Center. For detailed information about the core, see the Endpoint for Block Plus [product page](#).

A license is not required to use the Endpoint Block Plus for PCI Express core. The core is provided under the terms of the [Xilinx End User Agreement](#).

Designs Using RocketIO Transceivers

RocketIO™ transceivers are defined by device family in this way:

- For Virtex-5 LXT and SXT FPGAs, RocketIO GTP transceivers
- For Virtex-5 FXT and TXT FPGAs, RocketIO GTX transceivers

Supported Tools and System Requirements

Operating System Requirements

For a list of system requirements, see the [ISE Design Suite 13: Release Notes Guide](#).

Tools

- ISE® v13.2 software
- Verification/Simulation

Table 1-1 lists the tools and their respective versions for the 13.2 release.

Table 1-1: Tools and Versions for 13.2

Tools	Version
ISE/XST	13.2
ISim	13.2
Synopsys Synplify PRO	E-2011.03
Mentor Graphics ModelSim	6.6d
Cadence IES	10.2
Synopsys VCS and VCS MX	2010.06

Recommended Design Experience

Although the Block Plus core is a fully verified solution, the challenge associated with implementing a complete design varies depending on the configuration and functionality of the application. For best results, previous experience building high-performance, pipelined FPGA designs using Xilinx implementation software and User Constraints Files (UCFs) is recommended.

Additional Core Resources

For detailed information and updates about the Endpoint Block Plus core, see:

- [Virtex-5 FPGA Endpoint Block Plus for PCI Express](#) documentation page
 - *LogiCORE IP Endpoint Block Plus for PCI Express Data Sheet*
 - *LogiCORE IP Endpoint Block Plus for PCI Express Release Notes*
- [UG197, Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide](#)

Additional information and resources related to the PCI Express technology are available from these websites:

- [PCI Express at PCI-SIG](#)
- [PCI Express Developer's Forum](#)

Technical Support

For technical support, go to www.xilinx.com/support. Questions are routed to a team of engineers with expertise using the Endpoint Block Plus for PCIe core.

Xilinx will provide technical support for use of this product as described in the *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide*. Xilinx cannot guarantee timing, functionality, or support of this product for designs that do not follow these guidelines.

Feedback

Xilinx welcomes comments and suggestions about the core and the accompanying documentation.

Core

For comments or suggestions about the core, submit a WebCase from www.xilinx.com/support. Be sure to include this information:

- Product name
- Core version number
- Explanation of your comments

Document

For comments or suggestions about this document, submit a WebCase from www.xilinx.com/support. Be sure to include this information:

- Document title
- Document number
- Page number(s) to which your comments refer
- Explanation of your comments

Core Overview

This chapter describes the main components of the Endpoint Block Plus for PCI Express® core architecture.

Overview

[Table 2-1](#) defines the Endpoint Block Plus for PCIe® solutions.

Table 2-1: Product Overview

Product Name	FPGA Architecture	User Interface Width	Lane Widths Supported	PCI Express Base Specification Compliance
1-lane Endpoint Block Plus	Virtex-5	64	x1	v1.1
2-lane Endpoint Block Plus	Virtex-5	64	x1, x2 ¹	v1.1
4-lane Endpoint Block Plus	Virtex-5	64	x1, x2, x4 ¹	v1.1
8-lane Endpoint Block Plus	Virtex-5	64	x1, x2, x4, x8 ¹	v1.1

1. See [Link Training: 2-Lane, 4-Lane and 8-Lane Endpoints](#) for additional information.

The Endpoint Block Plus core internally instances the Virtex®-5 FPGA Integrated Endpoint Block. See *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide* ([UG197](#)) for information about the internal architecture of the block. The integrated block follows the *PCI Express Base Specification* layering model, which consists of the Physical, Data Link, and Transaction Layers.

[Figure 2-1](#) illustrates the interfaces to the core, as defined below:

- System (SYS) interface
- PCI Express (PCI_EXP) interface
- Configuration (CFG) interface
- Transaction (TRN) interface

The core uses packets to exchange information between the various modules. Packets are formed in the Transaction and Data Link Layers to carry information from the transmitting component to the receiving component. Necessary information is added to the packet being transmitted, which is required to handle the packet at those layers. At the receiving end, each layer of the receiving element processes the incoming packet, strips the relevant information and forwards the packet to the next layer.

As a result, the received packets are transformed from their Physical Layer representation to their Data Link Layer representation and the Transaction Layer representation.

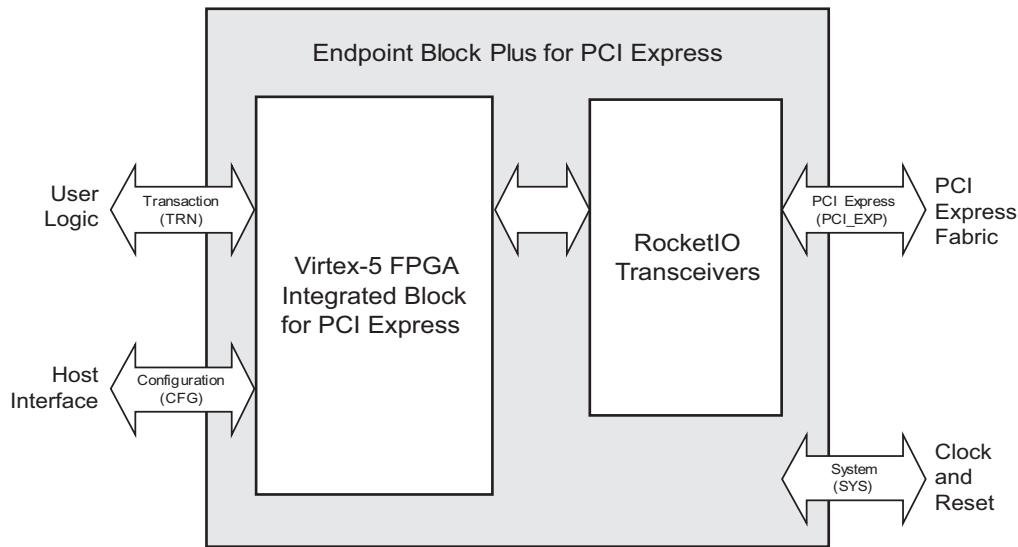


Figure 2-1: Top-Level Functional Blocks and Interfaces

Protocol Layers

The functions of the protocol layers, as defined by the *PCI Express Base Specification*, include generation and processing of Transaction Layer Packets (TLPs), flow control management, initialization and power management, data protection, error checking and retry, physical link interface initialization, maintenance and status tracking, serialization, deserialization, and other circuitry for interface operation. Each layer is defined below.

Transaction Layer

The Transaction Layer is the upper layer of the PCI Express architecture, and its primary function is to accept, buffer, and disseminate Transaction Layer packets or TLPs. TLPs communicate information through the use of memory, I/O, configuration, and message transactions. To maximize the efficiency of communication between devices, the Transaction Layer enforces PCI compliant Transaction ordering rules and manages TLP buffer space via credit-based flow control.

Data Link Layer

The Data Link Layer acts as an intermediate stage between the Transaction Layer and the Physical Layer. Its primary responsibility is to provide a reliable mechanism for the exchange of TLPs between two components on a link.

Services provided by the Data Link Layer include data exchange (TLPs), error detection and recovery, initialization services and the generation and consumption of Data Link Layer Packets (DLLPs). DLLPs are used to transfer information between Data Link Layers of two directly connected components on the link. DLLPs convey information such as Power Management, Flow Control, and TLP acknowledgments.

Physical Layer

The Physical Layer interfaces the Data Link Layer with signalling technology for link data interchange, and is subdivided into the Logical sub-block and the Electrical sub-block.

- The Logical sub-block is responsible for framing and de-framing of TLPs and DLLPs. It also implements the Link Training and Status State machine (LTSSM) which handles link initialization, training, and maintenance. Scrambling, descrambling, and 8B/10B encoding and decoding of data is also performed in this sub-block.
- The Electrical sub-block defines the input and output buffer characteristics that interfaces the device to the PCIe link.

The Physical Layer also supports Lane Reversal (for multi-lane designs) and Lane Polarity Inversion, as indicated in the *PCI Express Base Specification rev 1.1* requirement.

Configuration Management

The Configuration Management layer maintains the PCI™ Type0 Endpoint configuration space and supports these features:

- Implements PCI Configuration Space
- Supports Configuration Space accesses
- Power Management functions
- Implements error reporting and status functionality
- Implements packet processing functions
 - Receive
 - Configuration Reads and Writes
 - Transmit
 - Completions with or without data
 - TLM Error Messaging
 - User Error Messaging
 - Power Management Messaging/Handshake
- Implements MSI and INTx interrupt emulation
- Implements the Device Serial Number Capability in the PCIe Extended Capability space

PCI Configuration Space

The configuration space consists of three primary parts, illustrated in [Table 2-4](#). These include:

- Legacy PCI v3.0 Type 0 Configuration Header
- Legacy Extended Capability Items
 - PCIe Capability Item
 - Power Management Capability Item
 - Message Signaled Interrupt Capability Item
- PCIe Extended Capabilities
 - Device Serial Number Extended Capability Structure

The core implements three legacy extended capability items. The remaining legacy extended capability space from address 0x6C to 0xFF is reserved. The core returns 0x00000000 when this address range is read.

The core also implements one PCIe Extended Capability. The remaining PCIe Extended Capability space from addresses 0x10C to 0xFFFF is reserved. The core returns 0x00000000 for reads to this range; writes are ignored.

Table 2-2: PCI Configuration Space Header

31	16	15	0		
Device ID			000h		
Status			004h		
Class Code			008h		
BIST	Header	Lat Timer	Cache Ln		
Base Address Register 0					
Base Address Register 1					
Base Address Register 2					
Base Address Register 3					
Base Address Register 4					
Base Address Register 5					
Cardbus CIS Pointer					
Subsystem ID		Subsystem Vendor ID			
Expansion ROM Base Address					
Reserved			CapPtr		
Reserved					
Max Lat	Min Gnt	Intr Pin	Intr Line		
PM Capability		NxtCap	PM Cap		
Data	BSE	PMCSR			
MSI Control		NxtCap	MSI Cap		
Message Address (Lower)					
Message Address (Upper)					
Reserved	Message Data				
Reserved Legacy Configuration Space (Returns 0x00000000)					
PE Capability		NxtCap	PE Cap		
PCI Express Device Capabilities					
Device Status		Device Control			
PCI Express Link Capabilities					
Link Status		Link Control			
Reserved Legacy Configuration Space (Returns 0x00000000)					
Next Cap	Cap. Ver.	PCI Express Capability			
PCI Express Device Serial Number (1st)					
PCI Express Device Serial Number (2nd)					
Reserved Extended Configuration Space (Returns 0x00000000)					

Core Interfaces

The Endpoint Block Plus core for PCIe includes top-level signal interfaces that have sub-groups for the receive direction, transmit direction, and signals common to both directions.

System Interface

The System (SYS) interface consists of the system reset signal, `sys_reset_n`, the system clock signal, `sys_clk`, and a free running reference clock output signal, `refclkout`, as described in [Table 2-3](#).

Table 2-3: System Interface Signals

Function	Signal Name	Direction	Description
System Reset	<code>sys_reset_n</code>	Input	An asynchronous input (active Low) signal reset from the root complex/system that places the Endpoint in a known initial state. Note: <code>sys_reset_n</code> can be tied deasserted in certain form factors where a global reset signal is unavailable. In this case, the core sees a warm reset only on device power-on and can be subsequently reset by the connected downstream port utilizing the in-band hot reset mechanism.
System Clock	<code>sys_clk</code>	Input	Reference clock: 100 MHz or 250 MHz.
Reference Clock	<code>refclkout</code>	Output	A free-running reference clock output, based on the reference clock.

The system reset signal is an asynchronous active-Low input. The assertion of `sys_reset_n` causes a hard reset of the entire core. The system input clock must be either 100 MHz or 250 MHz, as selected in the CORE Generator™ tool GUI. For important information about resetting and clocking the Endpoint Block Plus core, see [Clocking and Reset of the Block Plus Core, page 131](#) and the *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide (UG197)*.

PCI Express Interface

The PCI Express (PCI_EXP) interface consists of differential transmit and receive pairs organized in multiple lanes. A PCI Express lane consists of a pair of transmit differential signals {`pci_exp_txp`, `pci_exp_txn`} and a pair of receive differential signals {`pci_exp_rxp`, `pci_exp_rxn`}. The 1-lane core supports only Lane 0, the 2-lane core supports lanes 0-1, the 4-lane core supports lanes 0-3, and the 8-lane core supports lanes 0-7. Transmit and receive signals of the PCI_EXP interface are defined in [Tables 2-4, 2-5, 2-6, and 2-7](#).

Table 2-4: PCI Express Interface Signals for the 1-Lane Endpoint Core

Lane Number	Name	Direction	Description
0	pci_exp_txp0	Output	PCI Express Transmit Positive: Serial Differential Output 0 (+)
0	pci_exp_txn0	Output	PCI Express Transmit Negative: Serial Differential Output 0 (-)
0	pci_exp_rxp0	Input	PCI Express Receive Positive: Serial Differential Input 0 (+)
0	pci_exp_rxn0	Input	PCI Express Receive Negative: Serial Differential Input 0 (-)

Table 2-5: PCI Express Interface Signals for the 2-Lane Endpoint Core

Lane Number	Name	Direction	Description
0	pci_exp_txp0	Output	PCI Express Transmit Positive: Serial Differential Output 0 (+)
0	pci_exp_txn0	Output	PCI Express Transmit Negative: Serial Differential Output 0 (-)
0	pci_exp_rxp0	Input	PCI Express Receive Positive: Serial Differential Input 0 (+)
0	pci_exp_rxn0	Input	PCI Express Receive Negative: Serial Differential Input 0 (-)
1	pci_exp_txp1	Output	PCI Express Transmit Positive: Serial Differential Output 1 (+)
1	pci_exp_txn1	Output	PCI Express Transmit Negative: Serial Differential Output 1 (-)
1	pci_exp_rxp1	Input	PCI Express Receive Positive: Serial Differential Input 1 (+)
1	pci_exp_rxn1	Input	PCI Express Receive Negative: Serial Differential Input 1 (-)

Table 2-6: PCI Express Interface Signals for the 4-Lane Endpoint Core

Lane Number	Name	Direction	Description
0	pci_exp_txp0	Output	PCI Express Transmit Positive: Serial Differential Output 0 (+)
0	pci_exp_txn0	Output	PCI Express Transmit Negative: Serial Differential Output 0 (-)
0	pci_exp_rxp0	Input	PCI Express Receive Positive: Serial Differential Input 0 (+)

Table 2-6: PCI Express Interface Signals for the 4-Lane Endpoint Core (Cont'd)

Lane Number	Name	Direction	Description
0	pci_exp_rxn0	Input	PCI Express Receive Negative: Serial Differential Input 0 (-)
1	pci_exp_txp1	Output	PCI Express Transmit Positive: Serial Differential Output 1 (+)
1	pci_exp_txn1	Output	PCI Express Transmit Negative: Serial Differential Output 1 (-)
1	pci_exp_rxp1	Input	PCI Express Receive Positive: Serial Differential Input 1 (+)
1	pci_exp_rxn1	Input	PCI Express Receive Negative: Serial Differential Input 1 (-)
2	pci_exp_txp2	Output	PCI Express Transmit Positive: Serial Differential Output 2 (+)
2	pci_exp_txn2	Output	PCI Express Transmit Negative: Serial Differential Output 2 (-)
2	pci_exp_rxp2	Input	PCI Express Receive Positive: Serial Differential Input 2 (+)
2	pci_exp_rxn2	Input	PCI Express Receive Negative: Serial Differential Input 2 (-)
3	pci_exp_txp3	Output	PCI Express Transmit Positive: Serial Differential Output 3 (+)
3	pci_exp_txn3	Output	PCI Express Transmit Negative: Serial Differential Output 3 (-)
3	pci_exp_rxp3	Input	PCI Express Receive Positive: Serial Differential Input 3 (+)
3	pci_exp_rxn3	Input	PCI Express Receive Negative: Serial Differential Input 3 (-)

Table 2-7: PCI Express Interface Signals for the 8-Lane Endpoint Core

Lane Number	Name	Direction	Description
0	pci_exp_txp0	Output	PCI Express Transmit Positive: Serial Differential Output 0 (+)
0	pci_exp_txn0	Output	PCI Express Transmit Negative: Serial Differential Output 0 (-)
0	pci_exp_rxp0	Input	PCI Express Receive Positive: Serial Differential Input 0 (+)
0	pci_exp_rxn0	Input	PCI Express Receive Negative: Serial Differential Input 0 (-)

Table 2-7: PCI Express Interface Signals for the 8-Lane Endpoint Core (Cont'd)

Lane Number	Name	Direction	Description
1	pci_exp_txp1	Output	PCI Express Transmit Positive: Serial Differential Output 1 (+)
1	pci_exp_txn1	Output	PCI Express Transmit Negative: Serial Differential Output 1 (-)
1	pci_exp_rxp1	Input	PCI Express Receive Positive: Serial Differential Input 1 (+)
1	pci_exp_rxn1	Input	PCI Express Receive Negative: Serial Differential Input 1 (-)
2	pci_exp_txp2	Output	PCI Express Transmit Positive: Serial Differential Output 2 (+)
2	pci_exp_txn2	Output	PCI Express Transmit Negative: Serial Differential Output 2 (-)
2	pci_exp_rxp2	Input	PCI Express Receive Positive: Serial Differential Input 2 (+)
2	pci_exp_rxn2	Input	PCI Express Receive Negative: Serial Differential Input 2 (-)
3	pci_exp_txp3	Output	PCI Express Transmit Positive: Serial Differential Output 3 (+)
3	pci_exp_txn3	Output	PCI Express Transmit Negative: Serial Differential Output 3 (-)
3	pci_exp_rxp3	Input	PCI Express Receive Positive: Serial Differential Input 3 (+)
3	pci_exp_rxn3	Input	PCI Express Receive Negative: Serial Differential Input 3 (-)
4	pci_exp_txp4	Output	PCI Express Transmit Positive: Serial Differential Output 4 (+)
4	pci_exp_txn4	Output	PCI Express Transmit Negative: Serial Differential Output 4 (-)
4	pci_exp_rxp4	Input	PCI Express Receive Positive: Serial Differential Input 4 (+)
4	pci_exp_rxn4	Input	PCI Express Receive Negative: Serial Differential Input 4 (-)
5	pci_exp_txp5	Output	PCI Express Transmit Positive: Serial Differential Output 5 (+)
5	pci_exp_txn5	Output	PCI Express Transmit Negative: Serial Differential Output 5 (-)
5	pci_exp_rxp5	Input	PCI Express Receive Positive: Serial Differential Input 5 (+)
5	pci_exp_rxn5	Input	PCI Express Receive Negative: Serial Differential Input 5 (-)

Table 2-7: PCI Express Interface Signals for the 8-Lane Endpoint Core (Cont'd)

Lane Number	Name	Direction	Description
6	pci_exp_txp6	Output	PCI Express Transmit Positive: Serial Differential Output 6 (+)
6	pci_exp_txn6	Output	PCI Express Transmit Negative: Serial Differential Output 6 (-)
6	pci_exp_rxp6	Input	PCI Express Receive Positive: Serial Differential Input 6 (+)
6	pci_exp_rxn6	Input	PCI Express Receive Negative: Serial Differential Input 6 (-)
7	pci_exp_txp7	Output	PCI Express Transmit Positive: Serial Differential Output 7 (+)
7	pci_exp_txn7	Output	PCI Express Transmit Negative: Serial Differential Output 7 (-)
7	pci_exp_rxp7	Input	PCI Express Receive Positive: Serial Differential Input 7 (+)
7	pci_exp_rxn7	Input	PCI Express Receive Negative: Serial Differential Input 7 (-)

Transaction Interface

The Transaction (TRN) interface provides a mechanism for the user design to generate and consume TLPs. The signal names and signal descriptions for this interface are shown in [Tables 2-8, 2-9, and 2-10](#).

Common TRN Interface

[Table 2-8](#) defines and describes the common TRN interface signals.

Table 2-8: Common Transaction Interface Signals

Name	Direction	Description		
trn_clk	Output	Transaction Clock: Transaction and Configuration interface operations are referenced-to and synchronous-with the rising edge of this clock. trn_clk is unavailable when the core sys_reset_n is held asserted. trn_clk is guaranteed to be stable at the nominal operating frequency once the core deasserts trn_reset_n. The trn_clk clock output is a fixed frequency configured in the CORE Generator tool. trn_clk does not shift frequencies in case of link recovery or training down.	Recommended	Optional
		Product	Frequency (MHz)	Frequency (MHz)
		1-lane Endpoint Block Plus	62.5	125.0
		2-lane Endpoint Block Plus	125.0	250.0
		4-lane Endpoint Block Plus	125.0	250.0
		8-lane Endpoint Block Plus	250.0	125.0
trn_reset_n	Output	Transaction Reset: Active Low. User logic interacting with the Transaction and Configuration interfaces must use trn_reset_n to return to their quiescent states. trn_reset_n is deasserted synchronously with respect to trn_clk, trn_reset_n is deasserted and is asserted asynchronously with sys_reset_n assertion. trn_reset_n is not asserted for core in-band reset events like Hot Reset or Link Disable.		
trn_lnku_up_n	Output	Transaction Link Up: Active Low. Transaction link-up is asserted when the core and the connected upstream link partner port are ready and able to exchange data packets. Transaction link-up is deasserted when the core and link partner are attempting to establish communication, and when communication with the link partner is lost due to errors on the transmission channel. When the core is driven to Hot Reset and Link Disable states by the link partner, trn_lnku_up_n is deasserted and all TLPs stored in the Endpoint core are lost.		

Transmit TRN Interface

Table 2-9 defines the transmit (Tx) TRN interface signals.

Table 2-9: Transaction Transmit Interface Signals

Name	Direction	Description
trn_tsof_n	Input	Transmit Start-of-Frame (SOF): Active low. Signals the start of a packet. Valid only along with assertion of trn_tsrdy_n.
trn_teof_n	Input	Transmit End-of-Frame (EOF): Active low. Signals the end of a packet. Valid only along with assertion of trn_tsrdy_n.
trn_td[63:0]	Input	Transmit Data: Packet data to be transmitted.
trn_trem_n[7:0]	Input	Transmit Data Remainder: Valid only if both trn_teof_n, trn_tsrdy_n, and trn_tdst_rdy_n are asserted. Legal values are: <ul style="list-style-type: none"> • 0000_0000b = packet data on all of trn_td[63:0] • 0000_1111b = packet data only on trn_td[63:32]
trn_tsrdy_n	Input	Transmit Source Ready: Active low. Indicates that the User Application is presenting valid data on trn_td[63:0].
trn_tdst_rdy_n	Output	Transmit Destination Ready: Active low. Indicates that the core is ready to accept data on trn_td[63:0]. The simultaneous assertion of trn_tsrdy_n and trn_tdst_rdy_n marks the successful transfer of one data beat on trn_td[63:0].
trn_tsrdsc_n	Input	Transmit Source Discontinue: Can be asserted any time starting on the first cycle after SOF to EOF, inclusive.
trn_tdst_dsc_n	Output	Transmit Destination Discontinue: Active low. Indicates that the core is aborting the current packet. Asserted when the physical link is going into reset. Not supported; signal is tied high.
trn_tbuf_av[3:0]	Output	Transmit Buffers Available: Indicates transmit buffer availability in the core. Each bit of trn_tbuf_av corresponds to one of the following credit queues: <ul style="list-style-type: none"> • trn_tbuf_av[0] => Non Posted Queue • trn_tbuf_av[1] => Posted Queue • trn_tbuf_av[2] => Completion Queue • trn_tbuf_av[3] => Look-Ahead Completion Queue A value of 1 indicates that the core can accept at least 1 TLP of that particular credit class. A value of 0 indicates no buffer availability in the particular queue. trn_tbuf_av[3] indicates that the core might be about to run out of Completion Queue buffers. If this is deasserted, performance can be optimized by sending a Posted or Non-Posted TLP instead of a Completion TLP. If a Completion TLP is sent when this signal is deasserted, the core can be forced to stall the TRN interface for all TLP types, until new Completion Queue buffers become available.

Receive TRN Interface

[Table 2-10](#) defines the receive (Rx) TRN interface signals.

Table 2-10: Receive Transaction Interface Signals

Name	Direction	Description
trn_rsof_n	Output	Receive Start-of-Frame (SOF): Active low. Signals the start of a packet. Valid only if trn_rsrc_rdy_n is also asserted.
trn_reof_n	Output	Receive End-of-Frame (EOF): Active low. Signals the end of a packet. Valid only if trn_rsrc_rdy_n is also asserted.
trn_rd[63:0]	Output	Receive Data: Packet data being received. Valid only if trn_rsrc_rdy_n is also asserted.
trn_rrem_n[7:0]	Output	Receive Data Remainder: Valid only if both trn_reof_n, trn_rsrc_rdy_n, and trn_rdst_rdy_n are asserted. Legal values are: <ul style="list-style-type: none"> • 0000_0000b = packet data on all of trn_rd[63:0] • 0000_1111b = packet data only on trn_rd[63:32]
trn_rerrfwd_n	Output	Receive Error Forward: Active low. Marks the packet in progress as error poisoned. Asserted by the core for the entire length of the packet.
trn_rsrc_rdy_n	Output	Receive Source Ready: Active low. Indicates the core is presenting valid data on trn_rd[63:0]
trn_rdst_rdy_n	Input	Receive Destination Ready: Active low. Indicates the User Application is ready to accept data on trn_rd[63:0]. The simultaneous assertion of trn_rsrc_rdy_n and trn_rdst_rdy_n marks the successful transfer of one data beat on trn_td[63:0].
trn_rsrc_dsc_n	Output	Receive Source Discontinue: Active low. Indicates the core is aborting the current packet. Asserted when the physical link is going into reset. Not supported; signal is tied high.
trn_rnp_ok_n	Input	Receive Non-Posted OK: Active low. The User Application asserts trn_rnp_ok_n when it is ready to accept a Non-Posted Request packet. When asserted, packets are presented to the user application in the order they are received unless trn_rcpl_streaming_n is asserted. When the User Application approaches a state where it is unable to service Non-Posted Requests, it must deassert trn_rnp_ok_n one clock cycle before the core presents EOF of the next-to-last Non-Posted TLP the User Application can accept allowing Posted and Completion packets to bypass Non-Posted packets in the inbound queue.

Table 2-10: Receive Transaction Interface Signals (Cont'd)

Name	Direction	Description
trn_rcpl_streaming_n	Input	Receive Completion Streaming: Active low. Asserted to enable Upstream Memory Read transmission without the need for throttling. See Performance Considerations on the Receive Transaction Interface, page 107 for details.
trn_rbar_hit_n[6:0]	Output	Receive BAR Hit: Active low. Indicates BAR(s) targeted by the current receive transaction. trn_rbar_hit_n[0] => BAR0 trn_rbar_hit_n[1] => BAR1 trn_rbar_hit_n[2] => BAR2 trn_rbar_hit_n[3] => BAR3 trn_rbar_hit_n[4] => BAR4 trn_rbar_hit_n[5] => BAR5 trn_rbar_hit_n[6] => Expansion ROM Address. If two BARs are configured into a single 64-bit address, both corresponding trn_rbar_hit_n bits are asserted.
trn_rfc_ph_av[7:0] ¹	Output	Receive Posted Header Flow Control Credits Available: The number of Posted Header FC credits available to the remote link partner.
trn_rfc_pd_av[11:0] ¹	Output	Receive Posted Data Flow Control Credits Available: The number of Posted Data FC credits available to the remote link partner.
trn_rfc_nph_av[7:0] ¹	Output	Receive Non-Posted Header Flow Control Credits Available: Number of Non-Posted Header FC credits available to the remote link partner.
trn_rfc_npd_av[11:0] ¹	Output	Receive Non-Posted Data Flow Control Credits Available: Number of Non-Posted Data FC credits available to the remote link partner. Always 0 as a result of advertising infinite initial data credits.

1. Credit values given to the user are instantaneous quantities, not the cumulative (from time zero) values seen by the remote link partner.

Configuration Interface

The Configuration (CFG) interface enables the user design to inspect the state of the Endpoint for PCIe configuration space. The user provides a 10-bit configuration address, which selects one of the 1024 configuration space double word (DWORD) registers. The Endpoint returns the state of the selected register over the 32-bit data output port.

[Table 2-11](#) defines the Configuration interface signals. See [Accessing Configuration Space Registers, page 111](#) for usage.

Table 2-11: Configuration Interface Signals

Name	Direction	Description
cfg_do[31:0]	Output	Configuration Data Out: A 32-bit data output port used to obtain read data from the configuration space inside the core.
cfg_rd_wr_done_n	Output	<p>Configuration Read Write Done: Active low. The read-write done signal indicates a successful completion of the user configuration register access operation.</p> <p>For a user configuration register read operation, the signal validates the cfg_do[31:0] data-bus value. In the event of an unsuccessful read operation (cfg_rd_wr_done_n does not assert within 10 clock cycles) user logic must assume the transaction has failed and must re-initiate the transaction.</p> <p>cfg_rd_wr_done_n is not supported for writes to the Configuration space (optional feature).¹</p>
cfg_di[31:0]	Input	Configuration Data In: 32-bit data input port used to provide write data to the configuration space inside the core. Optionally supported. ¹
cfg_dwaddr[9:0]	Input	Configuration DWORD Address: A 10-bit address input port used to provide a configuration register DWORD address during configuration register accesses.
cfg_wr_en_n	Input	Configuration Write Enable: Active-low write-enable for configuration register access. Optionally supported. ¹
cfg_rd_en_n	Input	<p>Configuration Read Enable: Active low read-enable for configuration register access. Only supported after 20 clock cycles after trn_lnk_up_n assertion.</p> <p>Note: cfg_rd_en_n must be asserted for no more than 1 trn_clk cycle at a time. Parking this signal asserted blocks updates to internal registers. Only assert when needed.</p>
cfg_byte_en_n[3:0]	Input	Configuration Byte Enable: Active-low byte enables for configuration register access signal. Optionally supported. ¹

Table 2-11: Configuration Interface Signals (Cont'd)

Name	Direction	Description										
cfg_interrupt_n	Input	Configuration Interrupt: Active-Low interrupt-request signal. The User Application can assert this to cause appropriate interrupt messages to be transmitted by the core.										
cfg_interrupt_rdy_n	Output	Configuration Interrupt Ready: Active-Low interrupt grant signal. Assertion on this signal indicates that the core has successfully transmitted the appropriate interrupt message.										
cfg_interrupt_mmenable[2:0]	Output	Configuration Interrupt Multiple Message Enable: This is the value of the Multiple Message Enable field. Values range from 000b to 101b. A value of 000b indicates that single vector MSI is enabled, while other values indicate the number of bits that can be used for multi-vector MSI.										
cfg_interrupt_msienable	Output	Configuration Interrupt MSI Enabled: Indicates that the Message Signaling Interrupt (MSI) messaging is enabled. If 0, then only Legacy (INTx) interrupts can be sent.										
cfg_interrupt_di[7:0]	Input	<p>Configuration Interrupt Data In: For Message Signaling Interrupts (MSI), the portion of the Message Data that the Endpoint must drive to indicate MSI vector number, if Multi-Vector Interrupts are enabled. The value indicated by cfg_interrupt_mmenable[2:0] determines the number of lower-order bits of Message Data that the Endpoint provides; the remaining upper bits of cfg_interrupt_di[7:0] are not used. For Single-Vector Interrupts, cfg_interrupt_di[7:0] is not used. For Legacy interrupt messages (Assert_INTx, Deassert_INTx), the following list defines the type of message to be sent:</p> <table> <thead> <tr> <th>Value</th> <th>Legacy Interrupt</th> </tr> </thead> <tbody> <tr> <td>00h</td> <td>INTA</td> </tr> <tr> <td>01h</td> <td>INTB</td> </tr> <tr> <td>02h</td> <td>INTC</td> </tr> <tr> <td>03h</td> <td>INTD</td> </tr> </tbody> </table>	Value	Legacy Interrupt	00h	INTA	01h	INTB	02h	INTC	03h	INTD
Value	Legacy Interrupt											
00h	INTA											
01h	INTB											
02h	INTC											
03h	INTD											
cfg_interrupt_do[7:0]	Output	Configuration Interrupt Data Out: The value of the lowest 8 bits of the Message Data field in the Endpoint's MSI capability structure. This value is used in conjunction with cfg_interrupt_mmenable[2:0] to drive cfg_interrupt_di[7:0].										

Table 2-11: Configuration Interface Signals (Cont'd)

Name	Direction	Description						
cfg_interrupt_assert_n	Input	<p>Configuration Legacy Interrupt Assert/Deassert Select: Selects between Assert and Deassert messages for Legacy interrupts when cfg_interrupt_n is asserted. Not used for MSI interrupts.</p> <table> <thead> <tr> <th>Value</th><th>Message Type</th></tr> </thead> <tbody> <tr> <td>0</td><td>Assert</td></tr> <tr> <td>1</td><td>Deassert</td></tr> </tbody> </table>	Value	Message Type	0	Assert	1	Deassert
Value	Message Type							
0	Assert							
1	Deassert							
cfg_to_turnoff_n	Output	Configuration To Turnoff: Notifies the user that a PME_TURN_Off message has been received and the main power will soon be removed.						
cfg_bus_number[7:0]	Output	Configuration Bus Number: Provides the assigned bus number for the device. The User Application must use this information in the Bus Number field of outgoing TLP requests. Default value after reset is 00h. Refreshed whenever a Type 0 Configuration packet is received.						
cfg_device_number[4:0]	Output	Configuration Device Number: Provides the assigned device number for the device. The User Application must use this information in the Device Number field of outgoing TLP requests. Default value after reset is 00000b. Refreshed whenever a Type 0 Configuration packet is received.						
cfg_function_number[2:0]	Output	Configuration Function Number: Provides the function number for the device. The User Application must use this information in the Function Number field of outgoing TLP request. Function number is hardwired to 000b.						
cfg_status[15:0]	Output	Configuration Status: Status register from the Configuration Space Header.						
cfg_command[15:0]	Output	Configuration Command: Command register from the Configuration Space Header.						
cfg_dstatus[15:0]	Output	Configuration Device Status: Device status register from the PCI Express Extended Capability Structure.						
cfg_dcommand[15:0]	Output	Configuration Device Command: Device control register from the PCI Express Extended Capability Structure.						
cfg_lstatus[15:0]	Output	Configuration Link Status: Link status register from the PCI Express Extended Capability Structure.						
cfg_lcommand[15:0]	Output	Configuration Link Command: Link control register from the PCI Express Extended Capability Structure.						

Table 2-11: Configuration Interface Signals (Cont'd)

Name	Direction	Description
cfg_pm_wake_n	Input	Configuration Power Management Wake: A one-clock cycle active low assertion signals the core to generate and send a Power Management Wake Event (PM_PME) Message TLP to the upstream link partner. Note: The user is required to assert this input only under stable link conditions as reported on the cfg_PCIE_link_state[2:0]. Assertion of this signal when the PCIe link is in transition results in incorrect behavior on the PCIe link.
cfg_PCIE_link_state_n[2:0]	Output	PCI Express Link State: One-hot encoded bus that reports the PCIe Link State Information to the user. 110b - PCI Express Link State is "L0" 101b - PCI Express Link State is "L0s" 011b - PCI Express Link State is "L1" 111b - PCI Express Link State is "in transition"
cfg_trn_pending_n	Input	User Transaction Pending: If asserted, sets the Transactions Pending bit in the Device Status Register. Note: The user is required to assert this input if the User Application has not received a completion to an upstream request.
cfg_dsn[63:0]	Input	Configuration Device Serial Number: Serial Number Register fields of the Device Serial Number extended capability.
fast_train_simulation_only	Input	Fast Train: Should only be asserted for simulation. PLL Lock counters are bypassed when the input is asserted (set to 1) to allow the simulation to train faster. Do not assert this input when using the core in hardware; doing so might cause link instability.

1. Writing to the configuration space through the user configuration port is optionally supported; See [Accessing Configuration Space Registers in Chapter 5](#) for more details.

Error Reporting Signals

[Table 2-12](#) defines the User Application error-reporting signals.

Table 2-12: User Application Error-Reporting Signals

Port Name	Direction	Description
cfg_err_ecrc_n	Input	ECRC Error Report: The user can assert this signal to report an ECRC error (end-to-end CRC).
cfg_err_ur_n	Input	Configuration Error Unsupported Request: The user can assert this signal to report that an unsupported request was received.

Table 2-12: User Application Error-Reporting Signals (Cont'd)

Port Name	Direction	Description
cfg_err_cpl_timeout_n	Input	<p>Configuration Error Completion Timeout: The user can assert this signal to report a completion timed out.</p> <p>Note: The user should assert this signal only if the device power state is D0. Asserting this signal in non-D0 device power states might result in an incorrect operation on the PCIe link. For additional information, see the <i>PCI Express Base Specification</i>, Rev.1.1, Section 5.3.1.2.</p>
cfg_err_cpl_unexpect_n	Input	Configuration Error Completion Unexpected: The user can assert this signal to report that an unexpected completion was received.
cfg_err_cpl_abort_n	Input	Configuration Error Completion Aborted: The user can assert this signal to report that a completion was aborted.
cfg_err_posted_n	Input	Configuration Error Posted: This signal is used to further qualify any of the cfg_err_* input signals. When this input is asserted concurrently with one of the other signals, it indicates that the transaction which caused the error was a posted transaction.
cfg_err_cor_n	Input	Configuration Error Correctable Error: The user can assert this signal to report that a correctable error was detected.
cfg_err_tlp_cpl_header[47:0]	Input	<p>Configuration Error TLP Completion Header: Accepts the header information from the user when an error is signaled. This information is required so that the core can issue a correct completion, if required.</p> <p>The following information should be extracted from the received error TLP and presented in the format below:</p> <ul style="list-style-type: none"> [47:41] Lower Address [40:29] Byte Count [28:26] TC [25:24] Attr [23:8] Requester ID [7:0] Tag

Table 2-12: User Application Error-Reporting Signals (Cont'd)

Port Name	Direction	Description
cfg_err_cpl_rdy_n	Output	<p>Configuration Error Completion Ready: When asserted, this signal indicates that the core can accept assertions on cfg_err_ur_n and cfg_err_cpl_abort_n for Non-Posted Transactions. Assertions on cfg_err_ur_n and cfg_err_cpl_abort_n are ignored when cfg_err_cpl_rdy_n is deasserted.</p>
cfg_err_locked_n	Input	<p>Configuration Error Locked: This signal is used to further qualify any of the cfg_err_* input signals. When this input is asserted concurrently with one of the other signals, it indicates that the transaction that caused the error was a locked transaction. This signal is intended to be used in Legacy mode. If the user needs to signal an unsupported request or an aborted completion for a locked transaction, this signal can be used to return a Completion Locked with UR or CA status. Note: When not in Legacy mode, the core automatically returns a Completion Locked, if appropriate.</p>

Quick Start Example Design

This chapter provides an overview of the Endpoint Block Plus for PCI Express® example design and instructions for generating the core. It also includes information about simulating and implementing the example design using the provided demonstration test bench.

Overview

The example simulation design consists of two discrete parts:

- The Root Port Model, a test bench that generates, consumes, and checks PCI Express bus traffic.
- The Programmed Input Output (PIO) example design, a completer application for PCI Express. The PIO example design responds to Read and Write requests to its memory space and can be synthesized for testing in hardware.

Simulation Design Overview

For the simulation design, transactions are sent from the Root Port Model to the Block Plus core and processed by the PIO example design. [Figure 3-1](#) illustrates the simulation design provided with the Block Plus core. For more information about the Root Port Model, see [Appendix B, Root Port Model Test Bench](#).

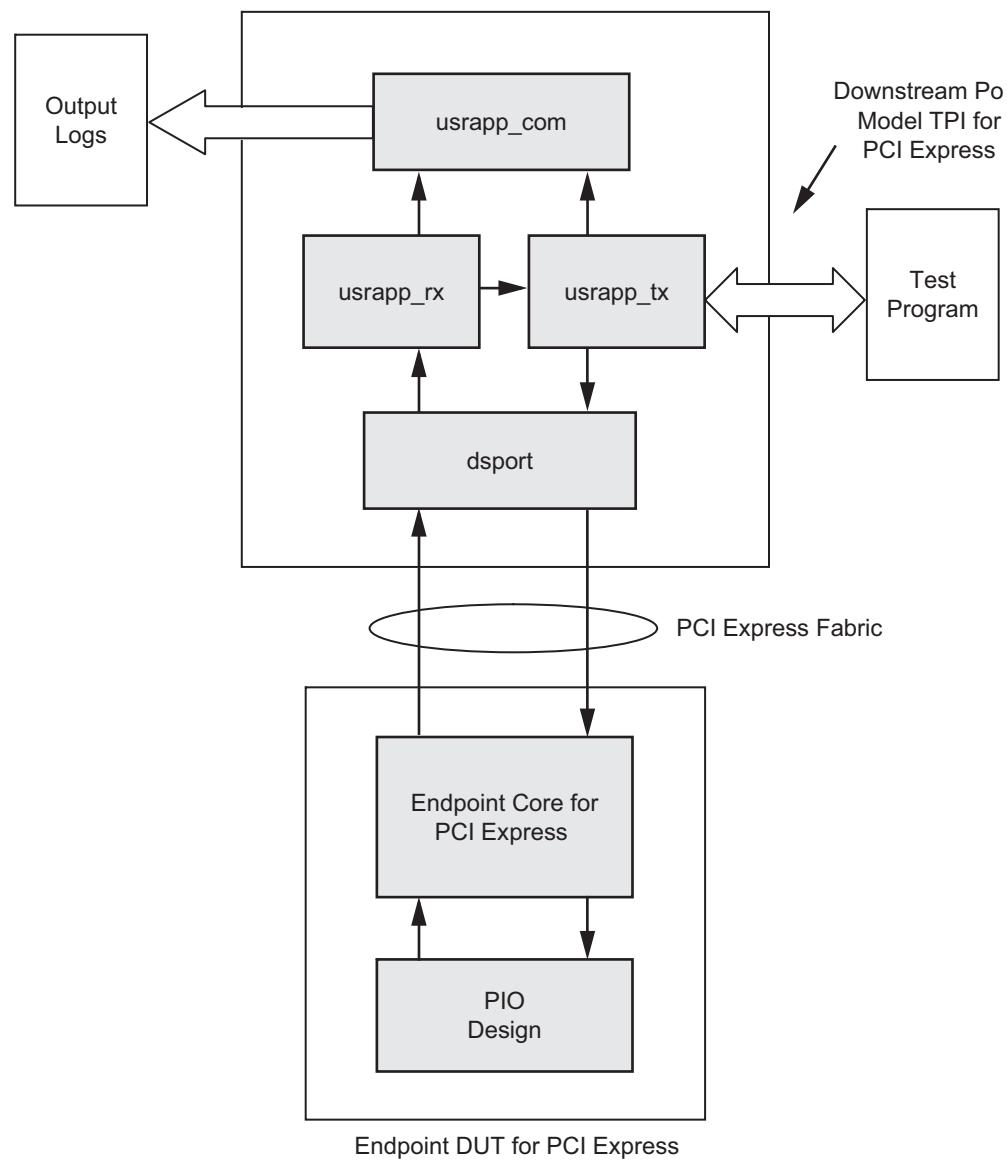


Figure 3-1: Simulation Example Design Block Diagram

Implementation Design Overview

The implementation design consists of a simple PIO example that can accept read and write transactions and respond to requests, as illustrated in [Figure 3-2](#). Source code for the example is provided with the core. For more information about the PIO example design, see [Appendix A, Programmed Input Output Example Design](#).

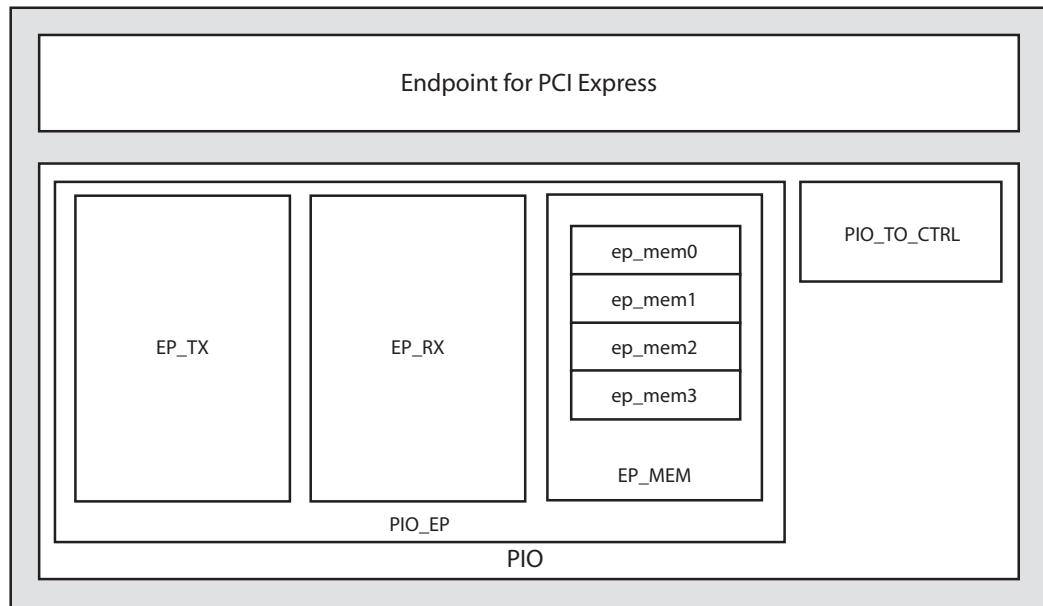


Figure 3-2: Implementation Example Design Block Diagram

Example Design Elements

The PIO example design elements include the following:

- Core wrapper
- An example Verilog HDL or VHDL wrapper (instantiates the cores and example design)
- A customizable demonstration test bench to simulate the example design

The example design has been tested and verified with Xilinx® ISE® v13.2 software and these simulators:

- Cadence Incisive Enterprise Simulator (IES)
- Synopsys VCS and VCS MX
- Mentor Graphics ModelSim

For the supported versions of the tools, see the [ISE Design Suite 13: Release Notes Guide](#).

Note: Currently, the VHDL demonstration test bench supports only ModelSim and Cadence Incisive Enterprise Simulator (IES).

Generating the Core

To generate a core using the default values in the CORE Generator™ tool GUI, do the following:

1. Start the CORE Generator tool.

For help starting and using the CORE Generator tool, see the [ISE Design Suite](#) web page.

2. Choose File > New Project.

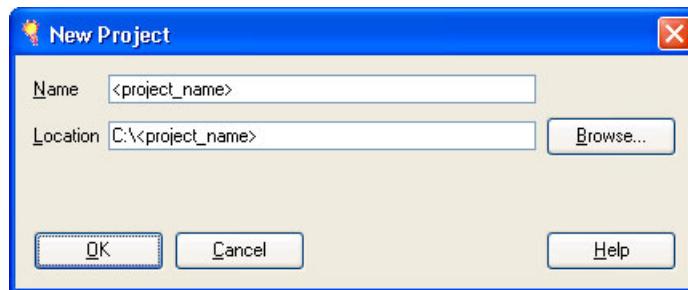


Figure 3-3: New Project Dialog Box

3. Enter a project name and location, then click OK. <project_dir> is used in this example. The Project Options dialog box appears.

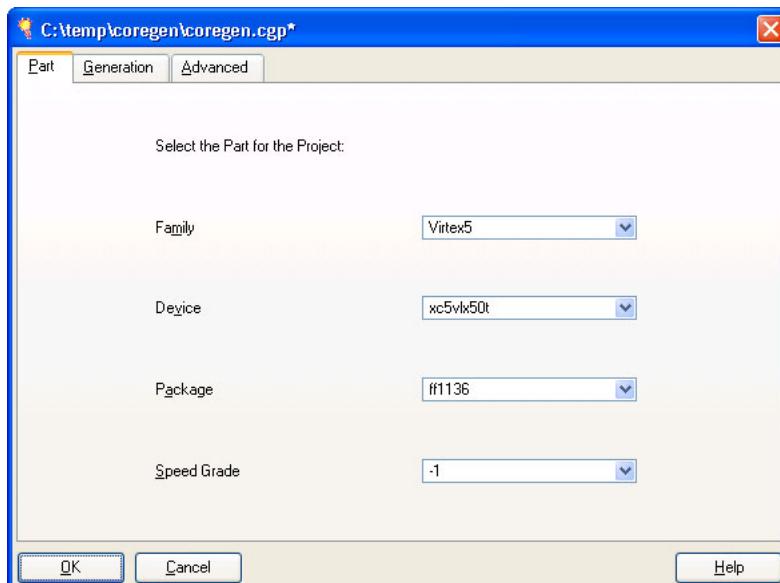


Figure 3-4: Project Options

4. Set the project options:

From the Part tab, select these options:

- **Family:** Virtex5
- **Device:** xc5vlx50t
- **Package:** ff1136
- **Speed Grade:** -1

Note: If an unsupported silicon device is selected, the core is dimmed (unavailable) in the list of cores.

From the Generation tab, select the following parameters, and then click OK.

- **Design Entry.** Select either **VHDL** or **Verilog**.
- **Vendor.** Select **Synplicity** or **ISE** (for XST).

5. Locate the core in the selection tree under Standard Bus Interfaces/PCI Express; then double-click the core name to display the Block Plus main screen.

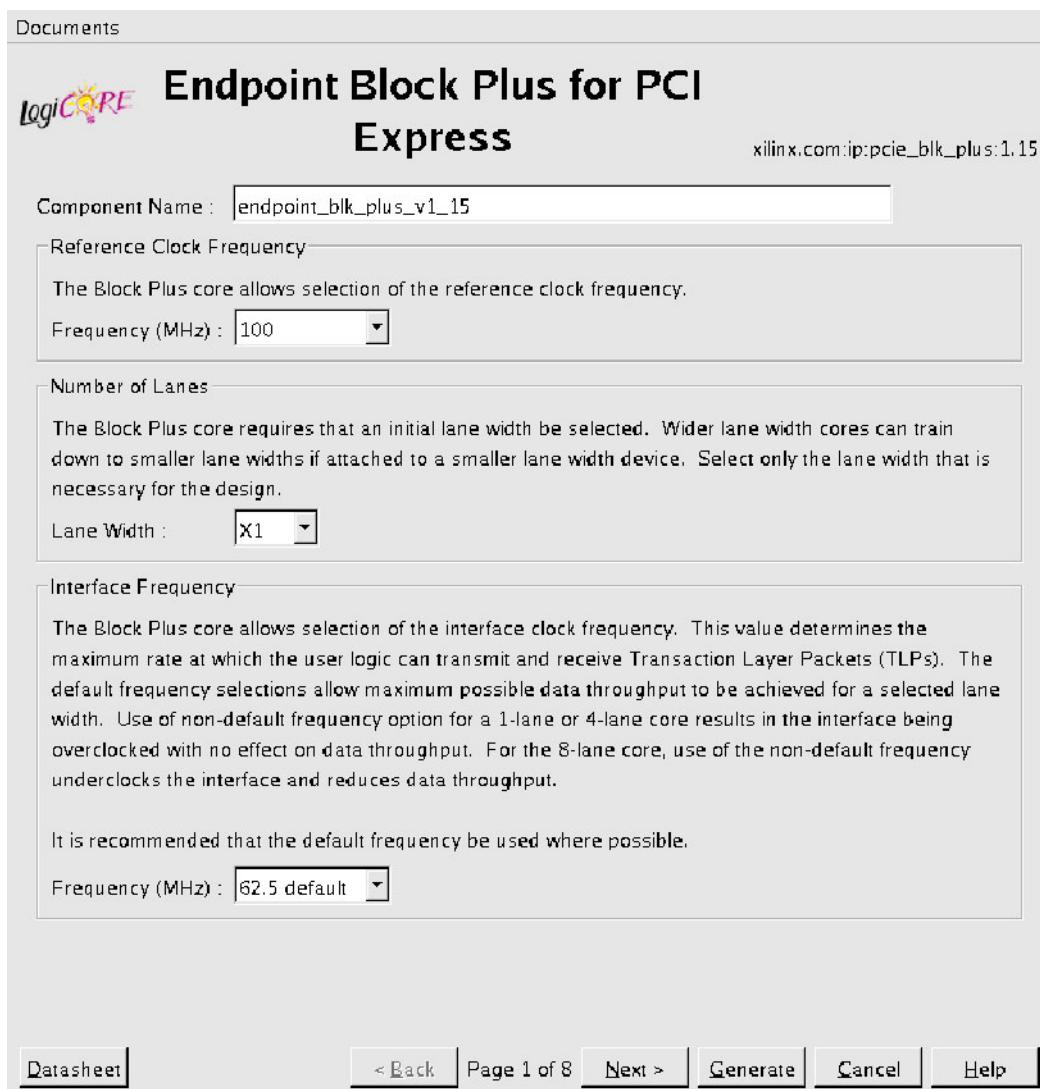


Figure 3-5: Endpoint Block Plus Main Screen

6. In the Component Name field, enter a name for the core. <component_name> is used in this example.
7. Click Finish to generate the core using the default parameters. The core and its supporting files, including the PIO example design and Root Port Model test bench, are generated in the project directory.

For detailed information about the example design files and directories see [Directory Structure and File Contents, page 62](#).

Simulating the Example Design

The example design provides a quick way to simulate and observe the behavior of the core. The simulation environment provided with the Block Plus core performs simple memory access tests on the PIO example design. Transactions are generated by the Root Port Model and responded to by the PIO example design.

- PCI Express Transaction Layer Packets (TLPs) are generated by the test bench transmit user application (`pci_exp_usrapp_tx`). As it transmits TLPs, it also generates a log file, `tx.dat`.
- PCI Express TLPs are received by the test bench receive user application (`pci_exp_usrapp_rx`). As the user application receives the TLPs, it generates a log file, `rx.dat`.

For more information about the test bench, see [Appendix B, Root Port Model Test Bench](#).

Setting up for Simulation

To run the gate-level simulation you must have the Xilinx Simulation Libraries compiled for your system. See the Compiling Xilinx Simulation Libraries (COMPXLIB) in the *Xilinx ISE Synthesis and Verification Design Guide*, and the *Xilinx ISE Software Manuals and Help*. Documents can be downloaded from www.xilinx.com/support/software_manuals.htm.

Simulator Requirements

Virtex®-5 device designs require either a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator or a SWIFT-compliant simulator.

- For a Verilog LRM-IEEE 1364-2005 encryption-compliant simulator, ModelSim v6.6d is currently supported.
- For a SWIFT-compliant simulator, Cadence Incisive Enterprise Simulator (IES) v10.2 and Synopsys VCS and VCS MX 2010.06 are currently supported.

Note for Cadence IES users: The work construct must be manually inserted into your CDS.LIB file as shown below.

```
DEFINE WORK WORK
```

Running the Simulation

For Cadence IES

The simulation scripts provided with the example design support pre-implementation (RTL) simulation. The existing test bench can be used to simulate with a post-implementation version of the example design.

The pre-implementation simulation consists of the following components:

- Verilog or VHDL model of the test bench
 - Verilog or VHDL RTL example design
 - Verilog wrapper of the Endpoint Block Plus for PCI Express and the Verilog source files
1. To run the simulation, go to the following directory:
`<project_dir>/<component_name>/simulation/functional`
 2. Run the script that corresponds to your simulation tool using one of the following:
 - **VCS:** `simulate_vcs.sh`
 - **Cadence IES:** `simulate_ncsim.sh`
 - **ModelSim:** `vsim -do simulate_mti.do`

Implementing the Example Design

Implementation Flow Using Command Line

After generating the core, the netlists and the example design can be processed using the Xilinx implementation tools. The generated output files include scripts to assist you in running the Xilinx software.

To implement the example design:

Open a command prompt or terminal window and type the following:

Windows

```
ms-dos> cd <project_dir>\<component_name>\implement  
ms-dos> implement.bat
```

Linux

```
% cd <project_dir>/<component_name>/implement  
% ./implement.sh
```

These commands execute a script that synthesizes, builds, maps, and place-and-routes the example design, and then generates a post-par simulation model for use in timing simulation. The resulting files are placed in the `results` directory and execute the following processes:

1. Removes data files from the previous runs.
2. Synthesizes the example design using either Synplicity Synplify or XST.
3. `ngdbuild`. Builds a Xilinx design database for the example design.

- Inputs:

Part-Package-Speed Grade selection:

XC5VLX50T-FF1136-1

Example design UCF:

`xilinx_pci_exp_blk_plus_1_lane_ep-XC5VLX50T-FF1136-1.ucf`

4. `map`: Maps design to the selected FPGA using the constraints provided.
5. `par`: Places cells onto FPGA resources and routes connectivity.
6. `trce`: Performs static timing analysis on design using constraints specified.

7. netgen: Generates a logical Verilog HDL or VHDL representation of the design and an SDF file for post-layout verification.
8. bitgen: Generates a bitstream file for programming the FPGA.

The following FPGA implementation related files are generated in the results directory:

- `routed.bit`
FPGA configuration information.
- `routed.v[hd]`
Verilog or VHDL functional Model.
- `routed.sdf`
Timing model Standard Delay File.
- `mapped.mrp`
Xilinx map report.
- `routed.par`
Xilinx place and route report.
- `routed.twr`
Xilinx timing analysis report.

The script file starts from an EDIF/NGC file and results in a bitstream file. It is possible to use the Xilinx ISE software GUI to implement the example design. However, the GUI flow is not presented in this document.

Implementation Flow using ISE Software

By default, the Block Plus for PCIe® example design supports a command line-based implementation flow; the implementation functions and options are specified within script files executed by the user at a command prompt. To implement the example design in the ISE software environment, you must integrate the command line flow with ISE software using these steps:

1. Using the CORE Generator tool, generate an Endpoint Block Plus for PCIe core and example design using these parameters:
 - Family: Virtex5
 - Device: xc5vlx50t
 - Package: ff1136
 - Speed Grade: -1

For information about generating a core, see [Generating the Core, page 48](#). Xilinx recommends that you start the CORE Generator tool as a separate application and not as a sub-process within the ISE software environment.

2. Create an ISE software project using device properties that correspond to the CORE Generator tool project options. Make sure that the Family, Device, Package, and Speed Grade options are identical to the values defined in Step 1.

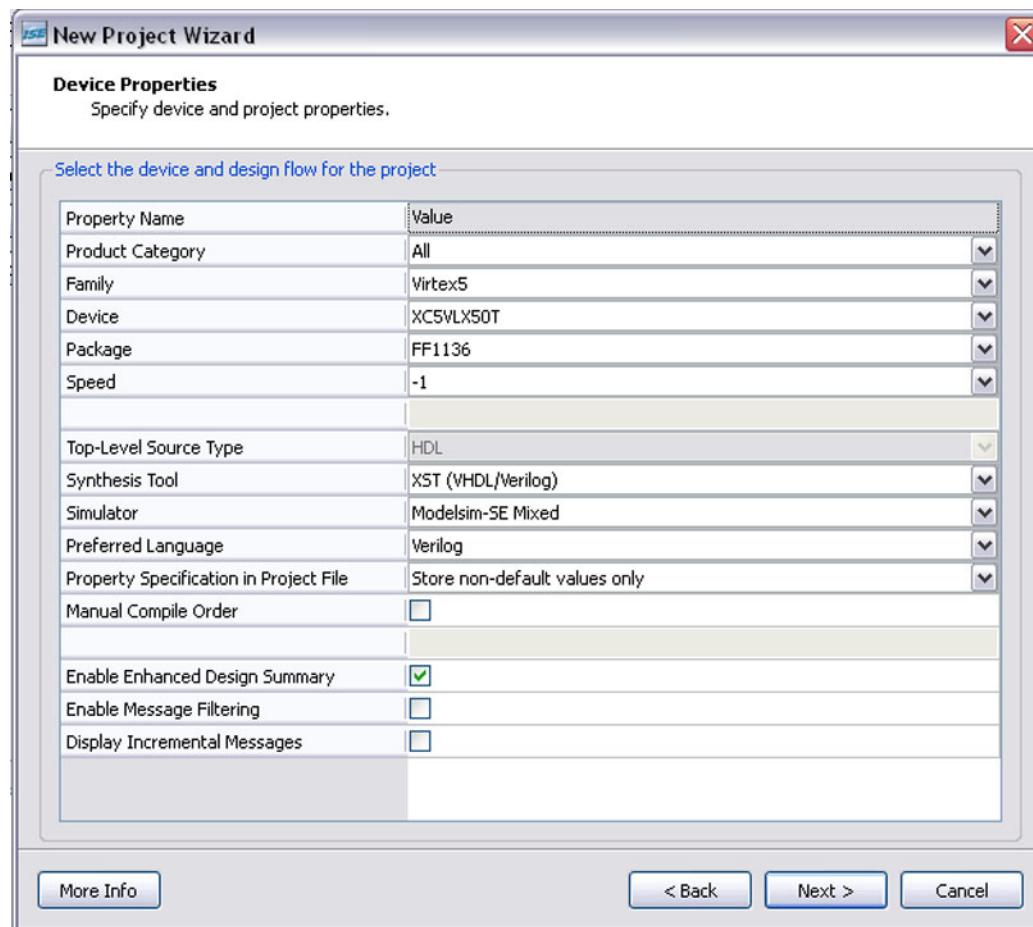


Figure 3-6: New Project Device Properties

3. Add the example design source files, located in the `<projectdirectory>/<component_name>/example_design` directory, to the ISE software project.

Note: For some Block Plus for PCIe example design configurations, the CORE Generator tool generates multiple UCF files. Be sure to add only one UCF to the project.

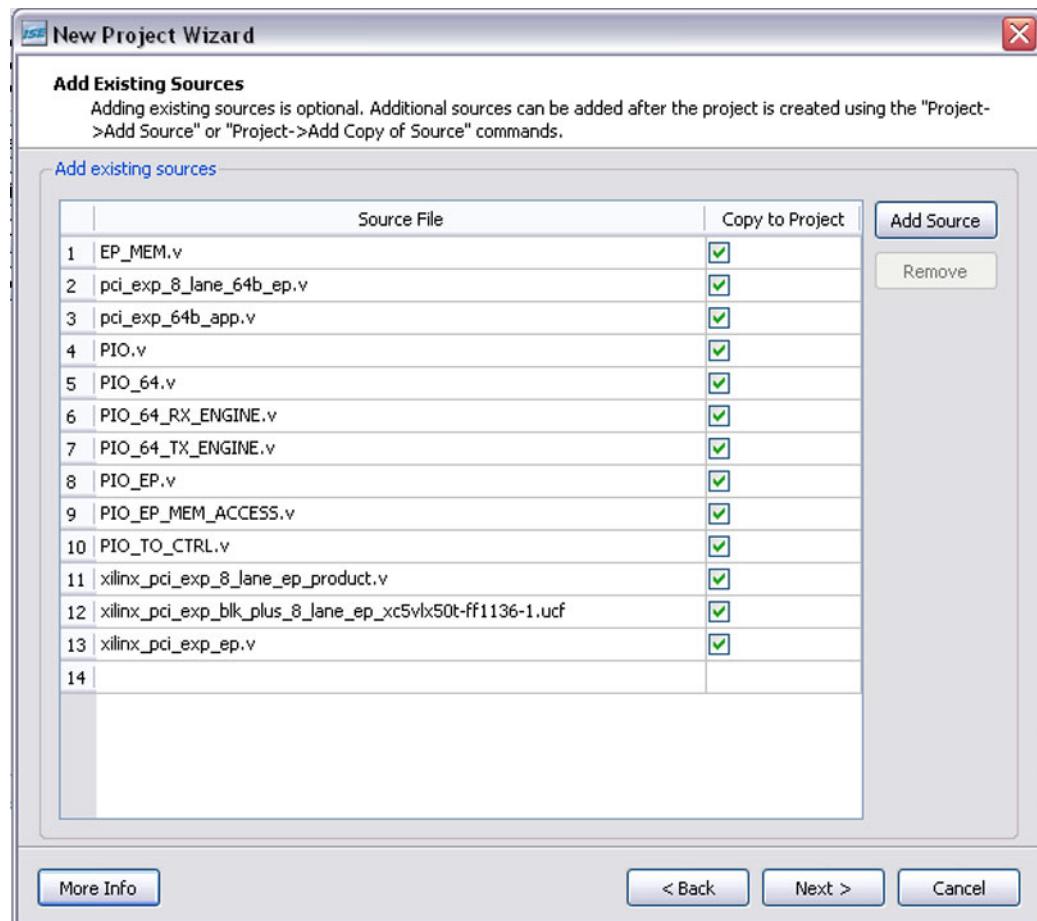


Figure 3-7: New Project: Add Existing Sources

4. Add the Block Plus wrapper source files located in <projectdirectory>/<component name>/source directory, to the ISE software project.

Note: Wrapper source code is only available in Verilog and requires mixed language mode synthesis if the User Application is VHDL based. Synthesis of the Block Plus wrapper source code is only supported with XST. If a synthesis tool other than XST is used to synthesize the User Application, the user must use XST to synthesize the Block Plus wrapper as a stand-alone core and then incorporate the ngc file produced by XST when implementing the design. See [Wrapper Source Code in Chapter 4](#) for more information.

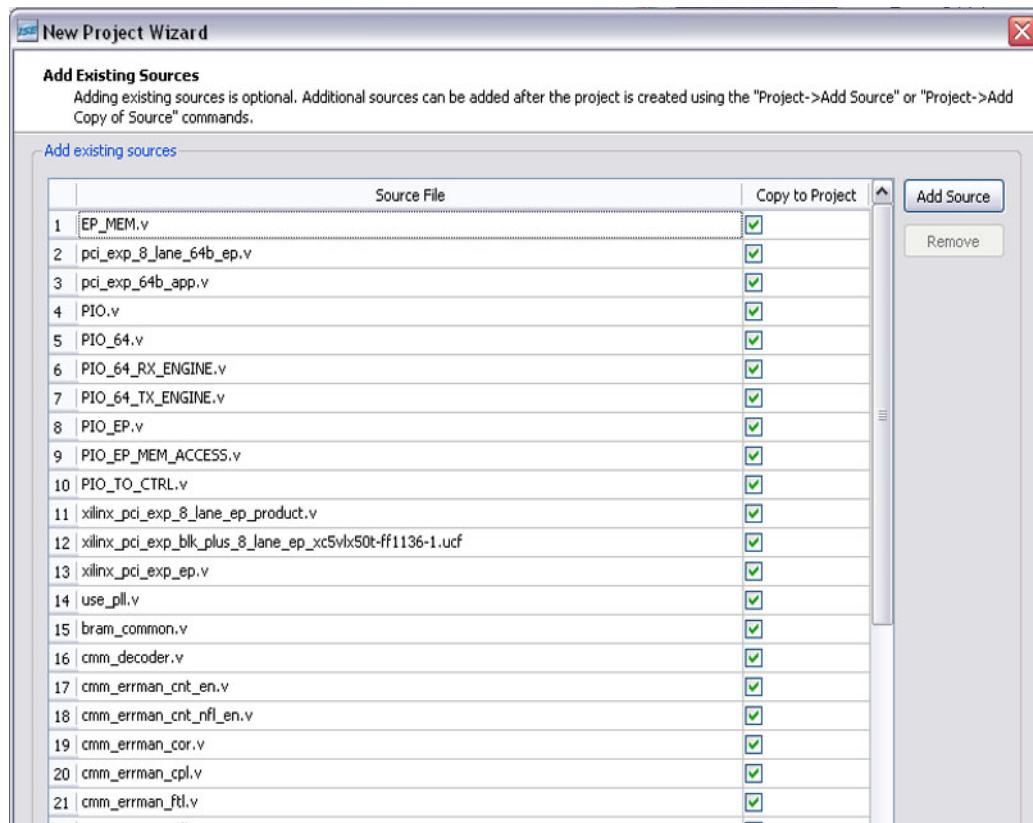


Figure 3-8: New Project: Add Source Files

5. In the Source Window, select the top-level example design instance xilinx_pci_exp_ep. The Synthesize - XST and Implement Design processes are displayed in the Processes window.

6. From the Processes window, right-click Synthesize - XST and select Properties, as displayed in [Figure 3-9](#). The Process Properties dialog box appears.

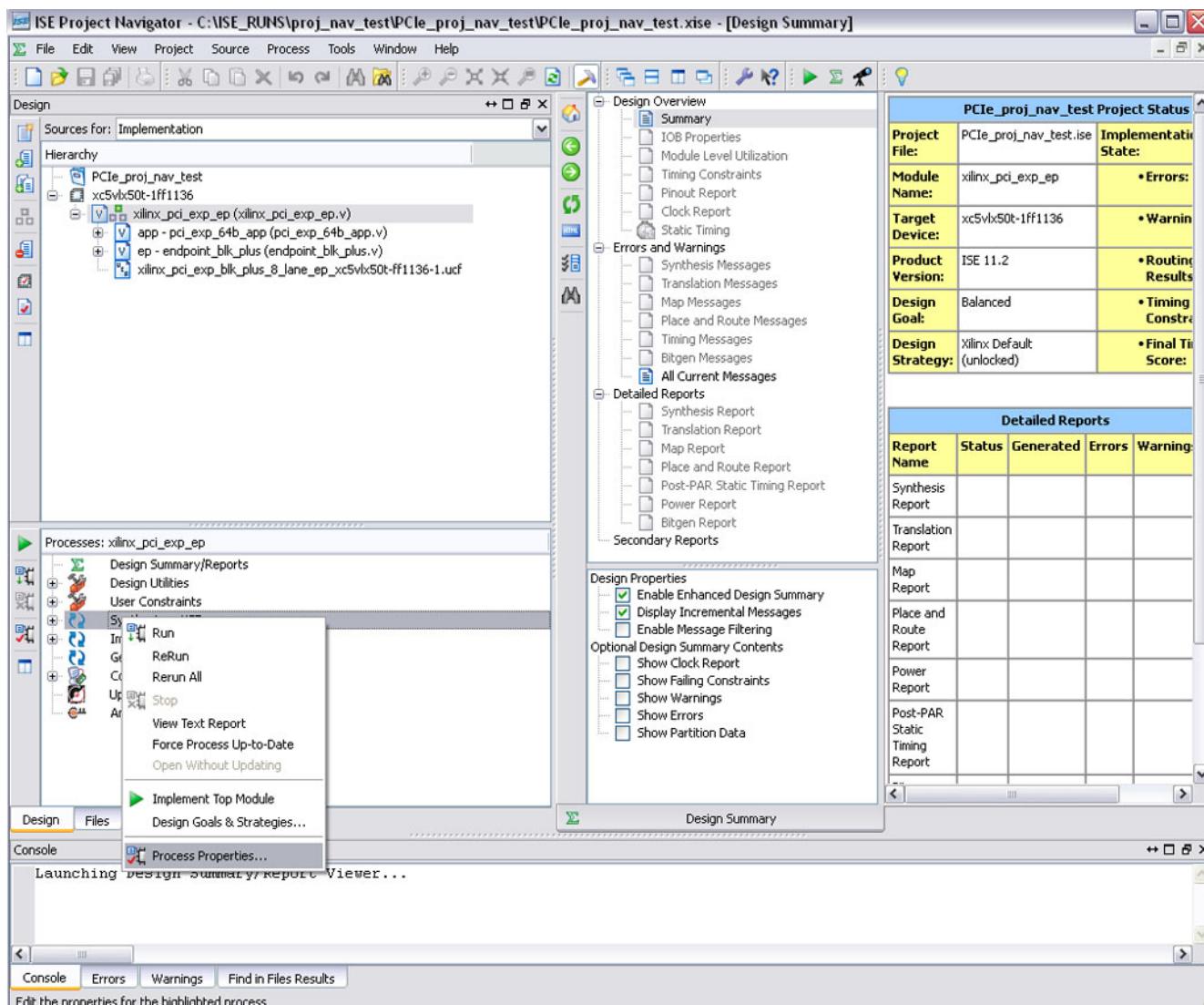


Figure 3-9: Processes Window: Synthesize - XST Properties

7. In the Process Properties dialog box, click the Synthesis Options category.

8. From the Optimization Effort drop-down menu, choose High.

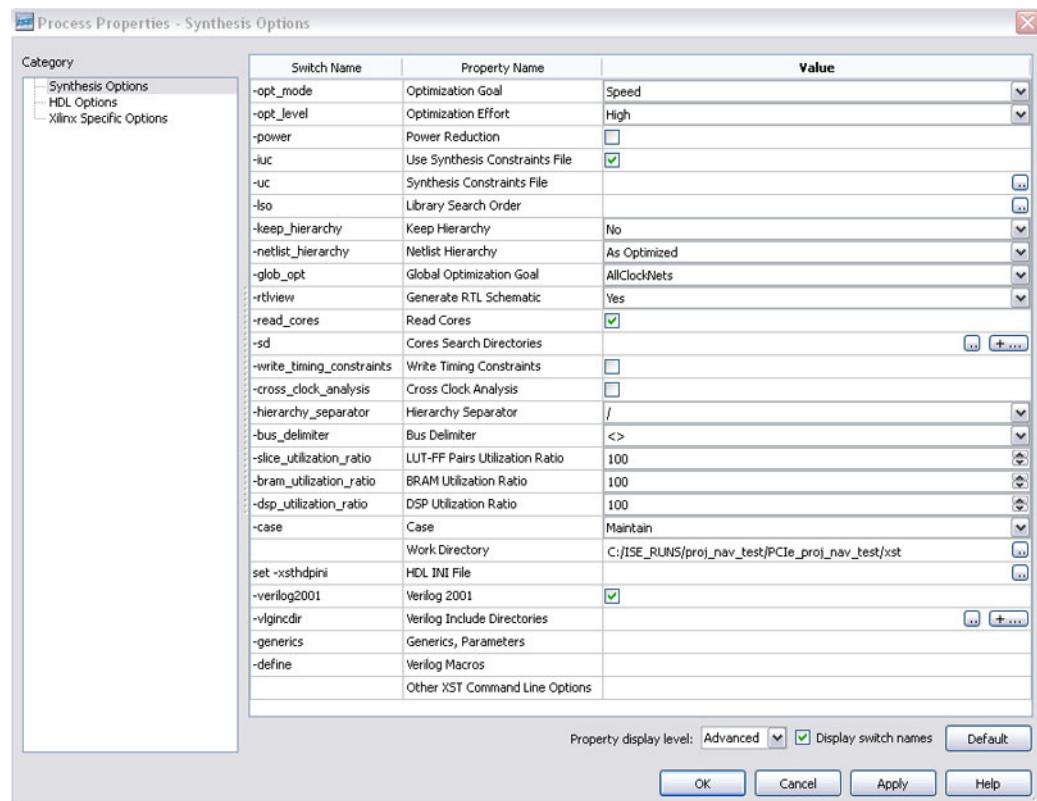


Figure 3-10: Process Properties: Synthesis Options

9. In the Processes window, right-click Implement Design process and select Properties, as shown in [Figure 3-11](#). The Process Properties dialog box appears.

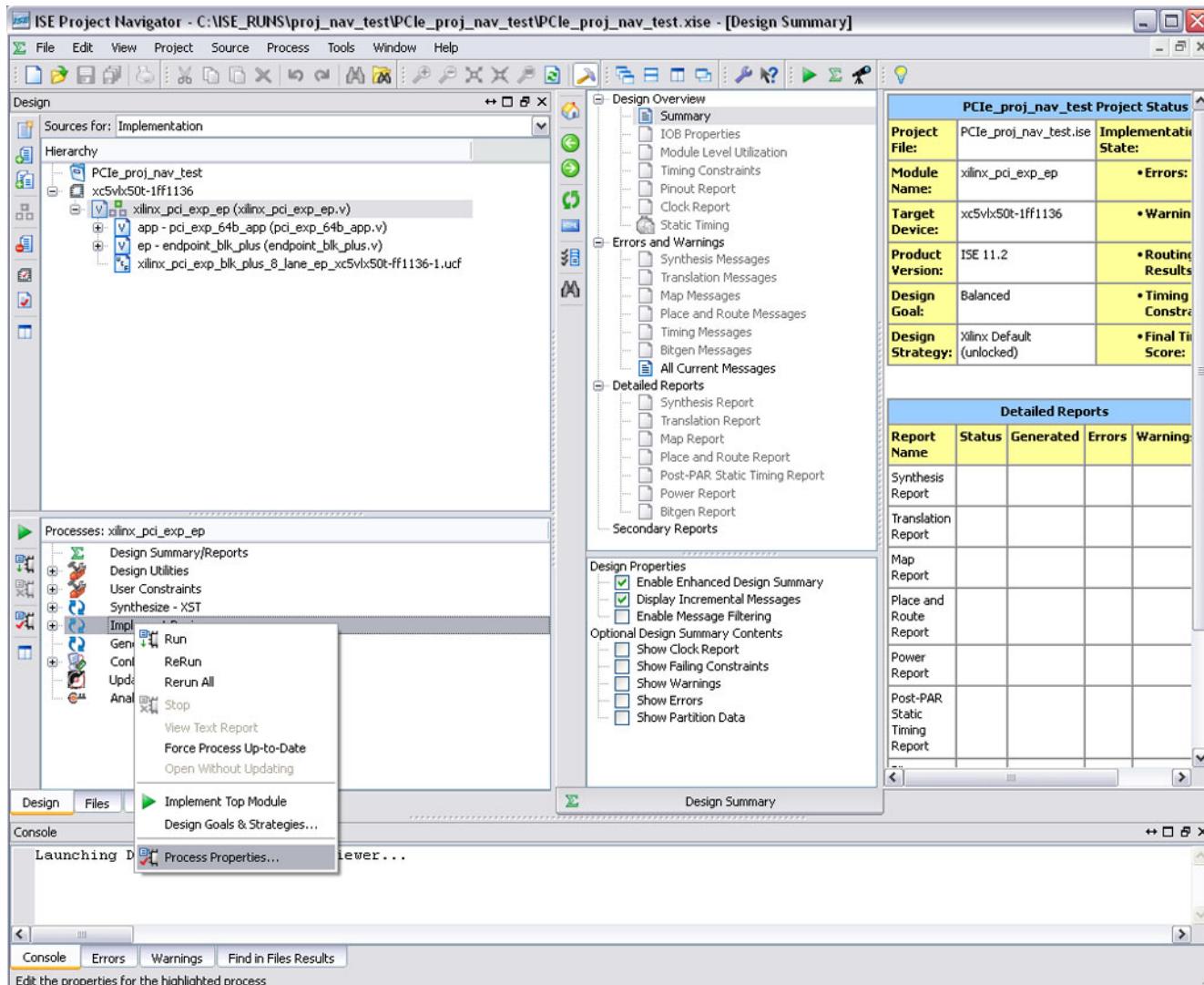


Figure 3-11: Processes Window: Implement Design Properties

10. In the Process Properties dialog box, click the Map Properties Category; then select the following options:
 - From the Placer Effort Level drop-down menu, choose High.
 - From the Placer Extra Effort Level drop-down menu, choose Continue on Impossible.
 - From the Pack I/O Registers/Latches into IOBs drop-down menu, choose Inputs and Outputs
11. Click Apply.

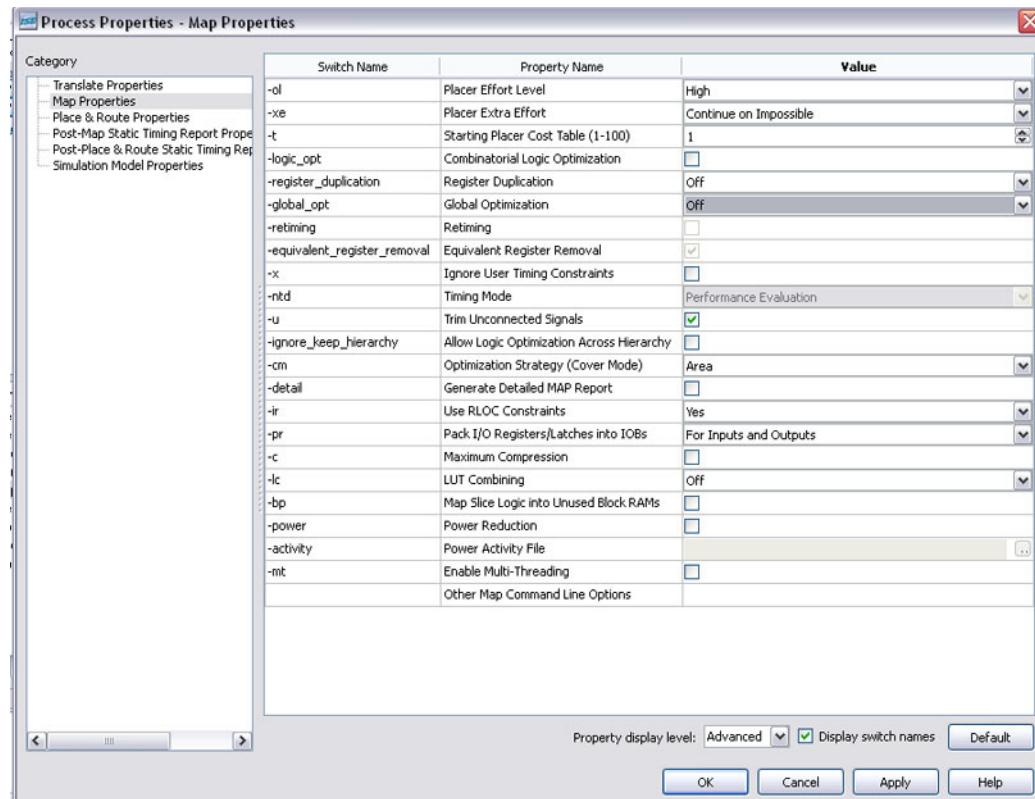


Figure 3-12: Map Properties Options

12. Next, click the Place & Route Properties Category; then select the following options:
 - From the Place & Route Effort (Overall) drop-down menu, choose High.
 - From the Extra Effort (Highest PAR Level Only) drop-down menu, choose Continue on Impossible.
13. Click OK to exit the dialog box. At this point, all implementation options are configured.

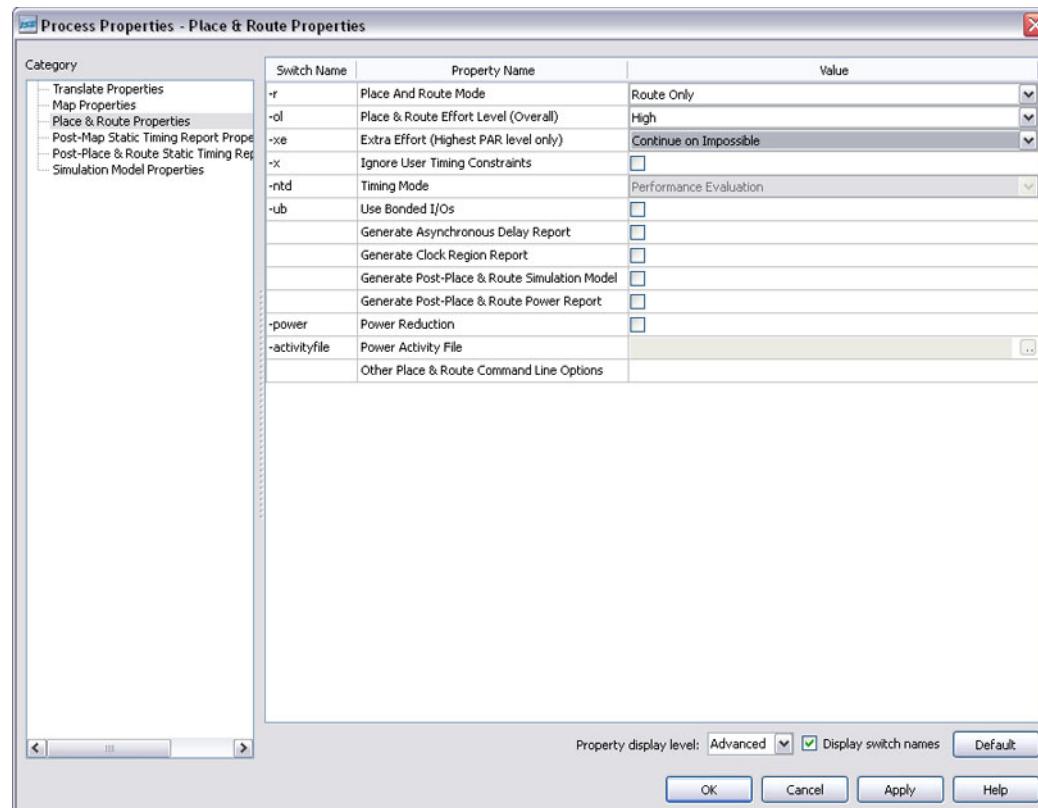


Figure 3-13: Place and Route Properties Option

14. From the Processes window, right-click Implement Design and select Rerun All to start the implementation, as displayed in [Figure 3-14](#).

When the implementation process is complete, the detailed reports section in the Design Summary window displays the results of how the design met timing.

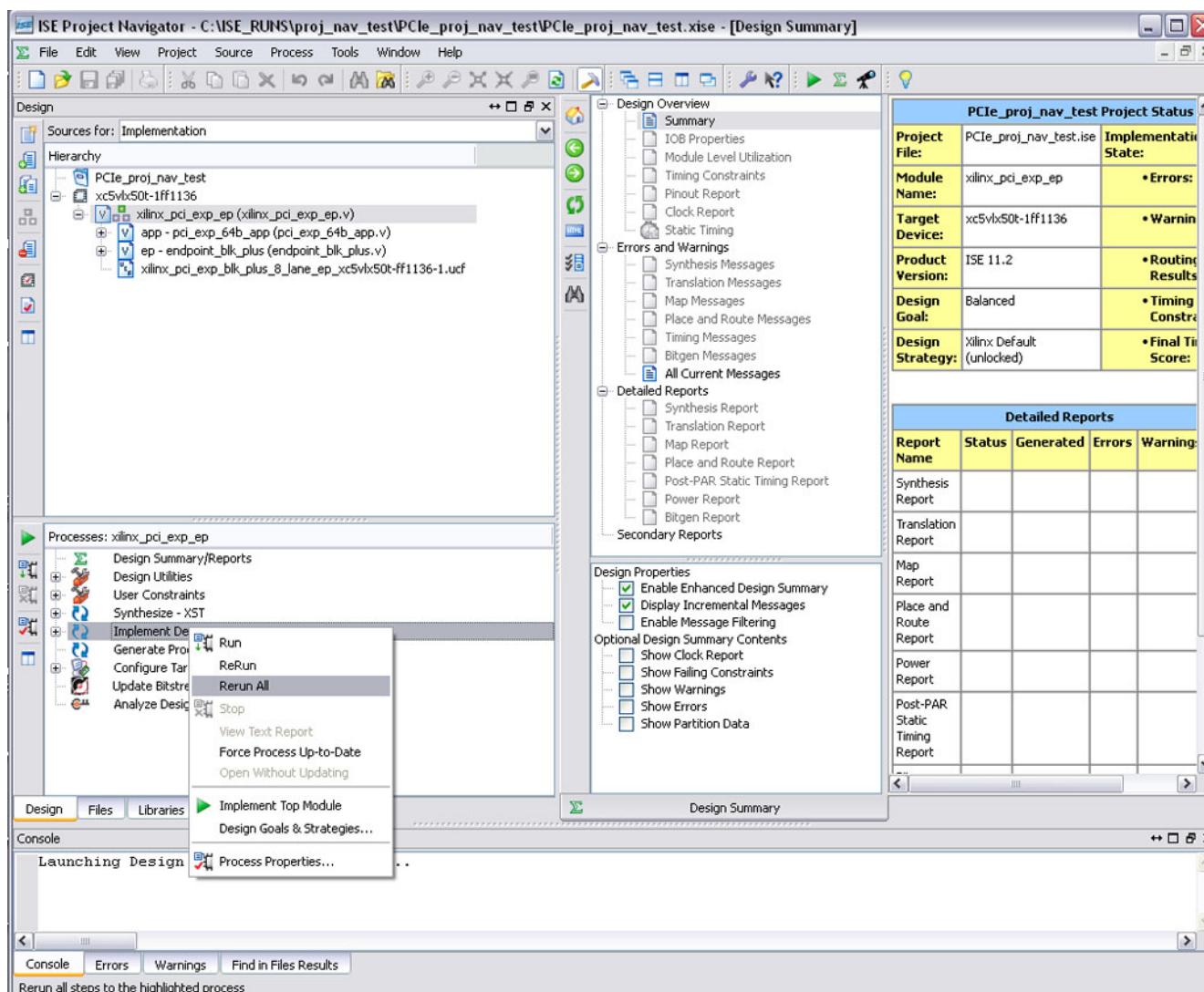


Figure 3-14: Implementation Timing Results

Directory Structure and File Contents

The Endpoint Block Plus for PCIe example design directories and their associated files are defined in the sections that follow. Click a directory name to go to the desired directory and its associated files.

Example Design

-  **<project directory>**
Top-level project directory; name is user-defined
-  **<project directory>/<component name>**
Core release notes readme file
 -  **<component name>/doc**
Product documentation
 -  **<component name>/example_design**
Verilog or VHDL design files
 -  **<component name>/source**
Core source files
 -  **<component name>/implement**
Implementation script files
 -  **implement/results**
Results directory, created after implementation scripts are run, and contains implement script results
 -  **<component name>/simulation**
Simulation scripts
 -  **simulation/dsport**
Simulation files
 -  **simulation/functional**
Functional simulation files
 -  **simulation/tests**
Test command files

<project directory>

The project directory contains all the CORE Generator tool project files.

Table 3-1: Project Directory

Name	Description
	<project_dir>
<component_name>.xmdf.tcl	Xilinx standard IP Core information file used by Xilinx design tools.
<component_name>.xco	CORE Generator tool project-specific option file; can be used as an input to the CORE Generator tool.
<component_name>.flist.txt	List of files delivered with core.
<component_name>. {veo vho}	Verilog or VHDL instantiation template.

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<project directory>/<component name>

The component name directory contains the release notes readme file provided with the core, which can include tool requirements, last-minute changes, updates, and issue resolution.

Table 3-2: Component Name Directory

Name	Description
	<project_dir>/<component_name>
pcie_blk_plus_v1_15_readme.txt	Release notes file.

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<component name>/doc

The doc directory contains the PDF documentation provided with the core.

Table 3-3: Doc Directory

Name	Description
	<project_dir>/<component_name>/doc
pcie_blk_plus_ds551.pdf	<i>LogiCORE IP Endpoint Block Plus for PCI Express Data Sheet</i>
pcie_blk_plus_ug341.pdf	<i>LogiCORE IP Endpoint Block Plus for PCI Express User Guide</i>

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<component name>/example_design

The example design directory contains the example design files provided with the core.

Table 3-4: Example Design Directory

Name	Description
<project_dir>/<component_name>/example_design	
pci_exp_8_lane_64b_ep.v pci_exp_4_lane_64b_ep.v pci_exp_2_lane_64b_ep.v pci_exp_1_lane_64b_ep.v	Verilog top-level port list, applicable to the 8-lane, 4-lane, 2-lane, and 1-lane Endpoint design, respectively.
<filename>.ucf	Example design UCF. Filename varies by lane-width, part, and package selected.
xilinx_pci_exp_8_lane_ep_product.v xilinx_pci_exp_4_lane_ep_product.v xilinx_pci_exp_2_lane_ep_product.v xilinx_pci_exp_1_lane_ep_product.v	Enables Block Plus 8-lane, 4-lane, 2-lane, and 1-lane cores, respectively, in the test bench.
xilinx_pci_exp_ep.v xilinx_pci_exp_ep.vhd	Verilog or VHDL top-level PIO example design files.
pci_exp_64b_app.v[hd] EP_MEM.v[hd] PIO.v[hd] PIO_EP.v[hd] PIO_EP_MEM_ACCESS.v[hd] PIO_TO_CTRL.v[hd] PIO_64_RX_ENGINE.v[hd] PIO_64_TX_ENGINE.v[hd]	PIO example design files.

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<component name>/source

The source directory contains the generated core source files.

Table 3-5: Source Directory

Name	Description
<project_dir>/<component_name>/source	
<component name>.v	Verilog top-level wrapper for Endpoint Block Plus for PCI Express
*.v	Verilog source files for Endpoint Block Plus for PCI Express

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<component name>/implement

The implement directory contains the core implementation script files.

Table 3-6: Implement Directory

Name	Description
<project_dir>/<component_name>/implement	
xst.scr	XST synthesis script.
implement.bat implement.sh	DOS and Linux implementation scripts.
synplify.prj	Synplify synthesis script.
xilinx_pci_exp_1_lane_ep_inc.xst xilinx_pci_exp_2_lane_ep_inc.xst xilinx_pci_exp_4_lane_ep_inc.xst xilinx_pci_exp_8_lane_ep_inc.xst	XST project file for 1-lane, 2-lane, 4-lane, and 8-lane example design, respectively.
source_files_xst.prj	XST project file for source code (for Synplify flow).

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implement/results

The results directory is created by the implement script, after which the implement script results are placed in the results directory.

Table 3-7: Results Directory

Name	Description
<project_dir>/<component_name>/implement/results	
Implement script result files.	

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<component name>/simulation

The simulation directory contains the simulation source files provided with the core.

Table 3-8: Simulation Directory

Name	Description
<project_dir>/<component_name>/simulation	
board_common.v	Contains test bench definitions.
board.v[hd]	Top-level simulation module.
sys_clk_gen_ds.v[hd]	System differential clock source.
sys_clk_gen.v[hd]	System clock source.
xilinx_pci_exp_cor_ep.f	List of files comprising the design being tested.
xilinx_pci_expDefines.v	PCI Express application macro definitions.

Table 3-8: Simulation Directory (Cont'd)

Name	Description
source_rtl.f	List of files comprising the source code for Endpoint Block Plus for PCI Express

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simulation/dsport

The dsport directory contains the data stream simulation scripts provided with the core.

Table 3-9: dsport Directory

Name	Description
<project_dir>/<component_name>/simulation/dsport	

gtx_tx_sync_rate_v6.v gtx_wrapper_v6.v pci_exp_expect_tasks.v pci_exp_usrapp_cfg.v[hd] pci_exp_usrapp_com.v pci_exp_usrapp_pl.v pci_exp_usrapp_rx.v[hd] pci_exp_usrapp_tx.v[hd] test_interface.vhd pcie_2_0_rport_v6.v pcie_bram_top_v6.v pcie_bram_v6.v pcie_brams_v6.v pcie_clocking_v6.v pcie_gtx_v6.v pcie_pipe_lane_v6.v pcie_pipe_misc_v6.v pcie_pipe_v6.v pcie_reset_delay_v6.v xilinx_pcie_2_0_rport_v6.v	Root Port Model files.
--	------------------------

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simulation/functional

The functional directory contains functional simulation scripts provided with the core.

Table 3-10: Functional Directory

Name	Description
<project_dir>/<component_name>/simulation/functional	
board_rtl_x01.f board_rtl_x02.f board_rtl_x04.f board_rtl_x08.f board_rtl_x01_ncv.f board_rtl_x02_ncv.f board_rtl_x04_ncv.f board_rtl_x08_ncv.f board_rtl.f rport_rtl_x01.f rport_rtl_x02.f rport_rtl_x04.f rport_rtl_x08.f rport_rtl_x01_ncv.f rport_rtl_x02_ncv.f rport_rtl_x04_ncv.f rport_rtl_x08_ncv.f rport_rtl.f	List of files for RTL simulations.
simulate_mti.do	Simulation script for ModelSim.
simulate_ncsim.sh	Simulation script for Cadence IES.
simulate_vcs.sh	Simulation script for VCS.
xilinx_lib_vcs.f xilinx_lib_vnc.f	Points to the required SmartModel.

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simulation/tests

The tests directory contains test definitions for the example test bench.

Table 3-11: Tests Directory

Name	Description
<project_dir>/<component_name>/simulation/tests	
pio_tests.v sample_tests1.v tests.v[hd]	Test definitions for example test bench.

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Generating and Customizing the Core

The Endpoint Block Plus for PCI Express® core is fully configurable and highly customizable, yielding a resource-efficient implementation tailored to your design requirements.

Wrapper Source Code

The Block Plus core wrapper source code is now delivered by the CORE Generator™ tool. The source code is located in the directory

`<projectdir>/<component_name>/source`. The CORE Generator tool no longer produces an NGC file for the core. The user must synthesize the core wrapper files as part of an overall User Application project during implementation. The user must point to the source files during simulation. See the example synthesis and implementation scripts found in the directory `<projectdir>/<component_name>/implement/`. In addition, see the example simulation scripts found in the directory `<projectdir>/<component_name>/simulation/`.

Wrapper source code is only available in Verilog and requires mixed language mode synthesis if the User Application is VHDL based. Synthesis of the Block Plus core wrapper source code is only supported with XST. If a synthesis tool other than XST is used to synthesize the User Application, the user must use XST to synthesize the Block Plus Wrapper as a stand-alone core and then incorporate the NGC file produced by XST when implementing the design.

Help and support for the Endpoint Block Plus for PCI Express is only provided for the original source as delivered by the CORE Generator tool. Xilinx does not support changes to the wrapper source code and will not help debug design problems if the wrapper source code has been modified.

Using the CORE Generator Tool

The Endpoint Block Plus core is customized using the CORE Generator tool GUI. The CORE Generator tool GUI for the Block Plus for PCIe® consists of eight screens:

- Screens 1 and 2: Basic Parameter Settings
- Screens 3 and 4: Base Address Registers
- Screens 5 and 6: Configuration Register Settings
- Screens 7 and 8: Advanced Settings

Basic Parameter Settings

The initial customization screens (Figure 4-1 and Figure 4-2) are used to define basic parameters for the core, including component name, lane width, interface frequency, ID initial values, class code, and Cardbus CIS pointer information.

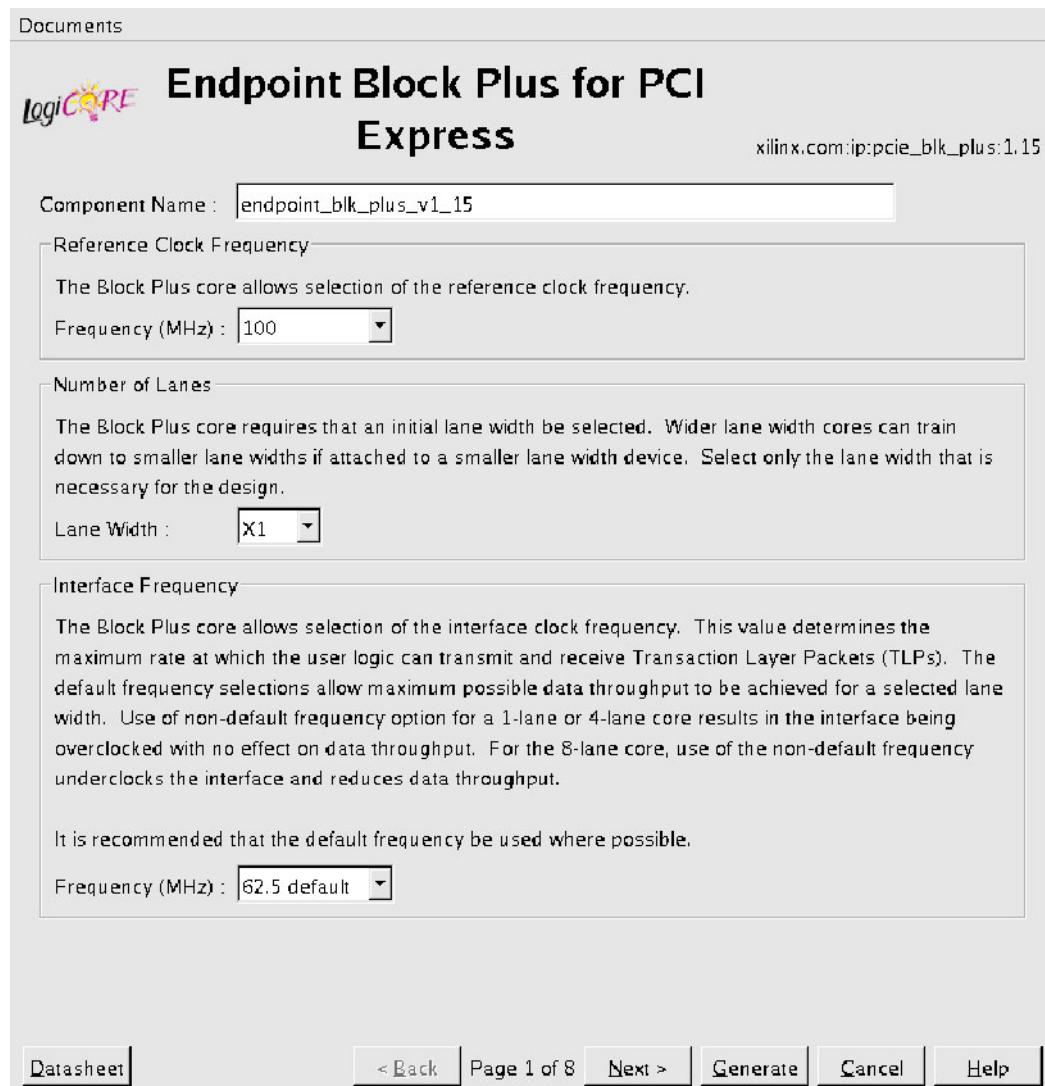


Figure 4-1: Block Plus Parameters: Screen 1

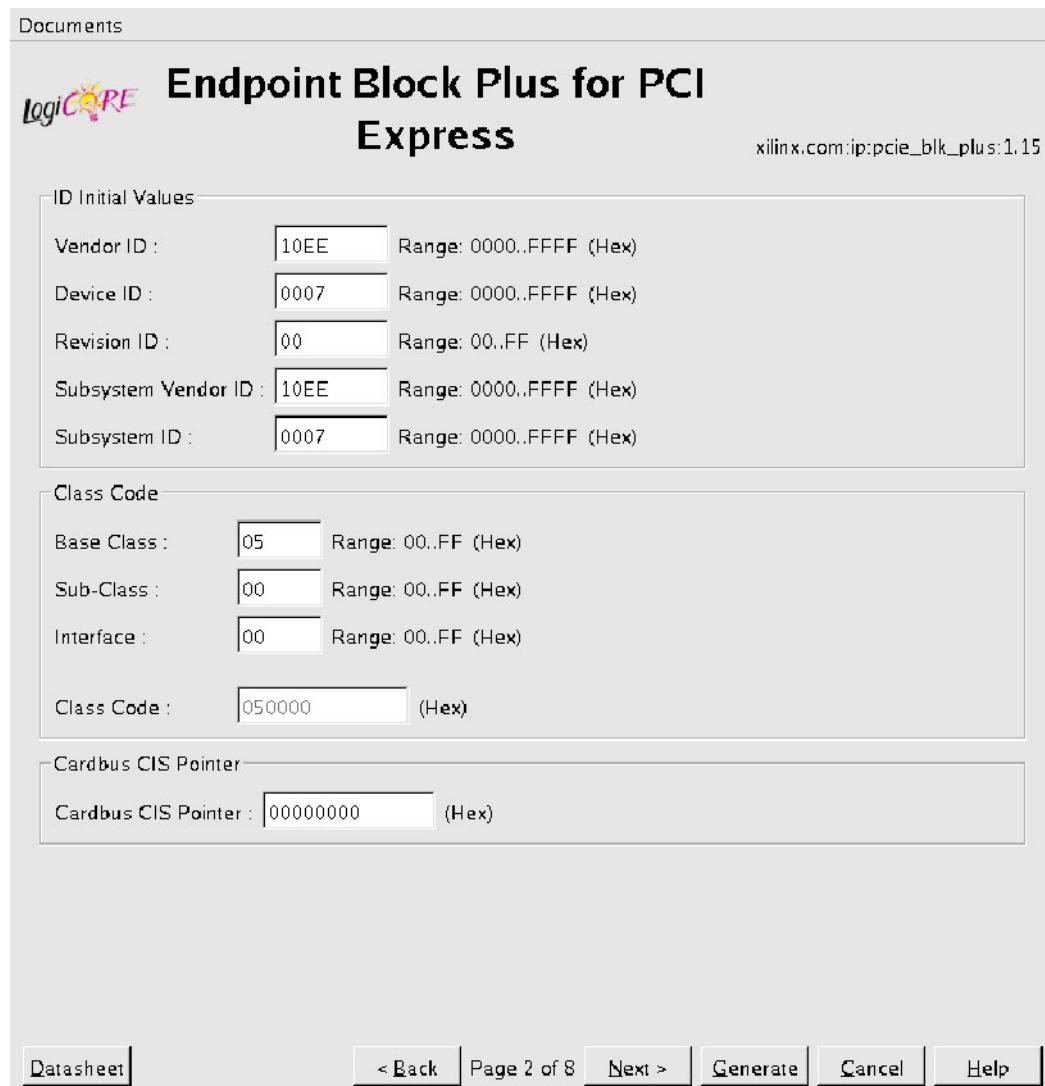


Figure 4-2: Block Plus Parameters: Screen 2

Component Name

Base name of the output files generated for the core. The name must begin with a letter and can be composed of the following characters: a to z, 0 to 9, and "_".

Reference Clock Frequency

Selects the frequency of the reference clock provided on sys_clk. For important information about clocking the Block Plus core, see [Clocking and Reset of the Block Plus Core, page 131](#) and the *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide (UG197)*.

Number of Lanes

The Block Plus for PCIe requires the selection of the initial lane width. [Table 4-1](#) defines the available widths and associated generated core. Wider lane width cores are capable of training down to smaller lane widths if attached to a smaller lane-width device. See [Link Training: 2-Lane, 4-Lane and 8-Lane Endpoints, page 130](#) for more information.

Table 4-1: Lane Width

Lane Width	Product Generated
x1	1-lane Endpoint Block Plus
x2	2-lane Endpoint Block Plus
x4	4-lane Endpoint Block Plus
x8	8-lane Endpoint Block Plus

Interface Frequency

The clock frequency of the core's user interface is selectable. Each lane width provides two frequency choices: a default frequency and an alternate frequency, as defined in [Table 4-2](#). Where possible, Xilinx recommends using the default frequency. Using the alternate frequency in a x8 configuration results in reduced throughput. Selecting the alternate frequency for x1 and x4 does not result in higher throughput in the core, but does allow the User Application to run at a higher speed.

Table 4-2: Default and Alternate Lane Width Frequency

Lane Width	Default Frequency	Alternate Frequency
x1	62.5 MHz	125 MHz
x2	125 MHz	250 MHz
x4	125 MHz	250 MHz
x8	250 MHz	125 MHz

ID Initial Values

- **Vendor ID.** Identifies the manufacturer of the device or application. Valid identifiers are assigned by the PCI Special Interest Group to guarantee that each identifier is unique. The default value, 10EEh, is the Vendor ID for Xilinx. Enter a vendor identification number here. FFFFh is reserved.
- **Device ID.** A unique identifier for the application; the default value is 0007h. This field can be any value; change this value for the application.
- **Revision ID.** Indicates the revision of the device or application; an extension of the Device ID. The default value is 00h; enter values appropriate for the application.
- **Subsystem Vendor ID.** Further qualifies the manufacturer of the device or application. Enter a Subsystem Vendor ID here; the default value is 10EE. Typically, this value is the same as Vendor ID. Setting the value to 0000h can cause compliance testing issues.
- **Subsystem ID.** Further qualifies the manufacturer of the device or application. This value is typically the same as the Device ID; default value is 0007h. Setting the value 0000h can cause compliance testing issues.

Class Code

The Class Code identifies the general function of a device, and is divided into three byte-size fields:

- **Base Class.** Broadly identifies the type of function performed by the device.
- **Sub-Class.** More specifically identifies the device function.
- **Interface.** Defines a specific register-level programming interface, if any, allowing device-independent software to interface with the device.

Class code encoding can be found at www.pcisig.com.

Cardbus CIS Pointer

Used in cardbus systems and points to the Card Information Structure for the cardbus card. If this field is non-zero, an appropriate Card Information Structure must exist in the correct location. The default value is 0000_0000h; value range is 0000_0000h-FFFF_FFFFh.

Base Address Registers

The Base Address Register (BAR) screens (Figure 4-3 and Figure 4-4) let you set the base address register space. Each BAR (0 through 5) represents a 32-bit parameter.

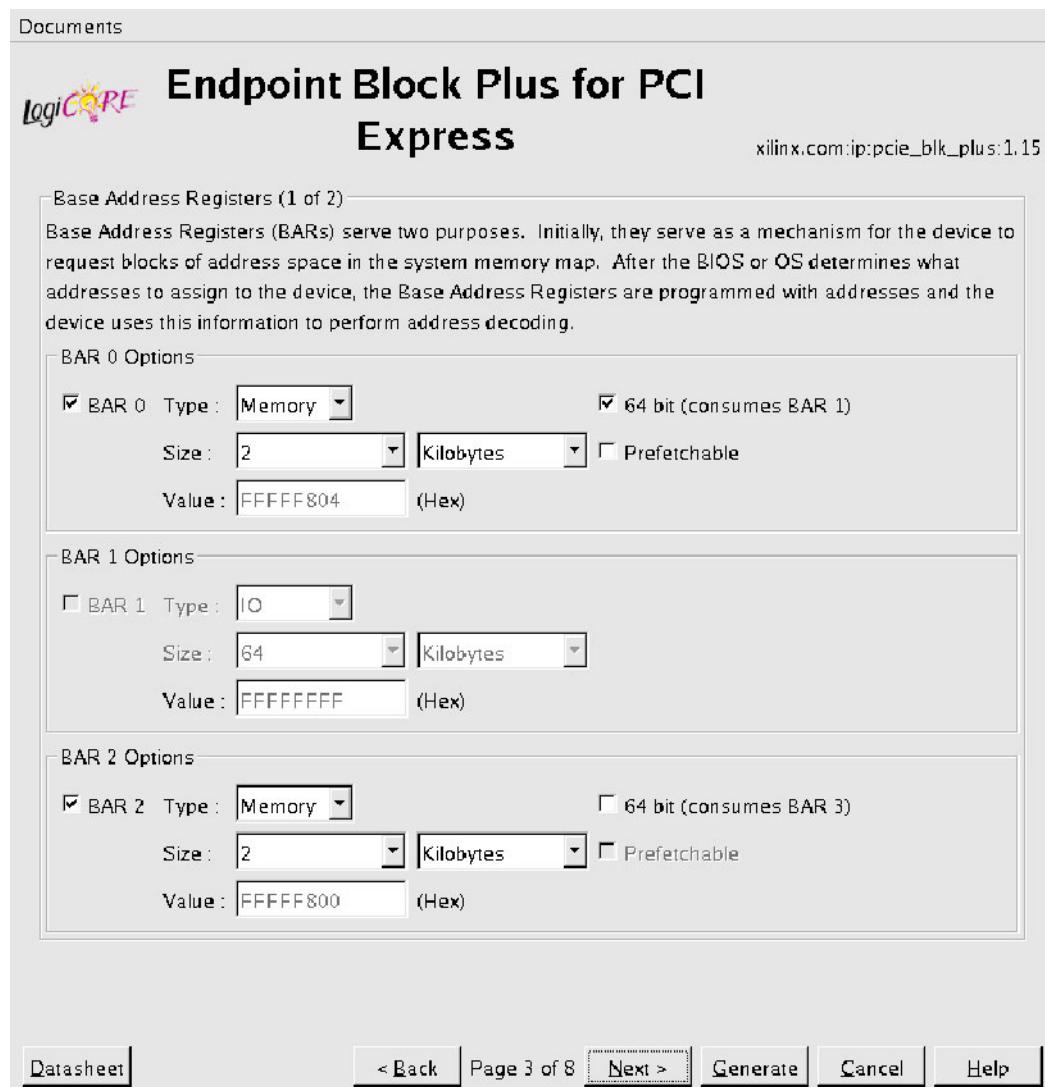


Figure 4-3: BAR Options: Screen 3

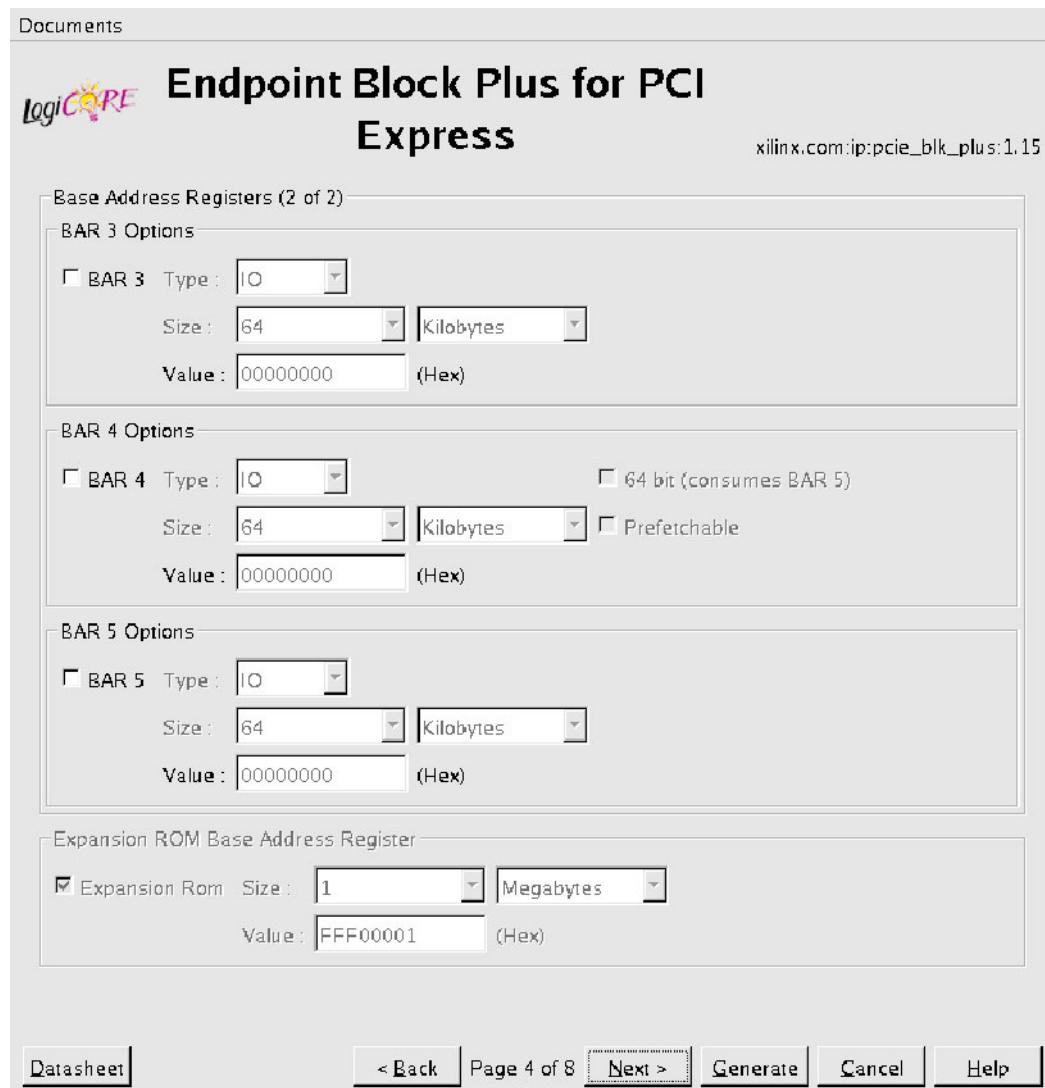


Figure 4-4: **BAR Options: Screen 4**

Base Address Register Overview

The Block core for PCIe supports up to six 32-bit Base Address Registers (BARs) or three 64-bit BARs, and the Expansion ROM BAR. BARs can be one of two sizes:

- **32-bit BARs.** The address space can be as small as 128 bytes or as large as 2 gigabytes. Used for Memory or I/O.
- **64-bit BARs.** The address space can be as small as 128 bytes or as large as 8 exabytes. Used for Memory only.

All BAR registers share these options:

- Checkbox. Click the checkbox to enable the BAR; deselect the checkbox to disable the BAR.
- Type. BARs can either be I/O or Memory.

- **I/O.** I/O BARs can only be 32-bit; the Prefetchable option does not apply to I/O BARs.
- **Memory.** Memory BARs can be either 64-bit or 32-bit and can be prefetchable. When a BAR is set as 64 bits, it uses the next BAR for the extended address space and makes the next BAR inaccessible to the user.
- **Size**
 - **Memory:** When Memory and 64-bit are *not selected*, the size can range from 128 bytes to 2 gigabytes. When Memory and 64-bit are *selected*, the size can range between 128 bytes and 8 exabytes.
 - **I/O.** When selected, the size can range from 128 bytes to 2 gigabytes.
- **Prefetchable.** Identifies the ability of the memory space to be prefetched.
- **Value.** The value assigned to the BAR based on the current selections.

For more information about managing the Base Address Register settings, see [Managing Base Address Register Settings](#) below.

Expansion ROM Base Address Register

The 1-megabyte Expansion ROM BAR is always enabled in the Block Plus core, and cannot be disabled. User applications that do not intend to use the Expansion ROM BAR need to implement logic to respond to accesses to the Expansion ROM BAR.

Accesses to the Expansion ROM BAR are indicated by trn_rbar_hit[6] assertion. Xilinx recommends that users return a Completion with Data of all zeroes if the Expansion ROM is not in use. Xilinx has found that some system BIOSs probe the Expansion ROM BAR during boot-up. Not returning a completion results in a completion timeout on the requesting device, which might lead to the system hanging.

Managing Base Address Register Settings

Memory, I/O, Type, and Prefetchable settings are handled by setting the appropriate GUI settings for the desired base address register.

Memory or I/O settings indicate whether the address space is defined as memory or I/O. The base address register only responds to commands that access the specified address space. Generally, memory spaces less than 4Kbytes in size should be avoided. The maximum I/O space allowed is 256 bytes. The use of I/O space should be avoided in all new designs.

Prefetchability is the ability of memory space to be prefetched. A memory space is prefetchable if there are no side effects on reads (that is, data is not destroyed by reading, as from a RAM). Byte write operations can be merged into a single doubleword write, when applicable.

When configuring the core as a PCI Express Endpoint (non-Legacy), 64-bit addressing must be supported for all BARs (except BAR5) that have the prefetchable bit set. 32-bit addressing is permitted for all BARs that do not have the prefetchable bit set. The prefetchable bit related requirement does not apply to a Legacy Endpoint. In either of the above cases (PCI Express Endpoint or Legacy Endpoint), the minimum memory address range supported by a BAR is 128 bytes.

Disabling Unused Resources

For best results, disable unused base address registers to trim associated logic. A base address register is disabled by deselecting unused BARs in the GUI.

Configuration Register Settings

The Configuration Registers screens (Figure 4-5 and Figure 4-6) let you set options for the Capabilities register, Device Capabilities register, and Link Capabilities register.

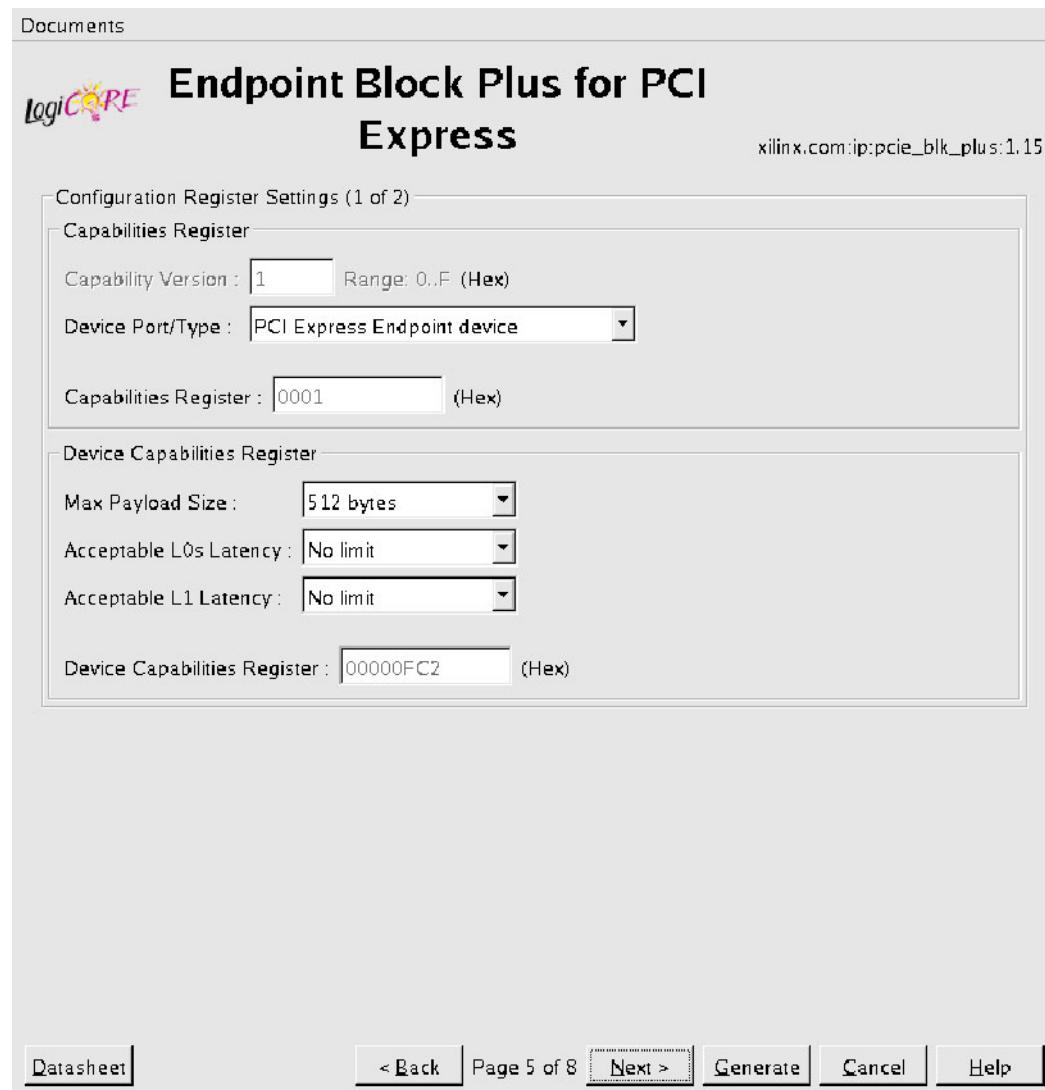


Figure 4-5: Configuration Settings: Screen 5

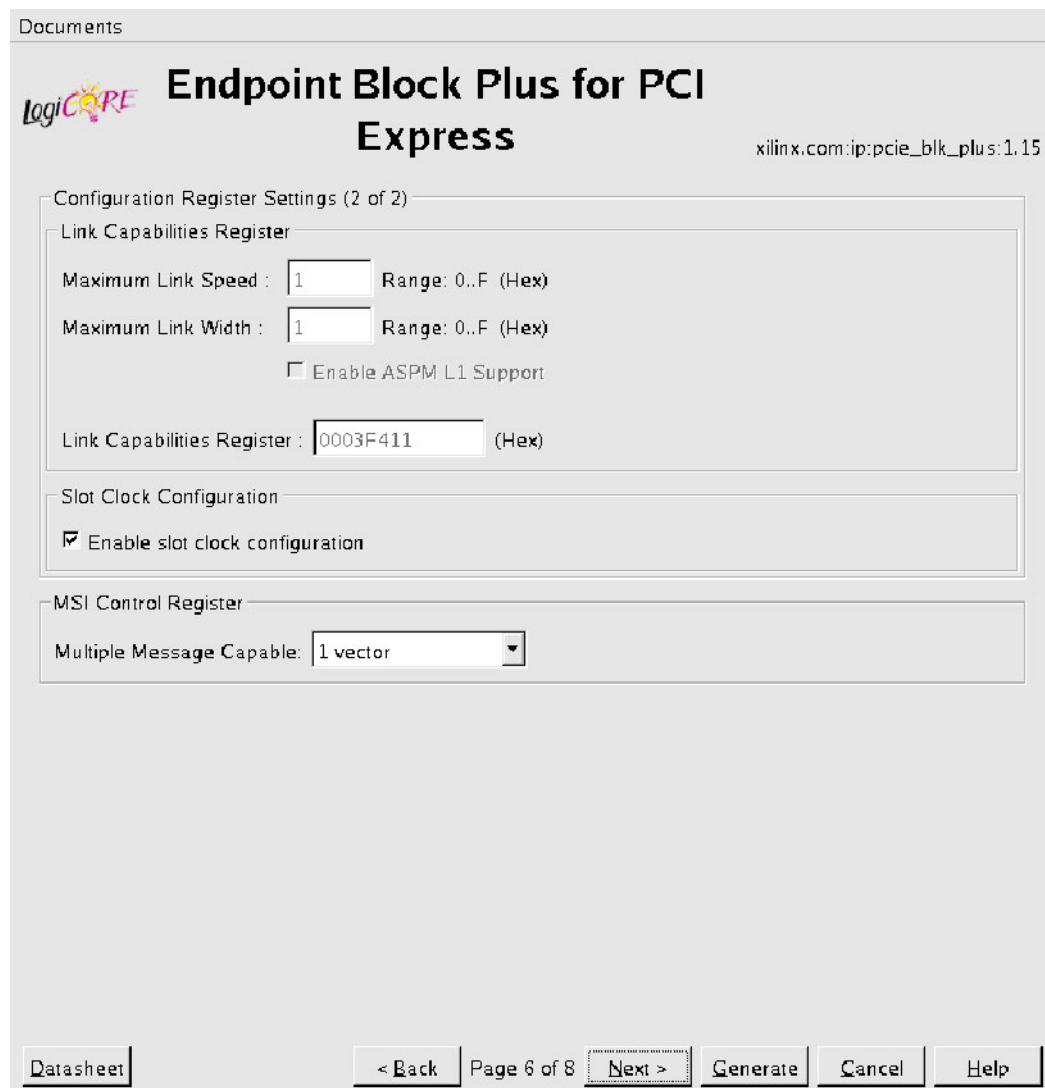


Figure 4-6: Configuration Settings: Screen 6

Capabilities Register

- **Capability Version.** Indicates PCI-SIG defined PCI Express capability structure version number; this value cannot be changed.
- **Device Port Type.** Indicates the PCI Express logical device type.
- **Capabilities Register.** Displays the value of the Capabilities register sent to the core, and is not editable.

Device Capabilities Register

- **Max Payload Size:** Indicates the maximum payload size that the device/function can support for TLPs.
- **Acceptable L0s Latency:** Indicates the acceptable total latency that an Endpoint can withstand due to the transition from L0s state to the L0 state.

- **Acceptable L1 Latency:** Indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state.
- **Device Capabilities Register:** Displays the value of the Device Capabilities register sent to the core, and is not editable.

Link Capabilities Register

This section is used to set the Link Capabilities register.

- **Maximum Link Speed:** Indicates the maximum link speed of the given PCI Express Link. This value is set to 2.5 Gbps and is not editable.
- **Maximum Link Width:** This value is set to the initial lane width specified in the first GUI screen and is not editable.
- **Enable ASPM L1 Support:** Indicates the level of ASPM supported on the given PCI Express Link. Only L0s entry is supported by the Block Plus core; this field is not editable.
- **Link Capabilities Register:** Displays the value of the Link Capabilities register sent to the core and is not editable.

Slot Clock Configuration

Enable Slot Clock Configuration: Indicates that the Endpoint uses the platform-provided physical reference clock available on the connector. Must be cleared if the Endpoint uses an independent reference clock.

MSI Control Register

Multiple Message Capable. Selects the number of MSI vectors to request from the Root Complex.

Advanced Settings

The Advanced Settings screens (Figure 4-7 and Figure 4-8) include settings for the Transaction layer, Physical layer, power consumption, power management registers, power consumption, and power dissipation options.

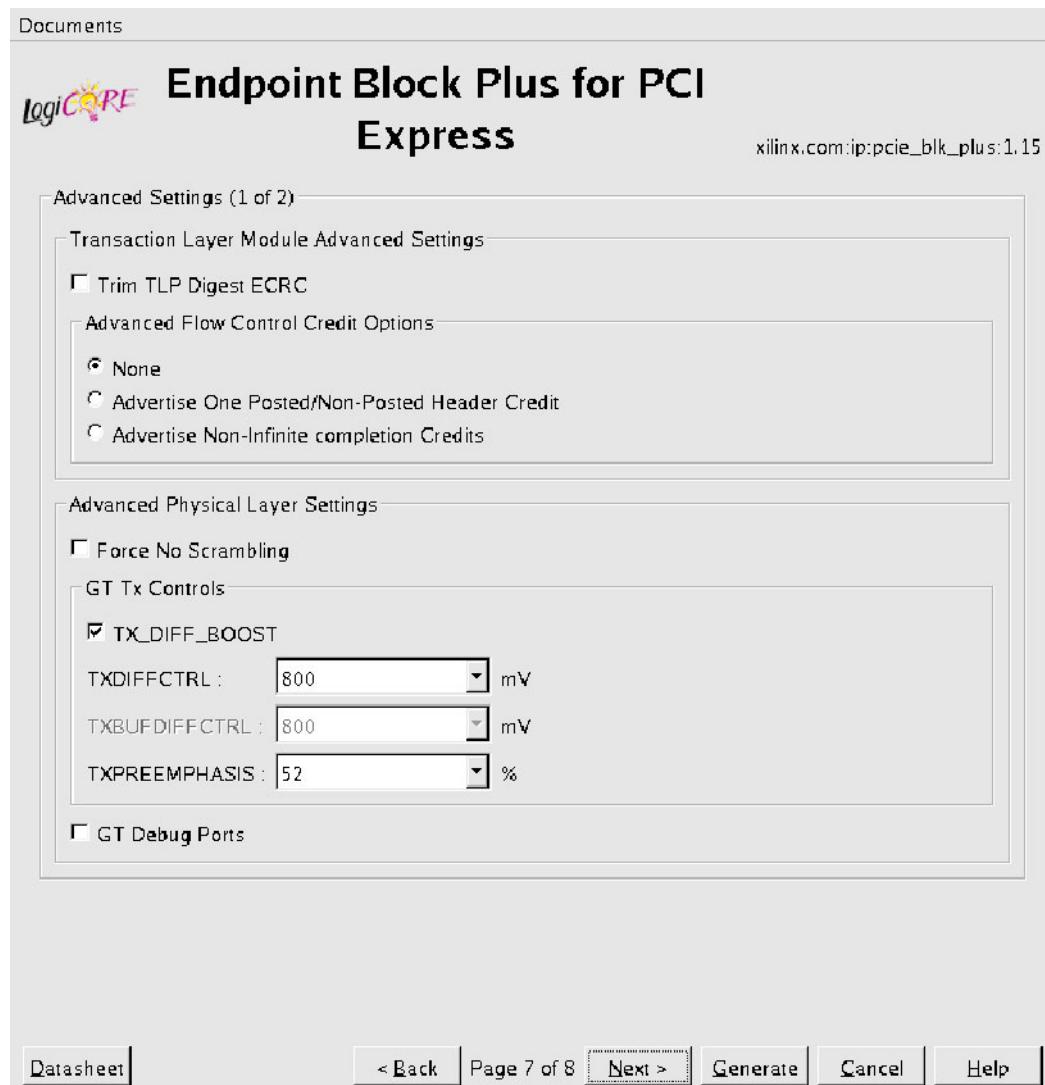


Figure 4-7: Advanced Settings: Screen 7

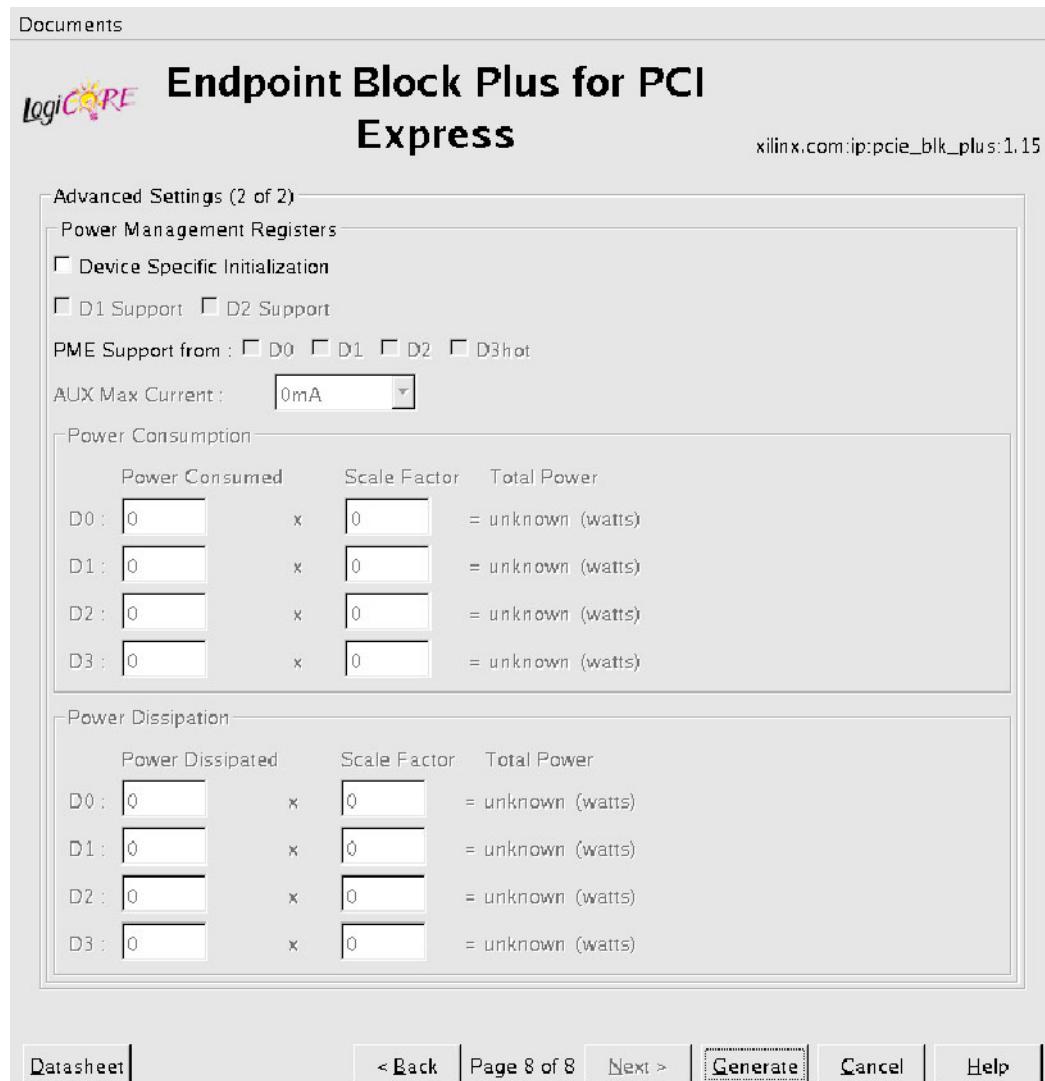


Figure 4-8: Advanced Settings: Screen 8

Transaction Layer Module

Trim TLP Digest ECRC. Causes the core to trim any TLP digest from an inbound packet before presenting it to the user.

Advanced Flow Control Credit

- **None.** No special flow control options are selected—this is the default selection for x4 cores using a 250 MHz interface frequency or x1 cores.
- **Advertise 1 Posted / Non-Posted Header Credit.** Causes the Endpoint to advertise one posted and one non-posted header flow control credit to the upstream device. This is the default selection for x4 cores using a 125 MHz interface frequency or x8 cores using a 125 MHz or 250 MHz interface frequency. See “[Using One Posted/Non-Posted Header Credit, page 110](#)”.

- **Advertise Non-Infinite Completion Credits.** The *PCI Express Base Specification* requires that Endpoints advertise infinite completion credits. This option allows the user to disregard the specification requirement and advertise non-infinite completion credits. See [Non-Infinite Completion Credits, page 110](#) for details.

Advanced Physical Layer

- **Force No Scrambling.** Used for diagnostic purposes only and should never be enabled in a working design. Setting this bit results in the data scramblers being turned off so that the serial data stream can be analyzed.

GT TX Controls

- **TX_DIFF_BOOST.** This option changes the strength of the TX driver and the pre-emphasis buffers. Setting this to TRUE causes the pre-emphasis percentage to be boosted or increased and the overall differential swing to be reduced. This option does not exist for the GTX transceiver.
- **TXDIFFCTRL.** This setting controls the differential output swing of the transmitter.
- **TXBUFDIFFCTRL.** This setting controls the strength of the pre-drivers and is tied to the setting of TXDIFFCTRL for the GTP transceiver.
- **TXPREEMPHASIS.** This setting controls the relative strength of the main drive and the pre-emphasis
- **Transceiver Debug Ports.** Checking this box enables the generation of DRP ports for the GTP/GTX transceivers, allowing dynamic control over the GTP/GTX transceiver attributes. This setting can be used to perform advanced debugging, and any modifications to the transceiver default attributes must be made only if directed by Xilinx Technical Support. On selecting this option, the core is generated with the transceiver DRP ports which are generated per tile, with the exception of the DRP interface clock port.

Note: The example design does not include support for cores with the GT Debug Ports option enabled.

For descriptions of these ports, see the “Dynamic Reconfiguration Port (DRP)” section in the Tile Features chapter in the Virtex®-5 FPGA RocketIO™ Transceiver User Guides.

The additional ports generated are shown in [Table 4-3](#).

Table 4-3: GT DRP Ports¹

Port Name	Direction
gt_dclk	In
gt<n>_daddr[6:0] ²	In
gt<n>_dwren	In
gt<n>_den	In
gt<n>_di[15:0]	In
gt<n>_drdy	Out
gt<n>_do[15:0]	Out

1. Any modifications to the transceiver attributes, by use of these ports, should only be made if directed by Xilinx Technical Support.

2. <n>= 0: Lanes 0 & 1; 2: Lanes 2 & 3; 4: Lanes 4 & 5, 6: Lanes 6 & 7.

Power Management Registers

- **Device Specific Initialization.** This bit indicates whether special initialization of this function is required (beyond the standard PCI configuration header) before the generic class device driver is able to use it. When selected, this option indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state. See section 3.2.3 of the *PCI Bus Power Management Interface Specification Revision 1.2*.
- **D1 Support.** Option disabled; not supported by the core. See section 3.2.3 of the *PCI Bus Power Management Interface Specification Revision 1.2*.
- **D2 Support.** Option disabled; not supported by the core. See section 3.2.3 of the *PCI Bus Power Management Interface Specification Revision 1.2*.
- **PME Support From:** Option disabled; not supported by the core. See section 3.2.3 of the *PCI Bus Power Management Interface Specification Revision 1.2*.
- **AUX Max Current.** The core always reports an auxiliary current requirement of 0 mA. See section 3.2.3 of the *PCI Bus Power Management Interface Specification Revision 1.2*.

Power Consumption

The Block Plus core for PCIe always reports a power budget of 0W. For information about power consumption, see section 3.2.6 of the *PCI Bus Power Management Interface Specification Revision 1.2*.

Power Dissipated

The Block Plus core for PCIe always reports a power dissipation of 0W. For information about power dissipation, see section 3.2.6 of the *PCI Bus Power Management Interface Specification Revision 1.2*.

Designing with the Core

This chapter provides design instructions for the Endpoint Block Plus for PCI Express® User Interface and assumes knowledge of the PCI Express Transaction Layer Packet (TLP) header fields. Header fields are defined in *PCI Express Base Specification v1.1*, Chapter 2, Transaction Layer Specification.

This chapter includes the following design guidelines:

- [TLP Format on the Transaction Interface](#)
- [Transmitting Outbound Packets](#)
- [Receiving Inbound Packets](#)
- [Accessing Configuration Space Registers](#)
- [Additional Packet Handling Requirements](#)
- [Power Management](#)
- [Generating Interrupt Requests](#)
- [Link Training: 2-Lane, 4-Lane and 8-Lane Endpoints](#)
- [Lane Reversal](#)
- [Clocking and Reset of the Block Plus Core](#)

TLP Format on the Transaction Interface

Data is transmitted and received in Big-Endian order as required by the *PCI Express Base Specification*. See Chapter 2 of the *PCI Express Base Specification* for detailed information about TLP packet ordering. [Figure 5-1](#) represents a typical 32-bit addressable Memory Write Request TLP (as illustrated in Chapter 2 of the specification).

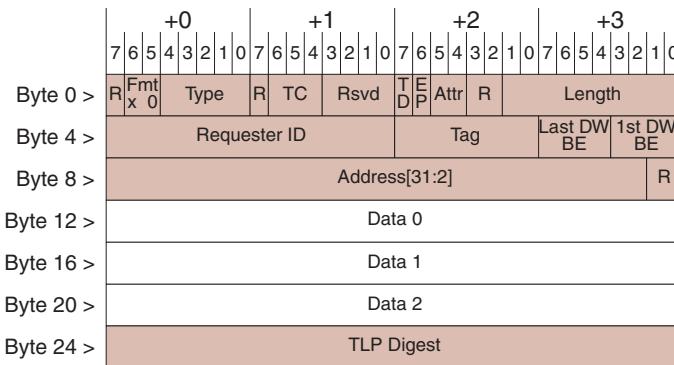


Figure 5-1: PCI Express Base Specification Byte Order

When using the Transaction interface, packets are arranged on the entire 64-bit datapath. [Figure 5-2](#) shows the same example packet on the Transaction interface. Byte 0 of the packet appears on `trn_td[63:56]` (outbound) or `trn_rd[63:56]` (inbound) of the first QWORD, byte 1 on `trn_td[55:48]` or `trn_rd[55:48]`, and so forth. Byte 8 of the packet then appears on `trn_td[63:56]` or `trn_rd[63:56]` of the second QWORD. The Header section of the packet consists of either three or four DWORDs, determined by the TLP format and type as described in section 2.2 of the *PCI Express Base Specification*.

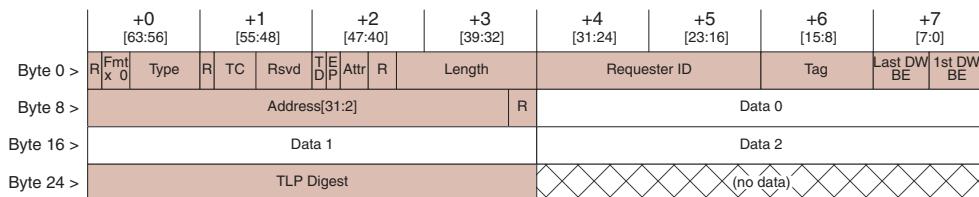


Figure 5-2: Endpoint Block Plus Byte Order

Packets sent to the core for transmission must follow the formatting rules for Transaction Layer Packets (TLPs) as specified in Chapter 2 of the *PCI Express Base Specification*. The User Application is responsible for ensuring its packets' validity, as the core does not check packet validity or validate packets. The exact fields of a given TLP vary depending on the type of packet being transmitted.

The presence of a TLP Digest or ECRC is indicated by the value of TD field in the TLP Header section. When TD=1, a correctly computed CRC32 remainder is expected to be presented as the last DWORD of the packet. The CRC32 remainder DWORD is not included in the length field of the TLP header. The User Application must calculate and present the TLP Digest as part of the packet when transmitting packets. Upon receiving packets with a TLP Digest present, the User Application must check the validity of the CRC32 based on the contents of the packet. The core does not check the TLP Digest for incoming packets.

Transmitting Outbound Packets

Basic TLP Transmit Operation

The Block Plus core for PCIe® automatically transmits the following types of packets:

- Completions to a remote device in response to Configuration Space requests.
- Error-message responses to inbound requests malformed or unrecognized by the core.

Note: Certain unrecognized requests, for example, unexpected completions, can only be detected by the User Application, which is responsible for generating the appropriate response.

The User Application is responsible for constructing these types of outbound packets:

- Memory and I/O Requests to remote devices.
- Completions in response to requests to the User Application, for example, a Memory Read Request.

The Block Plus core for PCIe performs weighted round-robin arbitration between packets presented on the transmit interface and packets formed on the Configuration Interface (user-reported error conditions and interrupts), with a priority for Configuration Interface packets.

[Table 2-9, page 35](#) defines the transmit User Application signals. To transmit a TLP, the User Application must perform the following sequence of events on the transmit Transaction interface:

1. The User Application logic asserts `trn_tsrdy_n`, `trn_tsof_n` and presents the first TLP QWORD on `trn_td[63:0]` when it is ready to transmit data. If the core is asserting `trn_tdst_rdy_n`, the QWORD is accepted immediately; otherwise, the User Application must keep the QWORD presented until the core asserts `trn_tdst_rdy_n`.
2. The User Application asserts `trn_tsrdy_n` and presents the remainder of the TLP QWORDs on `trn_td[63:0]` for subsequent clock cycles (for which the core asserts `trn_tdst_rdy_n`).
3. The User Application asserts `trn_tsrdy_n` and `trn_teof_n` together with the last QWORD data. If all 8 data bytes of the last transfer are valid, they are presented on `trn_td[63:0]` and `trn_trem_n[7:0]` is driven to 00h; otherwise, the 4 remaining data bytes are presented on `trn_td[63:32]` and `trn_trem_n[7:0]` is driven to 0Fh.
4. At the next clock cycle, the User Application deasserts `trn_tsrdy_n` to signal the end of valid transfers on `trn_td[63:0]`.

Figure 5-3 illustrates a 3-DW TLP header without a data payload; an example is a 32-bit addressable Memory Read request. When the User Application asserts `trn_teof_n`, it also places a value of 0Fh on `trn_trem_n[7:0]` notifying the core that only `trn_td[63:32]` contains valid data.

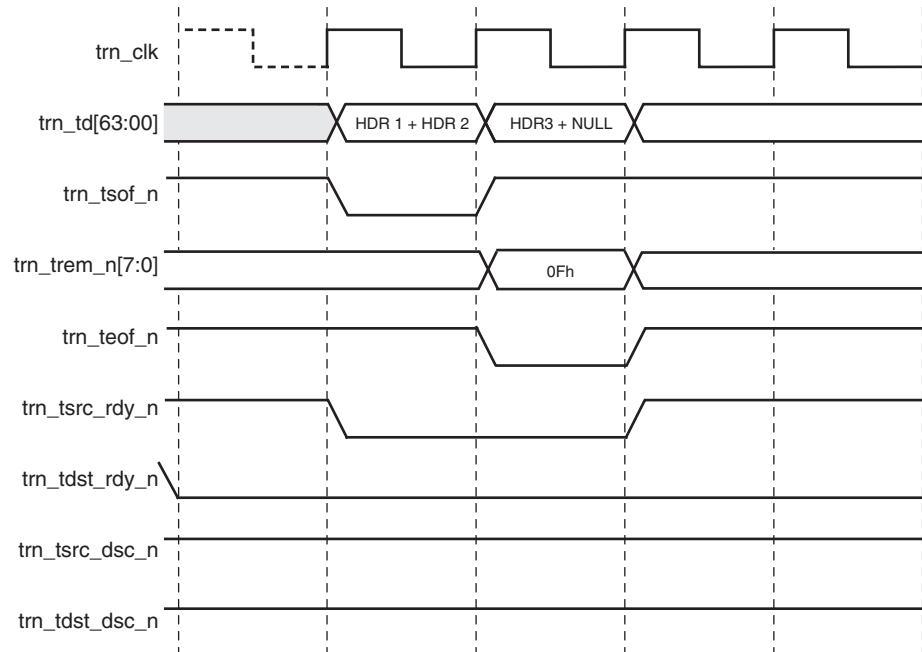


Figure 5-3: TLP 3-DW Header without Payload

Figure 5-4 illustrates a 4-DW TLP header without a data payload; an example is a 64-bit addressable Memory Read request. When the User Application asserts `trn_teof_n`, it also places a value of 00h on `trn_trem_n[7:0]` notifying the core that `trn_td[63:00]` contains valid data.

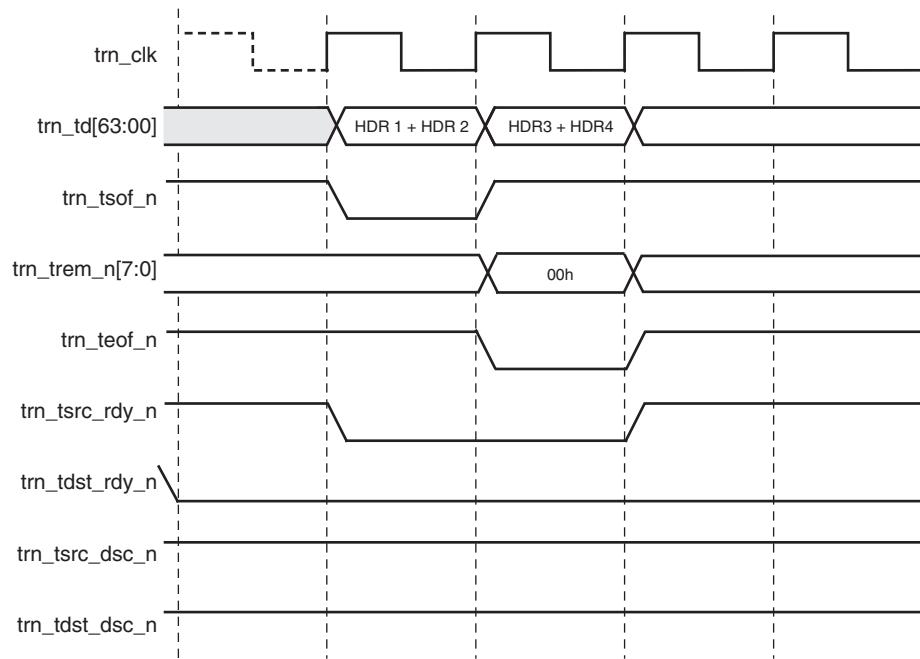


Figure 5-4: TLP with 4-DW Header without Payload

Figure 5-5 illustrates a 3-DW TLP header with a data payload; an example is a 32-bit addressable Memory Write request. When the User Application asserts `trn_teof_n`, it also puts a value of 00h on `trn_trem_n[7:0]` notifying the core that `trn_td[63:00]` contains valid data. The user must ensure the remainder field selected for the final data cycle creates a packet of length equivalent to the length field in the packet header.

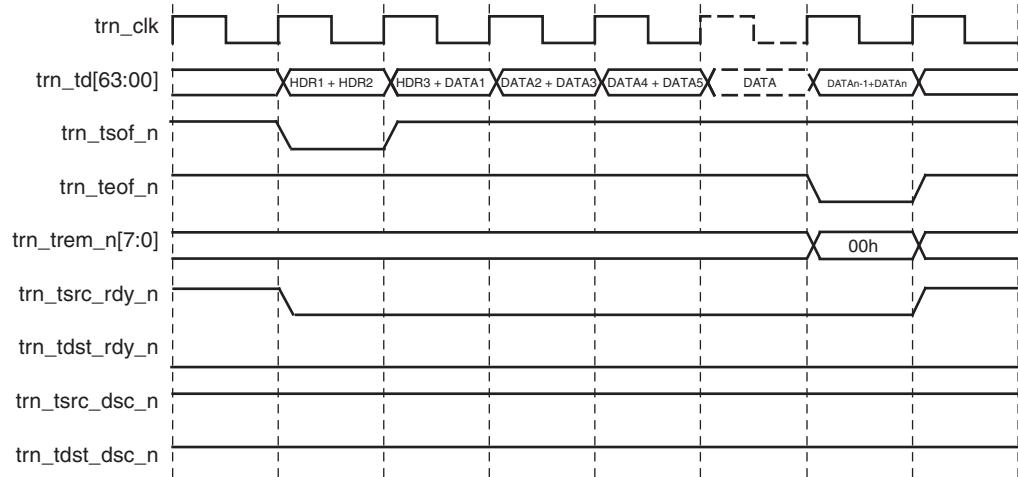


Figure 5-5: TLP with 3-DW Header with Payload

Figure 5-6 illustrates a 4-DW TLP header with a data payload; an example is a 64-bit addressable Memory Write request. When the User Application asserts `trn_teof_n`, it also places a value of 0Fh on `trn_trem_n[7:0]`, notifying the core that only `trn_td[63:32]` contains valid data. The user must ensure the remainder field is selected for the final data cycle creates a packet of length equivalent to the length field in the packet header.

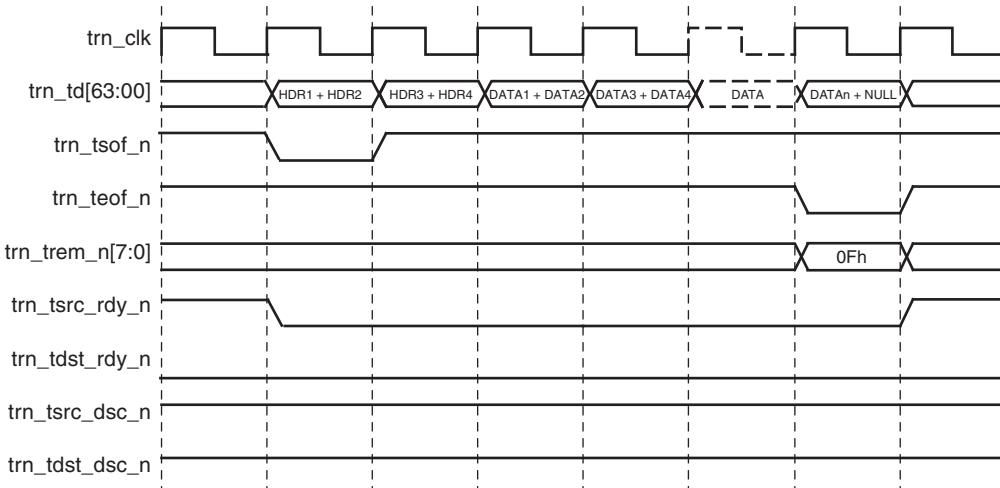


Figure 5-6: TLP with 4-DW Header with Payload

Presenting Back-to-Back Transactions on the Transmit Interface

The User Application can present back-to-back TLPs on the transmit Transaction interface to maximize bandwidth utilization. **Figure 5-7** illustrates back-to-back TLPs presented on the transmit interface. The User Application asserts `trn_tsوف_n` and presents a new TLP on the next clock cycle after asserting `trn_teof_n` for the previous TLP.

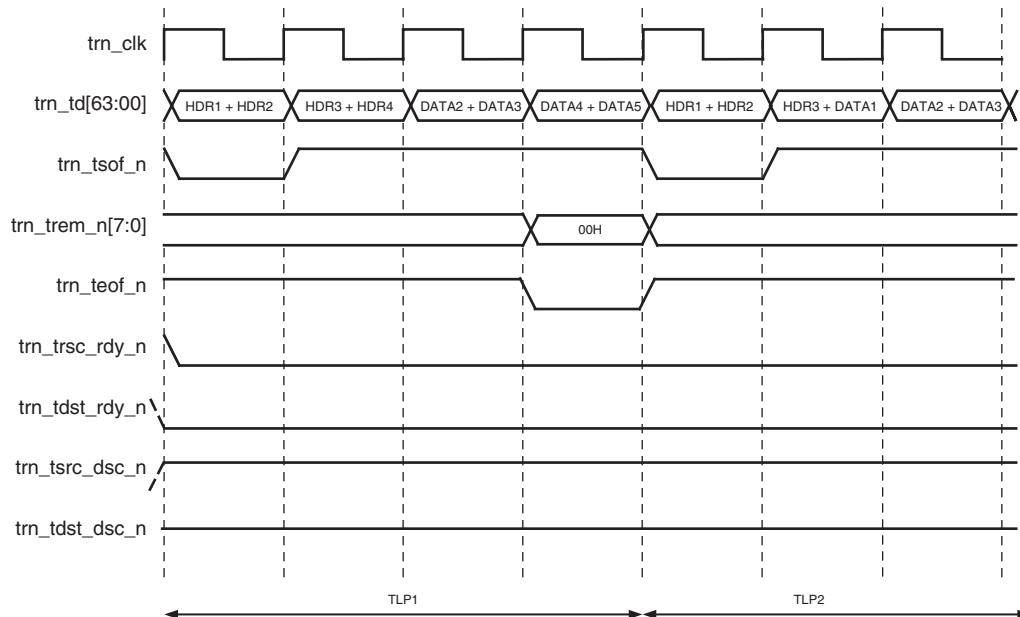


Figure 5-7: Back-to-Back Transaction on Transmit Transaction Interface

Source Throttling on the Transmit Datapath

The Block Plus core for PCIe Transaction interface lets the User Application throttle back if it has no data to present on `trn_td[63:0]`. When this condition occurs, the User Application deasserts `trn_tsrdy_n`, which instructs the core Transaction interface to disregard data presented on `trn_td[63:0]`. [Figure 5-8](#) illustrates the source throttling mechanism, where the User Application does not have data to present every clock cycle, and for this reason must deassert `trn_tsrdy_n` during these cycles.

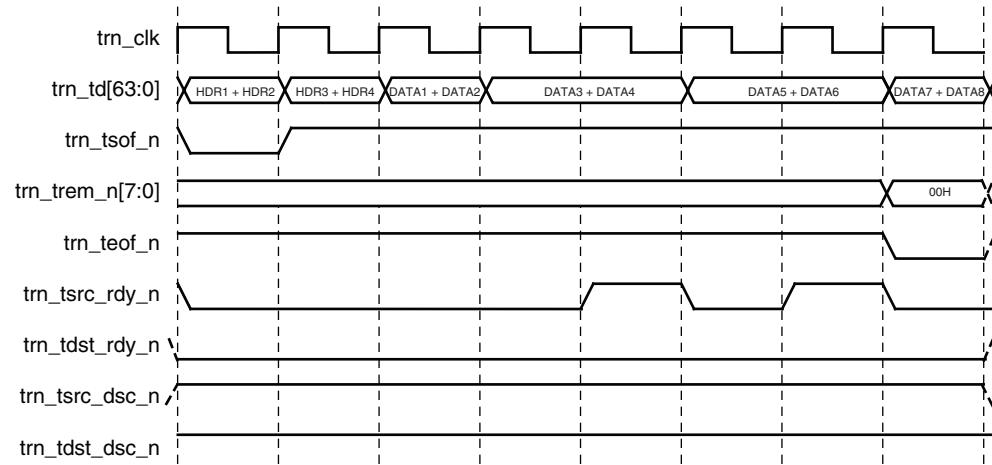


Figure 5-8: Source Throttling on the Transmit Datapath

Destination Throttling of the Transmit Datapath

The core Transaction interface throttles the transmit User Application if there is no space left for a new TLP in its transmit buffer pool. This can occur if the link partner is not processing incoming packets at a rate equal to or greater than the rate at which the User Application is presenting TLPs. Figure 5-9 illustrates the deassertion of `trn_tdst_rdy_n` to throttle the User Application when the core's internal transmit buffers are full.

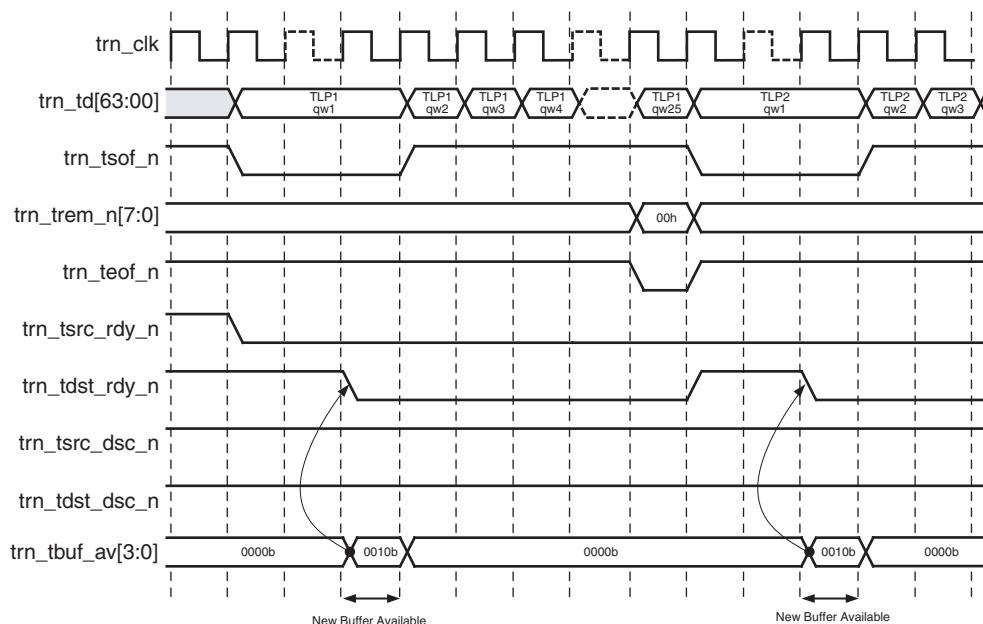


Figure 5-9: Destination Throttling of the Endpoint Transmit Transaction Interface

The core transmit Transaction interface throttles the User Application when the Power State field in Power Management Control/Status Register (Offset 0x4) of the PCI Power Management Capability Structure is changed to a non-D0 state. When this occurs, any on-going TLP is accepted completely and `trn_tdst_rdy_n` is subsequently deasserted, disallowing the User Application from initiating any new transactions—for the duration that the core is in the non-D0 power state.

Discontinuing Transmission of Transaction by Source

The core Transaction interface lets the User Application terminate transmission of a TLP by asserting `trn_tsdc_n`. Both `trn_tsdc_rdy_n` and `trn_tdst_rdy_n` must be asserted together with `trn_tsdc_n` for the TLP to be discontinued. The signal `trn_tsdc_n` must not be asserted together with `trn_tsof_n`. It can be asserted on any cycle after `trn_tsof_n` deasserts up to and including the assertion of `trn_teof_n`. Asserting `trn_tsdc_n` has no effect if no TLP transaction is in progress on the transmit interface. Figure 5-10 illustrates the User Application discontinuing a packet using `trn_tsdc_n`. Asserting `trn_teof_n` together with `trn_tsdc_n` is optional.

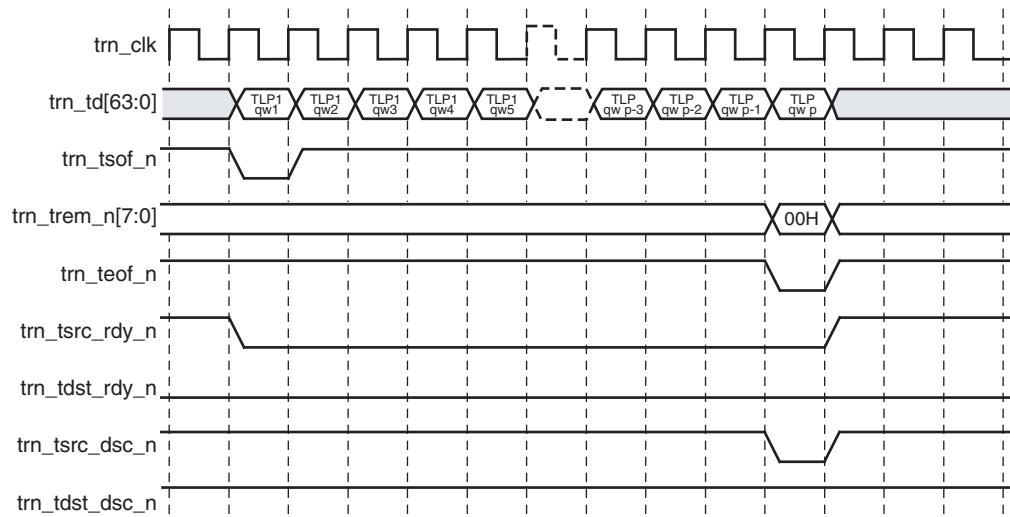


Figure 5-10: Source Driven Transaction Discontinue on Transmit Interface

Packet Data Poisoning on the Transmit Transaction Interface

The User Application uses the following mechanism to mark the data payload of a transmitted TLP as poisoned:

- Set EP=1 in the TLP header. This mechanism can be used if the payload is known to be poisoned when the first DWORD of the header is presented to the core on the TRN interface.

Appending ECRC to Protect TLPs

If the User Application needs to send a TLP Digest associated with a TLP, it must construct the TLP header such that the TD bit is set and the User Application must properly compute and append the 1-DWORD TLP Digest after the last valid TLP payload section (if applicable).

Maximum Payload Size

TLP size is restricted by the capabilities of both link partners. A maximum-sized TLP is a TLP with a 4-DWORD header plus a data payload equal to the MAX_PAYLOAD_SIZE of the core (as defined in the Device Capability register) plus a TLP Digest. After the link is trained, the root complex sets the MAX_PAYLOAD_SIZE value in the Device Control register. This value is equal to or less than the value advertised by the core's Device Capability register. The advertised value in the Device Capability register of the Block Plus

core is either 128, 256, or 512 bytes, depending on the setting in the CORE Generator™ tool GUI. For more information about these registers, see section 7.8 of the *PCI Express Base Specification*. The value of the core's Device Control register is provided to the user application on the `cfg_dcommand[15:0]` output. See [Accessing Configuration Space Registers](#) for information about this output.

Transmit Buffers

The Endpoint Block Plus core for PCIe provides buffering for up to 8 TLPs per transaction type: posted, non-posted, and completion. However, the actual number that can be buffered depends on the size of each TLP. There is space for a maximum of three 512 byte (or seven 256 byte) posted TLPs, three 512 byte (or seven 256 byte) completion TLPs, and 8 non-posted TLPs. Transmission of smaller TLPs allows for more TLPs to be buffered, but never more than 8 per type.

Outgoing TLPs are held in the core's transmit buffer until transmitted on the PCI Express interface. After a TLP is transmitted, it is stored in an internal retry buffer until the link partner acknowledges receipt of the packet.

The Endpoint Block Plus for PCIe core supports the PCI Express transaction ordering rules and promotes Posted and Completion packets ahead of blocked Non-Posted TLPs.

Non-Posted TLPs can become blocked if the link partner is in a state where it momentarily has no Non-Posted receive buffers available, which it advertises through Flow Control updates. In this case, the core promotes Completion and Posted TLPs ahead of these blocked Non-Posted TLPs. However, this can only occur if the Completion or Posted TLP has been loaded into the core by the User Transmit Application. Promotion of Completion and Posted TLPs only occurs when Non-Posted TLPs are blocked; otherwise, packets are sent on the link in the order they are received from the user transmit application. See section 2.4 of the *PCI Express Base Specification* for more information about ordering rules.

The Transmit Buffers Available (`trn_tbuf_av[3:0]`) signal enables the User Application to completely utilize the PCI transaction ordering feature of the core transmitter. By monitoring the `trn_tbuf_av` bus, the User Application can ensure at least one free buffer available for any Completion or Posted TLP. [Table 5-1](#) defines the `trn_tbuf_av[3:0]` bits. A value of 1 indicates that the core can accept at least 1 TLP of that particular credit class. A value of 0 indicates that no buffers are available in that particular queue.

The `trn_tbuf_av[3]` bit indicates that the core might be about to run out of Completion Queue buffers. If this is deasserted, performance can be optimized by sending a Posted or Non-Posted TLP instead of a Completion TLP. If a Completion TLP is sent when this signal is deasserted, the core can be forced to stall the TRN interface for all TLP types until new Completion Queue buffers become available.

Table 5-1: trn_tbuf_av[3:0] Bits

Bit	Definition
<code>trn_tbuf_av[0]</code>	Non-posted buffer available
<code>trn_tbuf_av[1]</code>	Posted buffer available
<code>trn_tbuf_av[2]</code>	Completion buffer available
<code>trn_tbuf_av[3]</code>	Look-Ahead Completion buffer

Receiving Inbound Packets

Basic TLP Receive Operation

Table 2-10, page 36 defines the receive Transaction interface signals. The following sequence of events must occur on the receive Transaction interface for the Endpoint core to present a TLP to the User Application logic:

1. When the User Application is ready to receive data, it asserts `trn_rdst_rdy_n`.
2. When the core is ready to transfer data, the core asserts `trn_rsrc_rdy_n` with `trn_rsrf_n` and presents the first complete TLP QWORD on `trn_rd[63:0]`.
3. The core then deasserts `trn_rsrf_n`, asserts `trn_rsrc_rdy_n`, and presents TLP QWORDs on `trn_rd[63:0]` for subsequent clock cycles, for which the User Application logic asserts `trn_rdst_rdy_n`.
4. The core then asserts `trn_rsrc_rdy_n` with `trn_reof_n` and presents either the last QWORD on `trn_td[63:0]` and a value of 00h on `trn_rrem_n[7:0]` or the last DWORD on `trn_td[63:32]` and a value of 0Fh on `trn_rrem_n[7:0]`.
5. If no further TLPs are available at the next clock cycle, the core deasserts `trn_rsrc_rdy_n` to signal the end of valid transfers on `trn_rd[63:0]`.

Note: The user application should ignore any assertions of `trn_rsrf_n`, `trn_reof_n`, `trn_rrem_n`, `trn_rd` unless `trn_rsrc_rdy_n` is concurrently asserted.

Figure 5-11 shows a 3-DW TLP header without a data payload; an example is a 32-bit addressable Memory Read request. When the core asserts `trn_reof_n`, it also places a value of 0Fh on `trn_rrem_n[7:0]`, notifying the user that only `trn_rd[63:32]` contains valid data.

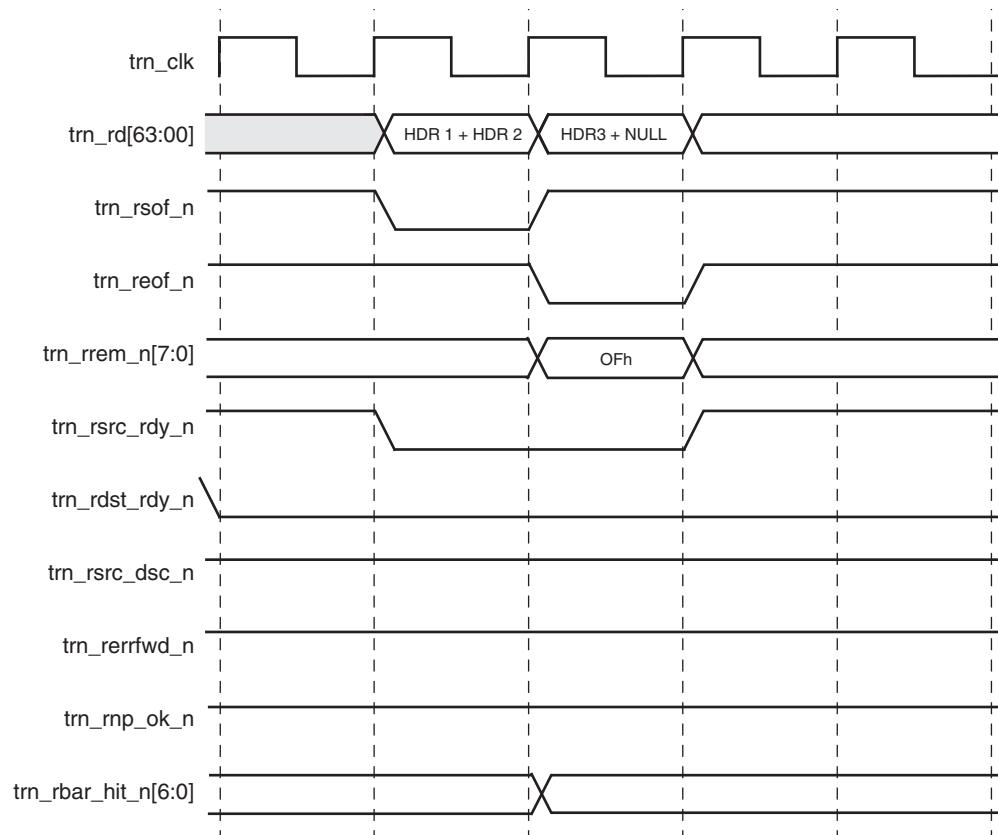


Figure 5-11: TLP 3-DW Header without Payload

Figure 5-12 shows a 4-DW TLP header without a data payload; an example is a 64-bit addressable Memory Read request. When the core asserts `trn_reof_n`, it also places a value of 00h on `trn_rrem_n[7:0]`, notifying the user that `trn_rd[63:0]` contains valid data.

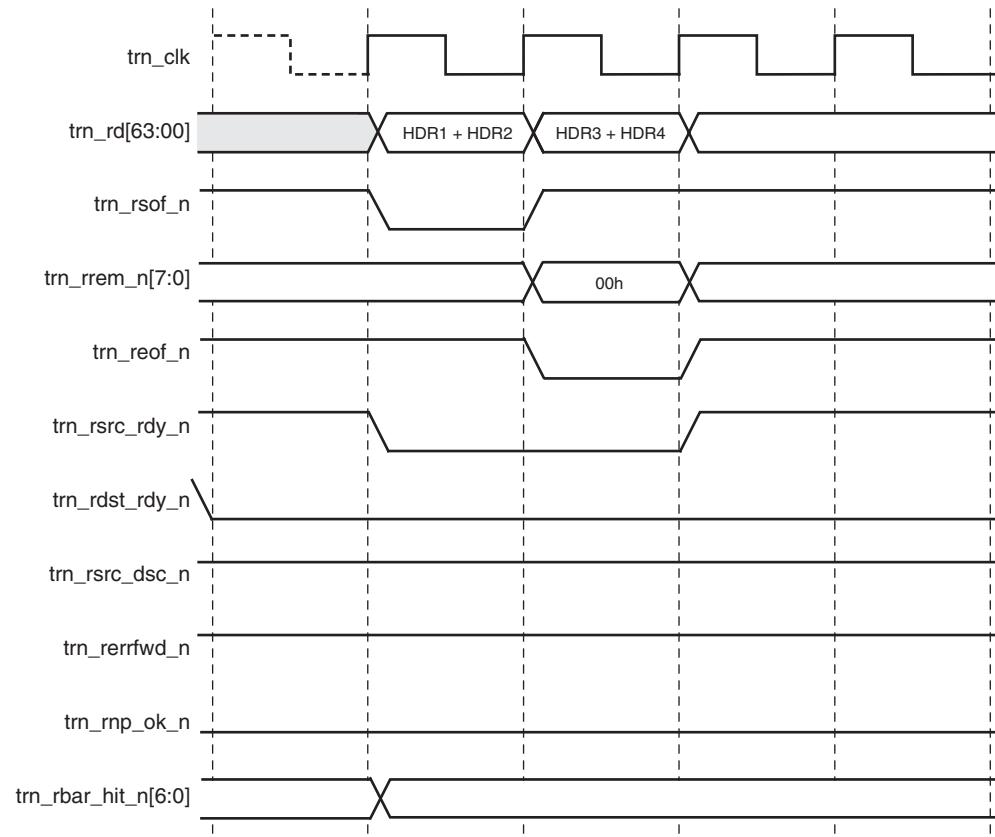


Figure 5-12: TLP 4-DW Header without Payload

Figure 5-13 shows a 3-DW TLP header with a data payload; an example is a 32-bit addressable Memory Write request. When the core asserts `trn_reof_n`, it also places a value of 00h on `trn_rrem_n[7:0]`, notifying the user that `trn_rd[63:00]` contains valid data.

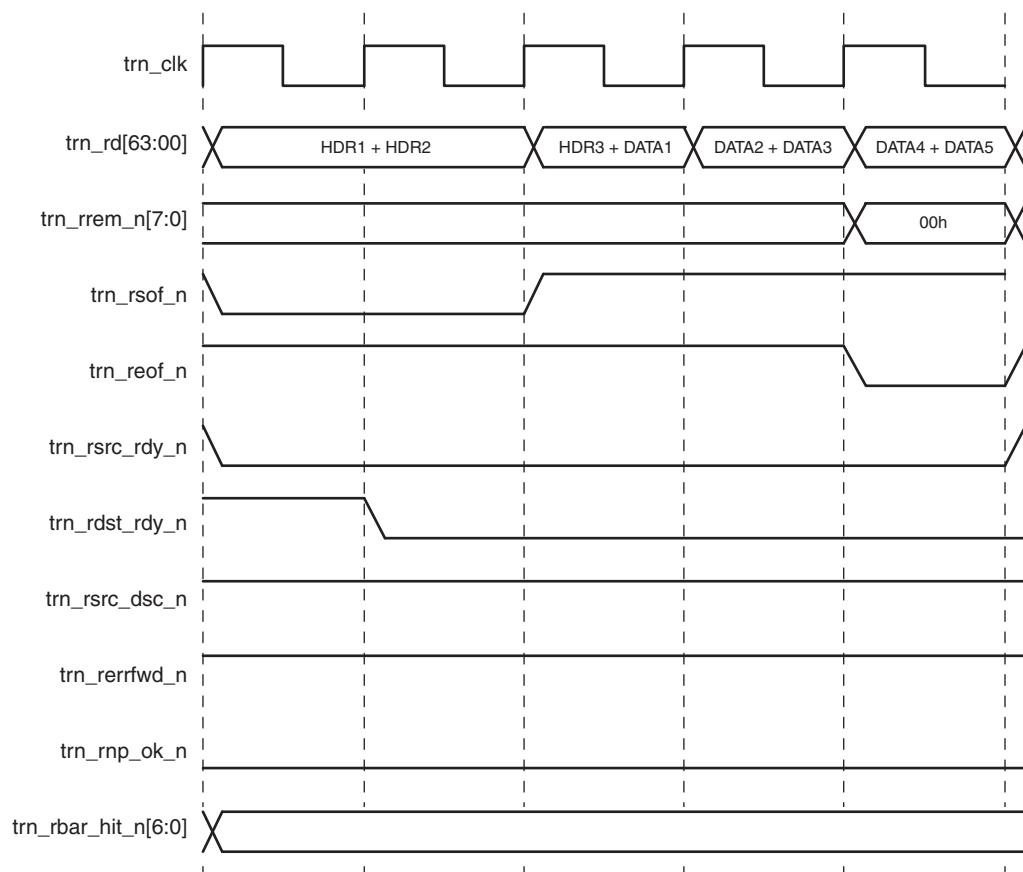


Figure 5-13: TLP 3-DW Header with Payload

Figure 5-14 shows a 4-DW TLP header with a data payload; an example is a 64-bit addressable Memory Write request. When the core asserts `trn_reof_n`, it also places a value of 0Fh on `trn_rrem_n[7:0]`, notifying the user that only `trn_rd[63:32]` contains valid data.

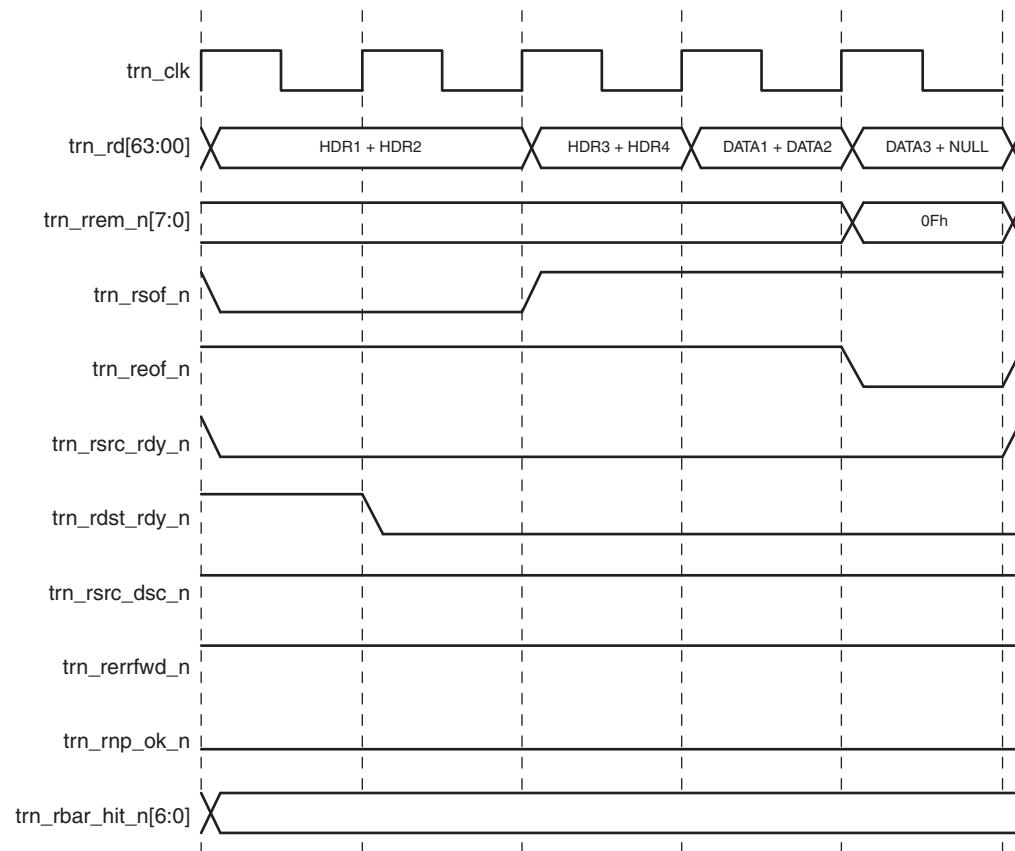


Figure 5-14: TLP 4-DW Header with Payload

Throttling the Datapath on the Receive Transaction Interface

The User Application can stall the transfer of data from the core at any time by deasserting `trn_rdst_rdy_n`. If the user deasserts `trn_rdst_rdy_n` while no transfer is in progress and if a TLP becomes available, the core asserts `trn_rsrc_rdy_n` and `trn_rsosf_n` and presents the first TLP QWORD on `trn_rd[63:0]`. The core remains in this state until the user asserts `trn_rdst_rdy_n` to signal the acceptance of the data presented on `trn_rd[63:0]`. At that point, the core presents subsequent TLP QWORDS as long as `trn_rdst_rdy_n` remains asserted. If the user deasserts `trn_rdst_rdy_n` during the middle of a transfer, the core stalls the transfer of data until the user asserts `trn_rdst_rdy_n` again. There is no limit to the number of cycles the user can keep `trn_rdst_rdy_n` deasserted. The core pauses until the user is again ready to receive TLPs.

Figure 5-15 illustrates the core asserting `trn_rsrc_rdy_n` and `trn_rsosf_n` along with presenting data on `trn_rd[63:0]`. The User Application logic inserts wait states by deasserting `trn_rdst_rdy_n`. The core does not present the next TLP QWORD until it detects `trn_rdst_rdy_n` assertion. The User Application logic can assert or deassert `trn_rdst_rdy_n` as required to balance receipt of new TLP transfers with the rate of TLP data processing inside the application logic.

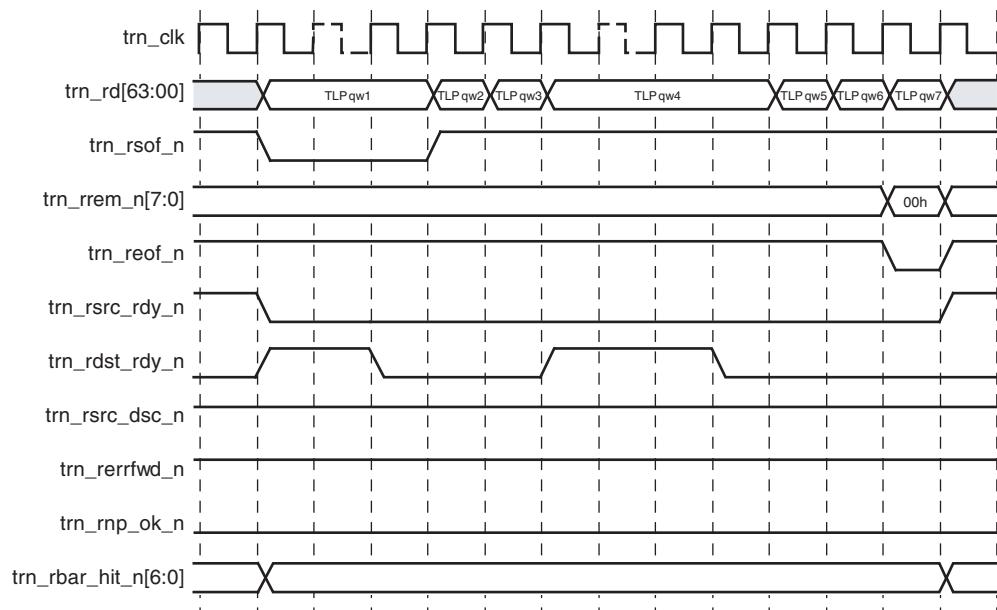


Figure 5-15: User Application Throttling Receive TLP

Receiving Back-to-Back Transactions on the Receive Transaction Interface

The User Application logic must be designed to handle presentation of back-to-back TLPs on the receive Transaction interface by the core. The core can assert `trn_rsوف_n` for a new TLP at the clock cycle after `trn_reof_n` assertion for the previous TLP. [Figure 5-16](#) illustrates back-to-back TLPs presented on the receive interface.

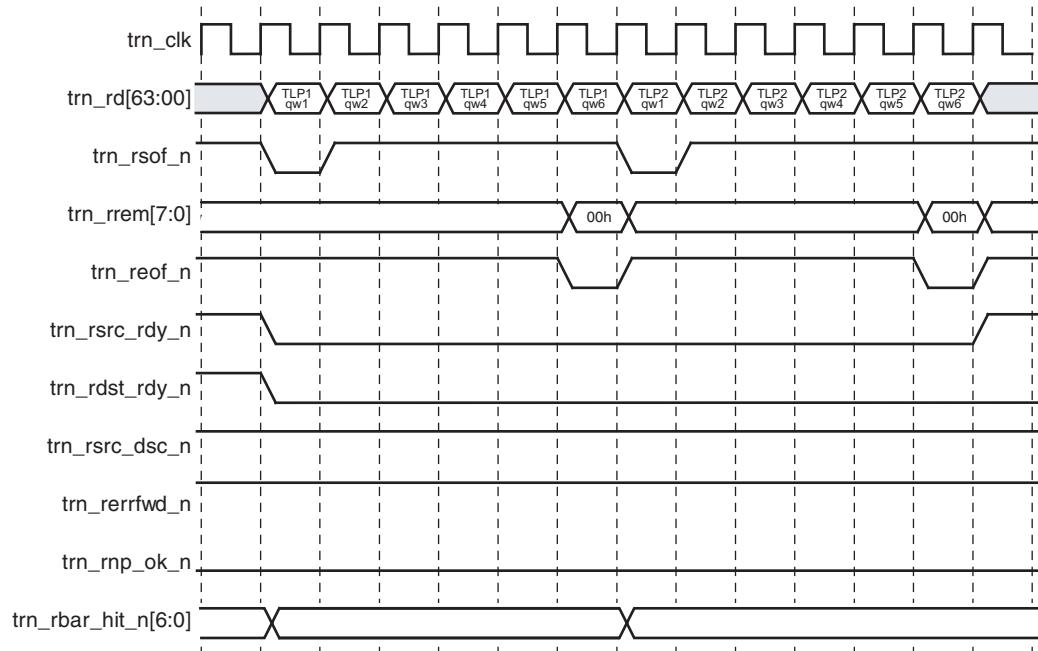


Figure 5-16: Receive Back-to-Back Transactions

If the User Application cannot accept back-to-back packets, it can stall the transfer of the TLP by deasserting `trn_rdst_rdy_n` as discussed in the previous section. [Figure 5-17](#) shows an example of using `trn_rdst_rdy_n` to pause the acceptance of the second TLP.

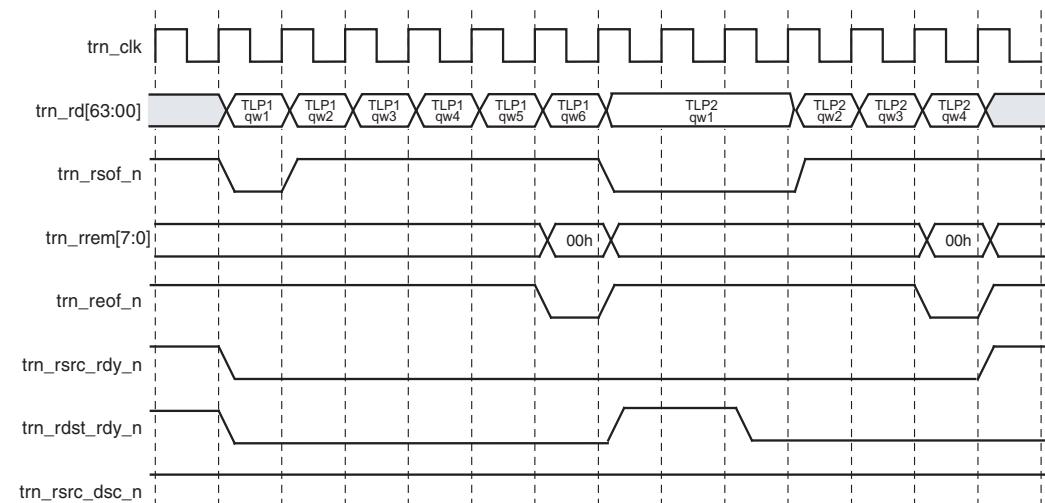


Figure 5-17: User Application Throttling Back-to-Back TLPs

Packet Re-ordering on Receive Transaction Interface

Transaction processing in the core receiver is fully compliant with the PCI transaction ordering rules when `trn_rcpl_streaming_n` is deasserted. The transaction ordering rules allow for Posted and Completion TLPs to bypass Non-Posted TLPs. See section 2.4 of the *PCI Express Base Specification* for more information about the ordering rules. See [Performance Considerations on the Receive Transaction Interface](#) for more information on `trn_rcpl_streaming_n`.

The User Application can deassert the signal `trn_rnp_ok_n` if it is not ready to accept Non-Posted Transactions from the core, as shown in [Figure 5-18](#), but can receive Posted and Completion Transactions. However, users must not deassert `rx_np_ok` for extended periods, because this can cause a completion time-out in the Requester. The User Application must deassert `trn_rnp_ok_n` at least one clock cycle before `trn_eof_n` of the next-to-last non-posted packet the user can accept. While `trn_rnp_ok_n` is deasserted, received Posted and Completion Transactions pass Non-Posted Transactions. After the User Application is ready to accept Non-Posted Transactions, it must reassert `trn_rnp_ok_n`. Previously bypassed Non-Posted Transactions are presented to the User Application before other received TLPs.

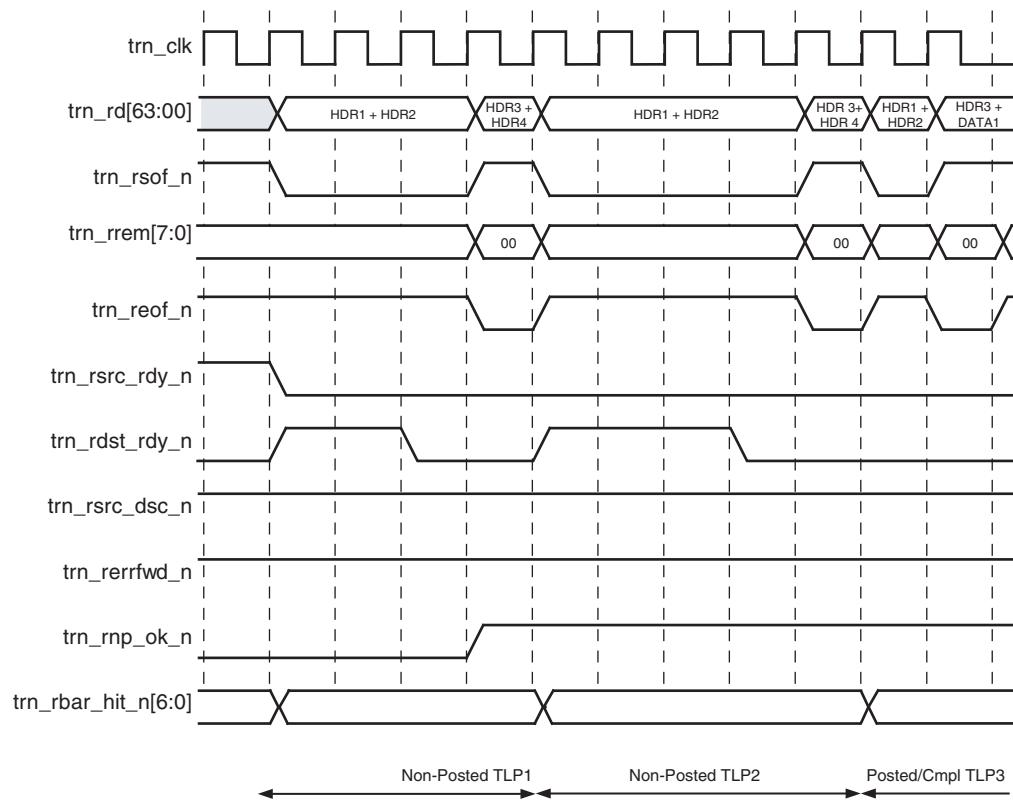


Figure 5-18: Packet Re-ordering on Receive Transaction Interface

To ensure that there is no overflow of Non-Posted storage space available in the user's logic, the following algorithm must be used:

```
For every clock cycle do {
    if (Non-Posted_Buffers_Available <= 2) {
        if (Valid transaction Start-of-Frame accepted by user application) {
            Extract TLP Format and Type from the 1st TLP DW
            if (TLP type == Non-Posted) {
                Deassert trn_rnp_ok_n on the following clock cycle
                - or -
                Other optional user policies to stall NP transactions
            } else {
            }
        }
    } else { // Non-Posted_Buffers_Available > 2
        Assert trn_rnp_ok_n on the following clock cycle.
    }
}
```

The following restrictions must be followed when using `trn_rnp_ok_n` to throttle Non-Posted packets. The user can keep `trn_rnp_ok_n` deasserted as long as `trn_rfc_nph_av` is 8. If `trn_rfc_nph_av` goes below 8, the user must start a counter that counts received Posted packets. The `trn_rfc_nph_av` signal might fluctuate briefly between 8 and lower values as packets are drained into the wrapper. The wrapper will buffer some NP packets. During any type of fluctuation, each time `trn_rfc_nph_av` goes to 8, the count can be restarted. After the count reaches 30, the user must assert `trn_rnp_ok_n` and drain all NP packets until `trn_rfc_nph_av` is 8 again. At that point, `trn_rnp_ok_n` can be deasserted again.

Packet Data Poisoning and TLP Digest on Receive Transaction Interface

To simplify logic within the User Application, the core performs automatic pre-processing based on values of TLP Digest (TD) and Data Poisoning (EP) header bit fields on the received TLP.

All received TLPs with the Data Poisoning bit in the header set (EP = 1) are presented to the user. The core asserts the `trn_rerrfwd_n` signal for the duration of each poisoned TLP, as illustrated in [Figure 5-19](#).

If the TLP Digest bit field in the TLP header is set (TD = 1), the TLP contains an End-to-End CRC (ECRC). The core performs the following operations based on how the user configured the core during core generation:

- If the Trim TLP Digest option is on, the core removes and discards the ECRC field from the received TLP and clears the TLP Digest bit in the TLP header.
- If the Trim TLP Digest option is off, the core does not remove the ECRC field from the received TLP and presents the entire TLP including TLP Digest to the User Application receiver interface.

See [Chapter 4, Generating and Customizing the Core](#) for more information about how to enable the Trim TLP Digest option during core generation.

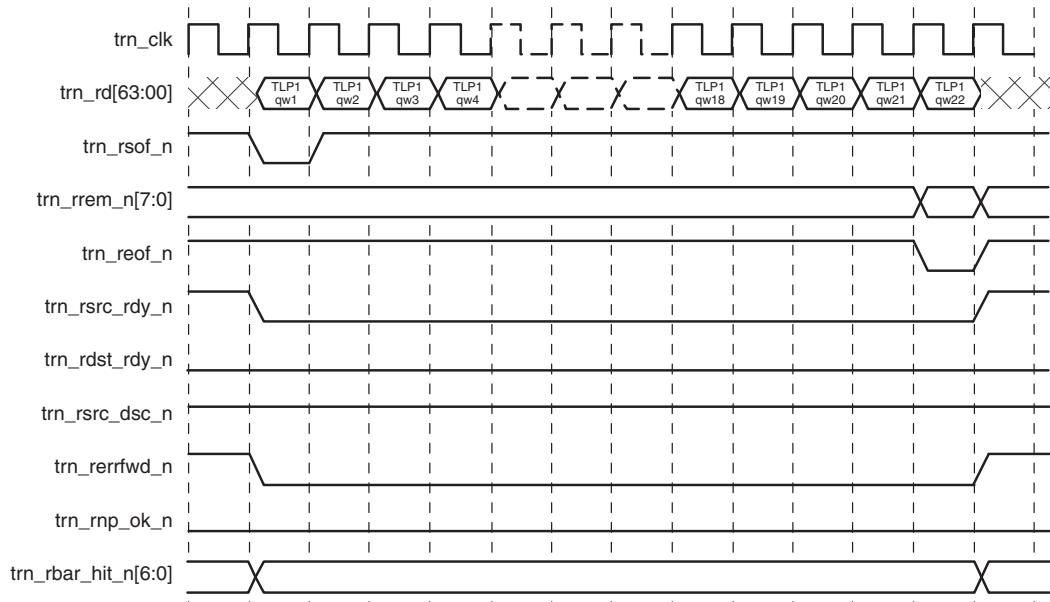


Figure 5-19: Receive Transaction Data Poisoning

Packet Base Address Register Hit on Receive Transaction Interface

The Endpoint core decodes incoming Memory and I/O TLP request addresses to determine which Base Address Register (BAR) in the core's Type0 configuration space is being targeted, and indicates the decoded base address on `trn_rbar_hit_n[6:0]`. For each received Memory or I/O TLP, a minimum of one and a maximum of two (adjacent) bit(s) are set to 1. If the received TLP targets a 32-bit Memory or I/O BAR, only one bit is asserted. If the received TLP targets a 64-bit Memory BAR, two adjacent bits are asserted. If the core receives a TLP that is not decoded by one of the BARs (that is, a misdirected TLP), then the core drops it without presenting it to the user and it automatically generates an Unsupported Request message. Even if the core is configured for a 64-bit BAR, the system might not always allocate a 64-bit address, in which case only one `trn_rbar_hit_n[6:0]` signal is asserted.

[Table 5-2](#) illustrates mapping between `trn_rbar_hit_n[6:0]` and the BARs, and the corresponding byte offsets in the core Type0 configuration header.

Table 5-2: `trn_rbar_hit_n` to Base Address Register Mapping

<code>trn_rbar_hit_n[x]</code>	BAR	Byte Offset
0	0	10h
1	1	14h
2	2	18h
3	3	1Ch
4	4	20h
5	5	24h
6	Expansion ROM BAR	30h

For a Memory or I/O TLP Transaction on the receive interface, `trn_rbar_hit_n[6:0]` is valid for the entire TLP, starting with the assertion of `trn_rsof_n`, as shown in [Figure 5-20](#). When receiving non-Memory and non-I/O transactions, `trn_rbar_hit_n[6:0]` is undefined.

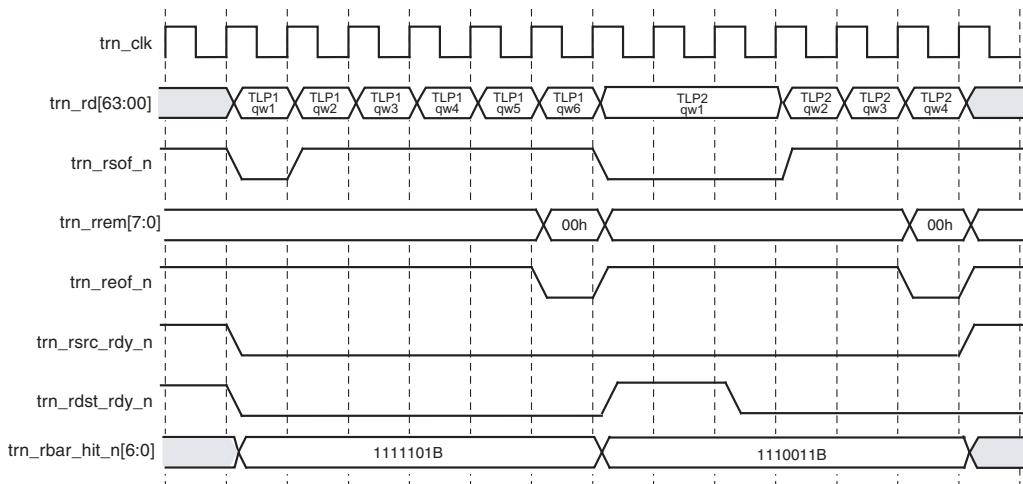


Figure 5-20: BAR Target Determination using `trn_rbar_hit`

The signal `trn_rbar_hit_n[6:0]` enables received Memory or I/O Transactions to be directed to the appropriate destination Memory or I/O apertures in the User Application. By utilizing `trn_rbar_hit_n[6:0]`, application logic can inspect only the lower order Memory or I/O address bits within the address aperture to simplify decoding logic.

Performance Considerations on the Receive Transaction Interface

The *PCI Express Base Specification v1.1* requires that all Endpoints advertise infinite Completion credits. To comply with this requirement, receive buffers must be allocated for Completions before Read Requests are initiated by the Endpoint. The Block Plus core receiver can store up to 8 Completion or Completion with Data TLPs to satisfy this requirement. If the user application generates requests that result in more than 8 outstanding Completion TLPs at any given time, caution must be taken to not overflow the core's completion buffer.

A variety of methods are available to avoid cases where the completion buffer might overflow. Applications targeting a x4 core using a 125 MHz interface frequency or x8 core using a 250 MHz interface frequency need to apply one or more of these methods.

- Completion Streaming
- Metering Reads
- Non-Infinite Completion Credits.

A x4 core using a 250 MHz interface frequency or a x1 core need not worry about applying these methods; under normal circumstances the user application should not cause the completion buffer to overflow. However, for information about designs targeting these cores, see [x4 Core Using 250 MHz Interface and x1 Core Designs, page 111](#).

Special consideration must be given to designs targeting a x8 core using a 125 MHz interface frequency. The Completion Streaming method does not help in this configuration because the interface frequency is running too slowly to keep up with the incoming packets. When operating in this mode, the user must either meter the reads and keep less than 8 completion TLPs outstanding at any time, or use Non-Infinite Completion Credits. [Table 5-3](#) provides of summary of operation modes and methods available to manage completion buffer space.

Table 5-3: Completion Buffer Space Management Solutions

Core	Interface Frequency	Potential for Overflow	Available Solutions
x8	250 MHz	Yes	<ul style="list-style-type: none"> • Completion Streaming • Metering Reads • Advertising Non-Infinite Completion Credits
	125 MHz	Yes	<ul style="list-style-type: none"> • Metering Reads • Advertising Non-Infinite Completion Credits
x4	250 MHz	No ¹	NA
	125 MHz	Yes	<ul style="list-style-type: none"> • Completion Streaming • Metering Reads • Advertising Non-Infinite Completion Credits
x2	250 MHz	No ¹	NA
	125 MHz	No ¹	NA
x1	125 MHz	No ¹	NA
	62.5 MHz	No ¹	NA

1. See [x4 Core Using 250 MHz Interface and x1 Core Designs, page 111](#) for more information.

Figure 5-21 illustrates the available options for managing completion space depending on the core being implemented.

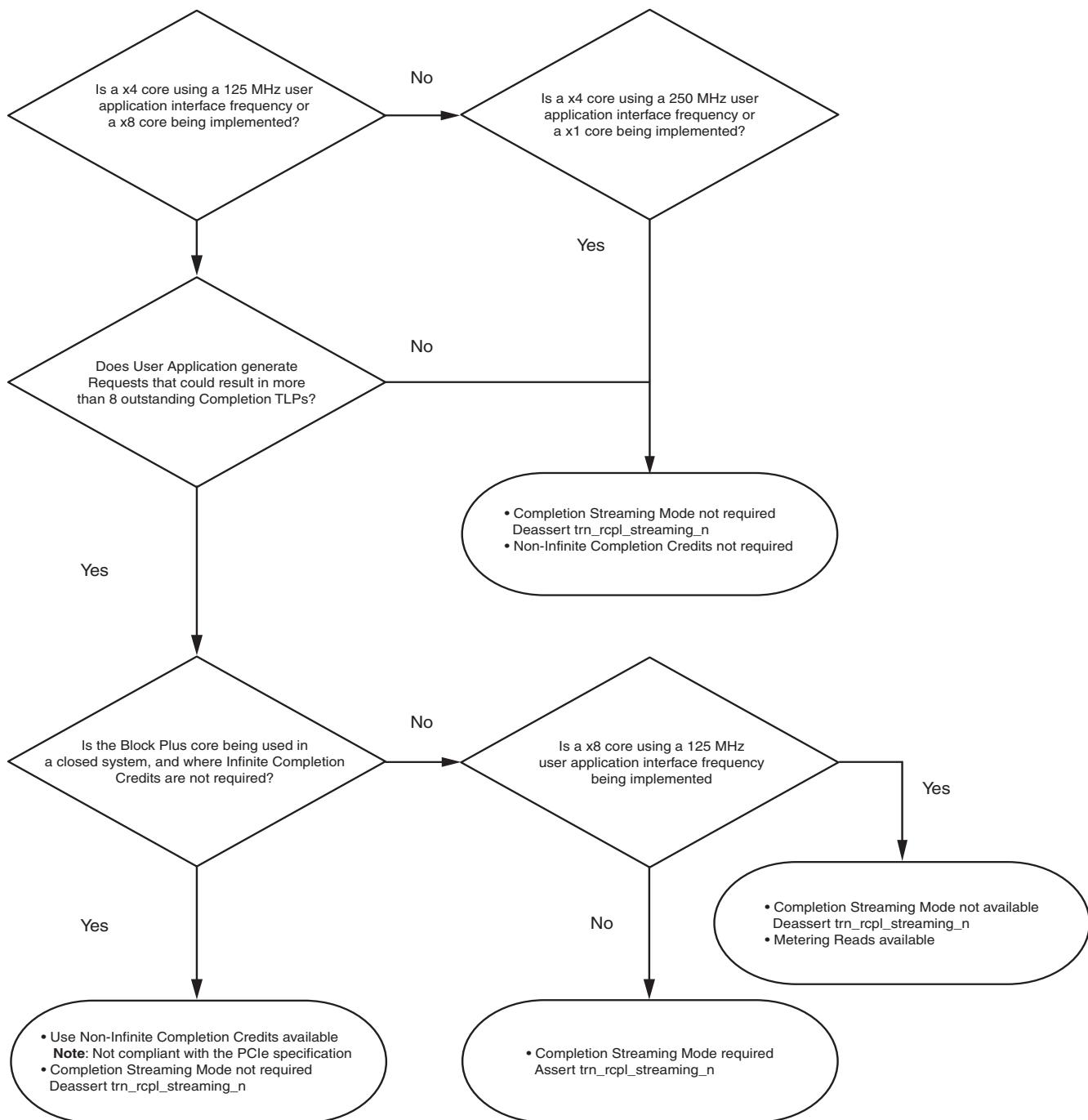


Figure 5-21: Options for Allocating Completion Buffer Space

Completion Streaming on Receive Transaction Interface

The PCI Express system responds to each Memory Read request initiated by the Endpoint with one or more Completion or Completion with Data TLPs. The exact number of Completions varies based on the RCB (Read Completion Boundary) and the starting address and size of the request. See Chapter 2 of the *PCI Express Base Specification v1.1* to determine the worst-case number of Completions that could be generated for a given request.

Pre-allocation of Completion buffers cannot provide sufficient upstream read bandwidth for all applications. For these cases the Block Plus core provides a second option, called Completion Streaming. Completion Streaming is enabled by asserting `trn_rcpl_streaming_n`, and allows a higher rate of Read Requests when certain system conditions can be met:

- Ability of User Application to receive data at line rate
- Control over relative payload sizes of downstream Posted and Completion TLPs

The Block Plus core allows the User Application to receive data in different ways depending on the requirements of the application. In most cases the different options provide a trade-off between raw performance and system restrictions. The designer must determine which option best suits the particular system requirements while ensuring the core receiver does not overflow. Options are:

- **Metered Reads:** The User Application can limit the number of outstanding reads such that there can never be more than 8 Completions at once in the receive buffer. This method precludes using the entire receive bandwidth for Completions, but does not place further restrictions on system design. In this case, the `trn_rcpl_streaming_n` signal should be deasserted.
- **Completion Streaming:** Completion Streaming increases the receive throughput with the trade-offs mentioned previously. The User Application can choose to continuously drain all available Completions from the receive buffer, before processing other TLP types, by asserting the `trn_rcpl_streaming_n` input to the core. When using Completion Streaming, the User Application must set the Relaxed Ordering bit for all Memory Read TLPs, and must continuously assert the `trn_rdst_rdy_n` signal when there are outstanding Completions. If precautions are not taken, it is possible to overflow the receive buffer if several small Completions arrive while a large received TLP (Posted or Completion) is being internally processed by the core and delaying the processing of these small Completions. There are two mechanisms to avoid this possibility; both assume the designer has control over the whole system:
 - **Control Payload Size:** The size of the payloads of incoming Posted TLPs must not be more than 4 times the size of the payloads of incoming Completion TLPs.
 - **Traffic Separation:** Completion traffic with small payloads (such as register reads) must be separated over time from Posted and Completion traffic with large payloads (more than 4 times the size of the small-payload Completions), such that one traffic type does not proceed until the other has finished.
- **Metered/Streaming Hybrid:** The `trn_rcpl_streaming_n` signal can be asserted only when bursts of Completions are expected. When bursts are not expected, `trn_rcpl_streaming_n` is deasserted so that Relaxed Ordering is not required and `trn_rdst_rdy_n` can be deasserted. Switching between Completion Streaming and regular operation can only occur when there are no outstanding Completions to be received.

Example Transactions In Violation of System Requirements

Below are examples of specific situations which violate the Block Plus core system requirements. These examples can lead to receive buffer overflows and are given as illustrations of system designs to be avoided.

- **Back-to-back completions returned without streaming:** Consider an example system wherein the Endpoint User Application transmits a Memory Read Request TLP with a Length of 512 DW (2048 Bytes). The system has a RCB of 64 Bytes, and the requested address is aligned on a 64-Byte boundary. The request can be fulfilled with up to 32 Completion with Data TLPs. If the User Application does not assert `trn_rcpl_streaming_n` and the Completions are transmitted back-to-back, this can overflow the core's receive buffers.
- **Payload size not controlled:** Consider the same system. This time, the User Application asserts `trn_rcpl_streaming_n`, but the ratio of Posted to Completion payload size is not controlled. If 9 or more 64 Byte Completions are received immediately after a 512 DW (Posted) Memory Write TLP, then the core's receive buffers can be overflowed because the Completions are less than 1/4th the size of the Memory Write TLP.

Using One Posted/Non-Posted Header Credit

The Block Plus core implements all necessary precautions for dealing with completion streaming and relaxed ordering as provided in [AR25473](#). The One Header Credit configuration option allows the core to leverage PCI Express flow control to limit transmission of posted and non-posted packets by the link partner, guaranteeing this issue is not exposed. When this option is selected, the user should not deassert `trn_rnp_ok_n`, because Non-Posted packets must be drained immediately on receipt to guarantee compliant operation. This option must be used in conjunction with Completion Streaming mode, thus `trn_rcpl_streaming_n` should be asserted.

For x4 cores running at 125 MHz and x8 cores, this option is selected by default to guarantee compliant operation in Completion Streaming mode. If the user requires a higher bandwidth for Posted and Non-Posted traffic than allowed by 1-header credit for Posted and Non-Posted TLPs, this option can be turned off, provided that the user can guarantee that the core will not receive a Posted or Non-Posted TLP immediately followed by a continuous burst of more than 64 Completions. If this situation *could* occur, the user can still turn off this option, but hardware testing is required to ensure proper operation.

Non-Infinite Completion Credits

If the Block Plus core is to be used in a closed system in which infinite Completion credits are not a requirement, the core can be configured to advertise finite completion credits. When configured this way, the core advertises 8 CplH and 128 (decimal) CplD credits. Enabling non-infinite Completion credits allows the core to leverage PCI Express flow control to prevent receive buffer overflows. If the core is used with this configuration, Completion Streaming is not used.

Note: Enabling non-infinite Completion credits violates the requirements of the *PCI Express Base Specification* and should only be used when necessary and in a closed system.

x4 Core Using 250 MHz Interface and x1 Core Designs

Under normal circumstances, the completion buffer should not overflow as long as the user does not throttle back when receiving data by deasserting trn_tdst_rdy_n. However, if the user application needs to throttle the datapath, then the application must meter the read requests to ensure that no more than 8 Completion or Completion with Data TLPs are outstanding at any given time.

Accessing Configuration Space Registers

Registers Mapped Directly onto the Configuration Interface

The Block Plus core provides direct access to select command and status registers in its Configuration Space. Values in these registers are modified by Configuration Writes received from the Root Complex and cannot be modified by the User Application.

Table 5-4 defines the command and status registers mapped to the configuration port.

Table 5-4: Command and Status Registers Mapped to the Configuration Port

Port Name	Direction	Description
cfg_bus_number[7:0]	Output	Bus Number: Default value after reset is 00h. Refreshed whenever a Type 0 Configuration packet is received.
cfg_device_number[4:0]	Output	Device Number: Default value after reset is 00000b. Refreshed whenever a Type 0 Configuration packet is received.
cfg_function_number[2:0]	Output	Function Number: Function number of the core, hardwired to 000b.
cfg_status[15:0]	Output	Status Register: Status register from the Configuration Space Header.
cfg_command[15:0]	Output	Command Register: Command register from the Configuration Space Header.
cfg_dstatus[15:0]	Output	Device Status Register: Device status register from the PCI Express Extended Capability Structure.
cfg_dcommand[15:0]	Output	Device Command Register: Device control register from the PCI Express Extended Capability Structure.
cfg_lstatus[15:0]	Output	Link Status Register: Link status register from the PCI Express Extended Capability Structure.
cfg_lcommand[15:0]	Output	Link Command Register: Link control register from the PCI Express Extended Capability Structure.

Device Control and Status Register Definitions

`cfg_bus_number[7:0], cfg_device_number[4:0], cfg_function_number[2:0]`

Together, these three values comprise the core ID, which the core captures from the corresponding fields of inbound Type 0 Configuration accesses. The User Application is responsible for using this core ID as the Requestor ID on any requests it originates, and using it as the Completer ID on any Completion response it sends. This core supports only one function; for this reason, the function number is hardwired to 000b.

`cfg_status[15:0]`

This bus allows the User Application to read the Status register in the PCI Configuration Space Header. [Table 5-5](#) defines these bits. See the *PCI Express Base Specification* for detailed information.

Table 5-5: Bit Mapping on Header Status Register

Bit	Name
<code>cfg_status[15]</code>	Detected Parity Error
<code>cfg_status[14]</code>	Signaled System Error
<code>cfg_status[13]</code>	Received Master Abort
<code>cfg_status[12]</code>	Received Target Abort
<code>cfg_status[11]</code>	Signaled Target Abort
<code>cfg_status[10:9]</code>	DEVSEL Timing (hardwired to 00b)
<code>cfg_status[8]</code>	Master Data Parity Error
<code>cfg_status[7]</code>	Fast Back-to-Back Transactions Capable (hardwired to 0)
<code>cfg_status[6]</code>	Reserved
<code>cfg_status[5]</code>	66 MHz Capable (hardwired to 0)
<code>cfg_status[4]</code>	Capabilities List Present (hardwired to 1)
<code>cfg_status[3]</code>	Interrupt Status
<code>cfg_status[2:0]</code>	Reserved

`cfg_command[15:0]`

This bus reflects the value stored in the Command register in the PCI Configuration Space Header. [Table 5-6](#) provides the definitions for each bit in this bus. See the *PCI Express Base Specification* for detailed information.

Table 5-6: Bit Mapping on Header Command Register

Bit	Name
<code>cfg_command[15:11]</code>	Reserved
<code>cfg_command[10]</code>	Interrupt Disable
<code>cfg_command[9]</code>	Fast Back-to-Back Transactions Enable (hardwired to 0)
<code>cfg_command[8]</code>	SERR Enable

Table 5-6: Bit Mapping on Header Command Register (Cont'd)

Bit	Name
cfg_command[7]	IDSEL Stepping/Wait Cycle Control (hardwired to 0)
cfg_command[6]	Parity Error Enable
cfg_command[5]	VGA Palette Snoop (hardwired to 0)
cfg_command[4]	Memory Write and Invalidate (hardwired to 0)
cfg_command[3]	Special Cycle Enable (hardwired to 0)
cfg_command[2]	Bus Master Enable
cfg_command[1]	Memory Address Space Decoder Enable
cfg_command[0]	I/O Address Space Decoder Enable

The User Application must monitor the Bus Master Enable bit (`cfg_command[2]`) and refrain from transmitting requests while this bit is not set. This requirement applies only to requests; completions can be transmitted regardless of this bit.

`cfg_dstatus[15:0]`

This bus reflects the value stored in the Device Status register of the PCI Express Extended Capabilities Structure. [Table 5-7](#) defines each bit in the `cfg_dstatus` bus. See the *PCI Express Base Specification* for detailed information.

Table 5-7: Bit Mapping on PCI Express Device Status Register

Bit	Name
cfg_dstatus[15:6]	Reserved
cfg_dstatus[5]	Transaction Pending
cfg_dstatus[4]	AUX Power Detected
cfg_dstatus[3]	Unsupported Request Detected
cfg_dstatus[2]	Fatal Error Detected
cfg_dstatus[1]	Non-Fatal Error Detected
cfg_dstatus[0]	Correctable Error Detected

`cfg_dcommand[15:0]`

This bus reflects the value stored in the Device Control register of the PCI Express Extended Capabilities Structure. [Table 5-8](#) defines each bit in the `cfg_dcommand` bus. See the *PCI Express Base Specification* for detailed information.

Table 5-8: Bit Mapping of PCI Express Device Control Register

Bit	Name
cfg_dcommand[15]	Reserved
cfg_dcommand[14:12]	Max_Read_Request_Size
cfg_dcommand[11]	Enable No Snoop
cfg_dcommand[10]	Auxiliary Power PM Enable

Table 5-8: Bit Mapping of PCI Express Device Control Register (Cont'd)

Bit	Name
cfg_dcommand[9]	Phantom Functions Enable
cfg_dcommand[8]	Extended Tag Field Enable
cfg_dcommand[7:5]	Max_Payload_Size
cfg_dcommand[4]	Enable Relaxed Ordering
cfg_dcommand[3]	Unsupported Request Reporting Enable
cfg_dcommand[2]	Fatal Error Reporting Enable
cfg_dcommand[1]	Non-Fatal Error Reporting Enable
cfg_dcommand[0]	Correctable Error Reporting Enable

cfg_lstatus[15:0]

This bus reflects the value stored in the Link Status register in the PCI Express Extended Capabilities Structure. [Table 5-9](#) defines each bit in the `cfg_lstatus` bus. See the *PCI Express Base Specification* for details.

Table 5-9: Bit Mapping of PCI Express Link Status Register

Bit	Name
cfg_lstatus[15:13]	Reserved
cfg_lstatus[12]	Slot Clock Configuration
cfg_lstatus[11]	Reserved
cfg_lstatus[10]	Reserved
cfg_lstatus[9:4]	Negotiated Link Width
cfg_lstatus[3:0]	Link Speed

cfg_lcommand[15:0]

This bus reflects the value stored in the Link Control register of the PCI Express Extended Capabilities Structure. [Table 5-10](#) provides the definition of each bit in `cfg_lcommand` bus. See the *PCI Express Base Specification* for more details.

Table 5-10: Bit Mapping of PCI Express Link Control Register

Bit	Name
cfg_lcommand[15:8]	Reserved
cfg_lcommand [7]	Extended Synch
cfg_lcommand [6]	Common Clock Configuration
cfg_lcommand [5]	Retrain Link (Reserved for an Endpoint device)
cfg_lcommand [4]	Link Disable
cfg_lcommand [3]	Read Completion Boundary
cfg_lcommand[2]	Reserved
cfg_lcommand [1:0]	Active State Link PM Control

Accessing Additional Registers through the Configuration Port

Configuration registers that are not directly mapped to the user interface can be accessed by configuration-space address using the ports shown in [Table 2-11, page 38](#).

Configuration Register Read Operation

The User Application must supply the read address as a DWORD address, not a byte address. To calculate the DWORD address for a register, divide the byte address by four. For example:

- The DWORD address of the Command/Status Register in the PCI Configuration Space Header is 01h. (The byte address is 04h.)
- The DWORD address for BAR0 is 04h. (The byte address is 10h.)

To read any register in this address space, the User Application drives the register DWORD address onto `cfg_dwaddr[9:0]` and asserts `cfg_rd_en_n` for one `trn_clk` cycle. The core drives the content of the addressed register onto `cfg_do[31:0]`. The value on `cfg_do[31:0]` is qualified by signal assertion on `cfg_rd_wr_done_n`. [Figure 5-22](#) illustrates an example with two consecutive reads from the Configuration Space.

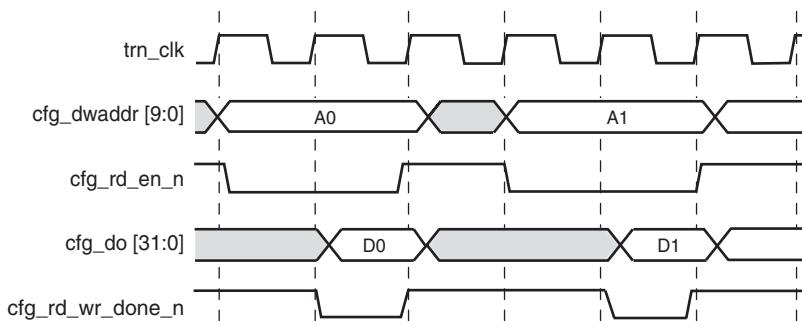


Figure 5-22: Example Configuration Space Access

Note: Configuration Register Read access is not supported in the duration between `trn_reset_n` deassertion and 20 clock cycles after `trn_link_up_n` assertion.

In the event of an unsuccessful read operation, user logic must assume the transaction has failed and must re-initiate the transaction. The User Application must implement a timeout circuit, which would re-initiate the Configuration Register Read Request in the event that `cfg_rd_wr_done_n` does not assert within 15 clock cycles from the Configuration Register Read Request (`cfg_rd_en_n` assertion). [Figure 5-23](#) illustrates an example of this scenario.

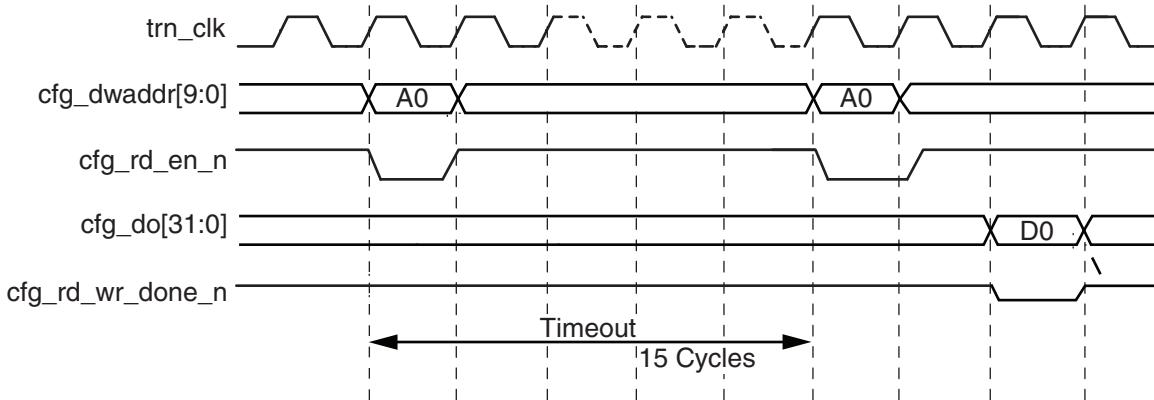


Figure 5-23: Re-initiation of Configuration Read Request

Back-to-back read operations can be performed by asserting `cfg_rd_en_n` and providing the next read address (`cfg_dwaddr[9:0]`) on the clock cycle after `cfg_rd_wr_done_n` assertion. A maximum of 10 back-to-back read operations are permitted at a time, after which user logic must wait a minimum of 1200 clock cycles before performing another series of back-to-back read operations. Polling of registers, to monitor for change in status, is also required to maintain a minimum 1200 clock cycle gap between successive polling cycles. In all cases, the User Application must implement the timeout counter of 15 clock cycles to determine a successful read operation.

Configuration Register Write

The Configuration Write access allows the application to write the configuration registers in the Integrated Block for PCI Express contained within the Block Plus core wrapper. Configuration Write accesses to the configuration space are allowed only when the Block Plus for PCI Express has been reset (assertion of `sys_reset_n`), or is beginning operation after FPGA power-up configuration. Configuration Write access to the Integrated Block for PCI Express configuration registers is permitted only prior to commencing PCIe transactions over the link and must be completed prior to `trn_lnk_up_n` assertion.

Configuration Write accesses are allowed only during the window of time between 20 clock cycles after `trn_reset_n` deassertion and `trn_lnk_up_n` assertion as shown in Figure 5-24. At power up after FPGA bitstream configuration and any time `sys_reset_n` input port signal is toggled, `trn_reset_n` is asserted. Once `trn_reset_n` is deasserted, it indicates to the User Application that the Integrated Block can accept Configuration Write accesses to the configuration space after 20 clock cycles. Configuration Write access is permitted until the transaction link-up (`trn_lnk_up_n`) signal is asserted and not supported thereafter. The Configuration Interface operates in the User clock domain (`trn_clk`). Any assertions of `trn_reset_n` resets the configuration registers in the Integrated Block for PCI Express and any Configuration Writes by the user must be repeated after deassertion of `trn_reset_n`.

It is possible that `trn_reset_n` might deassert and assert again during initial link training before the first assertion of `trn_lnk_up_n`. This could happen if link training fails to complete and starts over in the LTSSM detect state as directed by the specification. If this happens, the configuration writes must be repeated after the deassertion of `trn_reset_n`.

The timing relationship between the deassertion of the `sys_reset_n` input port signal and the `trn_reset_n` output port signal asserting is dependent on the time taken by the Virtex®-5 FPGA GT PLL to lock to the input `sys_clk` signal. This time is approximately

70 µs, but performance might vary. Further, the timing relationship between `trn_reset_n` deassertion and `trn_lnk_up` assertion is the time it takes the block to link train (reach L0) and then exchange initial flow control credits and achieve the DL.Active state. At this point, `trn_lnk_up_n` asserts. For more information on L0 and DL.Active, see the *PCI Express Base Specification*.

Note: The time from `trn_reset_n` deassertion to `trn_lnk_up_n` assertion is different in simulation compared to real hardware. This is because in simulation scaled down timers are used during the various LTSSM states. See [Scaled Simulation Timeouts in Appendix B](#) for more information.

The User Application needs to assert `cfg_wr_en_n` to request Configuration Write access and must hold this asserted for the duration of all the Configuration Writes needed.

When the User Application has completed the required configuration register accesses, it must release the Configuration Interface to enable the Integrated Block for PCI Express to resume normal operation. This is accomplished by the User Application de-asserting `cfg_wr_en_n` and must be done before `trn_lnk_up_n` deasserts.

After this write request is deasserted, any further Configuration Write access to the configuration space is not supported while the system is in operation.

Configuration Write Operation

A Configuration Write operation uses the Write Enable control signal (`cfg_wr_en_n`) in conjunction with a Byte Enables control signal (`cfg_byte_en_n[3:0]`) and the address bus (`cfg_dwaddr[9:0]`). The Read-Write done signal (`cfg_rd_wr_done_n`) is not used in the Configuration Write operation mode.

[Figure 5-24](#) shows a Configuration Write operation

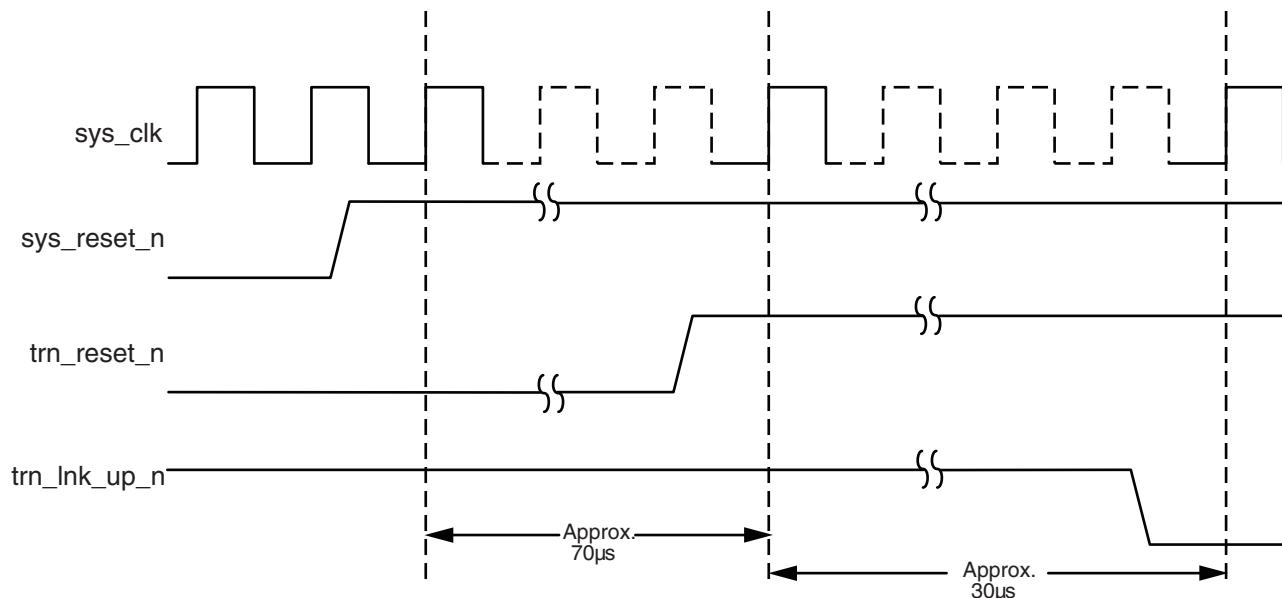


Figure 5-24: Configuration Write Timing

To perform a write operation, the user places the configuration register DWORD address on the `cfg_dwaddr[9:0]` bus, and the write data on the `cfg_di[31:0]` bus. In addition to the address and data, the user must also specify which bytes of the 32-bit data are valid.

This is done by placing the appropriate value on the `cfg_byte_en_n[3:0]` byte enable bus.

The byte enable signals, `cfg_byte_en_n [3:0]`, are active-low (a value of 0 enables a byte) and used to enable a single byte within the write DWORD. The mapping is as follows:

- `cfg_byte_en_n [0] => cfg_di[7:0]`
- `cfg_byte_en_n [1] => cfg_di[15:8]`
- `cfg_byte_en_n [2] => cfg_di[23:16]`
- `cfg_byte_en_n [3] => cfg_di[31:24]`

Enabling Configuration Write Access

Configuration write access is available in the Block Plus Core wrapper, but is not enabled by default. To enable this feature, uncomment the following source file included in the simulation and implementation file lists:

```
<project_dir>/<component_name>/source/cfg_wr_enable.v
```

Enabling Configuration Write Access in Project Navigator

Configuration write access can be enabled for implementation using Project Navigator by the following process:

1. Go to **Synthesis** properties
2. Change Property Display Level to **Advanced**
3. In Switch, select **-define (Verilog macros)**
4. Add **MANAGEMENT_WRITE=b1**

Configuration Registers

Table 5-11 describes the registers in the Integrated Block that are accessible through the Block Plus core configuration interface. All registers can be read through the configuration interface, and those designated read/write (RW) can also be written. The addresses given in the following tables refer to the configuration interface address (`cfg_dwaddr[9:0]`). The addresses used when accessing the configuration registers through configuration read and write packets by the PCI Express link are different, and can be found in the PCI-SIG specifications.

Table 5-11: Configuration Registers

Configuration Address (Hex) <code>cfg_dwaddr[9:0]</code>	Register Name ¹	Read Only or Read/Write
0	Device ID; Vendor ID	RW; RW
1	Status; Command	RO; RO
2	Class Code; Revision ID	RW; RW
3	Header Type; Cache Line Size	RO; RO
4	Base Address Registers (BAR0)	RO
5	Base Address Registers (BAR1)	RO
6	Base Address Registers (BAR2)	RO

Table 5-11: Configuration Registers (Cont'd)

Configuration Address (Hex) cfg_dwaddr[9:0]	Register Name ¹	Read Only or Read/Write
7	Base Address Registers (BAR3)	RO
8	Base Address Registers (BAR4)	RO
9	Base Address Registers (BAR5)	RO
A	Cardbus CIS Pointer	RW
B	Subsystem ID; Subsystem Vendor ID	RW; RW
C	Expansion ROM Base Address	RO
D	Interrupt Pin; Interrupt Line; Capabilities Pointer	RW; RO; RW
E – 1C	Reserved	NA
1D	Power Management Capabilities (PMC) ² ; Next Capability Pointer; Capability ID	RW; RO; RO
1E	Reserved (16 bits); Power Management Control/Status (PMCSR)	NA; RO
1F – 21	Reserved	NA
22	Message Control; Next Pointer; Capability ID	RO; RO; RO
23	Message Address	RO
24	Message Upper Address	RO
25	Reserved (16 bits); Message Data (16 bits)	RO; RO
26	Mask Bits	RO
27	Pending Bits	RO
28	PCIe Capabilities Register; Next Cap Pointer; PCIe Cap ID	RO
29	Device Capabilities	RW
2A	Device Status; Device Control	RO; RO
2B	Link Capabilities ³	RW
2C	Link Status ³ ; Link Control	RW; R0
2D – 3FF	Reserved	NA

1. The register names are listed as they are read on cfg_do[31:0] or written to cfg_di[31:0].
2. The PM version correctly has a value of 3 when read through the PCI Express link, but returns a value of 2 when read through the configuration interface.
3. Bit 20 of the Link Capabilities register (Data Link Layer Active Reporting Capable) and bit 13 of the Link Status register (Data Link Layer Link Active) both have a correct value of 0 when read through the PCI Express serial link, but return a value of 1 when read from the Management interface.

Additional Packet Handling Requirements

The User Application must manage the following mechanisms to ensure protocol compliance, because the core does not manage them automatically.

Generation of Completions

The Endpoint Block Plus for PCIe does not generate Completions for Memory Reads or I/O requests made by a remote device. The user is expected to service these completions according to the rules specified in the *PCI Express Base Specification*.

Tracking Non-Posted Requests and Inbound Completions

The Endpoint Block Plus for PCIe does not track transmitted I/O requests or Memory Reads that have yet to be serviced with inbound Completions. The User Application is required to keep track of such requests using the Tag ID or other information. The PCI Express specification requires that each outstanding Non-Posted request include a unique tag to identify the request.

Keep in mind that one Memory Read request can be answered by several Completion packets. The User Application must accept all inbound Completions associated with the original Memory Read until all requested data has been received. In addition, completions for an individual request are returned in address order; however, completions for a different request can be returned in any order. For more information on transaction ordering, see Chapter 2 of the *PCI Express Base Specification*.

The *PCI Express Base Specification* requires that an Endpoint advertise infinite Completion Flow Control credits as a receiver; the Endpoint can only transmit Memory Reads and I/O requests if it has enough space to receive subsequent Completions.

The Block Plus core does not keep track of receive-buffer space for Completion. Rather, it sets aside a fixed amount of buffer space for inbound Completions. The User Application must keep track of this buffer space to know if it can transmit requests requiring a Completion response.

See [Performance Considerations on the Receive Transaction Interface, page 107](#) for information about implementing this mechanism.

Reporting User Error Conditions

The User Application must report errors that occur during Completion handling using dedicated error signals on the core interface, and must observe the Device Power State before signaling an error to the core. If the User Application detects an error (for example, a Completion Timeout) while the device has been programmed to a non-D0 state, the User Application is responsible to signal the error after the device is programmed back to the D0 state.

After the User Application signals an error, the core reports the error on the PCI Express Link and also sets the appropriate status bit(s) in the Configuration Space. Because status bits must be set in the appropriate Configuration Space register, the User Application cannot generate error reporting packets on the transmit interface. The type of error-reporting packets transmitted depends on whether or not the error resulted from a Posted or Non-Posted Request. All user-reported errors cause Message packets to be sent to the Root Complex, unless the error is regarded as an Advisory Non-Fatal Error. For more information about Advisory Non-Fatal Errors, see Chapter 6 of the *PCI Express Base*

Specification. Errors on Non-Posted Requests can result in either Messages to the Root Complex or Completion packets with non-Successful status sent to the original Requester.

Error Types

The User Application triggers six types of errors using the signals defined in [Table 2-12, page 41](#).

- End-to-end CRC ECRC Error
- Unsupported Request Error
- Completion Timeout Error
- Unexpected Completion Error
- Completer Abort Error
- Correctable Error

Multiple errors can be detected in the same received packet; for example, the same packet can be an Unsupported Request and have an ECRC error. If this happens, only one error should be reported. Because all user-reported errors have the same severity, the User Application design can determine which error to report. The `cfg_err_posted_n` signal, combined with the appropriate error reporting signal, indicates what type of error-reporting packets are transmitted. The user can signal only one error per clock cycle. See [Figure 5-25](#), [Figure 5-26](#), and [Figure 5-27](#), and [Table 5-12](#) and [Table 5-13](#).

Table 5-12: User-indicated Error Signaling

Reported Error	<code>cfg_err_posted_n</code>	Action
None	Don't care	No Action Taken
<code>cfg_err_ur_n</code>	0 or 1	0: If enabled, a Non-Fatal Error Message is sent. 1: A Completion with a non-successful status is sent.
<code>cfg_err_cpl_abort_n</code>	0 or 1	0: If enabled, a Non-Fatal Error message is sent. 1: A Completion with a non-successful status is sent.
<code>cfg_err_cpl_timeout_n</code>	Don't care	If enabled, a Non-Fatal Error Message is sent.
<code>cfg_err_ecrc_n</code>	Don't care	If enabled, a Non-Fatal Error Message is sent.
<code>cfg_err_cor_n</code>	Don't care	If enabled, a Correctable Error Message is sent.
<code>cfg_err_cpl_unexpected_n</code>	Don't care	Regarded as an Advisory Non-Fatal Error (ANFE); no action taken.

Table 5-13: Possible Error Conditions for TLPs Received by the User Application

Received TLP Type	Possible Error Condition					Error Qualifying Signal Status	
	Unsupported Request (cfg_err_ur_n)	Completion Abort (cfg_err_cpl_abort_n)	Correctable Error (cfg_err_cor_n)	ECRC Error (cfg_err_ecrc_n)	Unexpected Completion (cfg_err_cpl_unexpect_n)	Value to Drive on (cfg_err_posted_n)	Drive Data on (cfg_err_tlp_cpl_header[47:0])
Memory Write	,	X	N/A	,	X	0	No
Memory Read	,	,	N/A	,	X	1	Yes
I/O	,	,	N/A	,	X	1	Yes
Completion	X	X	N/A	,	,	0	No

Whenever an error is detected in a Non-Posted Request, the User Application deasserts cfg_err_posted_n and provides header information on cfg_err_tlp_cpl_header[47:0] during the same clock cycle the error is reported, as illustrated in Figure 5-25. The additional header information is necessary to construct the required Completion with non-Successful status. Additional information about when to assert or deassert cfg_err_posted_n is provided in the following sections.

If an error is detected on a Posted Request, the User Application instead asserts cfg_err_posted_n, but otherwise follows the same signaling protocol. This results in a Non-Fatal Message being sent, if enabled.

The core's ability to generate error messages can be disabled by the Root Complex issuing a configuration write to the Endpoint core's Device Control register and the PCI Command register setting the appropriate bits to 0. For more information about these registers, see Chapter 7 of the *PCI Express Base Specification*. However, error-reporting status bits are always set in the Configuration Space whether or not their Messages are disabled.

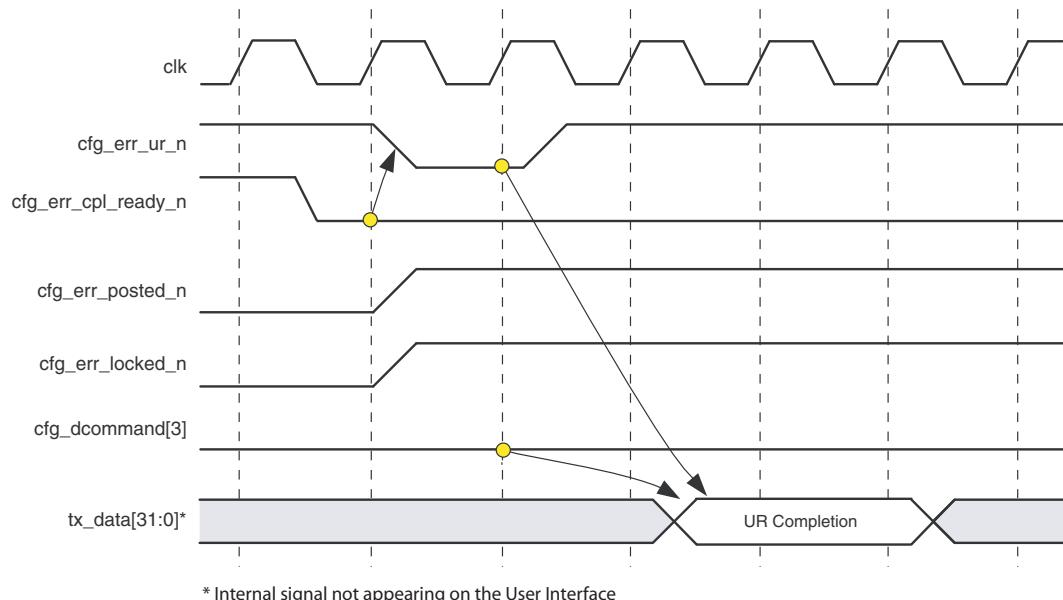


Figure 5-25: Signaling Unsupported Request for Non-Posted TLP

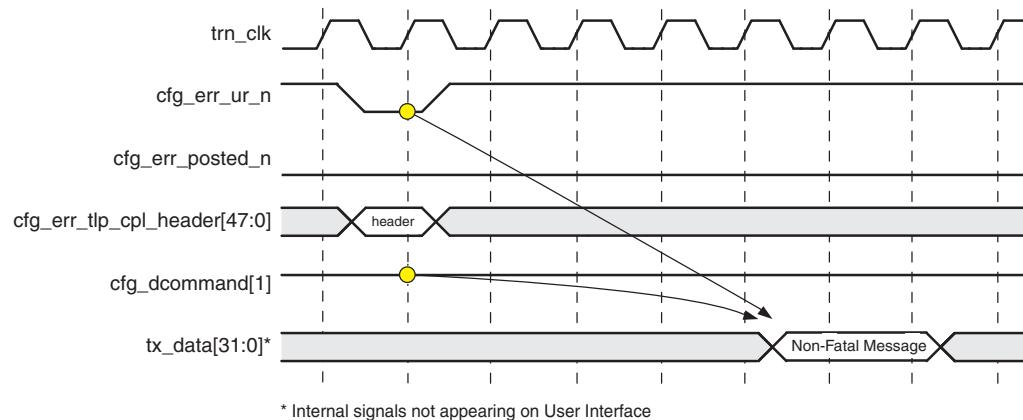


Figure 5-26: Signaling Unsupported Request for Posted TLP

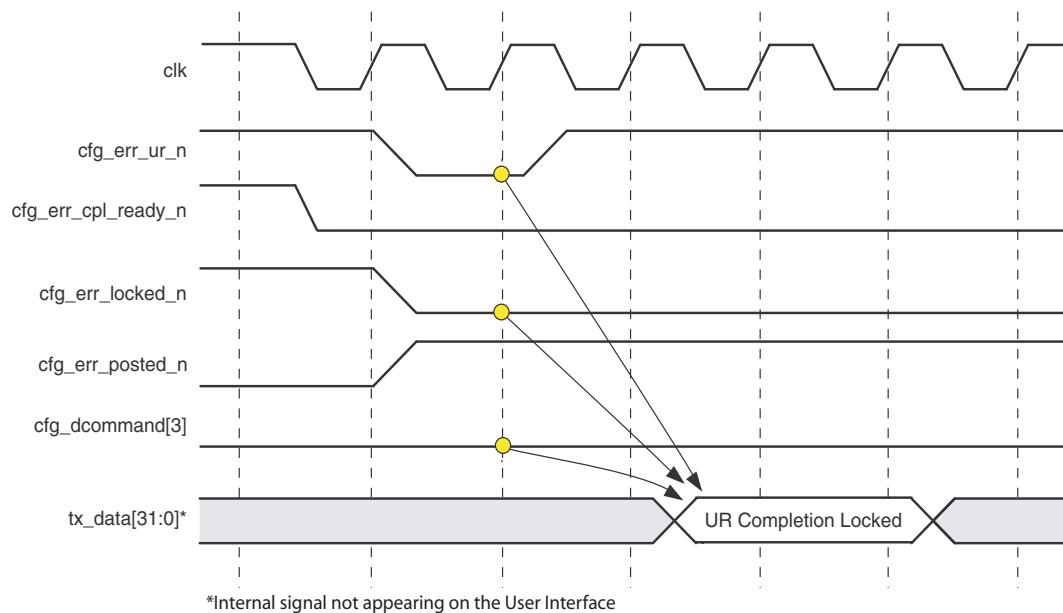


Figure 5-27: Signaling Locked Unsupported Request for Locked Non-Posted TLP

Completion Timeouts

The Block Plus core does not implement Completion timers; for this reason, the User Application must track how long its pending Non-Posted Requests have each been waiting for a Completion and trigger timeouts on them accordingly. The core has no method of knowing when such a timeout has occurred, and for this reason does not filter out inbound Completions for expired requests.

If a request times out, the User Application must assert **cfg_err_cpl_timeout_n**, which causes an error message to be sent to the Root Complex. If a Completion is later received after a request times out, the User Application must treat it as an Unexpected Completion.

Unexpected Completions

The Endpoint Block Plus for PCIe automatically reports Unexpected Completions in response to inbound Completions whose Requestor ID is different than the Endpoint ID programmed in the Configuration Space. These completions are not passed to the User Application. The current version of the core regards an Unexpected Completion to be an Advisory Non-Fatal Error (ANFE), and no message is sent.

Completer Abort

If the User Application is unable to transmit a normal Completion in response to a Non-Posted Request it receives, it must signal `cfg_err_cpl_abort_n`. The `cfg_err_posted_n` signal can also be set to 1 simultaneously to indicate Non-Posted and the appropriate request information placed on `cfg_err_tlp_cpl_header[47:0]`. This sends a Completion with non-Successful status to the original Requester. Due to a known restriction in the Virtex-5 FPGA Integrated Block, if the user signals a completion abort, then a Non-Fatal error message is also sent. See [UG197, Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs](#) for more information.

It is recommended that an unsupported request be signalled instead. When in Legacy mode if the `cfg_err_locked_n` signal is set to 0 (to indicate the transaction causing the error was a locked transaction), a Completion Locked with Non-Successful status is sent. If the `cfg_err_posted_n` signal is set to 0 (to indicate a Posted transaction), no Completion is sent, but a Non-Fatal Error Message is sent (if enabled).

Unsupported Request

If the User Application receives an inbound Request it does not support or recognize, it must assert `cfg_err_ur_n` to signal an Unsupported Request. The `cfg_err_posted_n` signal must also be asserted or deasserted depending on whether the packet in question is a Posted or Non-Posted Request. If the packet is Posted, a Non-Fatal Error Message is sent out (if enabled); if the packet is Non-Posted, a Completion with a non-Successful status is sent to the original Requester. When in Legacy mode if the `cfg_err_locked_n` signal is set to 0 (to indicate the transaction causing the error was a locked transaction), a Completion Locked with Unsupported Request status is sent.

The Unsupported Request condition can occur for several reasons, including the following:

- An inbound Memory Write packet violates the User Application's programming model, for example, if the User Application has been allotted a 4 kB address space but only uses 3 kB, and the inbound packet addresses the unused portion. (Note: If this occurs on a Non-Posted Request, the User Application should use `cfg_err_cpl_abort_n` to flag the error.)
- An inbound packet uses a packet Type not supported by the User Application, for example, an I/O request to a memory-only device.

ECRC Error

The Block Plus core does not check the ECRC field for validity. If the User Application chooses to check this field, and finds the CRC is in error, it can assert `cfg_err_ecrc_n`, causing a Non-Fatal Error Message to be sent.

Power Management

The Endpoint Block Plus for PCIe supports these power management modes:

- Active State Power Management (ASPM)
- Programmed Power Management (PPM)

Implementing these power management functions as part of the PCI Express design enables the PCI Express hierarchy to seamlessly exchange power-management messages to save system power. All power management message identification functions are implemented. The sections below describe the user logic definition to support the above modes of power management.

For additional information on ASPM and PPM implementation, see the *PCI Express Base Specification*.

Active State Power Management

The Active State Power Management (ASPM) functionality is autonomous and transparent from a user-logic function perspective. The core supports the conditions required for ASPM.

Programmed Power Management

To achieve considerable power savings on the PCI Express hierarchy tree, the core supports the following link states of Programmed Power Management (PPM):

- L0: Active State (data exchange state)
- L1: Higher Latency, lower power standby state
- L3: Link Off State

All PPM messages are always initiated by an upstream link partner. Programming the core to a non-D0 state, results in PPM messages being exchanged with the upstream link-partner. The PCI Express Link transitions to a lower power state after completing a successful exchange.

PPM L0 State

The L0 state represents *normal* operation and is transparent to the user logic. The core reaches the L0 (active state) after a successful initialization and training of the PCI Express Link(s) as per the protocol.

PPM L1 State

The following steps outline the transition of the core to the PPM L1 state.

1. The transition to a lower power PPM L1 state is always initiated by an upstream device, by programming the PCI Express device power state to D3-hot.
2. The core then throttles/stalls the user logic from initiating any new transactions on the user interface by deasserting `trn_tdst_rdy_n`. Any pending transactions on the user interface are, however, accepted fully and can be completed later.
3. The core exchanges appropriate power management messages with its link partner to successfully transition the link to a lower power PPM L1 state. This action is transparent to the user logic.

4. All user transactions are stalled for the duration of time when the device power state is non-D0.
5. The device power state is communicated to the user logic through the user configuration port interface. The user logic is responsible for performing a successful read operation to identify the device power state.
6. The user logic, after identifying the device power state as D3, can initiate a request through the `cfg_pm_wake_n` to the upstream link partner to transition the link to a higher power state L0.

PPM L3 State

The following steps outline the transition of the Endpoint Block Plus for PCIe to the PPM L3 state.

1. The core moves the link to the PPM L3 power state upon the upstream device programming the PCI Express device power state to D3.
2. During this duration, the core may receive a Power-Management Turn-Off (PME-turnoff) Message from its upstream partner.
3. The core notifies the user logic that power is about to be removed by asserting `cfg_to_turnoff_n`.
4. The core transmits a transmission of the Power Management Turn-off Acknowledge (PME-turnoff_ack) Message to its upstream link partner after a delay of no less than 250 nanoseconds.
5. The core closes all its interfaces, disables the Physical/Data-Link/Transaction layers and is ready for *removal* of power to the core.

Power-down negotiation follows these steps:

1. Before power and clock are turned off, the Root Complex or the Hot-Plug controller in a downstream switch issues a PME_TO_Ack broadcast message.
2. When the core receives this TLP, it asserts `cfg_to_turnoff_n` to the User Application.
3. When the User Application detects the assertion of `cfg_to_turnoff_n`, it must complete any packet in progress and stop generating any new packets.
4. The core sends a PME_TO_Ack after approximately 250 nanoseconds.

Generating Interrupt Requests

The Endpoint Block Plus for PCIe supports sending interrupt requests as either legacy interrupts or Message Signaled Interrupts (MSI). The mode is programmed using the MSI Enable bit in the Message Control Register of the MSI Capability Structure. For more information on the MSI capability structure see section 6.8 of the *PCI Local Base Specification v3.0*. If the MSI Enable bit is set to a 1, the core generates an MSI request by sending Memory Write TLPs. If the MSI Enable bit is set to 0, the core generates legacy interrupt messages as long as the Interrupt Disable bit in the PCI Command Register is set to 0:

- `cfg_command[10] = 0`: interrupts enabled
- `cfg_command[10] = 1`: interrupts disabled (request are blocked by the core)

MSI Enable bit in MSI Control Register:

- `cfg_interrupt_msienable = 0`: Legacy Interrupt
- `cfg_interrupt_msienable = 1`: MSI

The MSI Enable bit in the MSI control register and the Interrupt Disable bit in the PCI Command register are programmed by the Root Complex. The User Application has no direct control over these bits. Regardless of the interrupt type used, the user initiates interrupt requests through the use of `cfg_interrupt_n` and `cfg_interrupt_rdy_n` as shown in [Table 5-14](#).

Table 5-14: Interrupt Signalling

Port Name	Direction	Description
<code>cfg_interrupt_n</code>	Input	Assert to request an interrupt. Leave asserted until the interrupt is serviced.
<code>cfg_interrupt_rdy_n</code>	Output	Asserted when the core accepts the signaled interrupt request.

The User Application requests interrupt service in one of two ways, each of which are described below.

MSI Mode

- As shown in [Figure 5-28](#), the User Application first asserts `cfg_interrupt_n`. Additionally, the User Application supplies a value on `cfg_interrupt_di[7:0]` if Multi-Vector MSI is enabled (see below).
- The core asserts `cfg_interrupt_rdy_n` to signal that the interrupt has been accepted and the core sends a MSI Memory Write TLP. On the following clock cycle, the User Application deasserts `cfg_interrupt_n` and reasserts `cfg_interrupt_n` if further interrupts are to be sent.

The MSI request is either a 32-bit addressable Memory Write TLP or a 64-bit addressable Memory Write TLP. The address is taken from the Message Address and Message Upper Address fields of the MSI Capability Structure, while the payload is taken from the Message Data field. These values are programmed by system software through configuration writes to the MSI Capability structure. When the core is configured for Multi-Vector MSI, system software may permit Multi-Vector MSI messages by programming a non-zero value to the Multiple Message Enable field.

The type of MSI TLP sent (32-bit addressable or 64-bit addressable) depends on the value of the Upper Address field in the MSI capability structure. By default, MSI messages are sent as 32-bit addressable Memory Write TLPs. MSI messages use 64-bit addressable Memory Write TLPs only if the system software programs a non-zero value into the Upper Address register.

When Multi-Vector MSI messages are enabled, the User Application may override one or more of the lower-order bits in the Message Data field of each transmitted MSI TLP to differentiate between the various MSI messages sent upstream. The number of lower-order bits in the Message Data field available to the User Application is determined by the lesser of the value of the Multiple Message Capable field, as set in the CORE Generator tool, and the Multiple Message Enable field, as set by system software and available as the `cfg_interrupt_mmenable[2:0]` core output. The core masks any bits in `cfg_interrupt_di[7:0]` which are not configured by system software via Multiple Message Enable.

This pseudo-code shows the processing required:

```
// Value MSI_Vector_Num must be in range: 0 <= MSI_Vector_Num <=
(2^cfg_interrupt_mmenable)-1
if (cfg_interrupt_msienable) {           // MSI Enabled
    if (cfg_interrupt_mmenable > 0) {     // Multi-Vector MSI Enabled
        cfg_interrupt_di[7:0] = {Padding_0s, MSI_Vector_Num};
    } else {                            // Single-Vector MSI Enabled
        cfg_interrupt_di[7:0] = Padding_0s;
    }
} else {
    // Legacy Interrupts Enabled
}
```

For example:

1. If `cfg_interrupt_mmenable[2:0] == 000b`, that is, 1 MSI Vector Enabled, then `cfg_interrupt_di[7:0] = 8'h0`;
2. if `cfg_interrupt_mmenable[2:0] == 101b`, that is, 32 MSI Vectors Enabled, then `cfg_interrupt_di[7:0] = {3'b000}, {MSI_Vector#}}`;

where `MSI_Vector#` is a 5-bit value and is allowed to be `00000b <= MSI_Vector# <= 11111b`

Legacy Interrupt Mode

- As shown in [Figure 5-28](#), the User Application first asserts `cfg_interrupt_n` and `cfg_interrupt_assert_n` to assert the interrupt. The User Application should select a specific interrupt (INTA, INTB, INTC, or INTD) using `cfg_interrupt_di[7:0]` as shown in [Table 5-15](#). The Virtex-5 FPGA Integrated Block for PCI Express only supports advertisement of Interrupt INTA in the Interrupt Pin Register. Users who want to use INTB, INTC, or INTD messages must evaluate the system to confirm that it still recognizes INTB, INTC, and INTD messages even though the interrupt pin only advertises INTA.
- The core then asserts `cfg_interrupt_rdy_n` to indicate the interrupt has been accepted. On the following clock cycle, the User Application deasserts `cfg_interrupt_n` and, if the Interrupt Disable bit in the PCI Command register is set to 0, the core sends an assert interrupt message (Assert_INTA, Assert_INTB, and so forth).
- When the User Application has determined that the interrupt has been serviced, it asserts `cfg_interrupt_n` while deasserting `cfg_interrupt_assert_n` to deassert the interrupt. The appropriate interrupt must be indicated via `cfg_interrupt_di[7:0]`.
- The core then asserts `cfg_interrupt_rdy_n` to indicate the interrupt deassertion has been accepted. On the following clock cycle, the User Application deasserts `cfg_interrupt_n` and the core sends a deassert interrupt message (Deassert_INTA, Deassert_INTB, and so forth).

Note: The Interrupt Status bit in the Status register in the PCI Configuration Space Header (`cfg_status[3]`) does not reflect the state of a pending interrupt in the device/function.

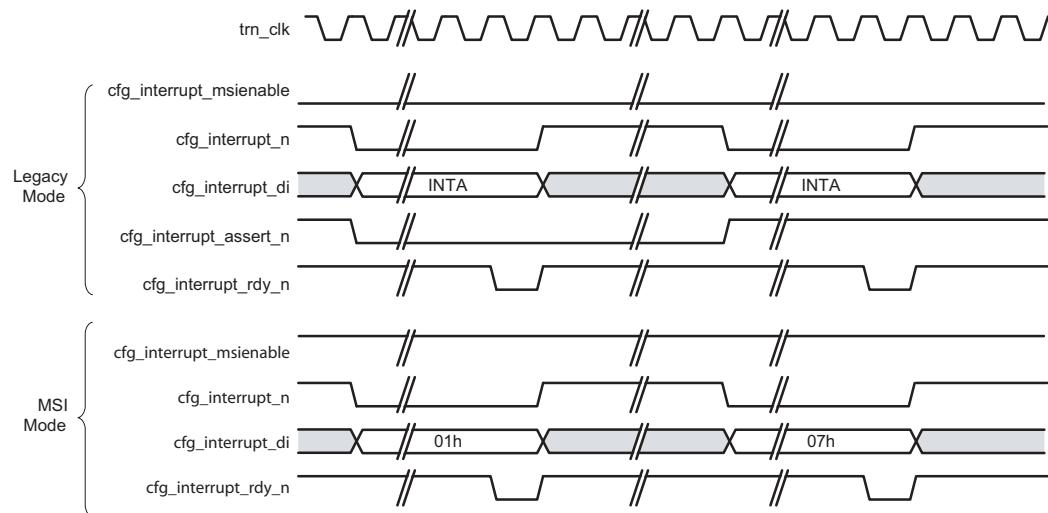


Figure 5-28: Requesting Interrupt Service: MSI and Legacy Mode

Table 5-15: Legacy Interrupt Mapping

<code>cfg_interrupt_di[7:0]</code> value	Legacy Interrupt
00h	INTA
01h	INTB ¹
02h	INTC ¹
03h	INTD ¹
04h - FFh	Not Supported

1. The Virtex-5 FPGA Integrated Block for PCI Express only supports advertisement of Interrupt INTA in the Interrupt Pin Register.

Link Training: 2-Lane, 4-Lane and 8-Lane Endpoints

The 2-lane, 4-lane and 8-lane Endpoint Block Plus cores for PCI Express are capable of operating at less than the maximum lane width as required by the *PCI Express Base Specification*. Two cases cause core to operate at less than its specified maximum lane width, as defined in the following sections.

Upstream Partner Supports Fewer Lanes

When the 4-lane core is connected to an upstream device that implements 1 lane, the 4-lane core trains and operates as a 1-lane device using lane 0, as shown in [Figure 5-29](#). Similarly, if the 4-lane core is connected to a 2-lane upstream device, the core trains and operates as a 2-lane device using lanes 0 and 1.

When the 8-lane core is connected to an upstream device that only implements 4 lanes, it trains and operates as a 4-lane device using lanes 0-3. Additionally, if the upstream device only implements 1 or 2 lanes, the 8-lane core trains and operates as a 1- or 2-lane device.

When the 2-lane core is connected to an upstream device that implements 1 lane, the 2-lane core trains and operates as a 1-lane device using lane 0.

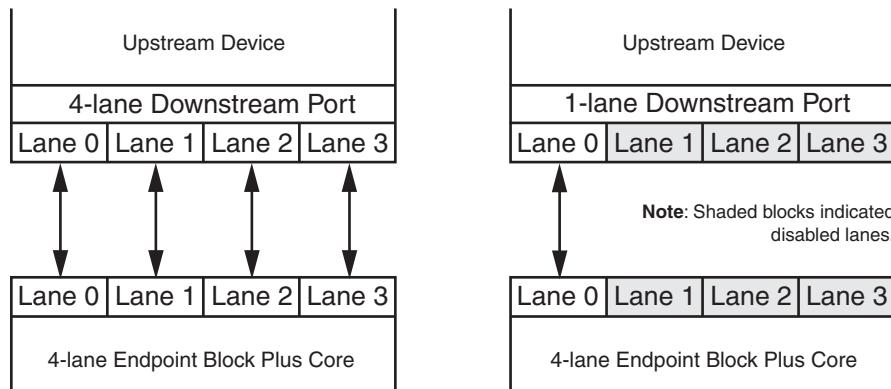


Figure 5-29: Scaling of 4-Lane Endpoint Core from 4-Lane to 1-Lane Operation

Lane Becomes Faulty

If a link becomes faulty after training to the maximum lane width supported by the core and the link partner device, the core attempts to recover and train to a lower lane width, if available. If lane 0 becomes faulty, the link is irrecoverably lost. If any or all of lanes 1-7 become faulty, the link goes into *recovery* and attempts to recover the largest viable link with whichever lanes are still operational.

For example, when using the 8-lane core, loss of lane 1 yields a recovery to 1-lane operation on lane 0, whereas the loss of lane 6 yields a recovery to 4-lane operation on lanes 0-3. After recovery occurs, if the failed lane(s) becomes *alive* again, the core does not attempt to recover to a wider link width. The only way a wider link width can occur is if the link actually goes down and it attempts to retrain from scratch.

The `trn_clk` clock output is a fixed frequency configured in the CORE Generator tool GUI. `trn_clk` does not shift frequencies in case of link recovery or training down.

Lane Reversal

The integrated Endpoint block supports limited lane reversal capabilities and therefore provides flexibility in the design of the board for the link partner. The link partner can choose to lay out the board with reversed lane numbers, and the integrated Endpoint block will continue to link train successfully and operate normally. The configurations that have lane reversal support are x8 and x4 (excluding downshift modes). Downshift refers to the link width negotiation process that occurs when link partners have different lane width capabilities advertised. As a result of lane width negotiation, the link partners negotiate down to the smaller of the two advertised lane widths. [Table 5-16](#) describes the several possible combinations including downshift modes and availability of lane reversal support.

Table 5-16: Lane Reversal Support

Endpoint Block Advertised Lane Width	Negotiated Lane Width	Lane Number Mapping (Endpoint Link Partner)		Lane Reversal Supported
		Endpoint	Link Partner	
x8	x8	Lane 0 ... Lane 7	Lane 7 ... Lane 0	Yes
x8	x4	Lane 0 ... Lane 3	Lane 7 ... Lane 4	No ¹
x8	x2	Lane 0 ... Lane 3	Lane 7 ... Lane 6	No ¹
x4	x4	Lane 0 ... Lane 3	Lane 3 ... Lane 0	Yes
x4	x2	Lane 0 ... Lane 1	Lane 3 ... Lane 2	No ¹

1. When the lanes are reversed in the board layout and a downshift adapter card is inserted between the Endpoint and link partner, Lane 0 of the link partner remains unconnected (as shown by the lane mapping in [Table 5-16](#)) and therefore does not link train.

Clocking and Reset of the Block Plus Core

Reset

The Endpoint Block Plus core for PCIe uses `sys_reset_n` to reset the system, an asynchronous, active-Low reset signal asserted during the PCI Express Fundamental Reset. Asserting this signal causes a hard reset of the entire core, including the RocketIO™ transceivers. After the reset is released, the core attempts to link train and resume normal operation. In a typical Endpoint application, for example, an add-in card, a sideband reset signal is normally present and should be connected to `sys_reset_n`. For Endpoint applications that do not have a sideband system reset signal, the initial hardware reset should be generated locally. Three reset events can occur in PCI Express:

- **Cold Reset.** A Fundamental Reset that occurs at the application of power. The signal `sys_reset_n` is asserted to cause the cold reset of the core.
- **Warm Reset.** A Fundamental Reset triggered by hardware without the removal and re-application of power. The `sys_reset_n` signal is asserted to cause the warm reset to the core.
- **Hot Reset:** In-band propagation of a reset across the PCI Express Link through the protocol. In this case, `sys_reset_n` is not used.

The User Application interface of the core has an output signal called `trn_reset_n`. This signal is deasserted synchronously with respect to `trn_clk`. `trn_reset_n` is asserted as a result of any of the following conditions:

- **Fundamental Reset:** Occurs (cold or warm) due to assertion of `sys_reset_n`.
- **PLL within the embedded Block:** Loses lock, indicating an issue with the stability of the clock input.
- **Loss of GTP/GTX PLL Lock:** The Lane 0 transceiver loses lock, indicating an issue with the PCI Express Link.

The `trn_reset_n` signal deasserts synchronously with `trn_clk` after all of the above reasons are resolved, allowing the core to attempt to train and resume normal operation.

Important Note: Systems designed to the PCI Express electro-mechanical specification provide a sideband reset signal, which uses 3.3V signaling levels—see the FPGA device data sheet to understand the requirements for interfacing to such signals.

Clocking

The Endpoint Block Plus core input system clock signal is called `sys_clk`. The core requires a 100 MHz or 250 MHz clock input. The clock frequency used must match the clock frequency selection in the CORE Generator tool GUI. For more information, see [Answer Record 18329](#).

In a typical PCI Express solution, the PCI Express reference clock is a Spread Spectrum Clock (SSC), provided at 100 MHz. In most commercial PCI Express systems, SSC cannot be disabled. For more information regarding SSC and PCI Express, see section 4.3.1.1.1 of the *PCI Express Base Specification*.

Synchronous and Non-Synchronous Clocking

There are two ways to clock the PCI Express system:

- Using synchronous clocking, where a shared clock source is used for all devices.
- Using non-synchronous clocking, where each device has its own clock source.

Important Note: Xilinx recommends that designers use synchronous clocking when using the core. All add-in card designs must use synchronous clocking due to the characteristics of the provided reference clock. See [UG196, Virtex-5 FPGA RocketIO GTP Transceiver User Guide](#) and the device data sheet for additional information regarding reference clock requirements.

Non-synchronous clocking can be used in embedded or backplane applications when the designer can guarantee that neither the oscillator sourcing the Xilinx® FPGA or the oscillator sourcing the link partner device uses Spread Spectrum Clocking (SSC). Also both clocks must meet the ppm tolerance requirements of the PCI Express specification and the Xilinx FPGA.

For synchronous clocked systems, each link partner device shares the same clock source. [Figure 5-30](#) and [Figure 5-32](#) show a system using a 100 MHz reference clock. When using the 250 MHz reference clock option, an external PLL must be used to do a multiply of 5/2 to convert the 100 MHz clock to 250 MHz, as illustrated in [Figure 5-31](#) and [Figure 5-33](#). See [Answer Record 18329](#) for more information about clocking requirements.

Further, even if the device is part of an embedded system, if the system uses commercial PCI Express root complexes or switches along with typical mother board clocking schemes, synchronous clocking should still be used as shown in [Figure 5-30](#) and [Figure 5-31](#).

Figure 5-31 and Figure 5-33 illustrate high-level representations of the board layouts. Designers must ensure that proper coupling, termination, and so forth are used when laying out the board.

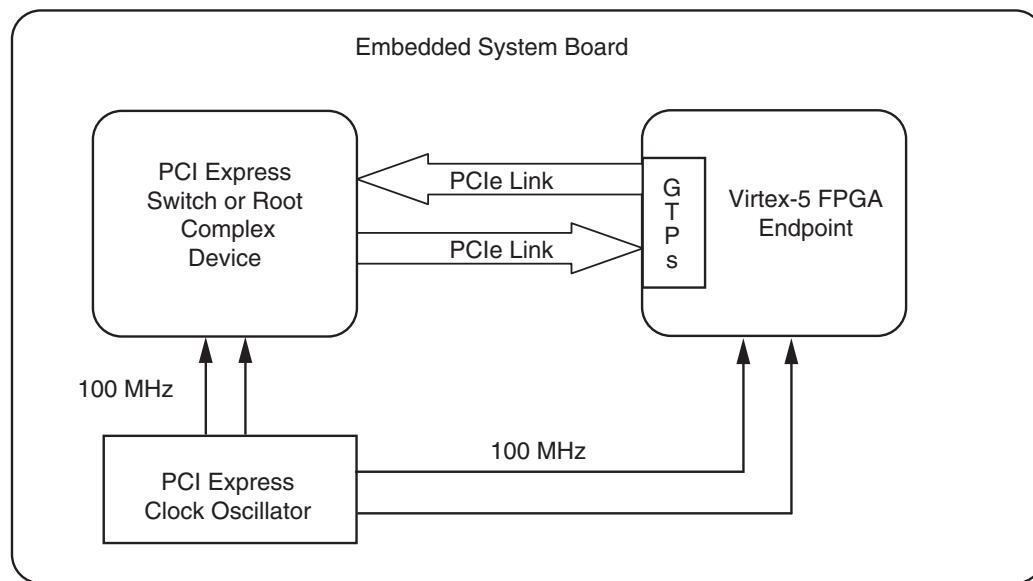


Figure 5-30: **Embedded System Using 100 MHz Reference Clock**

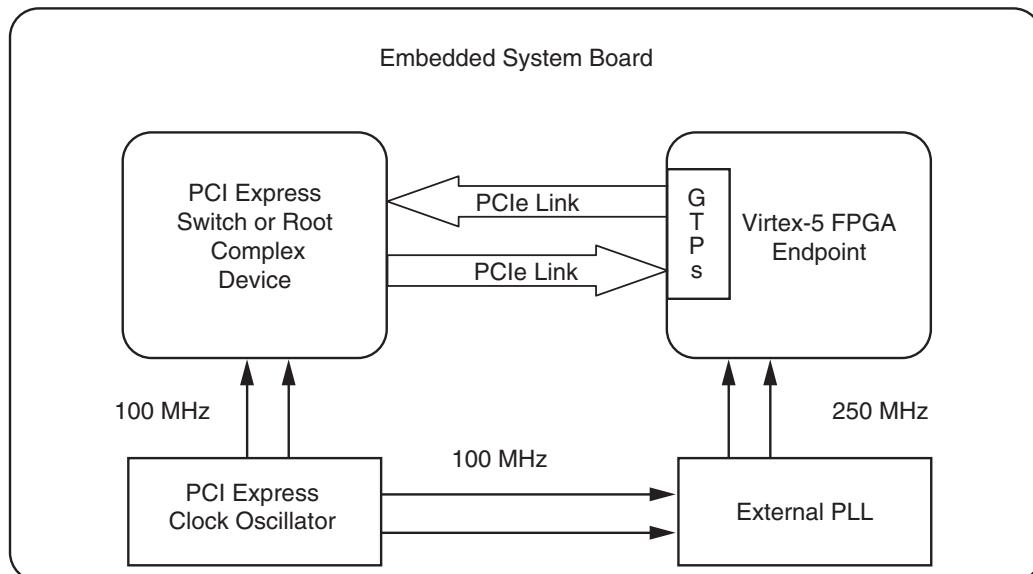


Figure 5-31: **Embedded System Using 250 MHz Reference Clock**

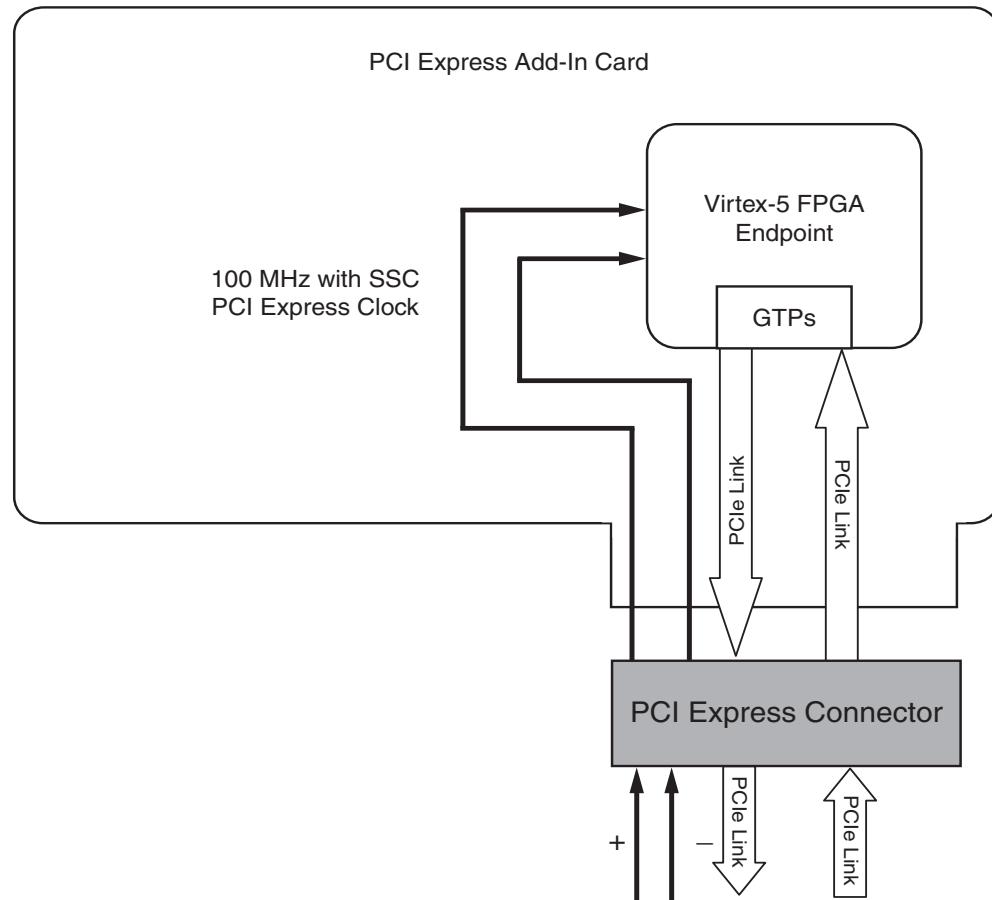


Figure 5-32: Open System Add-In Card Using 100 MHz Reference Clock

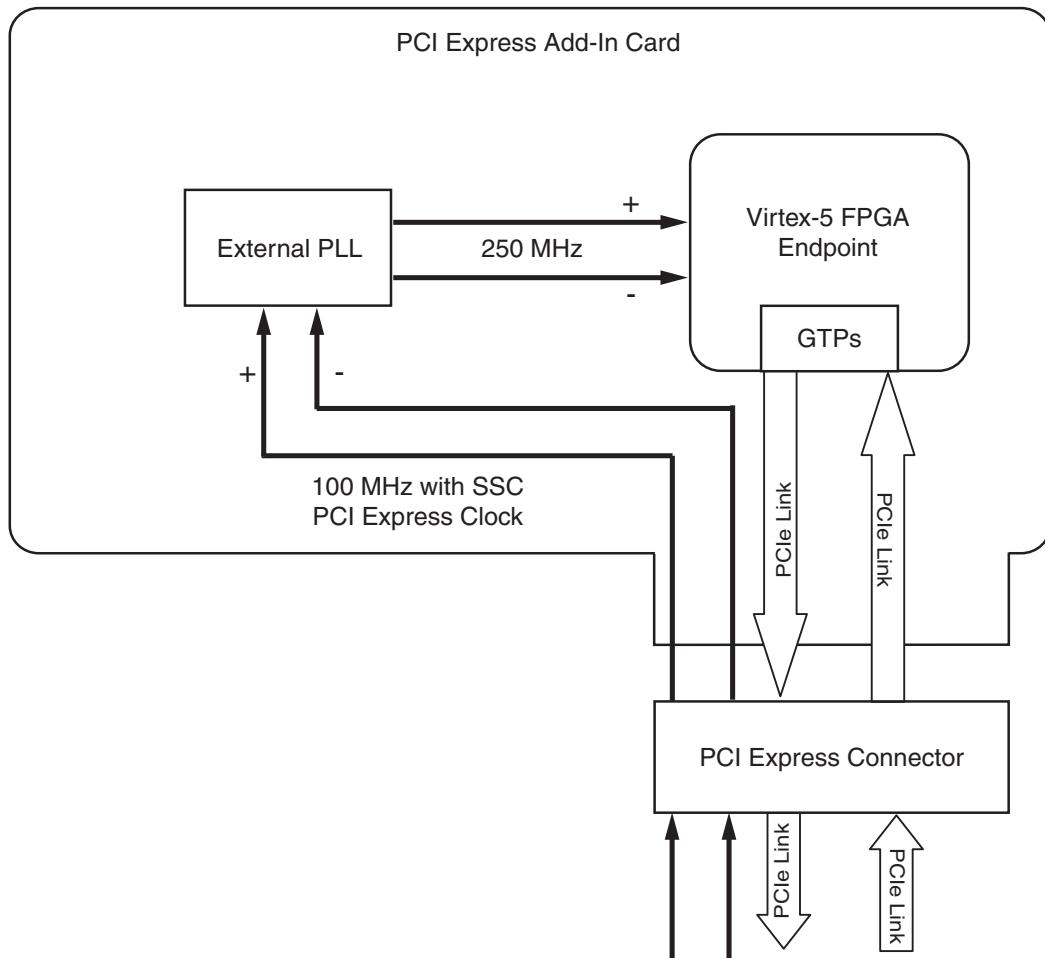


Figure 5-33: Open System Add-In Card Using 250 MHz Reference Clock

Core Constraints

The Endpoint Block Plus for PCI Express® solutions require the specification of timing and other physical implementation constraints to meet specified performance requirements for PCI Express. These constraints are provided with the Endpoint Solutions in a User Constraints File (UCF).

To achieve consistent implementation results, a UCF containing these original, unmodified constraints must be used when a design is run through the Xilinx tools. For additional details on the definition and use of a UCF or specific constraints, see the Xilinx Libraries Guide and/or Development System Reference Guide.

Constraints provided with Block Plus solutions have been tested in hardware and provide consistent results. Constraints can be modified, but modifications should only be made with a thorough understanding of the effect of each constraint. Additionally, support is not provided for designs that deviate from the provided constraints.

Contents of the User Constraints File

Although the UCF delivered with each core shares the same overall structure and sequence of information, the content of each core's UCF varies. The sections that follow define the structure and sequence of information in a generic UCF.

Part Selection Constraints: Device, Package, and Speed Grade

The first section of the UCF specifies the exact device for the implementation tools to target, including the specific part, package, and speed grade. In some cases, device-specific options are included.

User Timing Constraints

The User Timing constraints section is not populated; it is a placeholder for the designer to provide timing constraints on user-implemented logic.

User Physical Constraints

The User Physical constraints section is not populated; it is a placeholder for the designer to provide physical constraints on user-implemented logic.

Core Pinout and I/O Constraints

The Core Pinout and I/O constraints section contains constraints for I/Os belonging to the core's System (SYS) and PCI Express (PCI_EXP) interfaces. It includes location constraints for pins and I/O logic as well as I/O standard constraints.

Core Physical Constraints

Physical constraints are used to limit the core to a specific area of the device and to specify locations for clock buffering and other logic instantiated by the core.

Core Timing Constraints

This Core Timing constraints file defines clock frequency requirements for the core and specifies which nets the timing analysis tool should ignore.

Required Modifications

Several constraints provided in the UCF utilize hierarchical paths to elements within the Block Plus core. These constraints assume an instance name of *ep* for the core. If a different instance name is used, replace *ep* with the actual instance name in all hierarchical constraints.

For example:

Using *xilinx_pcie_ep* as the instance name, the physical constraint

```
INST "ep/pcie_ep0/pcie_blk/clocking_i/use_pll pll_adv_i"
LOC = PLL_ADV_X0Y2;
```

becomes

```
INST "xilinx_pcie_ep/pcie_ep0/pcie_blk/clocking_i/use_pll pll_adv_i"
LOC = PLL_ADV_X0Y2;
```

The provided UCF includes blank sections for constraining user-implemented logic. While the constraints provided adequately constrain the Block Plus core itself, they cannot adequately constrain user-implemented logic interfaced to the core. Additional constraints must be implemented by the designer.

Device Selection

The device selection portion of the UCF informs the implementation tools which part, package, and speed grade to target for the design. Because Block Plus cores are designed for specific part and package combinations, this section should not be modified by the designer.

The device selection section always contains a part selection line, but can also contain part or package-specific options. An example part selection line:

```
CONFIG PART = XC5VLX50T-FF1136-1
```

Core I/O Assignments

This section controls the placement and options for I/Os belonging to the core's System (SYS) interface and PCI Express (PCI_EXP) interface. NET constraints in this section control the pin location and I/O options for signals in the SYS group. Locations and options vary depending on which derivative of the core is used and should not be changed without fully understanding the system requirements.

For example:

```
NET "sys_reset_n" LOC = "AF21" | IOSTANDARD = LVCMOS33 | NODELAY;
NET "sys_clk_p" LOC = "Y4"
```

```

NET "sys_clk_n" LOC = "Y3"
INST "refclk_ibuf" DIFF_TERM= "TRUE" ;
// The GTP has a fixed internal differential termination, which cannot
be disabled.

```

See [Clocking and Reset of the Block Plus Core, page 131](#) for detailed information about reset and clock requirements.

Each GTP_DUAL tile contains two transceivers. The even numbered lane is always placed on transceiver 0 and the odd numbered lane is on transceiver 1 for a given GTP_DUAL tile in use. For GTP_DUAL pinout information, see “Package Placement Information” in the Implementation chapter of the *Virtex®-5 FPGA RocketIO GTP Transceiver User Guide* ([UG196](#)).

INST constraints are used to control placement of signals that belong to the PCI_EXP group. These constraints control the location of the transceiver(s) used, which implicitly controls pin locations for the transmit and receive differential pair. One-lane cores consume *both* transceivers in a tile even though only one is used.

For example:

```

INST "ep/pcie_ep0/pcie_blk/SIO/.pcie_gt_wrapper_i/GTD[0].GT_i"
LOC = GTP_DUAL_X0Y0;

```

Table 6-1 shows how the GTP_DUAL tiles in the INST constraints correspond to the GTP transceiver locations and the Block Plus core lane numbers for x1, x2, x4, and x8 designs.

Table 6-1: Corresponding Lane Numbers and GTP Transceiver Locations

UCF GTP_DUAL Instance Name	GTP Transceiver 0 or 1	x01	x02	x04	x08
GTD[0].GT_i	0	Lane 0	Lane 0	Lane 0	Lane 0
	1	N/C	Lane 1	Lane 1	Lane 1
GTD[2].GT_i	0			Lane 2	Lane 2
	1			Lane 3	Lane 3
GTD[4].GT_i	0				Lane 4
	1				Lane 5
GTD[6].GT_i	0				Lane 6
	1				Lane 7

Core Physical Constraints

Physical constraints are included in the constraints file to control the location of clocking and other elements and to limit the core to a specific area of the FPGA fabric. Specific physical constraints are chosen to match each supported device and package combination—it is very important to leave these constraints unmodified.

Physical constraints example:

```

INST "ep/pcie_ep0/pcie_blk/clocking_i/use_pll pll_adv_i"
LOC = PLL_ADV_X0Y2;
AREA_GROUP "GRP0" RANGE = SLICE_X58Y59:SLICE_X59Y56 ;
INST "ep/ep/pcie_blk/SIO/.pcie_gt_wrapper_i/gt_tx_data_k_reg_0"
AREA_GROUP = "GRP0" ;

```

Core Timing Constraints

Timing constraints are provided for all Block Plus solutions, although they differ for each product. In all cases they are crucial and must not be modified, except to specify the top-level hierarchical name. Timing constraints are divided into two categories:

- **TIG constraints.** Used on paths where specific delays are unimportant, to instruct the timing analysis tools to refrain from issuing *Unconstrained Path* warnings.
- **Frequency constraints.** Group clock nets into time groups and assign properties and requirements to those groups.
- **Delay constraints.** Controls delays on internal nets.

TIG constraints example:

```
NET "sys_reset_n" TIG;
```

Clock constraints example:

First, the input reference clock period is specified, which can be either 100 MHz or 250 MHz (selected in the CORE Generator™ tool GUI).

```
NET "sys_clk_c"          PERIOD = 10ns;    # OR
NET "sys_clk_c"          PERIOD = 4ns;
```

Next, the internally generated clock net and period is specified, which can be either 100 MHz or 250 MHz. (*Both* clock constraints must be specified as either 100 MHz or 250 MHz.)

```
NET "ep/pcie_ep0/pcie_blk/SIO/.pcie_gt_wrapper_i/gt_refclk_out[0]"
TNM_NET = "MGTCLOCK" ;
TIMESPEC "TS_MGTCLOCK" = PERIOD "MGTCLOCK" 250.00 MHz HIGH 50 % ; # OR
TIMESPEC "TS_MGTCLOCK" = PERIOD "MGTCLOCK" 100.00 MHz HIGH 50 % ;
```

Delay constraints example:

```
NET "ep/ep/pcie_blk/SIO/.pcie_gt_wrapper_i/gt_tx_elec_idle_reg"
MAXDELAY = 1.0 ns;
```

Core Implementation Constraints

While implementing the core in ISE® software, the map and bitgen stage give this warning message:

```
WARNING:PhysDesignRules:372 - Gated clock. Clock net
I_pcie_core_wrapper/I_pci_express_wrapper/BU2/U0/pcie_ep0/pcie_blk/SIO
/.pcie_gt_wrapper_i/icdrreset<0> is sourced by a combinatorial pin.
This is not good design practice. Use the CE pin to control the loading
of data into the flip-flop.
```

The warning message can be safely ignored and is due to a required circuit for the serial transceivers to function properly.

Relocating the Endpoint Block Plus Core

While Xilinx does not provide technical support for designs whose system clock input, GTP transceivers, or block RAM locations are different from the provided examples, it is possible to relocate the core within the FPGA. The locations selected in the provided examples are the recommended pinouts. These locations have been chosen based on the proximity to the Endpoint block, which enables meeting 250 MHz timing, and because

they are conducive to layout requirements for add-in card design. If the core is moved, the relative location of all transceivers and clocking resources should be maintained to ensure timing closure.

Supported Core Pinouts

[Table 6-2](#), [Table 6-3](#), and [Table 6-4](#) define the supported core pinouts for various LXT, SXT, FXT, and TXT part and package combinations. The CORE Generator software provides a UCF for the selected part and package that matches the content of this table.

Table 6-2: Supported Core Pinouts Virtex-5 LXT/SXT FPGAs

Package	Virtex-5 LXT / SXT Part		x1, x2	x4	x8
FF665	XC5VLX30T XC5VSX35T	Lane 0/1	X0Y3	X0Y3	X0Y3
		Lane 2/3		X0Y2	X0Y2
		Lane 4/5			X0Y1
		Lane 6/7			X0Y0
	XC5VLX50T XC5VSX50T	Lane 0/1	X0Y4	X0Y4	X0Y4
		Lane 2/3		X0Y3	X0Y3
		Lane 4/5			X0Y2
		Lane 6/7			X0Y1
FF1136	XC5VLX50T XC5VLX85T XC5VSX50T	Lane 0/1	X0Y3	X0Y3	X0Y3
		Lane 2/3		X0Y2	X0Y2
		Lane 4/5			X0Y1
		Lane 6/7			X0Y0
	XC5VLX110T XC5VLX155T XC5VSX95T	Lane 0/1	X0Y4	X0Y4	X0Y4
		Lane 2/3		X0Y3	X0Y3
		Lane 4/5			X0Y2
		Lane 6/7			X0Y1
FF1738	XC5VLX110T XC5VLX155T XC5VLX220T XC5VSX240T	Lane 0/1	X0Y5	X0Y5	X0Y5
		Lane 2/3		X0Y4	X0Y4
		Lane 4/5			X0Y3
		Lane 6/7			X0Y2
	XC5VLX330T	Lane 0/1	X0Y7	X0Y7	X0Y7
		Lane 2/3		X0Y6	X0Y6
		Lane 4/5			X0Y5
		Lane 6/7			X0Y4
FF323	XC5VLX20T XC5VLX30T	Lane 0/1	X0Y2	X0Y2	NA
		Lane 2/3		X0Y1	NA

Table 6-3: Supported Core Pinouts Virtex-5 FXT FPGAs

Package	Virtex-5 FXT Part	PCIe Block Location		x1, x2	x4	x8
FF665	XC5VFX30T	X0Y0	Lane 0/1	X0Y3	X0Y3	X0Y3
			Lane 2/3		X0Y2	X0Y2
			Lane 4/5			X0Y1
			Lane 6/7			X0Y0
	XC5VFX70T	X0Y1	Lane 0/1	X0Y5	X0Y5	X0Y5
			Lane 2/3		X0Y4	X0Y4
			Lane 4/5			X0Y3
			Lane 6/7			X0Y2
FF1136	XC5VFX70T XC5VFX100T	X0Y0	Lane 0/1	X0Y3	X0Y3	X0Y3
			Lane 2/3		X0Y2	X0Y2
			Lane 4/5			X0Y1
			Lane 6/7			X0Y0
	XC5VFX70T XC5VFX100T	X0Y1	Lane 0/1	X0Y4	X0Y4	X0Y4
			Lane 2/3		X0Y3	X0Y3
			Lane 4/5			X0Y2
			Lane 6/7			X0Y1
	XC5VFX70T XC5VFX100T	X0Y2	Lane 0/1	X0Y7	X0Y7	X0Y7
			Lane 2/3		X0Y6	X0Y6
			Lane 4/5			X0Y5
			Lane 6/7			X0Y4

Table 6-3: Supported Core Pinouts Virtex-5 FXT FPGAs (Cont'd)

Package	Virtex-5 FXT Part	PCIe Block Location		x1, x2	x4	x8
FF1738	XC5VFX100T	X0Y0	Lane 0/1	X0Y3	X0Y3	X0Y3
			Lane 2/3		X0Y2	X0Y2
			Lane 4/5			X0Y1
			Lane 6/7			X0Y0
	XC5VFX100T	X0Y1	Lane 0/1	X0Y4	X0Y4	X0Y4
			Lane 2/3		X0Y3	X0Y3
			Lane 4/5			X0Y2
			Lane 6/7			X0Y1
	XC5VFX100T	X0Y2	Lane 0/1	X0Y7	X0Y7	X0Y7
			Lane 2/3		X0Y6	X0Y6
			Lane 4/5			X0Y5
			Lane 6/7			X0Y4
	XC5VFX130T	X0Y0	Lane 0/1	X0Y1	X0Y1	X0Y3
			Lane 2/3		X0Y0	X0Y2
			Lane 4/5			X0Y1
			Lane 6/7			X0Y0
	XC5VFX130T	X0Y1	Lane 0/1	X0Y3	X0Y3	X0Y4
			Lane 2/3		X0Y2	X0Y3
			Lane 4/5			X0Y2
			Lane 6/7			X0Y1
	XC5VFX130T	X0Y2	Lane 0/1	X0Y7	X0Y7	X0Y9
			Lane 2/3		X0Y6	X0Y8
			Lane 4/5			X0Y7
			Lane 6/7			X0Y6
	XC5VFX200T	X0Y0	Lane 0/1	X0Y0	X0Y1	X0Y3
			Lane 2/3		X0Y0	X0Y2
			Lane 4/5			X0Y1
			Lane 6/7			X0Y0

Table 6-3: Supported Core Pinouts Virtex-5 FXT FPGAs (Cont'd)

Package	Virtex-5 FXT Part	PCIe Block Location		x1, x2	x4	x8
FF1738	XC5VFX200T	X0Y1	Lane 0/1	X0Y2	X0Y3	X0Y4
			Lane 2/3		X0Y2	X0Y3
			Lane 4/5			X0Y2
			Lane 6/7			X0Y1
	XC5VFX200T	X0Y2	Lane 0/1	X0Y4	X0Y5	X0Y5
			Lane 2/3		X0Y4	X0Y4
			Lane 4/5			X0Y3
			Lane 6/7			X0Y2
	XC5VFX200T	X0Y3	Lane 0/1	X0Y8	X0Y9	X0Y10
			Lane 2/3		X0Y8	X0Y9
			Lane 4/5			X0Y8
			Lane 6/7			X0Y7

Table 6-4: Supported Core Pinouts Virtex-5 TXT FPGAs

Package	Virtex-5 TXT Part		x1, x2	x4	x8
FF1759	XC5VTX150T XC5VTX240T	Lane 0/1	X1Y5	X1Y5	X1Y5
		Lane 2/3		X1Y4	X1Y4
		Lane 4/5			X1Y3
		Lane 6/7			X1Y2
	XC5VTX150T	Lane 0/1	X1Y4	X1Y4	X1Y4
		Lane 2/3		X1Y3	X1Y3
		Lane 4/5			X1Y2
		Lane 6/7			X1Y1

Hardware Verification

PCI Special Interest Group

Xilinx cannot list the actual systems tested at the PCI Special Interest Group ([PCI-SIG](#)) Compliance Workshops due to requirements of the PCI-SIG bylaws; however, Xilinx IP designers can view the [PCI-SIG integrators list](#).

PCI-SIG Integrators List

The integrators list confirms that Xilinx has satisfied the PCI-SIG Compliance Program and that the Endpoint Block Plus wrapper successfully interoperated with other available systems at the event. Virtex®-5 FPGA entries can be found in the Components and Add-In Cards sections under the company name Xilinx.

Hardware validation testing is performed at Xilinx for each release of the Endpoint Block Plus wrapper with the list of platforms defined in [Table 7-1](#). Hardware testing performed by Xilinx also available to customers includes the PCIECV tool available from the PCI-SIG website, BMD Design, available from [XAPP1052](#), and the MET design, available from [XAPP1022](#).

Table 7-1: Platforms Tested

System or Motherboard	Processor	Chipset	OS	Lanes
Dell Poweredge 1900 Server	Intel Xeon 5110 dual-core 1.60 GHz	Intel E5000	<ul style="list-style-type: none">Windows XP Professional v2002 Service Pack 2Red Hat Enterprise Linux 4	x8
SuperMicro X6DH8-G2 motherboard	Intel 64-bit Xeon 2.4 GHz, 800 MHz FSB	Intel 7520 (Lindenhurst)	Windows XP Professional Service Pack 2	x8
SuperMicro H8DCE motherboard	Dual-core AMD Opteron 200 Series processor	NVIDIA nForce Pro 2200 (CK804)	<ul style="list-style-type: none">Windows XP Professional Service Pack 2Red Hat Enterprise Linux 4	x8

Table 7-1: Platforms Tested (Cont'd)

System or Motherboard	Processor	Chipset	OS	Lanes
ASUS P5B-VM DO motherboard	Intel Pentium 4 531 Single Processor 3.0 GHz	Intel Q965 Express/Intel ICH8D0	Windows XP Professional v2002 Service Pack 2	x8
ASUSTeK Computer P5N32-SLI-Deluxe	Intel Pentium D 940 dual-core 3.2 GHz	NVIDIA nForce 4 SLI Intel Edition	Windows XP Professional v2002 Service Pack 2	x1, x4
Intel Platform Development Kit	Intel 64-bit dual-core Xeon 3.8 GHz, 1333 MHz FSB	Intel 5400 (Seaburg)	<ul style="list-style-type: none"> • Windows XP Professional v2002 Service Pack 2 • Red Hat Enterprise Linux 4 	x16

FPGA Configuration

This chapter discusses how to configure the Virtex®-5 FPGA so that the device can link up and be recognized by the system. This information is provided so you can choose the correct FPGA configuration method for your system and verify that it will work as expected.

This chapter discusses how specific requirements of the *PCI Express Base Specification* and *PCI Express Card Electromechanical Specification* apply to FPGA configuration. Where appropriate, Xilinx recommends that you read the actual specifications for detailed information. This chapter is divided into three sections:

- **Configuration Access Time.** Several specification items govern when an Endpoint device needs to be ready to receive configuration accesses from the host (Root Complex).
- **Board Power in Real-World Systems.** Understanding real-world system constraints related to board power and how they affect the specification requirements.
- **Recommendations.** Describes methods for FPGA configuration and includes sample problem analysis for FPGA configuration timing issues.

Configuration Terminology

In this chapter, the following terms are used to differentiate between FPGA configuration and configuration of the PCI Express® device:

- **Configuration of the FPGA.** *FPGA configuration* is used.
- **Configuration of the PCI Express device.** After the link is active, *configuration* is used.

Configuration Access Time

In standard systems for PCI Express, when the system is powered up, configuration software running on the processor starts scanning the PCI Express bus to discover the machine topology.

The process of scanning the PCI Express hierarchy to determine its topology is referred to as the *enumeration process*. The root complex accomplishes this by initiating configuration transactions to devices as it traverses and determines the topology.

All PCI Express devices are expected to have established the link with their link partner and be ready to accept configuration requests during the enumeration process. As a result, there are requirements as to when a device needs to be ready to accept configuration requests after power up; if the requirements are not met, the following occurs:

- If a device is not ready and does not respond to configuration requests, the root complex does not discover it and treats it as non-existent.
- The operating system does not report the device's existence and the user's application is not able to communicate with the device.

Choosing the appropriate FPGA configuration method is key to ensuring the device is able to communicate with the system in time to achieve link up and respond to the configuration accesses.

Configuration Access Specification Requirements

Two PCI Express specification items are relevant to configuration access:

1. Section 6.6 of *PCI Express Base Specification*, rev 1.1 states “A system must guarantee that all components intended to be software visible at boot time are ready to receive Configuration Requests within 100 ms of the end of Fundamental Reset at the Root Complex.” For detailed information about how this is accomplished, see the specification; it is beyond the scope of this discussion.

Xilinx has verified the Block Plus wrapper using the Virtex-5 FPGA Integrated Block for PCI Express is compliant with this requirement. From the end of the fundamental reset, the Block Plus wrapper is ready to receive configuration accesses within the 100 ms window.

Xilinx compliance to this specification is validated by the PCI Express-CV tests. The [PCI Special Interest Group \(PCI-SIG\)](#) provides the PCI Express Configuration Test Software to verify the device meets the requirement of being able to receive configuration accesses within 100 ms of the end of the fundamental reset. The software, available to any member of the PCI-SIG, generates several resets using the in-band reset mechanism and PERST# toggling to validate robustness and compliance to the specification. The Block Plus wrapper using the Virtex-5 FPGA Integrated Block for PCI Express has successfully passed this test and other requirements for compliance and is located on the [PCI-SIG integrator's list](#).

2. Section 6.6 of *PCI Express Base Specification*, rev 1.1 defines three parameters necessary “where power and PERST# are supplied.” The parameter T_{PVPERL} applies to FPGA configuration timing and is defined as:

T_{PVPERL} - PERST# must remain active at least this long after power becomes valid.

The PCI Express Base Specification does not give a specific value for T_{PVPERL} – only its meaning is defined. The most common form factor used by designers with the Endpoint Block Plus wrapper is an ATX-based form factor. The PCI Express Card Electromechanical Specification focuses on requirements for ATX-based form factors. This applies to most designs targeted to standard desktop or server type motherboards. Figure 8-1 shows the relationship between Power Stable and PERST#. (This figure is based on Figure 2-10 from section 2.1 of PCI Express Card Electromechanical Specification, rev 1.1.)

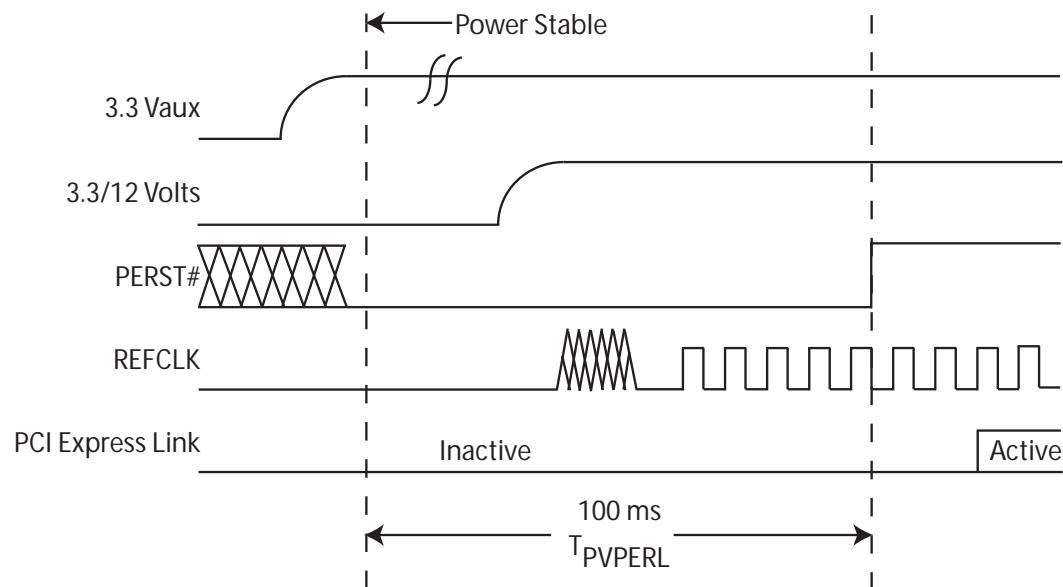


Figure 8-1: Power Up

Section 2.6.2 of the PCI Express Card Electromechanical Specification defines T_{PVPERL} as a minimum of 100 ms, indicating that from the time power is stable the system reset is asserted for at least 100 ms (as shown in Table 8-1).

Table 8-1: T_{PVPERL} Specification

Symbol	Parameter	Min	Max	Units
T_{PVPERL}	Power stable to PERST# inactive	100		ms

From [Figure 8-1](#) and [Table 8-1](#), it is possible to obtain a simple equation to define the FPGA configuration time as follows:

$$\text{FPGA Configuration Time} \leq T_{\text{PWRVLD}} + T_{\text{PVPERL}}$$

Given that T_{PVPERL} is defined as 100 ms minimum, this becomes:

$$\text{FPGA Configuration Time} \leq T_{\text{PWRVLD}} + 100 \text{ ms}$$

Note: Although T_{PWRVLD} is included in the previous equation, it has yet to be defined in this discussion because it depends on the type of system in use. The next section, [Board Power in Real-World Systems](#) defines T_{PWRVLD} for both ATX-based and non ATX-based systems.

FPGA configuration time is only relevant at cold boot; subsequent warm or hot resets do not cause reconfiguration of the FPGA. If you suspect the design is having problems due to FPGA configuration, issue a warm reset as a simple test, which resets the system, including the PCI Express link, but keeps the board powered. If the problem does not appear, the issue could be FPGA configuration time related.

Board Power in Real-World Systems

Several boards are used in PCI Express systems. The *ATX Power Supply Design* specification, endorsed by Intel, is used as a guideline and for this reason followed in the majority of motherboards and 100% of the time if it is an Intel-based motherboard. The relationship between power rails and power valid signaling is described in the [ATX 12V Power Supply Design Guide](#). [Figure 8-2](#), redrawn here and simplified to show the information relevant to FPGA configuration, is based on the information and diagram found in section 3.3 of the *ATX 12V Power Supply Design Guide*. For the entire diagram and definition of all parameters, see the *ATX 12V Power Supply Design Guide*.

[Figure 8-2](#) shows that power stable indication from [Figure 8-1](#) for the PCI Express system is indicated by the assertion of `PWR_OK`. `PWR_OK` is asserted High after some delay after the power supply has reached 95% of nominal.

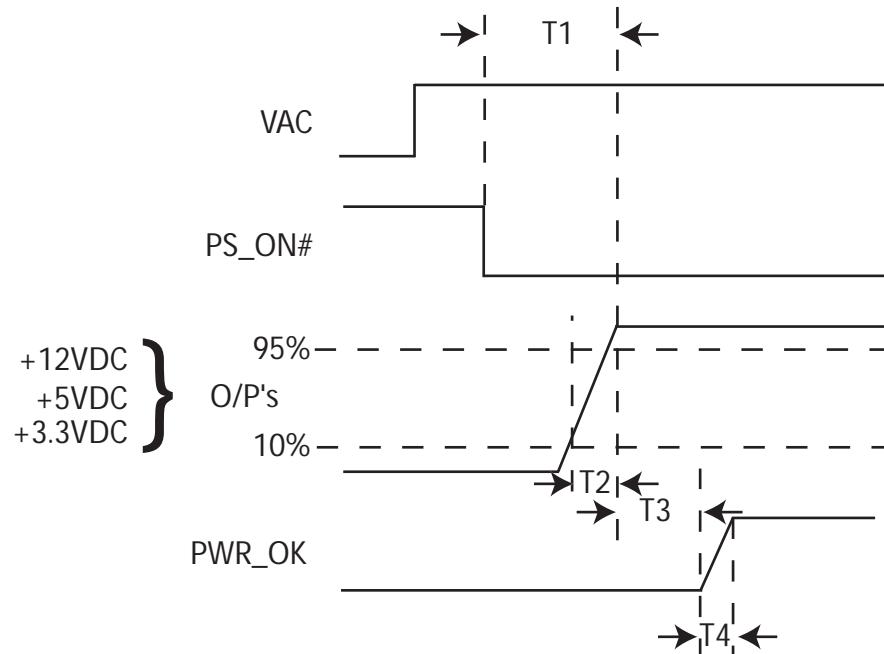


Figure 8-2: ATX Power Supply

Figure 8-2 shows that power is actually valid before PWR_OK is asserted High. This is represented by T3 and is the PWR_OK delay. The *ATX 12V Power Supply Design Guide* defines PWR_OK as $100 \text{ ms} < T3 < 500 \text{ ms}$, indicating the following: From the point at which the power level reaches 95% of nominal, there is a minimum of at least 100 ms but no more than 500 ms of delay before PWR_OK is asserted. Remember, according to the *PCI Express Card Electromechanical Specification*, the PERST# is guaranteed to be asserted a minimum of 100 ms from when power is stable indicated in an ATX system by the assertion of PWR_OK.

Again, the FPGA configuration time equation is:

$$\text{FPGA Configuration Time} \leq T_{\text{PWRVLD}} + 100 \text{ ms}$$

T_{PWRVLD} is defined as PWR_OK delay period, that is, T_{PWRVLD} represents the amount of time that power is valid in the system before PWR_OK is asserted. This time can be added to the amount of time the FPGA has to configure. The minimum values of T2 and T4 are negligible and considered zero for purposes of these calculations. For ATX-based motherboards, which represent the majority of real-world motherboards in use, T_{PWRVLD} can be defined as:

$$100 \text{ ms} \leq T_{\text{PWRVLD}} \leq 500 \text{ ms}$$

This provides the following requirement for FPGA configuration time in both ATX and non-ATX-based motherboards:

- FPGA Configuration Time \leq 200 ms (for ATX based motherboard)
- FPGA Configuration Time \leq 100 ms (for non-ATX based motherboard)

The second equation for the non-ATX based motherboards assumes a T_{PWRVLD} value of 0 ms because it is not defined in this context. Designers with non-ATX based motherboards should evaluate their own power supply design to obtain a value for T_{PWRVLD} .

Recommendations

Xilinx recommends using the [Platform Flash XL High-Density Storage and Configuration Device](#) (XCF128X) in Slave SelectMAP x16 Mode with a CCLK frequency of 50 MHz, which allows time for FPGA configuration on any Virtex-5 FPGA in ATX-based motherboards. Other valid configuration options are represented by green cells in [Table 8-2](#) and [Table 8-3](#) depending on the type of system in use. This section discusses these recommendations and includes sample analysis of potential problems that may arise during FPGA configuration.

FPGA Configuration Times for Virtex-5 Devices

During power up, the FPGA configuration sequence is performed in four steps:

1. Wait for POR (Power on Reset) for all voltages (V_{CCINT} , V_{CCAUX} , and V_{CCO}) in the FPGA to trip, referred to as POR Trip Time
2. Wait for completion (deassertion) of INIT to allow the FPGA to initialize before accepting a bitstream transfer.
- Note:** As a general rule, steps 1 and 2 require \leq 50 ms
3. Wait for assertion of DONE, the actual time required for a bitstream to transfer, and depends on the following:
 - Bitstream size
 - Clock frequency
 - Transfer mode used in the Flash Device
 - SPI = Serial Peripheral Interface
 - BPI = Byte Peripheral Interface
 - PFP = Platform Flash PROMs

For detailed information about the configuration process, see the *Virtex-5 FPGA Configuration User Guide* ([UG191](#)).

[Tables 8-2](#) and [8-3](#) show the comparative data for all Virtex-5 FPGA LXT and SXT devices with respect to a variety of flash devices and programming modes. The default clock rate for configuring the device is always 2 MHz. Any reference to a different clock rate implies a change in the settings of the device being used to program the FPGA. The configuration clock (CCLK), when driven by the FPGA, has variation and is not exact. See the *Virtex-5 FPGA Configuration Guide* for more information on CCLK tolerances.

Configuration Time Matrix: ATX Motherboards

Table 8-2 shows the configuration methods that allow the device to be configured before the end of the fundamental reset in ATX-based systems. The table values represent the bitstream transfer time only. The matrix is color-coded to show which configuration methods allow the device to configure within 200 ms once the FPGA initialization time is included. Choose a configuration method shaded in green when using ATX-based systems to ensure that the device is recognized.

Table 8-2: Configuration Time Matrix (ATX Motherboards): Virtex-5 FPGA Bitstream Transfer Time in Milliseconds

Virtex-5 FPGA	Bitstream (Bits)	SPIx1 ⁽¹⁾	BPIx16 ⁽²⁾ (Page Mode)	PFPx8 ⁽³⁾	XCF128X (Master BPIx16)	XCF128X ⁽⁴⁾ (Slave SelectMAPx16)
XC5VLX20T	6,251,200	125	57	24	25	8
XC5VLX30T	9,371,136	187	85	35	38	12
XC5VLX50T	14,052,352	281	128	53	57	18
XC5VLX85T	23,341,312	467	213	88	94	29
XC5VLX110T	31,118,848	622	284	118	125	39
XC5VLX155T	43,042,304	861	392	163	174	54
XC5VLX220T	55,133,696	1103	503	209	222	69
XC5VLX330T	82,696,192	1654	754	313	333	103
XC5VSX35T	13,349,120	267	122	51	54	17
XC5VSX50T	20,019,328	400	182	76	81	25
XC5VSX95T	35,716,096	714	326	135	144	45
XC5VSX240T	79,610,368	1592	726	302	321	100
XC5VFX30T	13,517,056	270	123	51	55	17
XC5VFX70T	27,025,408	541	246	102	109	34
XC5VFX100T	39,389,696	788	359	149	159	49
XC5VFX130T	49,234,944	985	449	186	199	62
XC5VFX200T	70,856,704	1417	646	268	286	89
XC5VTX150T	43,278,464	866	394	164	175	54
XC5VTX240T	65,755,648	1315	599	249	265	82

Bitstream Transfer Time + FPGA INIT Time (50 ms) ≤200 ms.

Bitstream Transfer Time + FPGA INIT Time (50 ms) > 200 ms

Bitstream Transfer Time > 200 ms

1. SPI flash assumptions: 50 MHz max
2. BPIx16 assumptions: P30 4-page read with 4-cycle first page read (4-1-1-1), maximum configuration time
3. PFP assumptions: 33 MHz max
4. XCF128X Slave SelectMAPx16 assumptions: CCLK = 50 MHz

Configuration Time Matrix: Non-ATX-Based Motherboards

Table 8-3 shows the configuration methods that allow the device to be configured before the end of the fundamental reset in non-ATX-based systems. This assumes T_{PWRVLD} is zero. The table values represent the bitstream transfer time only. The matrix is color-coded to show which configuration methods allow the device to configure within 100 ms once the FPGA initialization time is included. Choose a configuration method shaded in green when using non-ATX-based systems to ensure that the device is recognized.

For some of the larger FPGAs, it might not be possible to configure within the 100 ms window. In these cases, evaluate your system to see if any margin is available that can be assigned to T_{PWRVLD} .

Table 8-3: Configuration Time Matrix (Generic Platforms: Non-ATX Motherboards): Virtex-5 FPGA Bitstream Transfer Time in Milliseconds

Virtex-5 FPGA	Bitstream (Bits)	SPIx1 ⁽¹⁾	BPIx16 ⁽²⁾ (Page mode)	PFPx8 ⁽³⁾	XCF128X (Master BPIx16)	XCF128X ⁽⁴⁾ (Slave SelectMAPx16)
XC5VLX20T	6,251,200	125	57	24	25	8
XC5VLX30T	9,371,136	187	85	35	38	12
XC5VLX50T	14,052,352	281	128	53	57	18
XC5VLX85T	23,341,312	467	213	88	94	29
XC5VLX110T	31,118,848	622	284	118	125	39
XC5VLX155T	43,042,304	861	392	163	174	54
XC5VLX220T	55,133,696	1103	503	209	222	69
XC5VLX330T	82,696,192	1654	754	313	333	103
XC5VSX35T	13,349,120	267	122	51	54	17
XC5VSX50T	20,019,328	400	182	76	81	25
XC5VSX95T	35,716,096	714	326	135	144	45
XC5VSX240T	79,610,368	1592	726	302	321	100
XC5VFX30T	13,517,056	270	123	51	55	17
XC5VFX70T	27,025,408	541	246	102	109	34
XC5VFX100T	39,389,696	788	359	149	159	49
XC5VFX130T	49,234,944	985	449	186	199	62
XC5VFX200T	70,856,704	1417	646	268	286	89
XC5VTX150T	43,278,464	866	394	164	175	54
XC5VTX240T	65,755,648	1315	599	249	265	82

Legend:

- Green box: Bitstream Transfer Time + FPGA INIT Time (50 ms) ≤ 100 ms. Note: These entries adhere to the configuration time requirement; equation [4] defined in [Board Power in Real-World Systems](#). For these calculations, $T_{95\% \text{ PWR}}$ is negligible or close to zero.
- Yellow box: Bitstream Transfer Time + FPGA INIT Time (50 ms) > 100 ms
- Red box: Bitstream Transfer Time > 100 ms

1. SPI flash assumptions: 50 MHz max
2. BPIx16 assumptions: P30 4-page read with 4-cycle first page read (4-1-1-1), maximum configuration time
3. PFP assumptions: 33 MHz max
4. XCF128X Slave SelectMAPx16 assumptions: CCLK = 50 MHz

Sample Problem Analysis

This section presents data from an ASUS PL5 system to demonstrate the relationships between Power Valid, FPGA Configuration, and PERST#. [Figure 8-3](#) shows a case where the Endpoint failed to be recognized due to a FPGA configuration time issue. [Figure 8-4](#) shows a successful FPGA configuration with the Endpoint being recognized by the system.

Failed FPGA Recognition

[Figure 8-3](#) illustrates a failed cold boot test using the default configuration time on an LX50T FPGA. In this example, the host failed to recognize the Xilinx® FPGA. Although a second PERST# pulse assists in allowing more time for the FPGA to configure, the slowness of the FPGA configuration clock (2 MHz) causes configuration to complete well after this second deassertion. During this time, the system enumerated the bus and did not recognize the FPGA.

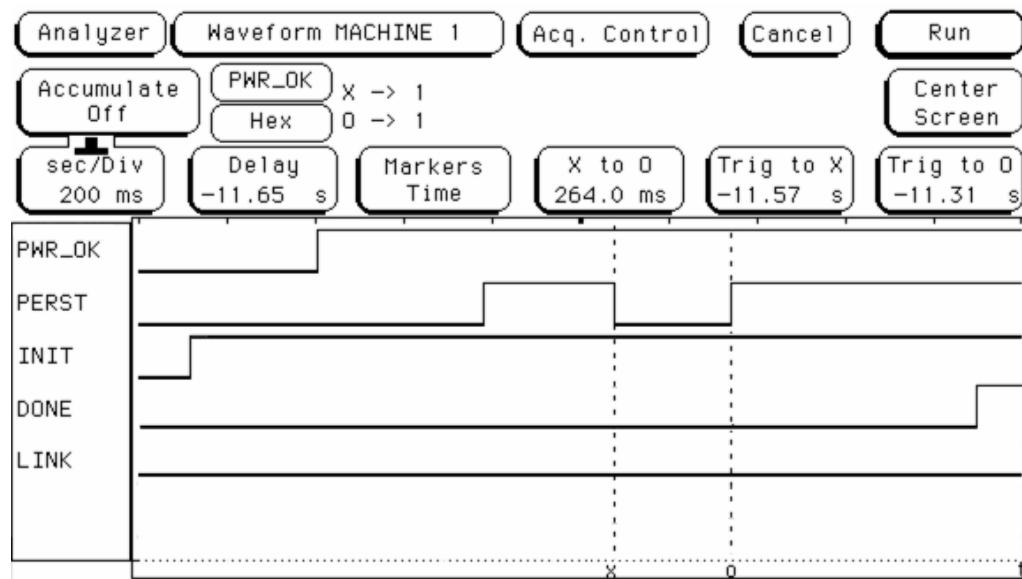


Figure 8-3: Default Configuration Time on LX50T Device (2 MHz Clock)

Successful FPGA Recognition

[Figure 8-4](#) illustrates a successful cold boot test on the same system. In this test, the CCLK was running at 50 MHz, allowing the FPGA to configure in time to be enumerated and recognized. The figure shows that the FPGA began initialization approximately 250 ns before PWR_OK. DONE going High shows that the FPGA was configured even before PWR_OK was asserted.

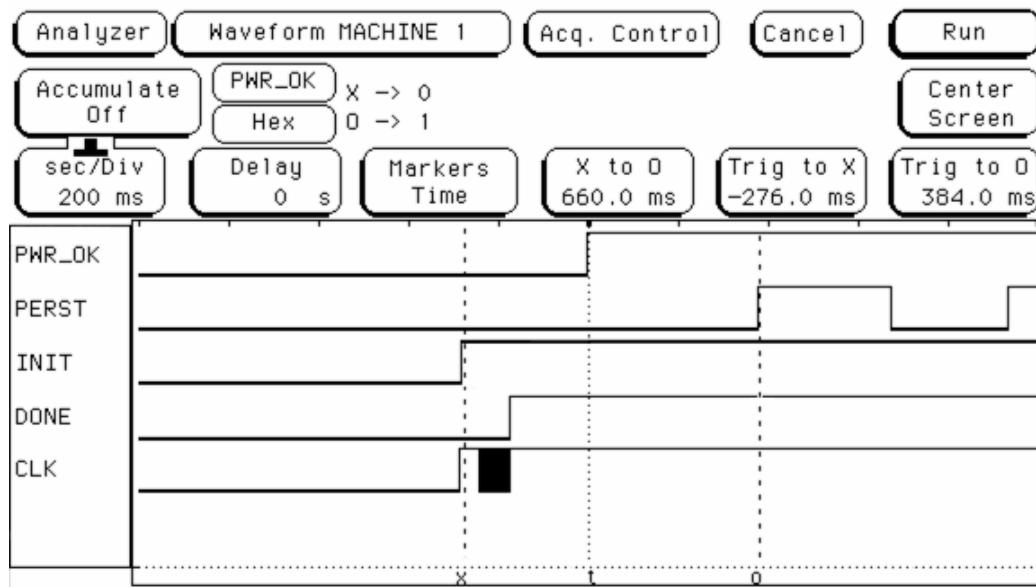


Figure 8-4: Fast Configuration Time on LX50T Device (50 MHz Clock)

Workarounds for Closed Systems

For failing FPGA configuration combinations, as represented by pink cells and yellow cells in [Table 8-2](#) and [Table 8-3](#), designers might be able to work around the problem in closed systems or systems where they can guarantee behavior. These options are not recommended for products where the targeted end system is unknown.

1. Check if the motherboard and BIOS generate multiple PERST# pulses at startup. This can be determined by capturing the signal on the board using an oscilloscope. (This is similar to what is shown in [Figure 8-3](#). If multiple PERST#s are generated, this typically adds extra time for FPGA configuration.

Define $T_{PERSTPERIOD}$ as the total sum of the pulse width of PERST# and deassertion period before the next PERST# pulse arrives. Because the FPGA is not power cycled or reconfigured with additional PERST# assertions, the $T_{PERSTPERIOD}$ number can be added to the FPGA configuration equation.

$$\text{FPGA Configuration Time} \leq T_{PWRVLD} + T_{PERSTPERIOD} + 100 \text{ ms}$$

2. In closed systems, it might be possible to create scripts to force the system to perform a warm reset after the FPGA is configured, after the initial power up sequence. This resets the system along with the PCI Express subsystem allowing the device to be recognized by the system.

Known Restrictions

There are three main components to the Endpoint Block Plus for PCI Express®:

- Virtex®-5 FPGA Integrated Block for PCI Express
- Virtex-5 FPGA RocketIO™ GTP or GTX transceivers
- Block Plus Wrapper FPGA logic

[Table 9-1](#) and [Table 9-2](#) provide an overview of the Virtex-5 FPGA Integrated Block and GTP/GTX transceiver known restrictions when designing for PCI Express. Detailed information on the Integrated Block's known restrictions can be found in the *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide* ([UG197](#)). For Endpoint Block Plus known issues, see the wrapper's current release notes in the *IP Release Notes Guide* ([XTP025](#)). The information in these tables was previously available in the obsolete *Xilinx Solutions Guide for PCI Express* (UG493).

Issues listed in [Table 9-1](#) and [Table 9-2](#) are considered low impact and not a concern for most applications. The “Comments” section for each issue describes where the problem might occur so that designers can decide quickly if further investigation is needed.

[Table 9-3](#) lists the known restrictions fixed in the Endpoint Block Plus for PCI Express.

Table 9-1: Virtex-5 FPGA Integrated Block for PCI Express Known Restrictions

Issue Name	Area of Impact	Descriptions	Comments
Continuous deassertion of LLKTXCONFIGREADYN	Error Handling	Receiving an undefined MsgD with a payload greater than two or receiving a malformed configuration request with format 2'b11 causes the internal configuration block to hang, resulting in continuous deassertion of LLKTXCONFIGREADYN.	By definition of the specification, receiving such illegal or undefined TLPs should result in a fatal error message that in most cases would halt the system. The integrated block does not produce a fatal error message and the block hangs and cause the system to halt. In a normally working system, the block should not receive such TLPs. The occurrence of this condition is rare.
Transmitting Completion TLP with Completer Abort Status	Error Handling	When the User Application sends a completion packet with the Completer Abort status bit set, the integrated block transmits a non-fatal error message that could result in a blue screen on the host.	This exposure exists if the application requires the transmission of a completion with the Completer Abort (CA) bit set. Applications can avoid this issue by not generating a completion packet with the Completer Abort bit set and should instead return a completion with the status of Unsupported Request (UR).
Link Retrain Due to an Absence of Update FC DLLPs	Link Training	When the partner device advertises infinite header and data credits for all packet types for a given virtual channel, the integrated block might not receive any UpdateFC DLLPs. When the integrated block does not receive any UpdateFC DLLPs, it initiates a link retrain because an internal timer used to track the receipt of UpdateFC DLLPs has expired. This behavior is non-compliant.	Advertising initial infinite credits on all three packet types can cause the link to retrain due to an absence of Flow Control DLLP updates. It would be unusual for a link partner to advertise infinite credits for all three traffic types, and no known silicon advertises infinite credits for Posted, Non-Posted and Completion types.
Automatic Transmission of PME_TO_Ack Message	Power Management	The integrated block automatically sends a PME_TO_Ack message in response to a received PME_Turn_Off message instead of allowing the user to control the transmission of the PME_Turn_Off message.	This issue limits the amount of time for internal house keeping before the device is powered off. Most applications do not require any or much house keeping. For applications that do require some housekeeping prior to power down, alternative message mechanisms in higher layer software can be considered.

Table 9-1: Virtex-5 FPGA Integrated Block for PCI Express Known Restrictions (Cont'd)

Issue Name	Area of Impact	Descriptions	Comments
48-packet threshold on posted packets passing non-posted and completion packets in TX direction	TLP Traffic	<p>If non-posted packets and completion packets are stalled inside the integrated block's transmit buffer and more than 48 packets pass a given stalled packet, then the following scenarios can occur:</p> <ul style="list-style-type: none"> Subsequent posted packets might get stalled until the stalled non-posted or completion packet is transmitted. Older non-posted and completion packets could become younger and are incorrectly blocked by a posted packet that arrives later. These non-posted and completion packets are transmitted if all posted packets that were in the transmit buffer when the blocking occurred are eventually transmitted. A nullified TLP can be transmitted. 	In a normal application for PCI Express, it is rare that a non-posted or completion packet would be passed by 48 Posted transactions, because non-posted or completion transactions are usually processed by the same element as the posted transactions (usually a memory controller).
REPLAY_NUM Rollover in LTSSM State TX.L0s	Power Management	<p>If a given packet is replayed several times, it causes REPLAY_NUM to rollover. According to the <i>PCI Express Base Specification v1.1</i>, this should always trigger link training. However, the integrated block does not initiate link training due to REPLAY_NUM rollover if the LTSSM state is TX.L0s. As a result, the integrated block returns to the L0 state instead of the Recovery state, and does not replay any packets. The integrated block remains in this state until link training is initiated.</p>	Active State Power Management (ASPM) is OFF by default in most systems at power-on. If the BIOS or system does not turn on ASPM in the Endpoint device, the system is not affected. If ASPM is enabled, the occurrence of this issue is still rare and would only occur in a faulty link where replays occur.

Table 9-1: Virtex-5 FPGA Integrated Block for PCI Express Known Restrictions (Cont'd)

Issue Name	Area of Impact	Descriptions	Comments
ACK ignored when followed by IDLE ordered set	Power Management	When the host sends an ACK followed by an IDLE ordered set to initiate L0s.Entry, the integrated block never sees the ACK and instead replays the packet. If this scenario repeats multiple times, REPLAY_NUM rolls over, causing the block to initiate link training.	Active State Power Management (ASPM) is OFF by default in most systems at power-on. If the BIOS or system does not turn on ASPM in the downstream peer device, the system is not affected. If ASPM is required, the ACK to the device gets dropped resulting in a TLP replay (due to ACK timeout), which can result in a performance impact and, in worst cases, a link retrain. When the integrated block replays the packet, it should result in another ACK. If the ACK is lost repeatedly, the link goes into RECOVERY and then returns to the L0 state.
Access to unimplemented Configuration Space	Driver/Software	According to <i>PCI Express Base Specification v1.1</i> , an Endpoint should treat access to an unimplemented configuration space as an unsupported request. The integrated block responds with a successful completion that is non-compliant.	System software should not access unimplemented configuration space. Compliant system software accesses the configuration space by walking the capability list.
Receive TLPs with illegal payload length	Handling RX malformed TLPs	According to the <i>PCI Express Base Specification v1.1</i> , any TLP with a payload length that is not a multiple of 1DW is illegal. The integrated block does not send an ERR_FATAL message when it receives a TLP with an illegal payload length. Instead, the block detects this TLP as a bad LCRC and sends back a NAK.	If the downstream port sends a malformed TLP (that does not have a payload that is DWORD aligned), then the block does not generate a fatal error as required. If TLPs with illegal payload lengths are being sent, this is typically an indication of poor link stability or a bad connected device (that is sending malformed TLPs). TLPs with illegal payload lengths are NACKed and replayed by the link partner. If the packet continues to be flawed, multiple NACKs cause the link to go back into link training (which may correct the problem). However, this condition should not occur in a normally operating system and is an indication of larger system problems.

Table 9-1: Virtex-5 FPGA Integrated Block for PCI Express Known Restrictions (Cont'd)

Issue Name	Area of Impact	Descriptions	Comments
Receiving PM_PME_TO_Ack messages	Power Management /Error Handling	According to the <i>PCI Express Base Specification v1.1</i> , an Endpoint should not receive a PM_PME or a PME_TO_Ack message. If it receives such a message, it should respond by sending an ERR_NON_FATAL message. The integrated block does not respond with any error message and silently drops the received messages.	PME_TO_ACK (ACK to a Power Management Event turn off request) messages are ignored and the link continues to operate as normal. It is non-compliant for the link partner to be transmitting these messages to an Endpoint so the occurrence of this is rare.
Loopback slave mode considerations	Loopback Testing	The integrated block supports Loopback Slave mode operation as described in the <i>PCI Express Base Specification v1.1</i> . When the integrated block is operating as a Loopback slave, all data received is looped back to the upstream component. The upstream component can initiate an exit from Loopback by transmitting an Electrical Idle ordered set followed by transitioning the serial lines to Electrical Idle. The integrated block is expected to loopback all data including the Electrical Idle ordered set before transitioning its TX serial line to Electrical Idle. The block does not loopback all data.	User Applications should be aware that when the connected component initiates an exit from Loopback, not all data is returned. Because Loopback is only used for test and verification and is not used during normal link operation, this should have little impact on designs.
Returning to L1 from L0 in D3hot state	Power Management and Disabling Drivers	When an upstream component programs the integrated block to the D3hot power state, the integrated block transitions into an L1 state. While the integrated block is in the D3hot state, if the upstream component sends a TLP, then the block initiates entry into the L0 state in order to process the incoming TLP and send completions, if necessary. After processing the TLP and sending any relevant completions, the integrated block does not return to the L1 state and remains in the L0 state, which is not compliant.	This problem is most notably seen when the device's driver is disabled. Upon doing so, Windows places the device in the D3 hot state. While in D3 hot, if a TLP is received by the Endpoint, it transitions back to L0 to process the TLP and then remain in L0 instead of returning to L1. This does not result in loss of data and eventually the software transitions the device back to D0 and normal link operations return.

Table 9-1: Virtex-5 FPGA Integrated Block for PCI Express Known Restrictions (Cont'd)

Issue Name	Area of Impact	Descriptions	Comments												
Receipt of ignored messages	Message TLPs	When an ignored message is received, the integrated block does not perform any action on it and the message is passed to the user logic.	"Ignored Messages" used in <i>PCI Express Base Specification v1.0a</i> are no longer supported. Receiving these messages is rare. The core passes these messages, which can be dropped by the User Application.												
Link partner initial advertisement of Data Limited Completion Credits	TLP Traffic	Advertisement of initial credits with Data Limited Completion Credits by a connected upstream component can cause the core to lock up and stall transmission of TLPs due to lack of data credits.	This issue is seen only in systems where the connected component makes an initial advertisement of Data Limited Completion Credits. Data Limited Completion Credits can be determined by the following equation: $\text{Initial CPLD credits} < \text{Initial CPLH} * 8 * 2^X$, where X is: <table style="margin-left: 40px;"> <tr><td>MPS</td><td> </td><td>X</td></tr> <tr><td>128</td><td> </td><td>0</td></tr> <tr><td>256</td><td> </td><td>1</td></tr> <tr><td>512</td><td> </td><td>2</td></tr> </table> For example, if the link partner advertises initial CPLH credits as 22 and the initial CPLD credits as 128, for an MPS of 128 then: $128 < 22 * 8 * 1$ $128 < 176$ If the equation evaluates to TRUE, the restriction is hit. Users should consult the link partner's data sheet for information on initial credit advertisement. Most link partners advertise infinite completion data credits. Users can work around this limitation by restricting Downstream Reads to 1 or 2 DW, which must be completed with exactly one completion. Note: 2 DW Read Requests to 1 DW below integer multiples of Read Completion Boundary (RCB) can result in multiple completions, violating this restriction.	MPS		X	128		0	256		1	512		2
MPS		X													
128		0													
256		1													
512		2													

Table 9-2 describes known restrictions due to the GTP (Virtex-5 SXT, LXT families) or GTX (Virtex-5 FXT family) transceivers that impact PCI Express.

Table 9-2: Virtex-5 FPGA GTP/GTX Transceiver Known Restrictions Impacting PCI Express

Issue Name	Area of Impact	Description	Comments	GTP ¹ , GTX ² or Both
Transceiver Exit from Rx.L0s	Power Management	<p>When the GTP transceiver exits from Rx.L0s, up to eight symbol times of valid data following the SKP symbol in the FTS-FTS-COM-SKP channel bonding sequence will be ignored by the block. This is a result of a delay in the assertion of the RXCHANISALIGNED signal from the GTP. If the packets are replayed by the upstream port and correctly ACKed by the integrated block, the link stays up. However, there is a chance that if the original missed data was an ACK, the upstream component sends the ACK, goes back to L0s, wakes up to send the ACK, and then returns to L0s. If this repeats continuously, it eventually triggers a link retrain. However, no data is lost and the link eventually recovers, causing minimal to no impact on safe operation.</p>	This issue would only arise if Active State Power Management is in use. Active State Power Management (ASPM) is OFF by default in most systems at power-on. If the BIOS or system does not turn on ASPM in the Endpoint device, the system is not affected.	Both
TX Path Entering L0s and Packet Received	Power Management	<p>When the TX path of the core is entering L0s and a packet is transmitted by the link partner, the transition back to L0 to send an ACK is very long. This causes the link partner to replay the packet. It results in two ACKs sent by the core (one for the original packet and one for the replayed packet). This is due to the time it takes for the GTP transceiver to return to L0 from L0s. This action is still compliant to the specification as two ACKs for the same packet can be legally sent.</p> <p>This could cause a minor impact on performance.</p>	This issue would only arise if Active State Power Management is in use. Active State Power Management (ASPM) is OFF by default in most systems at power-on. If the BIOS or system does not turn on ASPM in the Endpoint device, the system is not affected.	Both

Table 9-2: Virtex-5 FPGA GTP/GTX Transceiver Known Restrictions Impacting PCI Express (Cont'd)

Issue Name	Area of Impact	Description	Comments	GTP ¹ , GTX ² or Both
Reporting 8B/10B Error	Link Traffic	The GTP transceiver is required to signal an 8B/10B error by setting RXSTATUS[2:0] to 3'b100, RXDATA[7:0] to 8'hFE and RXCHARISK to 1. The transceiver correctly sets RXSTATUS, but does not indicate the correct values on RXDATA and RXCHARISK. As a result, an 8B/10B error manifests itself as an LCRC error and the integrated block transmits a NAK DLLP. This does not cause any fatal errors, but results in a non-compliant response. The link partner should resend the packet in response to the NAK. If the 8B/10B error continues to occur, the link retrains.	In most functioning systems, 8B/10B errors are rare. Although they might occur, since they manifest to the integrated block as an LCRC failure, it NAKs the packet which results in the link partner resending the packet. This might have a slight impact on performance, but since the occurrence is rare, there have been no reported concerns due to this issue.	GTP only
Simulating GTP Reset	Simulation	In simulation when the GTP transceiver is in reset, the TX outputs are held to the last logic value driven instead of driving both TXp and TXn to either 1 or 0. This might cause the link partner model to incorrectly interpret the behavior and see it as potential START of packet	This has been reported using the Denali BFM and it causes the Denali model to report errors as it interprets these values as potential START of packet. To work around this issue, turn off the Denali error reporting when the GTP/GTX transceiver is in reset. Although this has been reported only by customers using the Denali BFM, it could affect other BFMs as well.	Both
Receive Path L0s Exit to L0	Power Management	When the link partner transmitter transitions from L0s to L0, the integrated Endpoint might experience an nFTS timeout, causing a transition to recovery. During recovery, the requisite number of training sets are not received from the GTP transceiver causing link training to start over in Detect.	This issue only arises if Active State Power Management is in use. Active State Power Management (ASPM) is OFF by default in most systems at power-on. If the BIOS or system does not turn on ASPM in the Endpoint device, the system is not affected.	GTP only

1. For Virtex-5 LXT and SXT devices.
2. For Virtex-5 FXT devices.

Table 9-3 lists the known restrictions referred to in the *Virtex-5 FPGA Integrated Endpoint Block for PCI Express Designs User Guide* ([UG197](#)) and three GTP/GTX transceiver issues that are fixed in the Endpoint Block for PCI Express.

Table 9-3: Fixed Known Restrictions

Issue Name	Version Fixed ¹
Issues from UG197 (Integrated Block Known Restrictions)	
TX Transmission Issues Due to Lack of Data Credits	v1.6.1
64-Packet Threshold for Completion Streaming on RX Interface	v1.3
Reset Considerations in LTSSM Polling State	v1.3
Invalid Cycles in LLKRXPREFERREDTYPE Signal	v1.3
Receipt of Unsupported Configuration Requests and Poisoned	v1.3
Receipt of back-to-back ACK DLLPs	v1.8
GTP/GTX Transceiver Known Restrictions	
Channel Bonding on Exit from L0s (footnote 1)	v1.3
Electrical Idle response to TXELECIDLE in the absence of clocks	v1.3
GTP/GTX transceiver driving 'X' during electrical idle.	ISE v10.1 SP3

1. Version Fixed shows the version of the Endpoint Block Plus core in which the issue was fixed, except for the last entry which was fixed in the general ISE® software release.

Programmed Input Output Example Design

Programmed Input Output (PIO) transactions are generally used by a PCI Express® system host CPU to access Memory Mapped Input Output (MMIO) and Configuration Mapped Input Output (CMIO) locations in the PCI Express fabric. Endpoints for PCI Express accept Memory and I/O Write transactions and respond to Memory and I/O Read transactions with Completion with Data transactions.

The PIO example design (PIO design) is included with the Endpoint for PCIe® generated by the CORE Generator™ tool, which allows a user to easily bring up their system board with a known established working design to verify the link and functionality of the board.

Note: The PIO design Port Model is shared by the Endpoint for PCI Express, Endpoint Block Plus for PCI Express, and Endpoint PIPE for PCI Express solutions. This appendix represents all the solutions generically using the name Endpoint for PCI Express (or Endpoint for PCIe).

System Overview

The PIO design is a simple target-only application that interfaces with the Endpoint for PCIe core's Transaction (TRN) interface and is provided as a starting point for customers to build their own designs. These features are included:

- Four transaction-specific 2 kB target regions using the internal Xilinx® FPGA block RAMs, providing a total target space of 8192 bytes
- Supports single DWORD payload Read and Write PCI Express transactions to 32-/64-bit address memory spaces and I/O space with support for completion TLPs
- Utilizes the core's `trn_rbar_hit_n[6:0]` signals to differentiate between TLP destination Base Address Registers
- Provides separate implementations optimized for 32-bit and 64-bit TRN interfaces

Figure A-1 illustrates the PCI Express system architecture components, consisting of a Root Complex, a PCI Express switch device, and an Endpoint for PCIe. PIO operations move data *downstream* from the Root Complex (CPU register) to the Endpoint, and/or *upstream* from the Endpoint to the Root Complex (CPU register). In either case, the PCI Express protocol request to move the data is initiated by the host CPU.

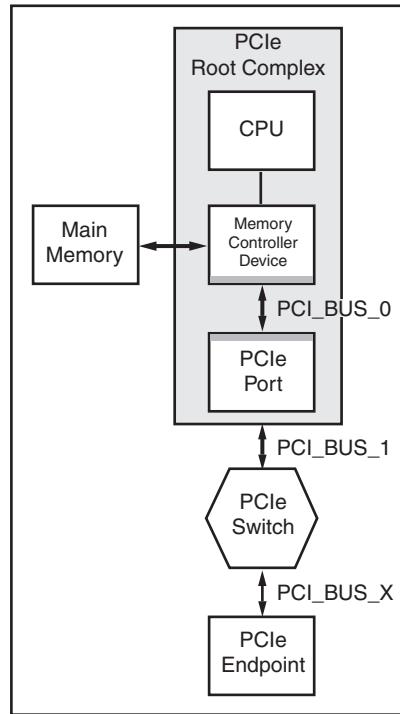


Figure A-1: System Overview

Data is moved downstream when the CPU issues a store register to a MMIO address command. The Root Complex typically generates a Memory Write TLP with the appropriate MMIO location address, byte enables and the register contents. The transaction terminates when the Endpoint receives the Memory Write TLP and updates the corresponding local register.

Data is moved upstream when the CPU issues a load register from a MMIO address command. The Root Complex typically generates a Memory Read TLP with the appropriate MMIO location address and byte enables. The Endpoint generates a Completion with Data TLP once it receives the Memory Read TLP. The Completion is steered to the Root Complex and payload is loaded into the target register, completing the transaction.

PIO Hardware

The PIO design implements a 8192 byte target space in FPGA block RAM, behind the Endpoint for PCIe. This 32-bit target space is accessible through single DWORD I/O Read, I/O Write, Memory Read 64, Memory Write 64, Memory Read 32, and Memory Write 32 TLPs.

The PIO design generates a completion with 1 DWORD of payload in response to a valid Memory Read 32 TLP, Memory Read 64 TLP, or I/O Read TLP request presented to it by the core. In addition, the PIO design returns a completion without data with successful status for I/O Write TLP request.

The PIO design processes a Memory or I/O Write TLP with 1 DWORD payload by updating the payload into the target address in the FPGA block RAM space.

Base Address Register Support

The PIO design supports four discrete target spaces, each consisting of a 2 kB block of memory represented by a separate Base Address Register (BAR). Using the default parameters, the CORE Generator tool produces a core configured to work with the PIO design defined in this section, consisting of the following:

- One 64-bit addressable Memory Space BAR
- One 32-bit Addressable Memory Space BAR

Users can change the default parameters used by the PIO design; however, in some cases they might need to change the back-end user application depending on their system. See [Changing CORE Generator Tool Default BAR Settings](#) for information about changing the default CORE Generator tool parameters and the effect on the PIO design.

Each of the four 2 kB address spaces represented by the BARs corresponds to one of four 2 kB address regions in the PIO design. Each 2 kB region is implemented using a 2 kB dual-port block RAM. As transactions are received by the core, the core decodes the address and determines which of the four regions is being targeted. The core presents the TLP to the PIO design and asserts the appropriate bits of `trn_rbar_hit_n[6:0]`, as defined in [Table A-1](#).

Note: Because the endpoint_blk_plus core does not support Expansion ROM TLP accesses, the PIO design's block RAM dedicated for EROM TLP transactions is disabled.

Table A-1: TLP Traffic Types

Block RAM	TLP Transaction Type	Default BAR	<code>trn_rbar_hit_n[6:0]</code>
ep_mem0	I/O TLP transactions	Disabled	Disabled
ep_mem1	32-bit address Memory TLP transactions	2	111_1011b
ep_mem2	64-bit address Memory TLP transactions	0-1	111_1100b
ep_mem3	Disabled	Disabled	Disabled

Changing CORE Generator Tool Default BAR Settings

Users can change the CORE Generator tool parameters and continue to use the PIO design to create customized Verilog or VHDL source to match the selected BAR settings.

However, because the PIO design parameters are more limited than the core parameters, consider the following example design limitations when changing the default CORE Generator tool parameters:

- The example design supports one I/O space BAR, one 32-bit Memory space (that cannot be the Expansion ROM space), and one 64-bit Memory space. If these limits are exceeded, only the first space of a given type is active—accesses to the other spaces do not result in completions.
- Each space is implemented with a 2 kB memory. If the corresponding BAR is configured to a wider aperture, accesses beyond the 2 kB limit wrap around and overlap the 2 kB memory space.
- The PIO design supports one I/O space BAR, which by default is disabled, but can be changed if desired.

Although there are limitations to the PIO design, Verilog or VHDL source code is provided so users can tailor the example design to their specific needs.

TLP Data Flow

This section defines the data flow of a TLP successfully processed by the PIO design. For detailed information about the interface signals within the sub-blocks of the PIO design, see [Receive Path, page 174](#) and [Transmit Path, page 176](#).

The PIO design successfully processes single DWORD payload Memory Read and Write TLPs and I/O Read and Write TLPs. Memory Read or Memory Write TLPs of lengths larger than one DWORD are not processed correctly by the PIO design; however, the core *does* accept these TLPs and passes them along to the PIO design. If the PIO design receives a TLP with a length of greater than 1 DWORD, the TLP is received completely from the core and discarded. No corresponding completion is generated.

Memory and I/O Write TLP Processing

When the Endpoint for PCIe receives a Memory or I/O Write TLP, the TLP destination address and transaction type are compared with the values in the core BARs. If the TLP passes this comparison check, the core passes the TLP to the Receive TRN interface of the PIO design. The PIO design handles Memory writes and I/O TLP writes in different ways: the PIO design responds to *I/O writes* by generating a Completion Without Data (cpl), a requirement of the PCI Express specification.

Along with the start of packet, end of packet, and ready handshaking signals, the Receive TRN interface also asserts the appropriate `trn_rbar_hit_n[6:0]` signal to indicate to the PIO design the specific destination BAR that matched the incoming TLP. On reception, the PIO design's RX State Machine processes the incoming Write TLP and extracts the TLPs data and relevant address fields so that it can pass this along to the PIO design's internal block RAM write request controller.

Based on the specific `trn_rbar_hit_n[6:0]` signal asserted, the RX State Machine indicates to the internal write controller the appropriate 2 kB block RAM to use prior to asserting the write enable request. For example, if an I/O Write Request is received by the core targeting BAR0, the core passes the TLP to the PIO design and asserts `trn_rbar_hit_n[0]`. The RX State machine extracts the lower address bits and the data field from the I/O Write TLP and instructs the internal Memory Write controller to begin a write to the block RAM.

In this example, the assertion of `trn_rbar_hit_n[0]` instructed the PIO memory write controller to access `ep_mem0` (which by default represents 2 kB of I/O space). While the write is being carried out to the FPGA block RAM, the PIO design RX state machine deasserts the `trn_rd_st_rdy_n` signal, causing the Receive TRN interface to stall receiving any further TLPs until the internal Memory Write controller completes the write to the block RAM. Deasserting `trn_rd_st_rdy_n` in this way is not required for all designs using the core—the PIO design uses this method to simplify the control logic of the RX state machine.

Memory and I/O Read TLP Processing

When the Endpoint for PCIe receives a Memory or I/O Read TLP, the TLP destination address and transaction type are compared with the values programmed in the core BARs. If the TLP passes this comparison check, the core passes the TLP to the Receive TRN interface of the PIO design.

Along with the start of packet, end of packet, and ready handshaking signals, the Receive TRN interface also asserts the appropriate `trn_rbar_hit_n[6:0]` signal to indicate to the PIO design the specific destination BAR that matched the incoming TLP. On reception, the PIO design's state machine processes the incoming Read TLP and extracts the relevant TLP

information and passes it along to the PIO design's internal block RAM read request controller.

Based on the specific `trn_rbar_hit_n[6:0]` signal asserted, the RX state machine indicates to the internal read request controller the appropriate 2 KB block RAM to use before asserting the read enable request. For example, if a Memory Read 32 Request TLP is received by the core targeting the default MEM32 BAR2, the core passes the TLP to the PIO design and asserts `trn_rbar_hit_n[2]`. The RX State machine extracts the lower address bits from the Memory 32 Read TLP and instructs the internal Memory Read Request controller to start a read operation.

In this example, the assertion of `trn_rbar_hit_n[2]` instructs the PIO memory read controller to access the Mem32 space, which by default represents 2 KB of memory space. A notable difference in handling of memory write and read TLPs is the requirement of the receiving device to return a Completion with Data TLP in the case of memory or I/O read request.

While the read is being processed, the PIO design RX state machine deasserts `trn_rdst_rdy_n`, causing the Receive TRN interface to stall receiving any further TLPs until the internal Memory Read controller completes the read access from the block RAM and generates the completion. Deasserting `trn_rst_rdy_n` in this way is not required for all designs using the core. The PIO design uses this method to simplify the control logic of the RX state machine.

PIO File Structure

[Table A-2](#) defines the PIO design file structure. Based on the specific core targeted, not all files delivered by the CORE Generator tool are necessary, and some files might not be delivered. The major difference is that some of the Endpoint for PCIe solutions use a 32-bit user datapath, others use a 64-bit datapath, and the PIO design works with both. The width of the datapath depends on the specific core being targeted.

Table A-2: PIO Design File Structure

File	Description
PIO.[v vhd]	Top-level design wrapper
PIO_EP.[v vhd]	PIO application module
PIO_TO_CTRL.[v vhd]	PIO turn-off controller module
PIO_32_RX_ENGINE.[v vhd]	32b Receive engine
PIO_32_TX_ENGINE.[v vhd]	32b Transmit engine
PIO_64_RX_ENGINE.[v vhd]	64b Receive engine
PIO_64_TX_ENGINE.[v vhd]	64b Transmit engine
PIO_EP_MEM_ACCESS.[v vhd]	Endpoint memory access module
EP_MEM.[v vhd]	Endpoint memory

Two configurations of the PIO Design are provided: PIO_32 and PIO_64, with 32- and 64-bit TRN interfaces, respectively. The PIO configuration generated depends on the selected Endpoint type (that is, PIPE, PCI Express, and Block Plus) as well as the number of

PCI Express lanes selected by the user. [Table A-3](#) identifies the PIO configuration generated based on the user's selection.

Table A-3: PIO Configuration

Core	x1	x2	x4	x8
Endpoint for PIPE	PIO_32	NA	NA	NA
Endpoint for PCI Express	PIO_32, PIO_64 ¹	NA	PIO_32, PIO_64 ¹	PIO_64
Endpoint for PCI Express Block Plus	PIO_64	PIO_64	PIO_64	PIO_64

1. The PIO Interface Width matches the core interface width. The Endpoint for PCI Express core is 32 bits by default for x1 and x4 cores, but the core is also available in a 64-bit version, which uses PIO_64.

[Figure A-2](#) shows the various components of the PIO design, which is separated into four main parts: the TX Engine, RX Engine, Memory Access Controller, and Power Management Turn-Off Controller.

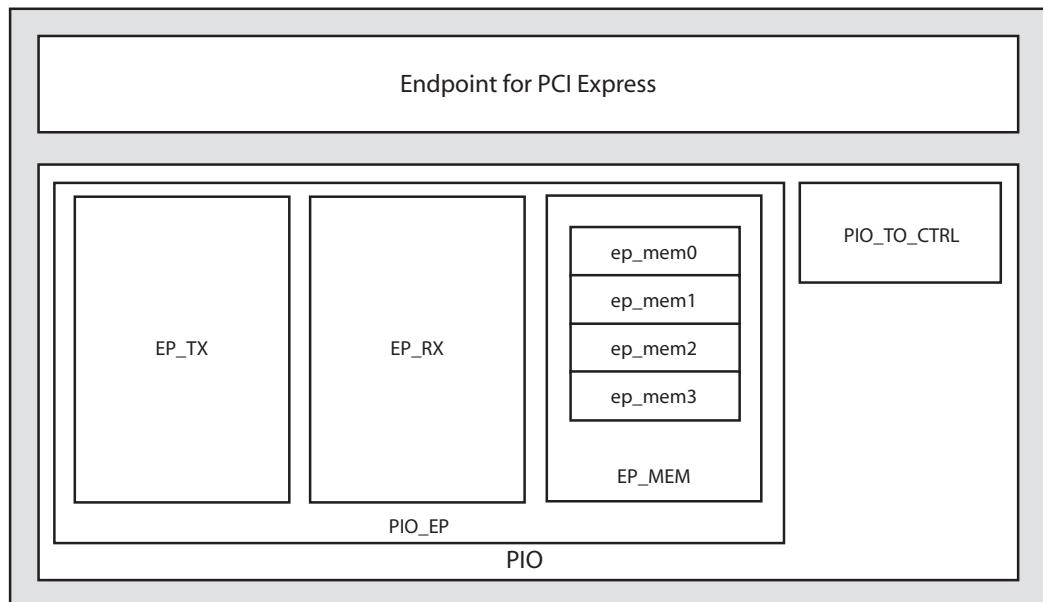


Figure A-2: PIO Design Components

PIO Application

[Figure A-3](#) and [Figure A-4](#) depict 64-bit and 32-bit PIO application top-level connectivity, respectively. The datapath width, either 32 bits or 64 bits, depends on which Endpoint for PCIe core is used. The PIO_EP module contains the PIO FPGA block RAM memory modules and the transmit and receive engines. The PIO_TO_CTRL module is the Endpoint Turn-Off controller unit, which responds to power turn-off message from the host CPU with an acknowledgement.

The PIO_EP module connects to the Endpoint Transaction (trn) and Configuration (cfg) interfaces.

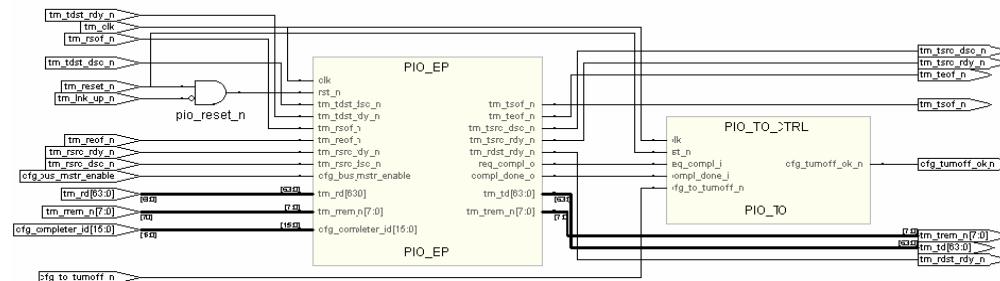


Figure A-3: PIO 64-Bit Application

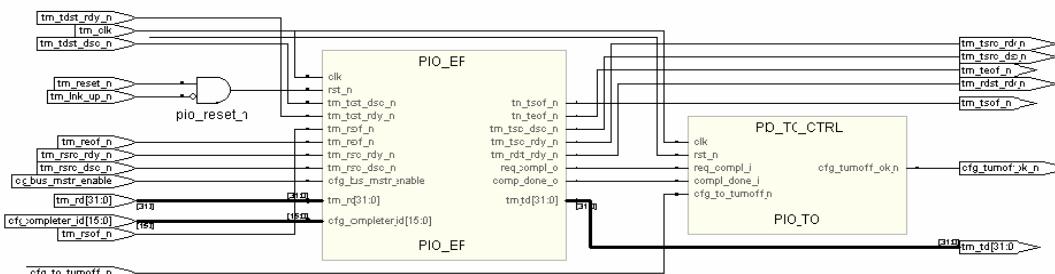


Figure A-4: PIO 32-Bit Application

Receive Path

[Figure A-5](#) illustrates the PIO_32_RX_ENGINE and PIO_64_RX_ENGINE modules. The datapath of the module must match the datapath of the core being used. These modules connect with Endpoint for PCIe Transaction Receive (trn_r*) interface.

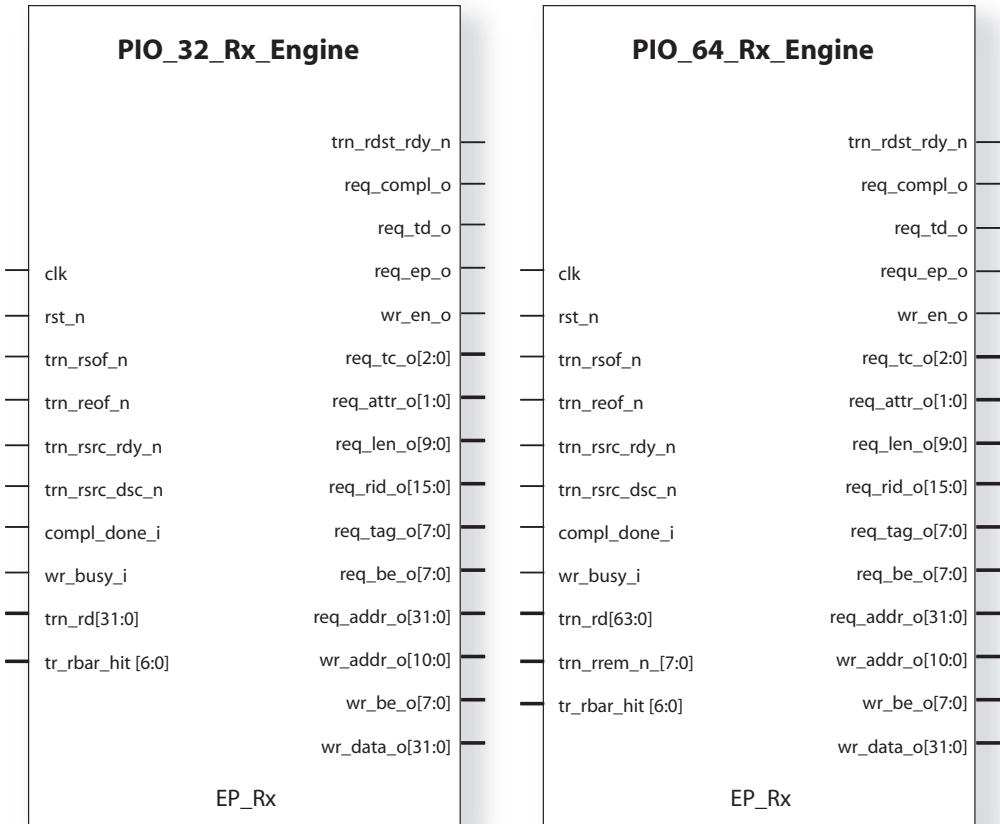


Figure A-5: Rx Engines

The PIO_32_RX_ENGINE and PIO_64_RX_ENGINE modules receive and parse incoming read and write TLPs.

The RX engine parses 1 DWORD 32- and 64-bit addressable memory and I/O read requests. The RX state machine extracts needed information from the TLP and passes it to the memory controller, as defined in [Table A-4](#).

Table A-4: Rx Engine: Read Outputs

Port	Description
req_compl_o	Completion request (active high)
req_td_o	Request TLP Digest bit
req_ep_o	Request Error Poisoning bit
req_tc_o[2:0]	Request Traffic Class
req_attr_o[1:0]	Request Attributes

Table A-4: Rx Engine: Read Outputs (Cont'd)

Port	Description
req_len_o[9:0]	Request Length
req_rid_o[15:0]	Request Requester Identifier
req_tag_o[7:0]	Request Tag
req_be_o[7:0]	Request Byte Enable
req_addr_o[10:0]	Request Address

The RX Engine parses 1 DWORD 32- and 64-bit addressable memory and I/O write requests. The RX state machine extracts needed information from the TLP and passes it to the memory controller, as defined in [Table A-5](#).

Table A-5: Rx Engine: Write Outputs

Port	Description
wr_en_o	Write received
wr_addr_o[10:0]	Write address
wr_be_o[7:0]	Write byte enable
wr_data_o[31:0]	Write data

The read datapath stops accepting new transactions from the core while the application is processing the current TLP. This is accomplished by `trn_rdst_rdy_n` deassertion. For an ongoing Memory or I/O Read transaction, the module waits for `compl_done_i` input to be asserted before it accepts the next TLP, while an ongoing Memory or I/O Write transaction is deemed complete after `wr_busy_i` is deasserted.

Transmit Path

Figure A-6 shows the PIO_32_TX_ENGINE and PIO_64_TX_ENGINE modules. The datapath of the module must match the datapath of the core being used. These modules connect with the core Transaction Transmit (trn_r*) interface.

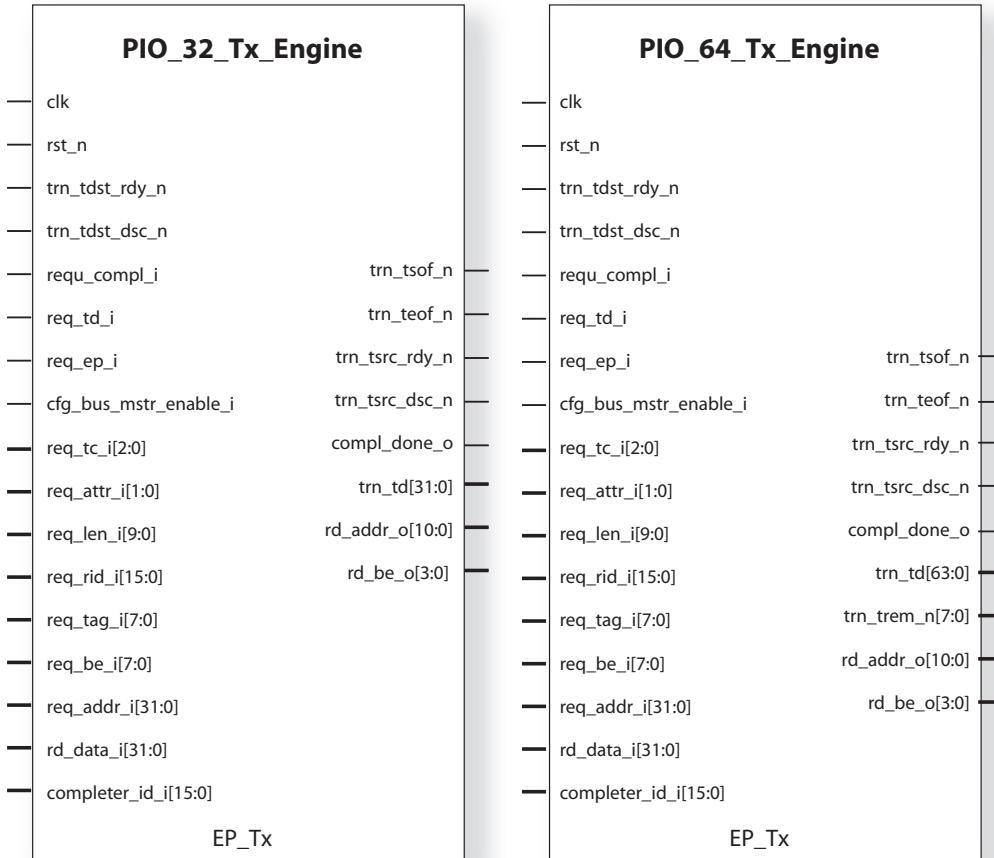


Figure A-6: Tx Engines

The PIO_32_TX_ENGINE and PIO_64_TX_ENGINE modules generate completions for received memory and I/O read TLPs. The PIO design does not generate outbound read or write requests. However, users can add this functionality to further customize the design.

The PIO_32_TX_ENGINE and PIO_64_TX_ENGINE modules generate completions in response to 1 DWORD 32- and 64-bit addressable memory and I/O read requests.

Information necessary to generate the completion is passed to the TX Engine, as defined in Table A-6.

Table A-6: Tx Engine Inputs

Port	Description
req_compl_i	Completion request (active high)
req_td_i	Request TLP Digest bit
req_ep_i	Request Error Poisoning bit

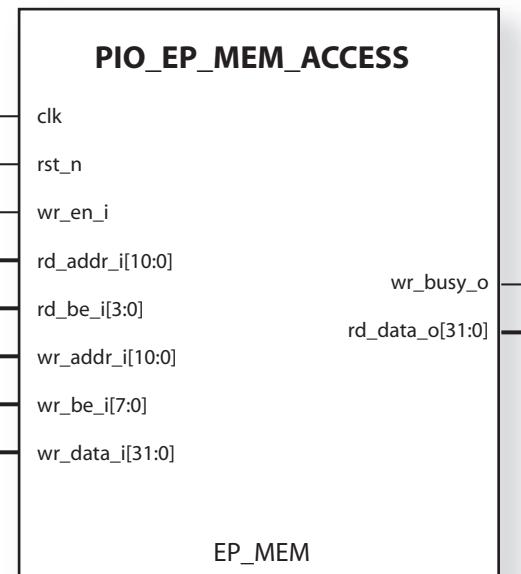
Table A-6: Tx Engine Inputs (Cont'd)

Port	Description
req_tc_i[2:0]	Request Traffic Class
req_attr_i[1:0]	Request Attributes
req_len_i[9:0]	Request Length
req_rid_i[15:0]	Request Requester Identifier
req_tag_i[7:0]	Request Tag
req_be_i[7:0]	Request Byte Enable
req_addr_i[10:0]	Request Address

After the completion is sent, the TX engine asserts the `compl_done_i` output indicating to the RX engine that it can assert `trn_rdst_rdy_n` and continue receiving TLPs.

Endpoint Memory

Figure A-7 displays the PIO_EP_MEM_ACCESS module. This module contains the Endpoint memory space.

**Figure A-7: EP Memory Access**

The PIO_EP_MEM_ACCESS module processes data written to the memory from incoming Memory and I/O Write TLPs and provides data read from the memory in response to Memory and I/O Read TLPs.

The EP_MEM module processes 1 DWORD 32- and 64-bit addressable Memory and I/O Write requests based on the information received from the RX Engine, as defined in

Table A-7. While the memory controller is processing the write, it asserts the `wr_busy_o` output indicating it is busy.

Table A-7: EP Memory: Write Inputs

Port	Description
<code>wr_en_i</code>	Write received
<code>wr_addr_i[10:0]</code>	Write address
<code>wr_be_i[7:0]</code>	Write byte enable
<code>wr_data_i[31:0]</code>	Write data

Both 32 and 64-bit Memory and I/O Read requests of one DWORD are processed based on the following inputs, as defined in **Table A-8**. After the read request is processed, the data is returned on `rd_data_o[31:0]`.

Table A-8: EP Memory: Read Inputs

Port	Description
<code>req_be_i[7:0]</code>	Request Byte Enable
<code>req_addr_i[31:0]</code>	Request Address

PIO Operation

PIO Read Transaction

Figure A-8 depicts a Back-to-Back Memory Read request to the PIO design. The receive engine deasserts `trn_rdst_rdy_n` as soon as the first TLP is completely received. The next Read transaction is accepted only after `compl_done_o` is asserted by the transmit engine, indicating that Completion for the first request was successfully transmitted.

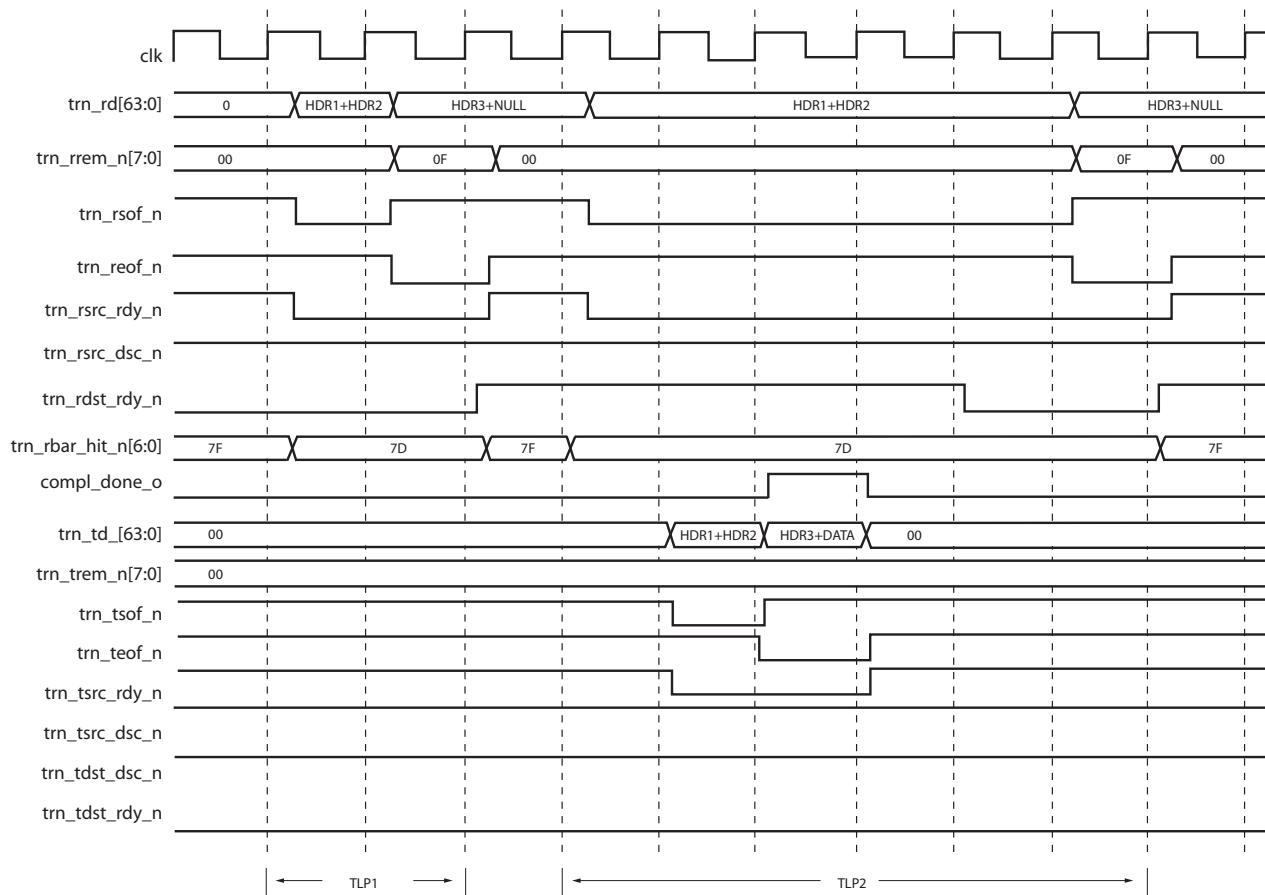


Figure A-8: Back-to-Back Read Transactions

PIO Write Transaction

[Figure A-9](#) depicts a back-to-back Memory Write to the PIO design. The next Write transaction is accepted only after `wr_busy_o` is deasserted by the memory access unit, indicating that data associated with the first request was successfully written to the memory aperture.

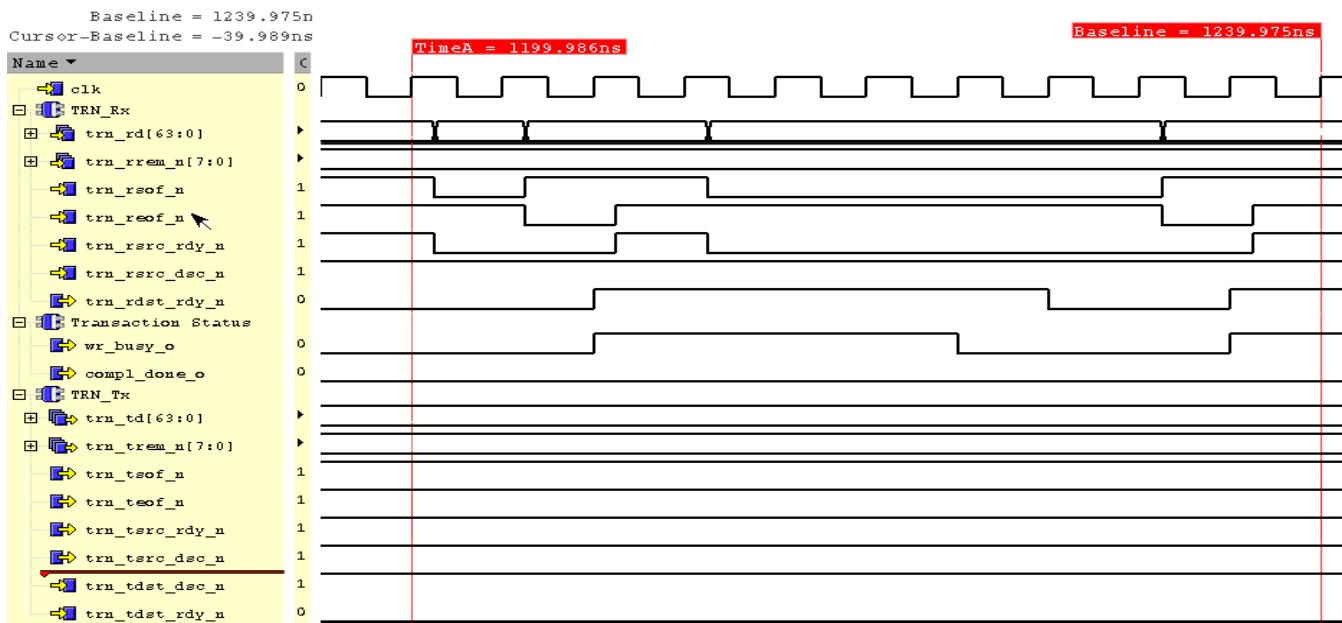


Figure A-9: Back-to-Back Write Transactions

Device Utilization

[Table A-9](#) shows the PIO design FPGA resource utilization.

Table A-9: PIO Design FPGA Resources

Resources	Utilization
LUTs	300
Flip-Flops	500
Block RAMs	4

Summary

The PIO design demonstrates the Endpoint for PCIe and its interface capabilities. In addition, it enables rapid bring-up and basic validation of end user Endpoint add-in card FPGA hardware on PCI Express platforms. Users can leverage standard operating system utilities that enable generation of read and write transactions to the target space in the reference design.

Root Port Model Test Bench

The Root Port Model for the Endpoint for PCI Express® is a robust test bench environment that provides a test program interface that can be used with the provided PIO design or with one's own design. The purpose of the Root Port Model is to provide a source mechanism for generating downstream PCI Express TLP traffic to stimulate the customer design, and a destination mechanism for receiving upstream PCI Express TLP traffic from the customer design in a simulation environment.

Note: The Root Port Model is shared by the Endpoint for PCI Express, Endpoint Block Plus for PCI Express, and Endpoint PIPE for PCI Express solutions. This appendix represents all the solutions generically using the name Endpoint for PCI Express or Endpoint (or Endpoint for PCle®).

Source code for the Root Port Model is included to provide the model for a starting point for your test bench. All the significant work for initializing the core's configuration space, creating TLP transactions, generating TLP logs, and providing an interface for creating and verifying tests are complete, allowing you to dedicate your efforts to verifying the correct functionality of the design rather than spending time developing an Endpoint core test bench infrastructure.

The Root Port Model consists of:

- Test Programming Interface (TPI), which allows the user to stimulate the Endpoint device for the PCI Express
- Example tests that illustrate how to use the test program TPI
- Verilog source code for all Root Port Model components, which allow the user to customize the test bench

Figure B-1 illustrates the Root Port Model coupled with the PIO design.

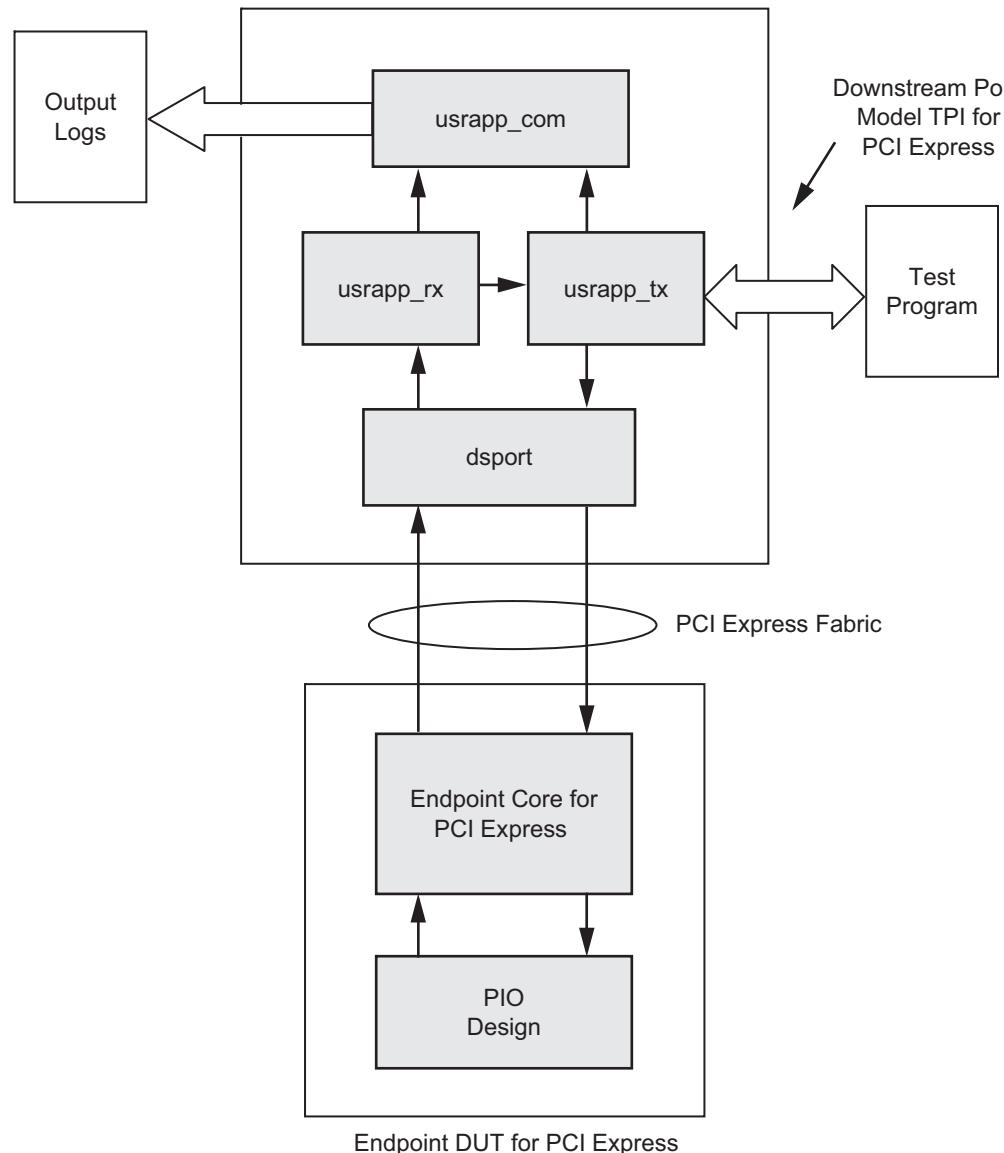


Figure B-1: Root Port Model and Top-Level Endpoint

Architecture

The Root Port Model consists of these blocks, illustrated in Figure B-1.

- **dsport** (downstream port)
- **usrapp_tx**
- **usrapp_rx**
- **usrapp_com** (Verilog only)

The **usrapp_tx** and **usrapp_rx** blocks interface with the **dsport** block for transmission and reception of TLPs to/from the Endpoint Design Under Test (DUT). The Endpoint DUT consists of the Endpoint for PCIe and the PIO design (displayed) or customer design.

The `usrapp_tx` block sends TLPs to the `dsport` block for transmission across the PCI Express Link to the Endpoint DUT. In turn, the Endpoint DUT device transmits TLPs across the PCI Express Link to the `dsport` block, which are subsequently passed to the `usrapp_rx` block. The `dsport` and core are responsible for the data link layer and physical link layer processing when communicating across the PCI Express fabric. Both the `usrapp_tx` and `usrapp_rx` utilize the `usrapp_com` block for shared functions, for example, TLP processing and log file outputting. Transaction sequences or test programs are initiated by the `usrapp_tx` block to stimulate the Endpoint device's fabric interface. TLP responses from the Endpoint device are received by the `usrapp_rx` block. Communication between the `usrapp_tx` and `usrapp_rx` blocks allow the `usrapp_tx` block to verify correct behavior and act accordingly when the `usrapp_rx` block has received TLPs from the Endpoint device.

The Root Port Model has a 128-byte MPS capability in the receive direction and a 512-byte MPS capability in the transmit direction.

Simulating the Design

Three simulation script files are provided with the model to facilitate simulation with Synopsys VCS, Cadence Incisive Enterprise Simulator (IES), and Mentor Graphics ModelSim simulators:

- `simulate_vcs.sh` (Verilog only)
- `simulate_ncsim.sh`
- `simulate_mti.do`

The example simulation script files are located in this directory:

```
<project_dir>/<component_name>/simulation/functional
```

Instructions for simulating the PIO design using the Root Port Model are provided in [Appendix A, Programmed Input Output Example Design](#).

Note: For VHDL users using the IES flow, the environment variable LMC_TIMEUNIT must be set to -12, which sets the timing resolution to 1 ps (required for the LogiCORE™ IP PCI Express simulation SmartModel to operate correctly).

For Linux, use this command line:

```
> setenv LMC_TIMEUNIT -12
```

Note: For IES users, the work construct must be manually inserted into your CDS.LIB file:

```
DEFINE WORK WORK
```

Scaled Simulation Timeouts

The simulation model of the Virtex®-5 FPGA Integrated Block for PCI Express uses scaled down timers during link training to allow for the link to train in a reasonable amount of time during simulation. According to the *PCI Express Specification*, there are various timeouts associated with the link training and status state machine (LTSSM) states. In simulation, the values of these timers are shown in [Table B-1](#).

Table B-1: Timer Simulation Values

Timer	Simulation Value
Number of TS1/TS2 transmitted in Polling	16 µs
Configuration LaneNum Wait (Downstream)	15. 63 µs

Table B-1: Timer Simulation Values

Timer	Simulation Value
Configuration LaneNum Wait (Upstream)	15.63 µs
Configuration LaneNum Accept	15.63 µs
Timeout Polling Configuration	375 µs
Timeout Polling Active	46.88 µs
Timeout Detect Quiet	5.86 µs
Timeout Detect Active	11.72 µs
Timeout Configuration LinkWidth Start	46.88 µs
Timeout Configuration Complete	46.88 µs
Timeout Configuration LinkWidth Accept	15.63 µs
Timeout Configuration Idle	15.63 µs
Timeout Recovery RcvrCfg	15.63 µs
Timeout Recovery RcvrLock	15.63 µs
Timeout Recovery Receiver Idle	15.63 µs
Timeout Disabled Idle	93.75 µs
Timeout Hot Reset Master Wait	46.88 µs
Timeout Hot Reset Slave Wait	15.63 µs
Timeout Loopback Entry	15.63 µs
Timeout Loopback Exit Idle	15.63 µs

Test Selection

Table B-2 describes the tests provided with the Root Port Model, followed by specific sections for VHDL and Verilog test selection.

Table B-2: Root Port Model Provided Tests

Test Name	Test in VHDL and Verilog	Description
sample_smoke_test0	Verilog and VHDL	Issues a PCI Type 0 Configuration Read TLP and waits for the completion TLP; then compares the value returned with the expected Device/Vendor ID value.
sample_smoke_test1	Verilog	Performs the same operation as sample_smoke_test0 but makes use of expectation tasks. This test uses two separate test program threads: one thread issues the PCI Type 0 Configuration Read TLP and the second thread issues the Completion with Data TLP expectation task. This test illustrates the form for a parallel test that uses expectation tasks. This test form allows for confirming reception of any TLPs from the customer's design. Additionally, this method can be used to confirm reception of TLPs when ordering is unimportant.
pio_writeReadBack_test0	Verilog and VHDL	Transmits a 1 DWORD Write TLP followed by a 1 DWORD Read TLP to each of the example design's active BARs, and then waits for the Completion TLP and verifies that the write and read data match. The test sends the appropriate TLP to each BAR based on the BARs address type (for example, 32 bit or 64 bit) and space type (for example, I/O or Memory).
pio_testByteEnables_test0	Verilog	Issues four sequential Write TLPs enabling a unique byte enable for each Write TLP, and then issues a 1 DWORD Read TLP to confirm that the data was correctly written to the example design. The test sends the appropriate TLP to each BAR based on the BARs address-type (for example, 32 bit or 64 bit) and space type (for example, I/O or Memory).
pio_memTestDataBus	Verilog	Determines if the PIO design's FPGA block RAMs data bus interface is correctly connected by performing a 32-bit walking ones data test to the first available BAR in the example design.

Table B-2: Root Port Model Provided Tests (Cont'd)

Test Name	Test in VHDL and Verilog	Description
pio_memTestAddrBus	Verilog	Determines whether the PIO design's FPGA block RAM's address bus interface is correctly connected by performing a walking ones address test. This test should only be called after successful completion of pio_memTestDataBus.
pio_memTestDevice	Verilog	Checks the integrity of each bit of the PIO design's FPGA block RAM by performing an increment/decrement test. This test should only be called after successful completion of pio_memTestAddrBus.
pio_timeoutFailureExpected	Verilog	Sends a Memory 32 Write TLP followed by Memory 32 Read TLP to an invalid address and waits for a Completion with data TLP. This test anticipates that waiting for the completion TLP times out and illustrates how the test programmer can gracefully handle this event.
pio_tlp_test0 (illustrative example only)	Verilog	Issues a sequence of Read and Write TLPs to the example design's RX interface. Some of the TLPs, for example, burst writes, are not supported by the PIO design.

VHDL Test Selection

Test selection is implemented in the VHDL Root Port Model by means of overriding the `test_selector` generic within the `tests` entity. The `test_selector generic` is a string with a one-to-one correspondence to each test within the `tests` entity.

The user can modify the generic mapping of the instantiation of the `tests` entity within the `pci_exp_usrapp_tx` entity. The default generic mapping is to override the `test_selector` with the test name `pio_writeReadBack_test0`. Currently there are two tests defined inside the `tests` entity, `sample_smoke_test0` and `pio_writeReadBack_test0`. Additional customer-defined tests should be added inside `tests.vhd`. Currently, specific tests cannot be selected from the VHDL simulation scripts.

Verilog Test Selection

The Verilog test model used for the Root Port Model lets you specify the name of the test to be run as a command line parameter to the simulator. For example, the `simulate_ncsim.sh` script file, used to start the IES simulator explicitly specifies the test `sample_smoke_test0` to be run using the following command line syntax:

```
ncsim work.boardx01 +TESTNAME=sample_smoke_test0
```

You can change the test to be run by changing the value provided to `TESTNAME` defined in the test files `sample_tests1.v` and `pio_tests.v`. The same mechanism is used for VCS and ModelSim.

Differences between VHDL and Verilog Root Port Models

The major difference between the Verilog and the VHDL test bench is that the Verilog test bench has expectation tasks. The expectation tasks are API calls used in conjunction with a bus mastering customer design. The test program issues a series of expectation task calls; for example, expect a memory write TLP, expect a memory read TLP. The test program fails if the customer design does not respond with the expected TLPs. This functionality was implemented using the fork-join construct in Verilog which is not available in VHDL and so was not implemented.

The Verilog testbench allows test programs to be specified at the command line, where the VHDL testbench specifies test programs within the tests.vhd module.

Another difference is the way that wave files are generated. The Verilog testbench uses recordvars and dumpfile commands within the code, whereas the VHDL testbench leaves this functionality up to the simulator.

The VHDL test bench is slower than the Verilog test bench, especially when testing out the x8 core. Customers using a 4-lane or 8-lane Endpoint for PCIe Block Plus Core might wish to initially simulate their designs with the x1 core due to speed reasons and to iron out their basic functionality. Then users can move on to the 4- or 8-lane simulation when testing out the performance of their design.

Waveform Dumping

Table B-3 describes the available simulator waveform dump file formats, each of which is provided in the simulator's native file format. The same mechanism is used for VCS and ModelSim.

Table B-3: Simulator Dump File Format

Simulator	Dump File Format
Synopsys VCS	.vpd
ModelSim	.vcd
Cadence IES	.trn

VHDL Flow

Waveform dumping in the VHDL flow does not use the +dump_all mechanism described in the Verilog flow section. Because the VHDL language itself does not provide a common interface for dumping waveforms, each VHDL simulator has its own interface for supporting waveform dumping. For both the supported ModelSim and IES flows, dumping is supported by invoking the VHDL simulator command line with a command line option that specifies the respective waveform command file, `wave.do` (ModelSim) and `wave.sv` (IES). This command line can be found in the respective simulation script files `simulate_mti.do` and `simulate_ncsim.sh`.

ModelSim

The following command line initiates waveform dumping for the ModelSim flow using the VHDL test bench:

```
>vsim +notimingchecks -do wave.do -L unisim -L work work.board
```

IES

The following command line initiates waveform dumping for the IES flow using the VHDL testbench:

```
>ncsim -gui work.board -input @"simvision -input wave.sv"
```

Verilog Flow

The Root Port Model provides a mechanism for outputting the simulation waveform to file by specifying the `+dump_all` command line parameter to the simulator.

For example, the script file `simulate_ncsim.sh` (used to start the IES simulator) can indicate to the Root Port Model that the waveform should be saved to a file using the following command line:

```
ncsim work.boardx01 +TESTNAME=sample_smoke_test0 +dump_all
```

Output Logging

When a test fails on the example or customer design, the test programmer debugs the offending test case. Typically, the test programmer inspects the wave file for the simulation and cross-reference this to the messages displayed on the standard output. Because this approach can be very time consuming, the Root Port Model offers an output logging mechanism to assist the tester with debugging failing test cases to speed the process.

The Root Port Model creates three output files (`tx.dat`, `rx.dat`, and `error.dat`) during each simulation run. Log files `rx.dat` and `tx.dat` each contain a detailed record of every TLP that was received and transmitted, respectively, by the Root Port Model. With an understanding of the expected TLP transmission during a specific test case, the test programmer may more easily isolate the failure.

The log file `error.dat` is used in conjunction with the expectation tasks. Test programs that utilize the expectation tasks generate a general error message to standard output. Detailed information about the specific comparison failures that have occurred due to the expectation error is located within `error.dat`.

Parallel Test Programs

There are two classes of tests supported by the Root Port Model:

- **Sequential tests.** Tests that exist within one process and behave similarly to sequential programs. The test depicted in [Test Program: pio_writeReadBack_test0](#) is an example of a sequential test. Sequential tests are very useful when verifying behavior that have events with a known order.
- **Parallel tests.** Tests involving more than one process thread. The test [sample_smoke_test1](#) is an example of a parallel test with two process threads. Parallel tests are very useful when verifying that a specific set of events have occurred; however, the order of these events are not known.

A typical parallel test uses the form of one command thread and one or more expectation threads. These threads work together to verify a device's functionality. The role of the command thread is to create the necessary TLP transactions that cause the device to receive and generate TLPs. The role of the expectation threads is to verify the reception of an expected TLP. The Root Port Model TPI has a complete set of expectation tasks to be used in conjunction with parallel tests.

Because the example design is a target-only device, only Completion TLPs can be expected by parallel test programs while using the PIO design. However, the full library of expectation tasks can be used for expecting any TLP type when used in conjunction with the customer's design (which may include bus-mastering functionality). Currently the VHDL version of the Root Port Model Test Bench does not support Parallel tests.

Test Description

The Root Port Model provides a Test Program Interface (TPI). The TPI provides the means to create tests by simply invoking a series of Verilog tasks. All Root Port Model tests should follow the same six steps:

1. Perform conditional comparison of a unique test name
2. Set up master timeout in case simulation hangs
3. Wait for Reset and link-up
4. Initialize the configuration space of the Endpoint
5. Transmit and receive TLPs between the Root Port Model and the Endpoint DUT
6. Verify that the test succeeded

Test Program: `pio_writeReadBack_test0` displays the listing of a simple test program `pio_writeReadBack_test0`, written for use in conjunction with the PIO Endpoint. This test program is located in the file `pio_tests.v`. As the test name implies, this test performs a one DWORD write operation *to* the PIO Design followed by a 1 DWORD read operation *from* the PIO Design, after which it compares the values to confirm that they are equal. The test is performed on the first location in each of the active Mem32 BARs of the PIO Design. For the default configuration, this test performs the write and read back to BAR2 and to the EROM space (BAR6) (Block Plus only). The following section outlines the steps performed by the test program.

- Line 1 of the sample program determines if the user has selected the test program `pio_writeReadBack_test1` when invoking the Verilog simulator.
- Line 4 of the sample program invokes the TPI call `TSK_SIMULATION_TIMEOUT` which sets the master timeout value to be long enough for the test to complete.
- Line 5 of the sample program invokes the TPI call `TSK_SYSTEM_INITIALIZATION`. This task causes the test program to wait for the system reset to be deasserted as well as the Endpoint's `trn_lnk_up_n` signal to be asserted. This is an indication that the Endpoint is ready to be configured by the test program via the Root Port Model.
- Line 6 of the sample program uses the TPI call `TSK_BAR_INIT`. This task performs a series of Type 0 Configuration Writes and Reads to the Endpoint core's PCI Configuration Space, determines the memory and I/O requirements of the Endpoint, and then programs the Endpoint's Base Address Registers so that it is ready to receive TLPs from the Root Port Model.
- Lines 7, 8, and 9 of the sample program work together to cycle through all the Endpoint's BARs and determine whether they are enabled, and if so to determine their type, for example, Mem32, Mem64, or I/O).

All PIO tests provided with the Root Port Model are written in a form that does not assume that a specific BAR is enabled or is of a specific type (for example, Mem32, Mem64, I/O). These tests perform on-the-fly BAR determination and execute TLP transactions dependent on BAR types (that is, Memory32 TLPs to Memory32 Space, I/O TLPs to I/O Space, and so forth). This means that if a user reconfigures the BARs of the Endpoint, the PIO continues to work because it dynamically explores and configures the BARs. Users are

not required to follow the form used and can create tests that assume their own specific BAR configuration.

- Line 7 sets a counter to increment through all of the Endpoint's BARs.
- Line 8 determines whether the BAR is enabled by checking the global array `BAR_INIT_P_BAR_ENABLED[]`. A non-zero value indicates that the corresponding BAR is enabled. If the BAR is not enabled, then test program flow moves on to check the next BAR. The previous call to `TSK_BAR_INIT` performed the necessary configuration TLP communication to the Endpoint device and filled in the appropriate values into the `BAR_INIT_P_BAR_ENABLED[]` array.
- Line 9 performs a case statement on the same global array `BAR_INIT_P_BAR_ENABLED[]`. If the array element is enabled (that is, non-zero), the element's value indicates the BAR type. A value of 1, 2, and 3 indicates I/O, Memory 32, and Memory 64 spaces, respectively.
If the BAR type is either I/O or Memory 64, then the test does not perform any TLP transactions. If the BAR type is Memory 32, program control continues to line 16 and starts transmitting Memory 32 TLPs.
- Lines 21-26 use the TPI call `TSK_TX_MEMORY_WRITE_32` and transmits a Memory 32 Write TLP with the payload DWORD '01020304' to the PIO Endpoint.
- Lines 32-33 use the TPI calls `TSK_TX_MEMORY_READ_32` followed by `TSK_WAIT_FOR_READ_DATA` in order to transmit a Memory 32 Read TLP and then wait for the next Memory 32 Completion with Data TLP. In case the Root Port Model never receives the Completion with Data TLP, the TPI call `TSK_WAIT_FOR_READ_DATA` would locally timeout and display an error message.
- Line 34 compares the DWORD received from the Completion with Data TLP with the DWORD that was transmitted to the PIO Endpoint and displays the appropriate success or failure message.

Test Program: pio_writeReadBack_test0

```
1. else if(testname == "pio_writeReadBack_test1"
2. begin
3. // This test performs a 32 bit write to a 32 bit Memory space and performs a read back
4. TSK_SIMULATION_TIMEOUT(10050);
5. TSK_SYSTEM_INITIALIZATION;
6. TSK_BAR_INIT;
7. for (ii = 0; ii <= 6; ii = ii + 1) begin
8.     if (BAR_INIT_P_BAR_ENABLED[ii] > 2'b00) // bar is enabled
9.         case(BAR_INIT_P_BAR_ENABLED[ii])
10.             2'b01 : // IO SPACE
11.                 begin
12.                     $display("[%t] : NOTHING: to IO 32 Space BAR %x", $realtime, ii);
13.                 end
14.             2'b10 : // MEM 32 SPACE
15.                 begin
16.                     $display("[%t] : Transmitting TLPs to Memory 32 Space BAR %x",
17.                             $realtime, ii);
18.                 //-----
19.                 // Event : Memory Write 32 bit TLP
20.                 //-----
21.                     DATA_STORE[0] = 8'h04;
22.                     DATA_STORE[1] = 8'h03;
23.                     DATA_STORE[2] = 8'h02;
24.                     DATA_STORE[3] = 8'h01;
25.                     P_READ_DATA = 32'hffff_ffff; // make sure P_READ_DATA has known initial value
26.                     TSK_TX_MEMORY_WRITE_32(DEFAULT_TAG, DEFAULT_TC, 10'd1, BAR_INIT_P_BAR[ii][31:0], 4'hF,
4'hF, 1'b0);
27.                     TSK_TX_CLK_EAT(10);
28.                     DEFAULT_TAG = DEFAULT_TAG + 1;
29.                 //-----
30.                 // Event : Memory Read 32 bit TLP
31.                 //-----
32.                     TSK_TX_MEMORY_READ_32(DEFAULT_TAG, DEFAULT_TC, 10'd1, BAR_INIT_P_BAR[ii][31:0], 4'hF,
4'hF);
33.                     TSK_WAIT_FOR_READ_DATA;
34.                     if (P_READ_DATA != {DATA_STORE[3], DATA_STORE[2], DATA_STORE[1], DATA_STORE[0] })
35.                         begin
36.                             $display("[%t] : Test FAILED --- Data Error Mismatch, Write Data %x != Read Data %x",
$realtime, {DATA_STORE[3], DATA_STORE[2], DATA_STORE[1], DATA_STORE[0]}, P_READ_DATA);
37.                         end
38.                     else
39.                         begin
40.                             $display("[%t] : Test PASSED --- Write Data: %x successfully received", $realtime,
P_READ_DATA);
41.                         end
42.                     TSK_TX_CLK_EAT(10);
43.                     DEFAULT_TAG = DEFAULT_TAG + 1;
44.                 end
45.             2'b11 : // MEM 64 SPACE
46.                 begin
47.                     $display("[%t] : NOTHING: to Memory 64 Space BAR %x", $realtime, ii);
48.                 end
49.             default : $display("Error case in usrapp_tx\n");
50.             endcase
51.         end
52.         $display("[%t] : Finished transmission of PCI-Express TLPs", $realtime);
53.         $finish;
54.     end
```

Expanding the Root Port Model

The Root Port Model was created to work with the PIO design, and for this reason is tailored to make specific checks and warnings based on the limitations of the PIO design. These checks and warnings are enabled by default when the Root Port Model is generated by the CORE Generator™ tool. However, these limitations can easily be disabled so that they do not affect the customer's design.

Because the PIO design was created to support at most one I/O BAR, one Mem64 BAR, and two Mem32 BARs (one of which must be the EROM space), the Root Port Model by default makes a check during device configuration that verifies that the core has been configured to meet this requirement. A violation of this check causes a warning message to be displayed as well as for the offending BAR to be gracefully disabled in the test bench. This check can be disabled by setting the `pio_check_design` variable to zero in the `pci_exp_usrapp_tx.v` file.

Root Port Model TPI Task List

The Root Port Model TPI tasks include the following, which are further defined in [Tables B-4](#) through [B-8](#):

- [Test Setup Tasks](#)
- [TLP Tasks](#)
- [BAR Initialization Tasks](#)
- [Example PIO Design Tasks](#)
- [Expectation Tasks](#)

Table B-4: Test Setup Tasks

Name	Input(s)		Description
TSK_SYSTEM_INITIALIZATION	None		Waits for transaction interface reset and link-up between the Root Port Model and the Endpoint DUT. This task must be invoked prior to the Endpoint core initialization.
TSK_USR_DATA_SETUP_SEQ	None		Initializes global 4096 byte DATA_STORE array entries to sequential values from zero to 4095.
TSK_TX_CLK_EAT	clock count	31:30	Waits clock_count transaction interface clocks.
TSK_SIMULATION_TIMEOUT	timeout	31:0	Sets master simulation timeout value in units of transaction interface clocks. This task should be used to ensure that all DUT tests complete.

Table B-5: TLP Tasks

Name	Input(s)	Description		
TSK_TX_TYPE0_CONFIGURATION_READ	tag_ reg_addr_ first_dw_be_	7:0 11:0 3:0	Waits for transaction interface reset and link-up between the Root Port Model and the Endpoint DUT. This task must be invoked prior to Endpoint core initialization.	
TSK_TX_TYPE1_CONFIGURATION_READ	tag_ reg_addr_ first_dw_be_	7:0 11:0 3:0	Sends a Type 1 PCI Express Config Read TLP from Root Port Model to reg_addr_ of Endpoint DUT with tag_ and first_dw_be_ inputs. CplD returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	
TSK_TX_TYPE0_CONFIGURATION_WRITE	tag_ reg_addr_ reg_data_ first_dw_be_	7:0 11:0 31:0 3:0	Sends a Type 0 PCI Express Config Write TLP from Root Port Model to reg_addr_ of Endpoint DUT with tag_ and first_dw_be_ inputs. Cpl returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	
TSK_TX_TYPE1_CONFIGURATION_WRITE	tag_ reg_addr_ reg_data_ first_dw_be_	7:0 11:0 31:0 3:0	Sends a Type 1 PCI Express Config Write TLP from Root Port Model to reg_addr_ of Endpoint DUT with tag_ and first_dw_be_ inputs. Cpl returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	
TSK_TX_MEMORY_READ_32	tag_ tc_ len_ addr_ last_dw_be_ first_dw_be_	7:0 2:0 9:0 31:0 3:0 3:0	Sends a PCI Express Memory Read TLP from downstream port to 32 bit memory address addr_ of Endpoint DUT. CplD returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	
TSK_TX_MEMORY_READ_64	tag_ tc_ len_ addr_ last_dw_be_ first_dw_be_	7:0 2:0 9:0 63:0 3:0 3:0	Sends a PCI Express Memory Read TLP from Root Port Model to 64 bit memory address addr_ of Endpoint DUT. CplD returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	

Table B-5: TLP Tasks (Cont'd)

Name	Input(s)				Description
TSK_TX_MEMORY_WRITE_32	tag_	7:0	Sends a PCI Express Memory Write TLP from Root Port Model to 32-bit memory address addr_ of Endpoint DUT.	tc_	2:0
	len_	9:0	CplID returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	addr_	31:0
	last_dw_be_	3:0	The global DATA_STORE byte array is used to pass write data to task.	first_dw_be_	3:0
	ep_	-			
TSK_TX_MEMORY_WRITE_64	tag_	7:0	Sends a PCI Express Memory Write TLP from Root Port Model to 64-bit memory address addr_ of Endpoint DUT.	tc_	2:0
	len_	9:0	CplID returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	addr_	63:0
	last_dw_be_	3:0	The global DATA_STORE byte array is used to pass write data to task.	first_dw_be_	3:0
	ep_	-			
TSK_TX_COMPLETION	tag_	7:0	Sends a PCI Express Completion TLP from Root Port Model to Endpoint DUT using global COMPLETE_ID_CFG as completion ID.	tc_	2:0
	len_	9:0		comp_status_	2:0
TSK_TX_COMPLETION_DATA	tag_	7:0	Sends a PCI Express Completion with Data TLP from Root Port Model to Endpoint DUT using global COMPLETE_ID_CFG as completion ID.	tc_	2:0
	len_	9:0	The global DATA_STORE byte array is used to pass completion data to task.	byte_count	11:0
	lower_addr	6:0		comp_status	2:0
	ep_	-			
TSK_TX_MESSAGE	tag_	7:0	Sends a PCI Express Message TLP from Root Port Model to Endpoint DUT.	tc_	2:0
	len_	9:0	Completion returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	data	63:0
	mesage_rtg	2:0		message_code	7:0
TSK_TX_MESSAGE_DATA	tag_	7:0	Sends a PCI Express Message with Data TLP from Root Port Model to Endpoint DUT.	tc_	2:0
	len_	9:0	The global DATA_STORE byte array is used to pass message data to task.	data	63:0
	mesage_rtg	2:0	Completion returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.	message_code	7:0

Table B-5: TLP Tasks (Cont'd)

Name	Input(s)			Description
TSK_TX_IO_READ	tag_ addr_ first_dw_be_	7:0 31:0 3:0		Sends a PCI Express I/O Read TLP from Root Port Model to I/O address addr_[31:2] of Endpoint DUT. CplD returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.
TSK_TX_IO_WRITE	tag_ addr_ first_dw_be_ data	7:0 31:0 3:0 31:0		Sends a PCI Express I/O Write TLP from Root Port Model to I/O address addr_[31:2] of Endpoint DUT. CplD returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.
TSK_TX_BAR_READ	bar_index byte_offset tag_ tc_	2:0 31:0 7:0 2:0		Sends a PCI Express 1 DWORD Memory 32, Memory 64, or I/O Read TLP from the Root Port Model to the target address corresponding to offset byte_offset from BAR bar_index of the Endpoint DUT. This task sends the appropriate Read TLP based on how BAR bar_index has been configured during initialization. This task can only be called after TSK_BAR_INIT has successfully completed. CplD returned from Endpoint DUT uses the contents of global COMPLETE_ID_CFG as completion ID.

Table B-5: TLP Tasks (Cont'd)

Name	Input(s)			Description
TSK_TX_BAR_WRITE	bar_index byte_offset tag_ tc_ data_	2:0 31:0 7:0 2:0 31:0		<p>Sends a PCI Express 1 DWORD Memory 32, Memory 64, or I/O Write TLP from the Downstream Port to the target address corresponding to offset byte_offset from BAR bar_index of the Endpoint DUT.</p> <p>This task sends the appropriate Write TLP based on how BAR bar_index has been configured during initialization. This task can only be called after TSK_BAR_INIT has successfully completed.</p>
TSK_WAIT_FOR_READ_DATA	None			<p>Waits for the next completion with data TLP that was sent by the Endpoint DUT. On successful completion, the first DWORD of data from the CplD is stored in the global P_READ_DATA. This task should be called immediately following any of the read tasks in the TPI that request Completion with Data TLPs to avoid any race conditions.</p> <p>By default, this task locally times out and terminates the simulation after 1000 transaction interface clocks. The global cpld_to_finish can be set to zero so that local time out returns execution to the calling test and does not result in simulation timeout. For this case test programs should check the global cpld_to, which when set to one indicates that this task has timed out and that the contents of P_READ_DATA are invalid.</p>

Table B-6: BAR Initialization Tasks

Name	Input(s)	Description
TSK_BAR_INIT	None	<p>Performs a standard sequence of Base Address Register initialization tasks to the Endpoint device using the PCI Express fabric. Performs a scan of the Endpoint's PCI BAR range requirements, performs the necessary memory and I/O space mapping calculations, and finally programs the Endpoint so that it is ready to be accessed.</p> <p>On completion, the user test program may begin memory and I/O transactions to the device. This function displays to standard output a memory/I/O table that details how the Endpoint has been initialized. This task also initializes global variables within the Root Port Model that are available for test program usage. This task should only be called after TSK_SYSTEM_INITIALIZATION.</p>
TSK_BAR_SCAN	None	<p>Performs a sequence of PCI Type 0 Configuration Writes and Configuration Reads using the PCI Express fabric in order to determine the memory and I/O requirements for the Endpoint.</p> <p>The task stores this information in the global array BAR_INIT_P_BAR_RANGE[]. This task should only be called after TSK_SYSTEM_INITIALIZATION.</p>
TSK_BUILD_PCIE_MAP	None	<p>Performs memory/I/O mapping algorithm and allocates Memory 32, Memory 64, and I/O space based on the Endpoint requirements.</p> <p>This task has been customized to work in conjunction with the limitations of the PIO design and should only be called after completion of TSK_BAR_SCAN.</p>
TSK_DISPLAY_PCIE_MAP	None	Displays the memory mapping information of the Endpoint core's PCI Base Address Registers. For each BAR, the BAR value, the BAR range, and BAR type is given. This task should only be called after completion of TSK_BUILD_PCIE_MAP.

Table B-7: Example PIO Design Tasks

Name	Input(s)		Description
TSK_TX_READBACK_CONFIG	None		<p>Performs a sequence of PCI Type 0 Configuration Reads to the Endpoint device's Base Address Registers, PCI Command Register, and PCIe Device Control Register using the PCI Express fabric.</p> <p>This task should only be called after TSK_SYSTEM_INITIALIZATION.</p>
TSK_MEM_TEST_DATA_BUS	bar_index	2:0	<p>Tests whether the PIO design FPGA block RAM data bus interface is correctly connected by performing a 32-bit walking ones data test to the I/O or memory address pointed to by the input bar_index.</p> <p>For an exhaustive test, this task should be called four times, once for each block RAM used in the PIO design.</p>
TSK_MEM_TEST_ADDR_BUS	bar_index nBytes	2:0 31:0	<p>Tests whether the PIO design FPGA block RAM address bus interface is accurately connected by performing a walking ones address test starting at the I/O or memory address pointed to by the input bar_index.</p> <p>For an exhaustive test, this task should be called four times, once for each block RAM used in the PIO design. Additionally, the nBytes input should specify the entire size of the individual block RAM.</p>
TSK_MEM_TEST_DEVICE	bar_index nBytes	2:0 31:0	<p>Tests the integrity of each bit of the PIO design FPGA block RAM by performing an increment/decrement test on all bits starting at the block RAM pointed to by the input bar_index with the range specified by input nBytes.</p> <p>For an exhaustive test, this task should be called four times, once for each block RAM used in the PIO design. Additionally, the nBytes input should specify the entire size of the individual block RAM.</p>

Table B-8: Expectation Tasks

Name	Input(s)		Output	Description
TSK_EXPECT_CPLD	traffic_class td ep attr length completer_id completer_status bcm byte_count requester_id tag address_low	2:0 - - 1:0 9:0 15:0 2:0 - 11:0 15:0 7:0 6:0	expect status	Waits for a Completion with Data TLP that matches traffic_class, td, ep, attr, length, and payload. Returns a 1 on successful completion; 0 otherwise.
TSK_EXPECT_CPL	traffic_class td ep attr completer_id completer_status bcm byte_count requester_id tag address_low	2:0 - - 1:0 15:0 2:0 - 11:0 15:0 7:0 6:0	Expect status	Waits for a Completion without Data TLP that matches traffic_class, td, ep, attr, and length. Returns a 1 on successful completion; 0 otherwise.
TSK_EXPECT_MEMRD	traffic_class td ep attr length requester_id tag last_dw_be first_dw_be address	2:0 - - 1:0 9:0 15:0 7:0 3:0 3:0 29:0	Expect status	Waits for a 32-bit Address Memory Read TLP with matching header fields. Returns a 1 on successful completion; 0 otherwise. This task can only be used in conjunction with Bus Master designs.

Table B-8: Expectation Tasks (Cont'd)

Name	Input(s)		Output	Description
TSK_EXPECT_MEMRD64	traffic_class td ep attr length requester_id tag last_dw_be first_dw_be address	2:0 - - 1:0 9:0 15:0 7:0 3:0 3:0 61:0	Expect status	Waits for a 64-bit Address Memory Read TLP with matching header fields. Returns a 1 on successful completion; 0 otherwise. This task can only be used in conjunction with Bus Master designs.
TSK_EXPECT_MEMWR	traffic_class td ep attr length requester_id tag last_dw_be first_dw_be address	2:0 - - 1:0 9:0 15:0 7:0 3:0 3:0 29:0	Expect status	Waits for a 32 bit Address Memory Write TLP with matching header fields. Returns a 1 on successful completion; 0 otherwise. This task can only be used in conjunction with Bus Master designs.
TSK_EXPECT_MEMWR64	traffic_class td ep attr length requester_id tag last_dw_be first_dw_be address	2:0 - - 1:0 9:0 15:0 7:0 3:0 3:0 61:0	Expect status	Waits for a 64 bit Address Memory Write TLP with matching header fields. Returns a 1 on successful completion; 0 otherwise. This task can only be used in conjunction with Bus Master designs.
TSK_EXPECT_IOWR	td ep requester_id tag first_dw_be address data	- - 15:0 7:0 3:0 31:0 31:0	Expect status	Waits for an I/O Write TLP with matching header fields. Returns a 1 on successful completion; 0 otherwise. This task can only be used in conjunction with Bus Master designs.

Migration Considerations

For users migrating to Endpoint Block Plus for PCI Express® from the Endpoint for PCI Express core for Virtex®-II Pro and Virtex-4 FX devices, the lists in this appendix describe the differences in behaviors and options between the Block Plus core and the Endpoint core (versions 3.6 and earlier). Many of the differences are illustrated in the changes to the CORE Generator™ tool GUI.

Transaction Interfaces

- The `trn_terr_fwd_n` signal does not exist. User applications that require transmitting poisoned TLPs must set the EP bit in the TLP header.
- Bit definitions for `trn_tbuf_av_n` vary between the two cores. See [Transaction Interface, page 34](#) for detailed information.
- MPS-violation checking and filtering is not implemented for transmitted TLPs. User applications that erroneously transmit TLPs that violate the MPS setting can cause a fatal error to be detected by the connected PCI Express port.
- `trn_tdst_rdy_n` signal can be deasserted at any time during TLP transmission. User applications are required to monitor `trn_tdst_rdy_n` and respond appropriately. See [Transaction Interface, page 34](#) for detailed information.
- Values reported on `trn_rfc_npd_av` are the actual credit values presented to the link partner, not the available space in the receive buffers. The value is 0, representing infinite non-posted credit.
- The `trn_rfc_cplh_av` and `trn_rfc_cpld_av` signals do not exist. User applications must follow the completion-limiting mechanism described in [Performance Considerations on the Receive Transaction Interface, page 107](#).

Configuration Interface

The Block Plus core automatically responds to PME-turnoff messages with `PME-turnoff_ack` after a short delay. There is no `cfg_turnoff_ok_n` input to the core.

System and PCI Express Interfaces

- The `trn_clk` output is a fixed frequency configured in the CORE Generator tool GUI. `trn_clk` does not shift frequencies in case of link recovery or training down.
- The reference clock (`sys_clk`) frequency is selectable: 100 MHz or 250 MHz. The reference clock input is a single-ended signal.
- A free running clock output (`refclkout`) is provided, based on the selection of the Reference clock (100 or 250 MHz)
- The 4-lane and 8-lane cores can train down to a 2-lane link when appropriate.
- The Endpoint Block Plus for PCI Express can be configured as a 2-lane core.

Configuration Space

- Slot Clock Configuration support is available using the CORE Generator tool GUI.
- Accesses to non-supported configuration space result in successful completions with null data.
- There is no support for user-implemented Extended PCI Configuration Space or PCI Express Extended Capabilities.
- Power budgeting values are fixed at 0.
- There is no support for D1 or D2 PPM power-management states or the L1 as part of ASPM power-management state.

Additional Design Considerations

Package Constraints

This appendix describes design considerations specific to the Endpoint Block Plus for PCIe® core. [Table D-1](#) lists the smallest supported device and interface combinations for the Block Plus core.

Table D-1: Supported Device and Interface Combinations

Smallest Supported Device/Part Number	Data Bus Width/Speed	Wrapper File
XC5VLX20T FF323-1	Width: 64-bit Port Speed: 62.5 MHz	xilinx_pci_exp_1_lane_ep.v
XC5VLX20T FF323-1	Width: 64-bit Port Speed: 125 MHz	xilinx_pci_exp_2_lane_ep.v
XC5VLX20T FF323-1	Width: 64-bit Port Speed: 125 MHz	xilinx_pci_exp_4_lane_ep.v
XC5VLX30T FF665-1	Width: 64-bit Port Speed: 250 MHz	xilinx_pci_exp_8_lane_ep.v

User Constraints Files

The user constraints file (UCF) contains various constraints required for the Block Plus core. The user constraints file must always be used while processing a design and is specific to the target device. Based on the chosen lane width, part, and package, a suitable UCF is created by the CORE Generator™ tool.

Wrapper File Usage

The wrapper contains an instance of the Block Plus core. When starting a new design, modify this wrapper to include all I/O elements and modules. One of the following files is generated by the CORE Generator tool based on the chosen lane width.

```
<project_dir>/<component_name>/example_design/xilinx_pci_exp_1_lane_ep.v
<project_dir>/<component_name>/example_design/xilinx_pci_exp_2_lane_ep.v
<project_dir>/<component_name>/example_design/xilinx_pci_exp_4_lane_ep.v
<project_dir>/<component_name>/example_design/xilinx_pci_exp_8_lane_ep.v
```

