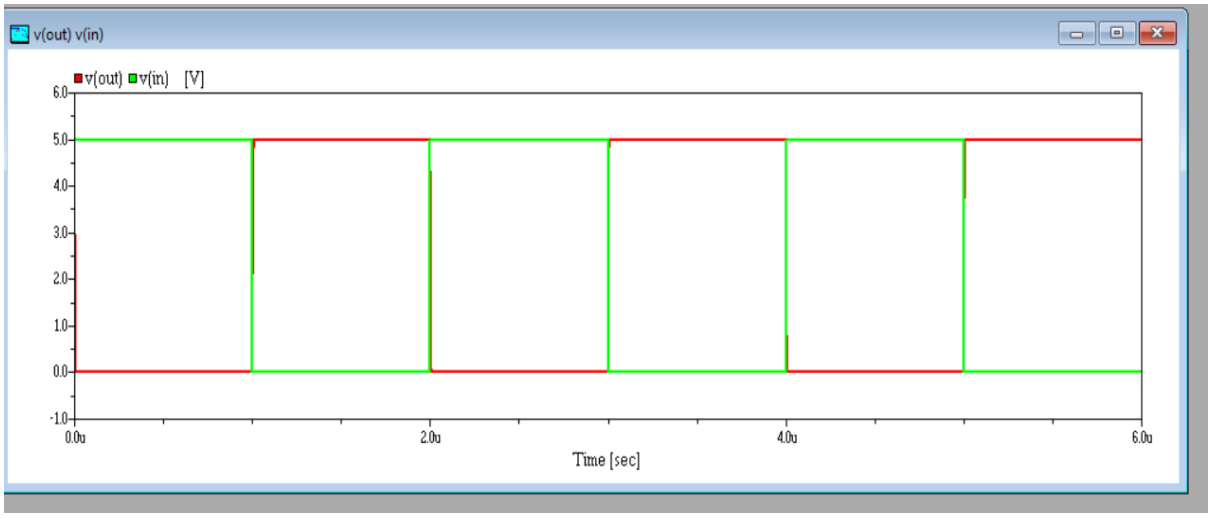
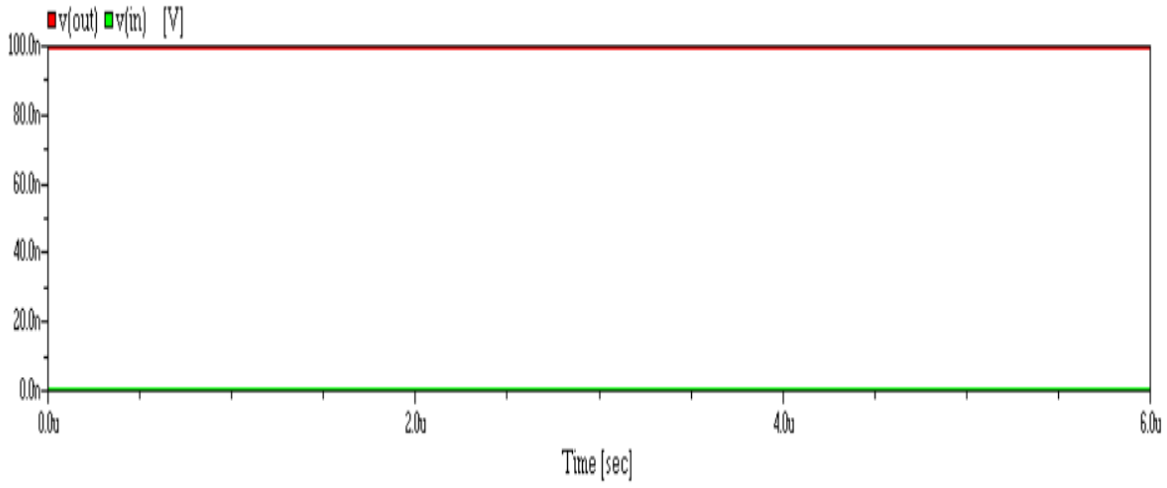
CMOS INVERTER

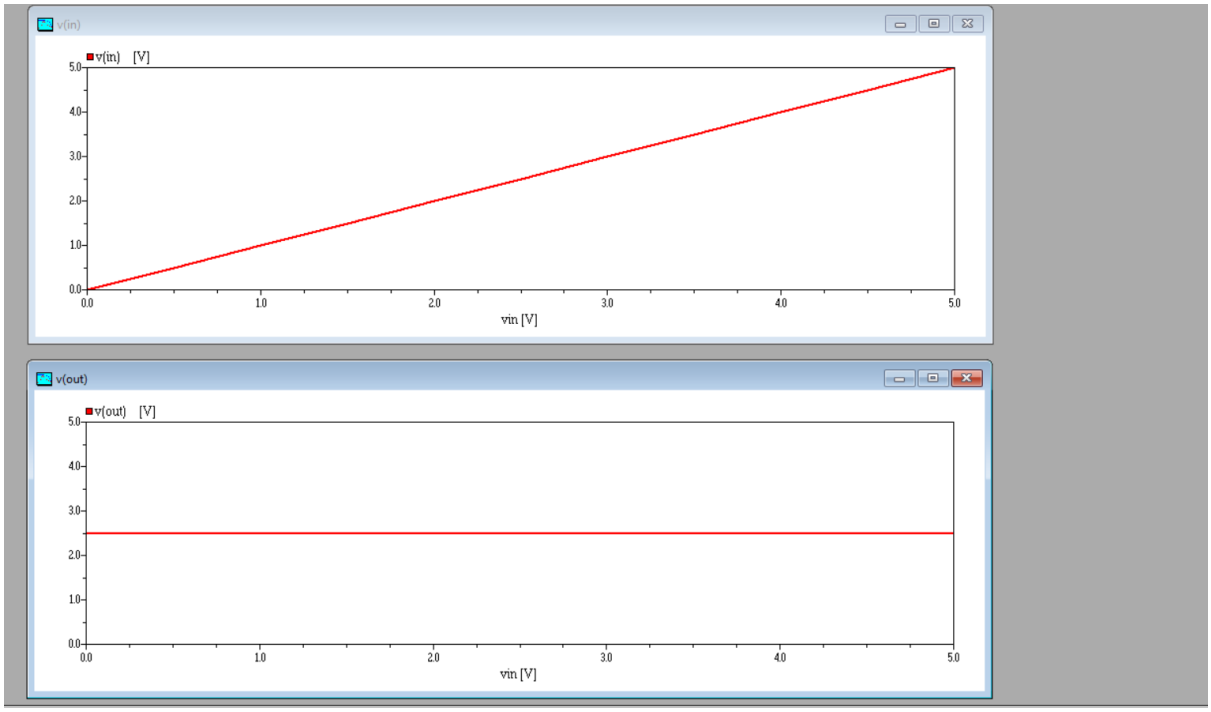
```
cmos inverter
!TR stepsize: 1e-9; Final time: 6e-6

mp out in d d  pmos_t
.model pmos_t pmos vto=-1.5

mn out in s s nmos_t
.model nmos_t nmos vto=1.5

vin in 0 dc 0 Pulse(0 5 0 1e-10 1e-10 1e-6 2e-6)
vdd d 0 dc 5
vss s 0 dc 0

cs out 0 0.1p
```

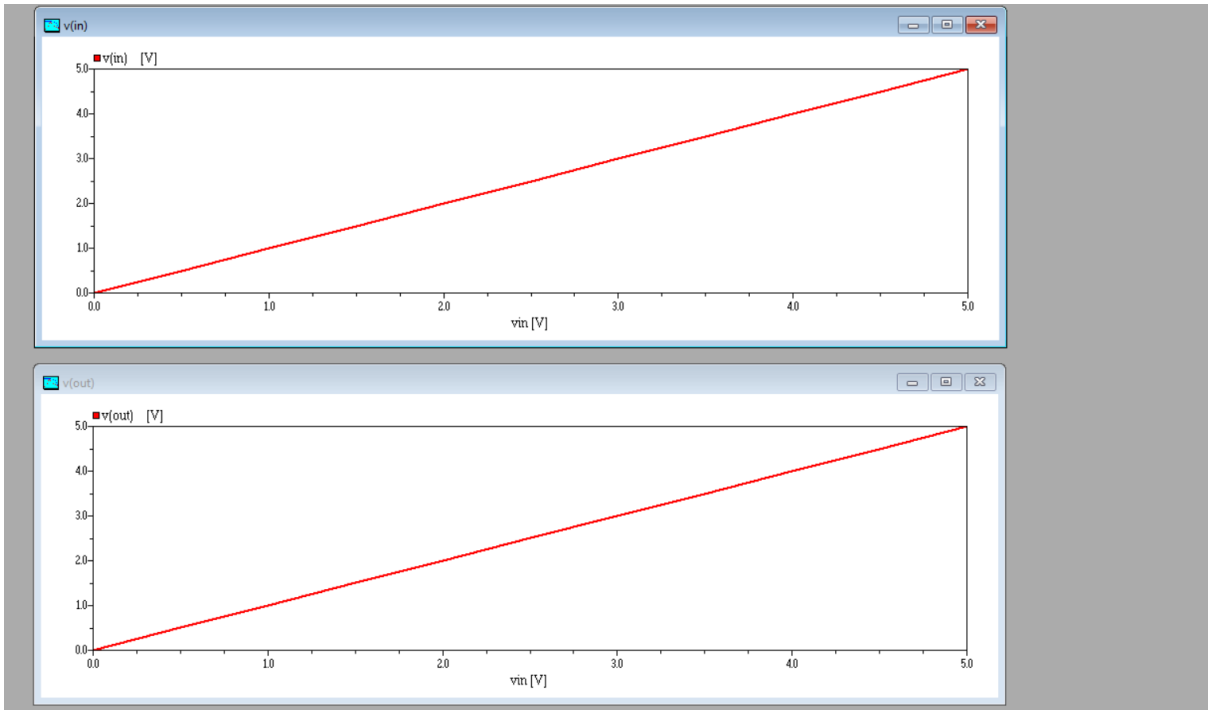


CMOS TRANSMISSION GATE

```
cmos transmission gate

mp out na in d pmos_t
.model pmos_t pmos vto=-1.5

mn out a in s nmos_t
.model nmos_t nmos vto=1.5


vdd d 0 dc 5
vss s 0 dc 0

va a 0 dc 5
vna na 0 dc 0

vin in 0 dc 0 !Pulse(0 5 0 1e-10 1e-10 1e-6 2e-6)
```




v(in)
v(in) [V]
5.0
4.0
3.0
2.0
1.0
0.0
0.0
1.0
2.0
3.0
4.0
5.0
vin [V]
v(out)
v(out) [V]
5.0
4.0
3.0
2.0
1.0
0.0
0.0
1.0
2.0
3.0
4.0
5.0
vin [V]


v(in)
v(in) [V]
5.0
4.0
3.0
2.0
1.0
0.0
0.0
1.0
2.0
3.0
4.0
5.0
vin [V]
v(out)
v(out) [V]
5.0
4.0
3.0
2.0
1.0
0.0
0.0
1.0
2.0
3.0
4.0
5.0
vin [V]