MoE-Lens: Towards the Hardware Limit of High-Throughput MoE LLM Serving Under Resource Constraints

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Abstract

Mixture of Experts (MoE) LLMs, characterized by their sparse activation patterns, offer a promising approach to scaling language models while avoiding proportionally increasing the inference cost. However, their large parameter sizes present deployment challenges in resource-constrained environments with limited GPU memory capacity, as GPU memory is often insufficient to accommodate the full set of model weights. Consequently, typical deployments rely on CPU-GPU hybrid execution: the GPU handles compute-intensive GEMM operations, while the CPU processes the relatively lightweight attention mechanism. This setup introduces a key challenge: *how to effectively optimize resource utilization across CPU and GPU?* Prior work has designed system optimizations based on performance models with limited scope. Specifically, such models do not capture the complex interactions between hardware properties and system execution mechanisms. Therefore, previous approaches neither identify nor achieve the hardware limit.

This paper presents MoE-Lens, a high-throughput MoE LLM inference system designed through holistic performance modeling for resource-constrained environments. Our performance model thoroughly analyzes various fundamental system components, including CPU memory capacity, GPU compute power, and workload characteristics, to understand the theoretical performance upper bound of MoE inference. Furthermore, it captures the system execution mechanisms, including workload scheduling and the effects of paged KV cache, to identify the key hardware bottlenecks and accurately predict the achievable throughput. Informed by our performance model, MoE-Lens introduces an inference system featuring a resource-aware scheduler for prefill and decode phases, an execution engine that overlaps their computation, a data transfer mechanism for model weights, and an optimized CPU-based attention implementation. Evaluated on diverse MoE models and datasets, MoE-Lens outperforms the state-of-the-art MoE-Lightening by 4.6× on average (up to 25.5×), with our theoretical model predicting performance with an average 94% accuracy.

Keywords

LLM, MoE, resource-constraint env, high-throughput serving

1 Introduction

The emergence of Mixture-of-Experts (MoE) models [11, 16, 37] has marked a significant evolution in the design of Large Language Models (LLMs). In contrast to dense models [5, 20] that activate the full set of model parameters for every input, MoE models introduce sparsity by routing each input through a small subset of expert networks. This design enables MoE models to scale up the total parameter count substantially without proportionally increasing the number of floating-point operations (FLOPs) per inference step. As a result, MoE-based LLMs have demonstrated strong empirical performance across a wide range of tasks [11, 15], while maintaining manageable compute requirements for inference.

However, the practical deployment of MoE models is challenging due to their high memory capacity demand to store the model weights. Although only a few experts are activated per token, all expert parameters must reside in memory to allow flexible routing decisions at runtime. This leads to substantial memory pressure that often exceeds the capacity of a GPU. For instance, recent models such as DeepSeek-V3/R1 [15, 16] and Mixtral-8x22B [2] size hundreds of gigabytes, significantly outpacing the requirements of dense models with similar FLOPs. These memory capacity demands hinder the use of MoE models in *resource-constrained environments*, such as low-cost servers, where the available GPU memory capacity is far less than the model size.

A key technique for enabling MoE inference in resource constrained environments is *CPU offloading* [9, 38]. In this approach, the model weights and Key-Value (KV) cache are stored in CPU memory and transferred to the GPU on demand during inference. As a result, CPU-GPU IO becomes a critical bottleneck. Prior work has sought to mitigate this bottleneck through improved scheduling strategies, including pipelining [38], attention offloading [9, 24], and model-aware prefetching [19]. While these techniques have led to notable, hardware utilization remains low even in state-of-the-art systems, leaving room for significant performance improvements. For example, we find only 16.5% of GPU utilization for MoE-Lightning [9] during the generation stage. This raises important questions: ***what is the upper bound on achievable performance, and how can the system achieve such upper bound?***

In this paper, we present MoE-Lens, a high-throughput MoE inference framework designed for resource-constrained environments, achieving up to 25.5× and an average of 4.6× speedup over state-of-the-art MoE-Lightening [9]. MoE-Lens's design contains three stages. First, unlike prior work that relies on limited-scope performance models for system optimizations, MoE-Lens employs a two-stage ***holistic performance model*** that considers factors beyond CPU-GPU I/O bandwidth. It not only identifies theoretical performance upper bounds but also accurately predicts the execution time. In the third stage, we propose a system design guided by this model and jointly optimize the execution pipeline and sequence-level scheduling to bring the system closer to hardware limits. Similar to prior works [9, 19, 38, 45], our focus is *offline, batching processing* inference tasks, such as model evaluation [27],

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data wrangling [31], form processing [10], LLM for relational analytics [30], and synthetic data generation [20], where maximizing inference throughput directly reduces total job completion time.

MoE-Lens's two-stage performance modeling accounts for critical factors that represent missed opportunities in prior works [9, 19, 38] to show how they influence throughput. In the first stage, the model analyzes the theoretical performance upper bound of MoE inference based on the fundamental system components. It identifies *CPU memory capacity*, an element overlooked by prior work, as a primary limiting factor and quantifies how prompt and generation lengths impact the memory utilization. The second stage captures how system execution mechanisms, including workload scheduling and paged KV cache, affect memory/compute utilization and overall system performance. By integrating all these dimensions, our model accurately predicts end-to-end wall-clock inference time for systems operating near hardware limits.

In the third stage, MoE-Lens introduces a high-throughput MoE LLM inference system design informed by our holistic performance model that significantly outperforms state-of-the-art solutions. The system maximizes hardware utilization by addressing key inefficiencies in CPU-side resource usage and balancing compute across the prefill and decode stages. To this end, we introduce resource-aware scheduling that enables effective prefill/decode overlapping, reducing idle time and smoothing workload distribution. We also propose a novel pipeline design, VSLpipe, which includes a contiguous data mover to maximize CPU-GPU bandwidth utilization during weight transfers. Our hand-optimized CPU attention kernel using instrinsics fully leverages the vector units of modern CPUs, preventing the CPU compute throughput from becoming a bottleneck and improving GPU utilization.

Evaluated on diverse models and datasets, MoE-Lens achieves on average 4.6×, up to 25.5×, speedup over the state-of-the-art solution MoE-Lightning [9]. The results show the importance of holistic performance modeling and architecture-aware design decisions for high-throughput MoE inference in resource-constrained environments. In summary, MoE-Lens makes the following contributions.

- A holistic performance model for MoE inference in resource-constrained environments capturing complex interactions between hardware properties and system execution mechanisms.
- An accurate throughput predictor for MoE LLM inference under hardware constraints.
- A system design informed by the model, featuring resource-aware phase scheduling, CPU-side attention execution, and efficient weight/KV cache transfer.
- MoE-Lens: an architecture-aware, end-to-end CPU-GPU hybrid system with theoretical underpinnings that achieves an average 4.6× throughput improvement over the state-of-the-art.

2 Background

Mixture-of-Expert (MoE) LLMs. MoE LLMs achieve strong benchmark performance while reducing compute needs compared to dense LLMs with similar parameter counts, primarily composed of attention and MoE layers. For architectural details, see [9, 19]. A defining trait of modern MoE models is their large size: hundreds of GBs [14–16]—which exceeds standard GPU memory [9, 19, 38].

Concepts in LLM Model Inference. One key module in LLM Models is the attention module, where *key* and *value* vectors are calculated and cached in *KV Cache*. *Group Query Attention (GQA)* is a commonly used attention variant in MoE models, which allows a group of query vectors to share a single pair of key and value vectors, thereby reducing the size of the KV cache. The LLM inference consists of two stages: the *prefill stage*, typically *compute-bound*, where the initial prompt is processed in parallel, and the *decode stage*, typically *memory-bound* [33], where tokens are generated sequentially in an auto-regressive manner.

Resource-Constrained LLM Inference. LLM inference in resource-constrained environments prioritizes high-throughput batch processing on systems where the GPU memory is significantly smaller than the model's total parameter size, while the CPU has sufficient memory or disk capacity to store model weights. This setting differs from traditional LLM serving systems [26, 33, 36] optimized for latency-sensitive applications like chatbots and code completion, where low response time is critical. Instead, resource-constrained inference systems, typically equipped with GPUs like T4 (16GB) or L4 (24GB) [9, 19, 38], prioritize overall throughput and can afford to trade off latency. Since these GPUs lack sufficient memory to store the full model, weights must be streamed from CPU memory over PCIe, introducing substantial overhead. MoE-Lightning [9] addresses this by offloading attention computation to the CPU, forming a CPU–GPU hybrid system. This design avoids transferring the large KV cache to GPU, which is essential as growing GPU parallelism leads to KV sizes exceeding memory capacity. Moreover, because attention has low arithmetic intensity [9, 13], the CPU can execute it efficiently while the GPU focuses on compute-intensive MoE layers.

3 Motivation

While MoE-Lightning [9], the state-of-the-art MoE inference system for resource-constrained environments, leverages a performance model to guide system design and achieves substantial speedups, an important question remains: ***does the state-of-the-art fully harness the capabilities of the underlying hardware?***

3.1 Limited-Scope of Performance Modeling in Prior Work

MoE-Lightning introduced the Hierarchical Roofline Model (HRM) to address the CPU-GPU IO bottleneck, achieving notable gains by offloading decode-stage attention to the CPU and avoiding frequent KV cache transfers. While effective, HRM's focus is limited to arithmetic intensity and IO bandwidth, overlooking two crucial factors that influence performance ceilings: CPU memory capacity and the characteristics of input requests, such as prompt and generation lengths. These factors directly affect how much weight transfer overhead can be amortized and how well pipelining can hide data movement latency. As shown in Table 1, typical execution plans generated by MoE-Lightning result in underutilized CPU memory, revealing inefficiencies in resource allocation. Moreover, sustaining high concurrency requires not just fast IO, but also ample memory bandwidth and compute throughput on the CPU side: elements

Prefill Length	Generation Length	CPU Memory (GB)	CPU Memory Utilization
98	32	265	52.0%
98	64	265	56.2%
926	128	265	35.0%

Table 1: CPU memory utilization for execution plans generated by MoE-Lightening [9], showcasing under-utilization.

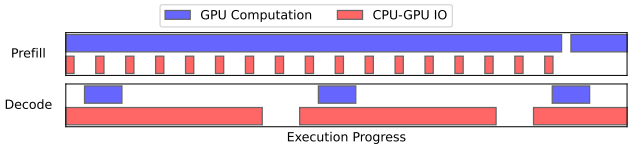


Figure 1: Sample of an execution timeline of GPU computation and CPU-GPU IO during the prefill and decode stages of MoE-Lightning.

HRM does not model. This presents a *significant opportunity* to rethink scheduling and architecture-aware execution strategies that better align with hardware constraints.

Motivated Approach. These limitations motivate the development of the *Stage 1 Model* in MoE-Lens's three-step approach, which extends beyond operator-level IO analysis to capture a more complete picture of system performance. This model establishes a theoretical upper bound on throughput for processing requests with varying prompt and generation lengths, incorporating the often-overlooked impact of CPU memory capacity.

3.2 Resource Utilization Imbalance between Prefill and Decode Stages.

To approach the throughput upper bound, it is essential to account for *workload heterogeneity* in LLM inference, which causes imbalanced resource utilization between the prefill and decode stages. As shown in Figure 1, the prefill stage fully utilizes GPU compute but leaves CPU-GPU IO bandwidth underutilized, while the decode stage suffers from low GPU utilization due to on-demand weight transfers from CPU to GPU, constrained by limited GPU memory. Existing MoE inference systems in resource-constrained settings handle these stages separately, simplifying scheduling but exacerbating the imbalance. Profiling MoE-Lightning [9] with a 98-token prompt and 32-token generation reveals this inefficiency: CPU-GPU IO is active only 23.9% of the time during prefill, while GPU utilization drops to 16.5% during decode.

Motivated Approach. This observation motivates the need to *overlap prefill and decode execution* to approach the hardware limit. MoE-Lens formalizes this in the *Stage 2 Model*, which incorporates key execution factors to make the model both resource- and workload-aware while still reflecting hardware constraints. By accounting for overlapped scheduling and system-level interactions, the *Stage 2 Model* aligns closely with real system behavior, enabling practical guidance for system design and accurate estimation of end-to-end execution time in MoE inference.

4 Overview of MoE-Lens

In this work, we aim to answer the following critical questions:

- *What is the throughput upper bound for a machine?*
- *How to systematically approach that performance upper bound?*

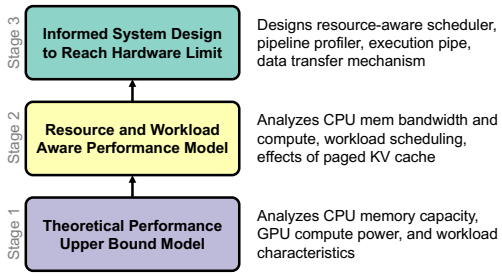


Figure 2: Overview of MoE-Lens that combines a theoretical performance upper bound, resource and workload aware performance model, and an informed system design to reach hardware limits.

In MoE-Lens, we take a three-step approach as shown in Figure 2, building up an increasingly detailed understanding of MoE inference in a resource-constrained environment, and eventually reach a concrete design that reaches the hardware limit. In *Stage 1*, we develop a model to understand the theoretical performance upper bound of MoE inference based on the fundamental system's architectural components (§5.1, §5.2). We further analyze the requirements on CPU memory bandwidth and compute throughput, which support the performance upper bound (§5.3) and the benefits of prefill/decode overlapped scheduling (§5.4). Holistically considering all factors above, and request batch size and paged KV cache, we derive our resource and workload aware performance model in *Stage 2* from an implementation viewpoint (§5.5), providing realistic insights for concert design and predict system performance (with 94% accuracy). One important property of our *Stage 2* model is that it *converges* to the performance upper bound with an increasing batch size, thus still modeling the hardware limits but pricing in the physical execution factors. Finally in *Stage 3*, we provide a system design based on the insights from modeling and the guidance of the *Stage 2* model, which adapts to the variance of the real execution environments while achieving the high hardware utilization outlined by the *Stage 2* model (§6).

5 MoE-Lens Performance Model

This section describes the details of our *Stage 1* and *2* models.

5.1 CPU Memory Capacity as a Limiting Factor

As the CPU memory stores the KV cache, its capacity directly determines the number of sequences that can be processed in parallel. A large number of active sequences allows a large number of tokens to reuse the weights loaded from the CPU for computation, amortizing the cost of moving the weights from the CPU to the GPU. *An important question is* ***how much CPU memory is necessary to fully utilize the GPU?***

Let N_e denote the number of experts, N_k the number of top-k experts selected per token token, h the model dimension, h_i the intermediate dimension of the expert networks (typically, $h_i = mh$, where $m > 1$), s the GQA group size and n as the number of tokens processed in parallel. The GEMM arithmetic-to-IO intensity, which is the amount of GEMM computation divided by the amount of

	Sequence Length 256			Sequence Length 512		
NVIDIA GPU	A40	L40	A100	A40	L40	A100
BF16 Throughput (in T FLOPS)	150	181	312	150	181	312
# of Tokens to Saturate GPU compute	19.2k	23.2k	40.0k	19.2k	23.2k	40.0k
KVCache Size to Saturate (in GB)	614	741	1277	1228	1482	2554

Table 2: KV Cache Size Needed to Saturate GPU compute.

weight data accessed, of a MoE model is

$$I = n\frac{6N_k hh_i + 4h^2 + 4\frac{h^2}{s}}{6N_e hh_i + 4h^2 + 4\frac{h^2}{s}} = n\frac{6mN_k + 2 + \frac{2}{s}}{6mN_e + 2 + \frac{2}{s}} \approx n\frac{N_k}{N_e} \tag{1}$$

Here, $\frac{N_k}{N_e}$ reflects the sparsity of the MoE layer. Let C_{GPU} be the GPU's GEMM throughput and B_{IO} the GPU-CPU IO bandwidth. To saturate the GPU computation power, we require

$$I \geq \frac{C_{GPU}}{B} \Leftrightarrow n \geq \frac{C_{GPU}}{B}\frac{N_e}{N_k} \tag{2}$$

For example, saturating the compute of a single NVIDIA A40 GPU (C_{GPU} = 150 TFLOPS, $B = 32$, $N_e = 8$, $N_k = 2$) when running `Mixtral-8x7B` requires processing *19,200 tokens* in parallel. Table 2 quantifies the number of tokens and corresponding KV cache size, assuming a 512-token sequence length (sum of prompt and generation length), needed to saturate different GPUs. Even under a throughput-optimized system design, where abundant pending sequences are assumed, achieving this level of parallelism is challenging due to the **large CPU memory capacity** required to hold the KV cache. Each token contributes to the cumulative KV cache footprint, which can quickly exceed the available CPU memory in resource-constrained settings. For instance, supporting 512-token sequences would require *1.2TB* of CPU memory for KV cache: disproportionate for a single GPU. This memory demand grows with increasing GPU compute capabilities, as illustrated in Table 2.

> ***Takeaway:*** *CPU memory capacity for KV cache storage is a limiting factor to fully utilize GPU compute resources.*

5.2 Stage 1 Model: Parallelism-Memory Efficiency Analysis

While CPU memory capacity constrains the number of tokens that can be processed in parallel, the memory footprint per token varies across stages of inference. During the prefill stage, all tokens in the prompt can be processed simultaneously, effectively amortizing the memory cost across multiple token computations. In contrast, the decode stage operates autoregressively: each sequence's KV cache enables computing only a single token at a time. Consequently, prefill tokens offer higher memory efficiency compared to decode tokens, in terms of parallel computation per unit of memory. This leads to: ***what is the theoretical upper bound on system throughput for a batch of requests with varying prompt and generation lengths, under a fixed hardware configuration?***

We introduce *Parallelism-Memory Efficiency* (*PME*), a metric quantifying how effectively a sequence translates memory capacity into the number of tokens that can be processed in parallel to saturate GPU resources. The *PME* for a sequence s with prompt length p and generation length g is

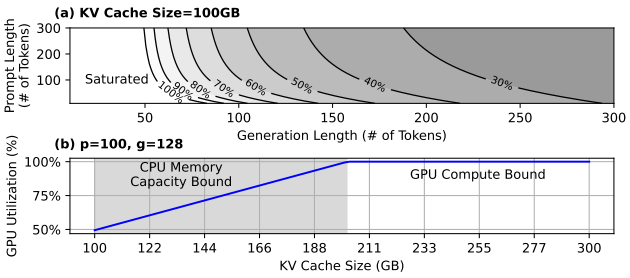


Figure 3: Visualization of the maximum GPU utilization $\frac{T_{max}}{T_{GPU}}$. (a) Maximum GPU utilization when running `Mixtral8x7B` on `A40` with 100GB KV cache. (b) For the same model and GPU, the maximum GPU utilization when $p = 100$ and $g = 128$.

$$\begin{aligned}\text{PME} &= \frac{\sum_{\text{gen. steps}} \text{Parallel Tokens}}{\sum_{\text{gen. steps}} \text{Sequence KV Cache Size}} \\ &= \frac{p+g}{\sum_{j=0}^{g}(p+j)} = \frac{2(p+g)}{(2p+g)g}\end{aligned} \tag{3}$$

Here, the denominator is the sum of the memory capacity a sequence occupies across its entire generation lifetime. We further define the time to transfer the weight of a model from CPU to GPU as $\delta = \frac{\text{Model Size}}{B_{IO}}$. For a batch of sequences with average prefill length p and generation length g, its theoretical maximum inference throughput (tokens/sec) can be estimated as:

$$T_{max} = min(\frac{\text{PME} \cdot M}{\delta}, T_{GPU}), \tag{4}$$

where M is the size of KV cache in number of tokens, and T_{GPU} is the maximum throughput of a GPU in number of tokens per second. Figure 3(a) illustrates how the theoretical maximum GPU utilization varies with prompt length (p) and generation length (g) under a 100GB KV cache budget. Longer sequences lead to lower theoretical GPU utilization, while a higher prompt-to-generation ratio improves utilization for a given sequence length. Figure 3(b) presents a roofline model of theoretical GPU utilization. As KV cache capacity increases, the system transitions from a CPU memory capacity-bound regime to a GPU-bound regime. In the memory-bound regime, limited CPU memory constrains the number of parallel sequences, leading to underutilized GPU compute and throughput that scales with available KV cache. Once the system becomes GPU-bound, the GPU is fully saturated, and further increases in KV cache capacity yield diminishing returns in performance.

> ***Takeaway:*** *Prompt and generation length jointly determine the theoretical upper bound on achievable GPU utilization.*

5.3 CPU Memory Bandwidth and Compute Throughput Requirements

In a hybrid CPU-GPU MoE inference system, the CPU hosts the KV cache and computes decode attention. To avoid bottlenecking the overall execution, the CPU needs to process the attention at a certain throughput, which stresses its memory bandwidth and

compute throughput. *It is crucial to understand:* ***what is the desired CPU memory bandwidth and compute throughput****?*

In a typical deployment scenario, CPU attention computation, CPU-GPU weight transfer, and GPU computation are fully overlapped in the execution pipeline. During each LLM inference iteration, both the model weights and the KV cache are read once from CPU memory, either for transfer to the GPU or for use by the CPU cores. As a result, the total CPU memory bandwidth requirement is the sum of the bandwidth needed to access the KV cache (B_{KV}) and the bandwidth to transfer weights from CPU to GPU (B_{IO}).

$$B_{Mem} = B_{KV} + B_{IO} = \frac{M}{M_{weight}/B_{IO}} = \frac{M}{M_{weight}} B_{IO} \tag{5}$$

Here, M and M_{weight} are the total memory capacity and the memory capacity reserved for the model weight, respectively. The required CPU compute throughput for attention is related to the memory access bandwidth for the KV cache. Assuming that the CPU up-converts the KV cached stored in BF16 to FP32 for computation, we have

$$T_{CPU} = 2 \cdot s \cdot I_{\text{cpu\_attn}} \cdot B_{KV} \tag{6}$$

where s is the GQA group size, and $I_{\text{cpu\_attn}}$ is the arithmetic intensity of attending to one query in the KV cache. $I_{\text{cpu\_attn}}$ is inherently small for the flash attention based implementation, as its primary operations are vector doc product and `saxpby`.

In resource-constrained environments, the CPU memory capacity is usually limited. While the CPU memory bandwidth requirement increases with the size of the KV cache, it typically does not become a bottleneck on modern CPUs equipped with multiple memory channels: often supporting bandwidths exceeding 100GB/s. For instance, consider an extreme case where the KV cache is twice the size of the model weights. In the case of `Mixtral8x7B`, this corresponds to a 200GB KV cache. According to Equation (5), the memory bandwidth required to avoid becoming a performance bottleneck is approximately three times the PCIe bandwidth, *i.e.,* $B_{\text{Mem}} = 60\,\text{GB/s}$. This is well within the capabilities of modern CPUs. On the other hand, sustaining GPU utilization requires the CPU attention computation to deliver throughput on the order of hundreds of GFLOPs. Achieving this performance necessitates efficient use of vector units on modern CPUs. We provide a detailed analysis of this challenge and our implementation in §6.6.

> ***Takeaway:*** *Fully utilizing CPU vector units and memory bandwidth through multiple channels is essential for high-throughput MoE inference.*

5.4 Understanding the Effect of Prefill - Decode Overlap

In §3.2, we briefly explain the motivation behind overlapping the prefill and decode stages. *Another important benefit of this strategy is:* ***prefill-decode overlap effectively improves the CPU memory usage.*** Overlapping allows the decoding process of some sequences to start earlier than others. This reduces the peak memory consumption of a batch of sequences in KV cache, as at each forward pass, some sequences finish execution and release their memory in the KV cache. For an inference batch with on average p prefill tokens and g generation tokens, when using prefill/decode overlapping, we effectively enlarge the KV cache capacity, C_{KV}, to

$$C_{KV,eff.} = \frac{p+g}{p+\frac{g}{2}} C_{KV} \tag{7}$$

compared to making the prefill/decode two isolated stages, without severely overflowing the KV cache. The memory usage per sequence can be estimated using the average sequence length $p + g/2$ in the KV cache instead of the maximum sequence length $p + g$. It is critical for resource-constrained MoE inference, where the memory capacity is a key limiter for large execution batch size.

> ***Takeaway:*** *Besides balancing hardware resource usage, prefill/decode overlapping effectively enlarges the KV cache.*

5.5 Stage 2 Model: Modeling Performance in Realistic Setting

In a realistic deployment scenario, the number of sequences in a batch request is not unbounded, but limited to a large finite value K. Additionally, the KV cache is typically organized into blocks [26], each containing b token slots, with a total of N blocks. In this section, we present our resource- and workload-aware performance model (*Stage 2* in §4). This model builds upon the idealized analysis in *Stage 1*, while incorporating additional considerations such as CPU resource constraints, prefill/decode overlapped scheduling strategies, bounded request batch size K, and paged KV cache organization. The goal is to provide a performance model that accurately predicts end-to-end execution time and remains practical for guiding real system designs (*Stage 3*), while still converging to the hardware-limited upper bound established in *Stage 1.*

We define $\delta = \frac{\text{Model Size}}{B_{IO}}$ same as §5.2. When the number of tokens processed in parallel is less than the GPU's limit T_{GPU}, each inference iteration takes time δ to finish as IO becomes a bottleneck. In each iteration, we schedule q sequences for prefill, where q is calculated as

$$q = \frac{N}{\sum_{i=0}^{g} \lceil \frac{p+i}{b} \rceil} \tag{8}$$

Such a scheduling strategy ensures maximal utilization of the KV cache without over-committing it. In each inference iteration, $q(p+g)$ tokens are released and generated, due to the completion of older sequences and the progression of generation. In contrast, under a naive scheduling approach that strictly separates the prefill and decode stages, the number of parallel decode tokens is limited to $\frac{N}{p+g}$. More active sequences can be decoded in parallel as

$$gq = g\frac{N}{\sum_{i=0}^{g} \lceil \frac{p+i}{b} \rceil} > g\frac{N}{g(p+g)} = \frac{N}{p+g} \tag{9}$$

The generation throughput for a batch with K sequences is

$$T_1 = \frac{K \cdot g}{(\frac{K}{q} + g)\delta} = \frac{K}{K+gq}\frac{gq}{\delta} \tag{10}$$

where $\frac{K}{K+gq}$ is the slowdown factor due to the epilogue of pipelining and $\frac{gq}{\delta}$ is the ideal decoding throughput with gq as the number of sequences active for decoding.

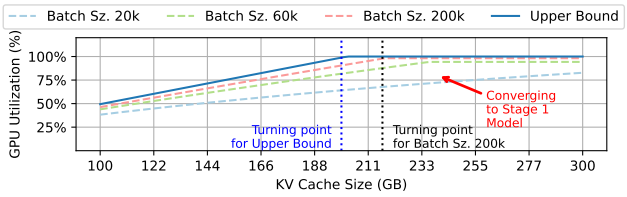


Figure 4: Predicted GPU utilization under different request batch sizes, with $p = 100$ and $g = 128$.

When $T_{GPU} < q(p+g)$, the inference is bottlenecked by GPU computation instead of CPU memory capacity. The total execution time is dominated by the speed we prefill sequences. During execution, both the decode tokens and prefill tokens consume GPU computation. The prefill throughput in the middle of the software pipeline is

$$T_{prefill} = T_{GPU} \frac{p}{p+g} \tag{11}$$

The prologue of the software pipeline takes g iterations, where the average prefill throughput is $\frac{T_{prefill}+T_{GPU}}{2}$. Consequently, $K \cdot p - \frac{T_{prefill}+T_{GPU}}{2} g$ tokens are processed in the main pipeline stages. The total number of iterations for the software pipeline is

$$It = 2 * g + (K \cdot p - \frac{T_{prefill} + T_{GPU}}{2} g)/T_{prefill} \tag{12}$$

The end-to-end throughput is

$$T_2 = \frac{k \cdot g}{It \cdot \delta} \tag{13}$$

An inference process is either bounded by computation or memory capacity, so the throughput will be

$$T = min(T_1, T_2) \tag{14}$$

As shown in §8.1, this model achieves on average 94% accuracy against real execution time.

Impact of real system execution factors. We present the predicted GPU utilization across different request batch sizes in Figure 4. Increasing the batch size improves both the throughput gains from a larger KV cache and the maximum achievable throughput as pipeline prologue and epilogue overhead is amortized. Comparing the curve for a batch size of 200k against the theoretical upper bound, we observe that the use of paged KV cache shifts the turning point to the right, effectively increasing the memory capacity requirement to reach the same level of GPU utilization. *As the batch size theoretically approaches infinity and the KV cache block size approaches 1, the Stage 2 model converges to the Stage 1 theoretical upper bound, delivering the same result.*

> ***Takeaway:*** *Limited number of sequences in a request batch and paged KV cache reduces the effectiveness of a large KV cache size compared to the theoretical analysis.*

6 MoE-Lens System Design

Building on the insights from our architecture-aware performance model (§5), MoE-Lens introduces a system design that closely tracks the theoretical performance limit projected by the *Stage 2* model while remaining adaptive to real-world variations in input sequence lengths and hardware performance.

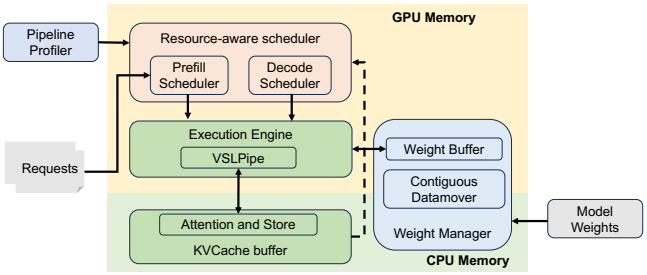


Figure 5: System overview of MoE-Lens.

6.1 Design Overview

Figure 5 illustrates the core components of the MoE-Lens system. When deployed on a given machine for a specific model, the **Pipeline Profiler** identifies the number of tokens required to saturate the GPU compute, guiding the scheduler to prevent pipeline overcommitment. Incoming inference requests are handled by the **Resource-Aware Scheduler**, which overlaps prefill and decode stages and makes scheduling decisions based on the current availability of CPU and GPU resources. At the heart of the execution engine is MoE-Lens's **VSLPipe**—short for *Versatile Pipeline*—which efficiently co-processes prefill and decode requests in resource-constrained environments. It utilizes weight tensors stored in the *Weight Buffer*, managed by the *Weight Manager*, which coordinates with the **Contiguous Data Mover** to eliminate IO stalls during weight transfers. All attention computations are offloaded to the CPU, and our optimized CPU-based flash attention kernel ensures this stage does not become a throughput bottleneck.

6.2 Resource-Aware Scheduler

The goal of the Resource-Aware Scheduler is to schedule sequence execution in a way that (a) fully utilizes available CPU memory capacity, and (b) enables effective prefill/decode overlap, as the models in §5.2 and §5.5 have shown the importance of CPU memory capacity and scheduling strategy in saturing the hardware. Unlike analytical models, the system implementation must adapt dynamically to variations in sequence lengths and hardware performance. The scheduler consists of two components: the **Prefill Scheduler** and the **Decode Scheduler**. Together, they orchestrate the flow of sequences through the prefill and decode stages, ensuring efficient use of memory for KV caching under resource constraints. New sequences are initially queued in the Prefill Scheduler, awaiting prompt processing. In the steady state, there are enough prefill and decode sequences to process. Once a sequence completes the prefill stage, control is handed off to the Decode Scheduler for token generation. During execution, both schedulers may issue sequences, whether in the prefill or decode stage, for parallel processing. To maximize efficiency, both schedulers run on the GPU and maintain their scheduling states directly in GPU memory.

Figure 6 illustrates the two modes of interaction between the Prefill Scheduler and the Decode Scheduler. Based on the availability of KV cache blocks, the system dynamically switches between: *Normal Inference Mode*, where both schedulers operate concurrently

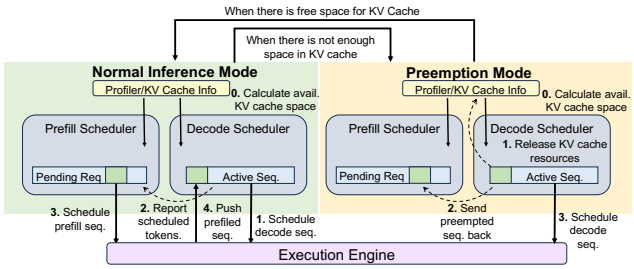


Figure 6: Operation of the Resource-Aware Scheduler.

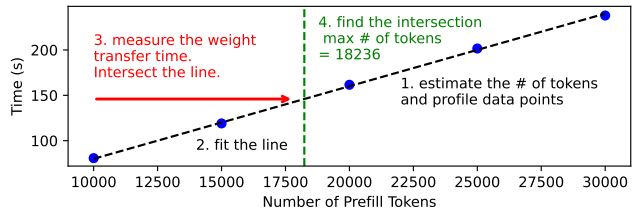


Figure 7: An Example for the threshold n_{real} searching process of MoE-Lens's pipeline profiler, which runs `Mixtral8x7B` on `A40`.

without interference, and *Preemption Mode*, where old decode sequences are prioritized by temporarily preempting new decode sequences to free up memory.

Normal Inference Mode. Before scheduling begins, the Decode Scheduler estimates the number of KV cache blocks required to decode the next token for its managed sequences. If a sufficient number of KV blocks are available, the system enters normal inference mode. In this mode, both the Prefill Scheduler and Decode Scheduler can schedule sequences concurrently. The Decode Scheduler first schedules all sequences currently in the decode stage onto the execution engine. Next, the Prefill Scheduler reads the number of active decode sequences and calculates how many additional prefill tokens it can schedule without exceeding the pipeline capacity, as measured by the Pipeline Profiler (§6.3). It then schedules prefill requests from the head of its queue, staying within this threshold. After the inference pass, newly prefilled sequences are handed off to the Decode Scheduler for subsequent token generation. As decode completes, the Decode Scheduler performs garbage collection to reclaim resources such as KV cache blocks.

Preemption Mode. If the Decode Scheduler detects insufficient KV cache blocks to schedule all decode-stage sequences, the system enters preemption mode. In this mode, a subset of active decode sequences are preempted to free up KV cache resources for other sequences that are ready to generate the next token. The KV cache entries and other associated resources from the preempted sequences are reclaimed and reassigned to the remaining decode sequences. Meanwhile, the Prefill Scheduler halts the scheduling of any new incoming sequences. Instead, it accommodates the preempted decode sequences, treating them as newly arrived sequences that must go through the prefill stage again. This effectively re-inserts them into the execution pipeline from the beginning, but with the advantage that their earlier progress has already been partially completed.

Discusstion. A key design in our scheduler is to alleviate preemption overhead with overlap. When a sequence is preempted, its KV cache is evicted and must be re-prefilled. Without overlapping prefill and decode, this recomputation can only begin after the current decode stage completes, incurring additional latency. In contrast, overlapping prefill with decode allows the recomputation to proceed concurrently, effectively hiding its cost and minimizing impact on overall execution time.

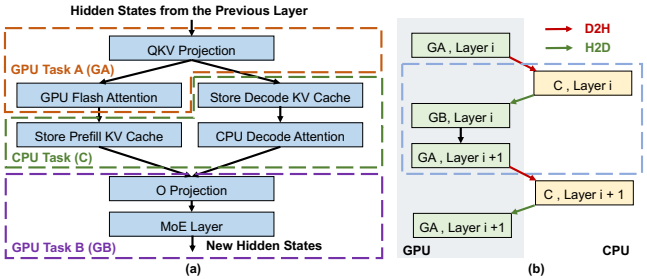


Figure 8: Compute graph division of MoE-Lens's VSLPipe.

6.3 Pipeline Profiler

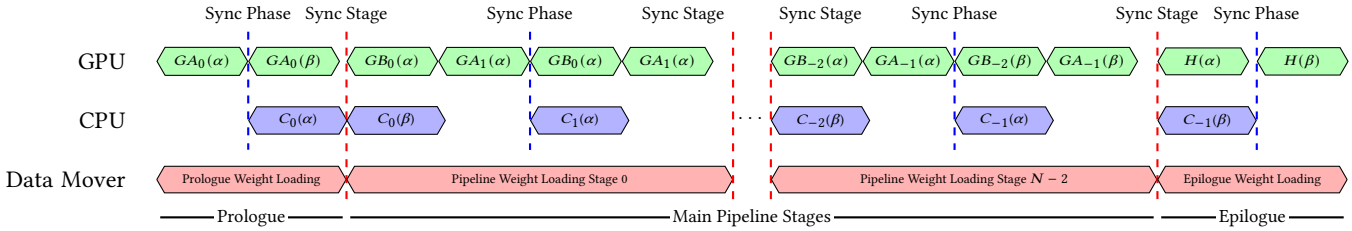
To maintain effective prefill/decode overlap as modeled in §5.5, MoE-Lens uses a Pipeline Profiler to estimate the token threshold n_{real} at which GPU-side GEMM becomes the bottleneck, *i.e.,* the measured n in Equation 2. The resource-aware scheduler ensures that the total number of scheduled tokens stays below n_{real}. This avoids prematurely exhausting prefill sequences and dimensing the effects of prefill/decoce overlapping, thereby sustaining high GPU utilization. The pipeline profiler estimates n using Equation 2, then varies the number of prefilled tokens and measures the corresponding GPU computation time. As shown by an example for `Mixtral8x7B` on the A40 in Figure 7, the profiler fits a line to capture the relationship between token count and GPU time. It also measures the time required to transfer a layer of weights to the GPU. It calculates the maximum number of parallel tokens using the line's slope and weight transfer time.

6.4 Execution Engine

To achieve prefill/decode overlapping without compromising CPU-GPU IO efficiency, as outlined in the performance model (§5.5), MoE-Lens's execution engine features a novel CPU-GPU hybrid pipelined schedule, *VSLPipe*. It is designed to maximize throughput when executing a batch of requests with both prefill and decode sequences.

VSLPipe Compute Graph Division. Figure 8(a) shows how VSLPipe restructures the compute graph of a MoE transformer layer. The per-token *QKV projection* and *GPU Flash Attention* are grouped into *GPU Task A (GA)*, producing KV values for both prefill (post-attention) and decode (pre-attention) sequences. These KV values are offloaded to the CPU, where *CPU Task (C)* stores them in the KV cache and performs *Decode Attention* for decode tokens. The attention results for decode tokens are transferred back to the GPU and combined with prefill outputs. Finally, *GPU Task B (GB)*, which includes the *O projection* and MoE layer, is applied to all tokens.

The CPU and GPU tasks from different layers can be regrouped to better delineate the boundaries between CPU and GPU computation, as illustrated in Figure 8(b). Specifically, the CPU task from layer i, GPU Task B from layer i, and GPU Task A from layer $i+1$ are combined into a single *execution stage*. Each stage consists of



GA_x, GB_x, and C_x are the GPU Task A, GPU Task B, and CPU Task, defined in Figure 8, at layer x. H means GB of the last layer and the model head.

Figure 9: MoE-Lens's VSLPipe execution timeline.

two *execution phases*: a CPU-only phase followed by a GPU-only phase. Between these phases, either a *Device-to-Host (D2H)* or *Host-to-Device (H2D)* transfer occurs: KV values are offloaded to the CPU after GPU computation, and decode attention results are later loaded back to the GPU. Importantly, the amount of computation-related data transferred is relatively small compared to the cost of weight transfers. The total data transferred per stage is bounded by $2n(d + \frac{2d}{s})$, which represents only a small fraction of the overhead when the number of tokens is large enough to saturate the GPU.

VSLPipe Scheduling. Upon receiving prefill and decode jobs, the execution engine partitions them into two groups, α and β, balancing the number of decode and prefill tokens in each. To maximize CPU-GPU utilization, *VSLPipe* applies a software-pipelined execution strategy, as shown in Figure 9. The pipeline comprises a *prologue*, $N-1$ *main stages*, and an *epilogue* for a model with N layers. Each stage is divided into two phases. In each phase, CPU-side attention computations for one partition run concurrently with GPU-side GEMM operations for the other. At the end of each phase, the CPU and GPU synchronize to exchange intermediate results: attended query vectors are transferred from the CPU to the GPU, while fresh query vectors and KV cache entries are offloaded from the GPU to CPU.

The computation-related data transfer is relatively small compared to the overhead of weight transfers. The total data transferred per computation is bounded by $2n(d + \frac{2d}{s})$. For instance, with $n = 18500$, this amounts to roughly 200MB: only a small fraction of the per-layer weight size. To mitigate the CPU-GPU IO bottleneck, weights for the next execution stage are prefetched at the beginning of each stage by the *Contiguous Data Mover*. This data mover runs asynchronously with the computation threads and synchronizes only at the stage boundaries: not at the end of each individual phase. This design allows it to schedule transfers independently and fully utilize the available CPU-GPU bandwidth. We describe the data mover's design in detail in the next section.

6.5 Weight Layout, Weight Buffer, and Contiguous Data Mover

MoE-Lens treats the weights of each layer as two components: layer-wise weights, which include the attention projection matrices and normalization parameters, and expert weights specific to the MoE layers. All weights are stored in pinned CPU memory to enable efficient CPU-GPU IO transfers. During inference, weights are dynamically loaded into the GPU's weight buffer on demand. The size of the weight buffer is two times the model weight size divided by the number of layers. Given that a MoE model usually has tens of layers, the weight buffer is only a few percent of the original model size.

Contiguous Data Mover. Rather than embedding data movement API calls within the execution pipeline, MoE-Lens implements a dedicated Contiguous Data Mover, running on a separate thread, to handle CPU-GPU IO. The execution pipeline pushes weight transfer requests to the data mover at *layer-wise granularity*, while the data mover internally performs fine-grained transfers for efficiency. It first partitions the requested weights into small packets and issues one packet transfer at a time to the runtime. This strategy prevents contention with other CPU-GPU transfers used by the compute pipeline, such as those triggered by PyTorch operations or attention-related data synchronization. Issuing all weight transfers at once would lead to head-of-line blocking, delaying latency-sensitive compute transfers. Empirically, a 100MB packet size strikes a good balance between transfer throughput and minimizing interference. The data mover is implemented in C++ as a PyTorch extension.

6.6 CPU Decode Attention

In §5.3, we highlight the importance of efficient vector unit utilization for CPU-side decode attention to fully exploit the CPU-GPU hybrid system. To this end, MoE-Lens implements a high-performance decode attention kernel using hand-written SIMD intrinsics. Figure 10 compares this implementation with an auto-vectorized baseline in terms of KV cache tokens attended per second. Although both leverage the AVX512 ISA on our test machine, they show stark performance differences. The auto-vectorized version under-utilizes vector units, falling short of system throughput requirements. In contrast, MoE-Lens's hand-optimized kernel—featuring manual vectorization, loop unrolling, and data prefetching—achieves 4.7× higher throughput in single-thread mode and 3.1× with full thread utilization, exceeding the system target. However, we observe that throughput gain saturates beyond 20 threads, likely due to memory controller contention.

7 Evaluation Methodology

Hardware Configuration and Test Environment. All experiments are conducted on a dual-socket server equipped with two Intel Platinum 8380 CPUs. Each socket has eight DDR4-3200 memory channels, totaling 750GB capacity, and is connected to two NVIDIA A40 GPUs. The measured aggregate CPU memory bandwidth per socket is approximately 150GB/s. To ensure consistency and isolate the experimental environment, we use `numactl` to restrict execution to a single CPU socket and a single GPU. The NVIDIA A40 GPU provides 48GB of memory; to simulate GPUs

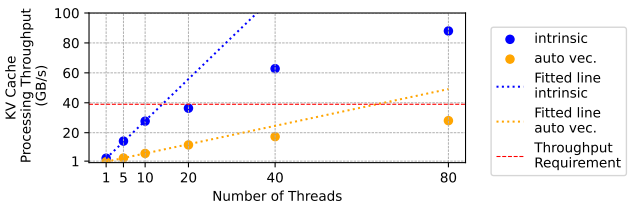


Figure 10: Performance comparison of decode flash attention implemented with intrinsic and auto vectorization. Trend lines are fitted using the first three data points to understand linear scaling. The throughput requirement is estimated assuming KV cache size is twice larger than the model size.

Dataset	Prefill Length		Max Generation Length	Category
	Avg.	Max		
MTBench [4]	98	450	32, 64, 128, 256	Multi-turn conversation
RAG [6]	926	1843	128	Retrieval-Augmented Q&A
AIME 2024 [22]	128	410	512	Math Problem Solving

Table 3: Model evaluation benchmarks used in evaluation.

with more constrained memory capacities, such as the NVIDIA T4 or L4 (16–24GB), we allocate 24–32GB of GPU memory with random tensors, thereby reducing the effective available memory for LLM serving. We configure the KV cache size in MoE-Lens to emulate systems with varying CPU memory capacities. Specifically, we experiment with KV cache sizes ranging from 70GB to 210GB, corresponding to machines with limited CPU-side memory.

Language Models. Following prior works [9, 19], we evaluate MoE-Lens using three diverse MoE models: `Mixtral8x7B` [1], `Mixtral8x22B` [2], and `DBRX` [14]. These models have 47B, 141B, and 132B parameters in BF16, with model sizes of 94GB, 282GB, and 264GB, respectively. We constrain the available GPU memory on the A40 to 16GB for `Mixtral8x7B`, and 24GB for both `Mixtral8x22B` and `DBRX`. Running `Mixtral8x7B` with a 70GB KV cache simulates a system with approximately 164GB of memory, while a 210GB KV cache corresponds to around 300GB. Similarly, using a 70GB KV cache for `Mixtral8x22B` and `DBRX` simulates systems with roughly 350GB of memory, and a 210GB KV cache corresponds to about 500GB.

LLM Benchmark/Datasets. We evaluate MoE-Lens using a diverse set of commonly used LLM model evaluation benchmarks. Following prior work, we use a replicated version of `MTBench` [4], which includes 80 high-quality multi-turn questions across various domains, to construct large batches for in-depth analysis. We also vary the maximum generation length across 32, 64, 128, and 256 tokens, consistent with previous studies. In addition, we assess MoE-Lens's performance on a RAG dataset [6] and the AIME dataset [22] to study its behavior under long-prompt and long-generation scenarios. The prefill length (p) and generation length (g) settings are summarized in Table 3. To ensure evaluations complete within reasonable time, we set the request batch size to 25k for $g = 32$, and 20k otherwise, when running `MTBench` with a 70GB KV cache. In all other settings, the request batch size is set to $5gq$, as defined in the performance model in §5.4.

Baselines. We compare MoE-Lens with two state-of-the-art baselines: `MoE-Lightning` [9] and `vllm` [26]. We use open-source implementations [8, 44] of both baselines for comparison.

- `MoE-Lightning` is the state-of-the-art throughput-oriented MoE inference system for resource-constrained environments. We evaluate `MoE-Lightning` with two CPU memory settings. The normal setting set the CPU memory size profile of `MoE-Lightning` as the sum of model size and KV cache size, plus an additional 30GB for execution overhead. We further evaluate a large CPU memory setting where we set the CPU memory capacity to 1.25× of the sum of the model and KV cache size.
- `vllm` is a widely used LLM serving system based on the idea of paged attention. We use its CPU offload option to run models larger than GPU memory size.

8 Evaluation Results

8.1 Overall Performance

System Generation Throughput. Figure 11 compares the generation throughput (*i.e.*, tokens generated per unit time) of vLLM, MoE-Lightening, and MoE-Lens. The vLLM baseline performs all computations, including GEMMs and attention, on the GPU while paging KV cache to and from CPU memory. Since model weights and KV cache exceed GPU memory capacity, vLLM is bottlenecked by the limited CPU–GPU PCIe bandwidth. MoE-Lightening mitigates this by offloading attention to the CPU, reducing I/O traffic and improving throughput. However, its modeling strategy overlooks key optimization opportunities, leaving substantial headroom before fully utilizing the hardware.

Figure 11 shows that MoE-Lens achieves an average throughput improvement of 4.6× (up to 12.4×) over MoE-Lightening. This gain stems from a key modeling insight overlooked in prior work: the role of CPU memory capacity in determining optimal workload scheduling. By incorporating this constraint, MoE-Lens identifies two critical decisions: (1) maximize the number of concurrent tokens on the GPU by fully utilizing CPU memory for KV cache usage, and (2) a prefill-decode overlap strategy that further expands effective KV cache capacity. In contrast, MoE-Lightening underutilizes CPU memory, as shown in Table 1, leading to fewer concurrent tokens and lower throughput. This disparity becomes more pronounced with a 210GB KV cache, where MoE-Lens delivers a higher average speedup of 6.4×, compared to 3.2× with a 70GB cache. The speedup is further improved to on average 5.3× when allowing MoE-Lens to terminate generation when the EOS token is reached.

With a large KV cache size (210GB), we observe that generation throughput increases with generation length up to a point. For example, running `MTBench` on `Mixtral-8x7B`, throughput improves as generation length increases from 32 to 128 tokens. However, at 256 generation tokens, KV cache becomes a bottleneck, causing throughput to drop. This rise-then-drop pattern is consistent across all models at 210GB KV cache. In contrast, with a 70GB KV cache, the rising trend disappears entirely, as even short generations saturate the limited cache, limiting throughput from the start.

System throughput decreases with longer generation lengths for a fixed prompt length. As analyzed in §5.2, longer generations reduce the PME, increasing CPU memory demand and reducing throughput under limited KV cache. When KV cache is sufficient, however, MoE-Lens approaches around 90% of GPU's computational limit: illustrated by the blue line with triangle markers in Figure 11 for $g_{\max} = 32/64$ with 210GB KV cache.

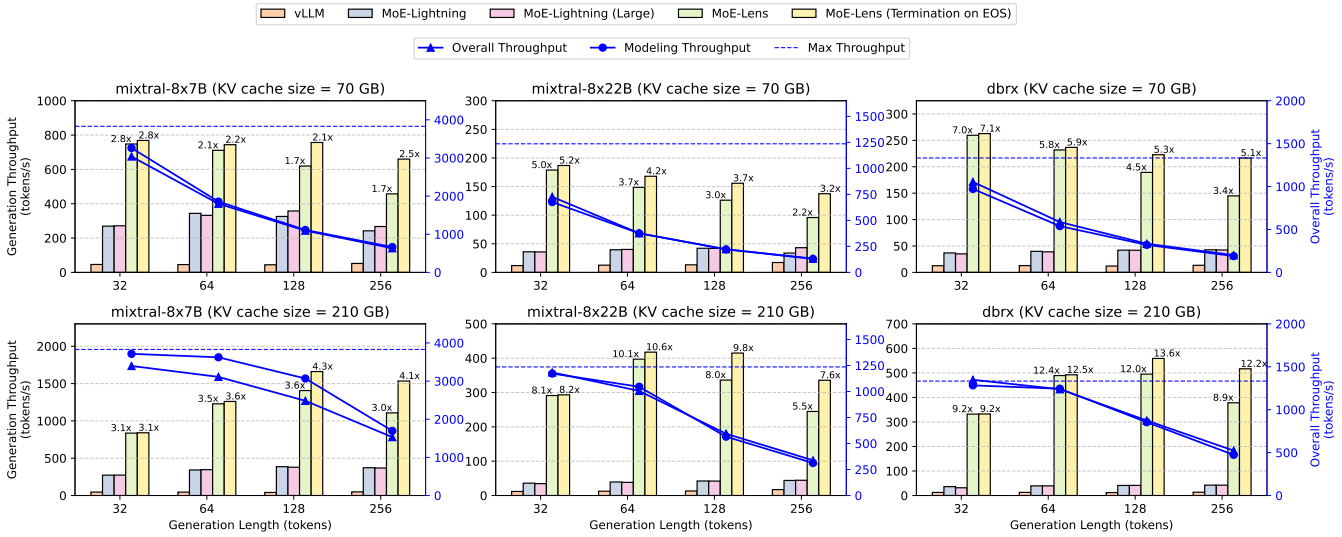


Figure 11: Overall performance of MoE-Lens compared to baselines. The text annotations represents the speedup of MoE-Lens against the best performance of MoE-Lightning. The secondary Y-axis shows the predicted and measured throughput of MoE-Lens, validating our theoretical model.

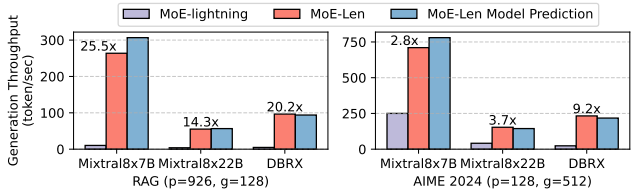


Figure 12: Performance comparison of MoE-Lens and MoE-Lightning for `RAG` and `AIME2024` datasets.

Figure 12 compares MoE-Lens's performance on the prefill-heavy `RAG` and generation-heavy `AIME2024` datasets. MoE-Lens achieves up to 25.5× (19.4× avg) speedup over MoE-Lightning on `RAG`, and up to 9.9× (4.7× avg) on `AIME2024`, demonstrating consistently high throughput across workloads of diverse characteristics.

MoE-Lens's Performance Model's Accuracy. On average, MoE-Lens's performance model (§5.4) predicts throughput with 94% accuracy, as shown in Figures 11 and 12. We estimate CPU-GPU IO bandwidth B_{IO} at 19.5GB/s, based on 1GB tensor transfers. Notably, MoE-Lens falls short of the model's prediction when running `Mixtral8x7B` with a 210GB KV cache, due to contention between CPU attention computation and IO, which delays weight transfers. We analyze this conflict further in §8.2.

8.2 Detailed Execution Status Analysis

The Execution Dynamic of MoE-Lens and the KV Cache Capacity Bottleneck. Figure 13 illustrates the detailed execution status of MoE-Lens when running `MTBench` on `Mixtral8x7B`. In the more resource-constrained 70GB KV cache setting, cache capacity significantly affects both overall system throughput and execution dynamics. When the maximum generation length is 32, the 70GB KV cache is sufficient to avoid sequence thrashing. Since no sequences are preempted, MoE-Lens achieves steady and high throughput in both prefill and decode phases. In this case, GPU utilization approaches around 90%, and system throughput is effectively distributed between prefill and decode phases, proportional to the ratio of prefill to decode tokens. As the maximum generation length increases, each sequence consumes more memory. Insufficient KV cache capacity causes sequence preemption, leading to observable fluctuations in the decode and prefill throughput curves.

When the maximum generation length is 64, the GPU is unable to prefill new sequences roughly half of the time due to insufficient KV cache capacity. During these preemption events, the prefill throughput drops to zero. As ongoing sequences complete their generation and release their KV cache blocks, the decode throughput also begins to decline. This decline continues until the rate of KV cache release exceeds the rate of token generation. Once enough KV cache blocks are freed, empty slots become available, allowing MoE-Lens's prefill scheduler to admit new sequences into the cache. This, in turn, increases the number of sequences being decoded in parallel, causing both prefill and decode throughput to rise again.

This phenomenon becomes more pronounced when the maximum generation length increases to 256. In this case, MoE-Lens performs prefilling for only a small fraction of the time, and the overall GPU utilization drops significantly. This is due to a limited number of active sequences in the decode stage, resulting in low PME. A similar trend is reflected in the per-forward-pass breakdown of GPU computation, CPU computation, and weight transfer I/O time. When the KV cache capacity is sufficient (*e.g.,* with a maximum generation length of 32), MoE-Lens effectively balances GPU computation and I/O time. However, when the generation length is 256, the KV cache becomes a bottleneck, leading to substantial GPU idle time.

The Effect of a Large KV Cache. By comparing the cases with 70GB and 210GB KV cache, we observe the impact of larger KV cache capacity on overall throughput and execution dynamics. When the generation length is 32, the 70GB cache is sufficient,

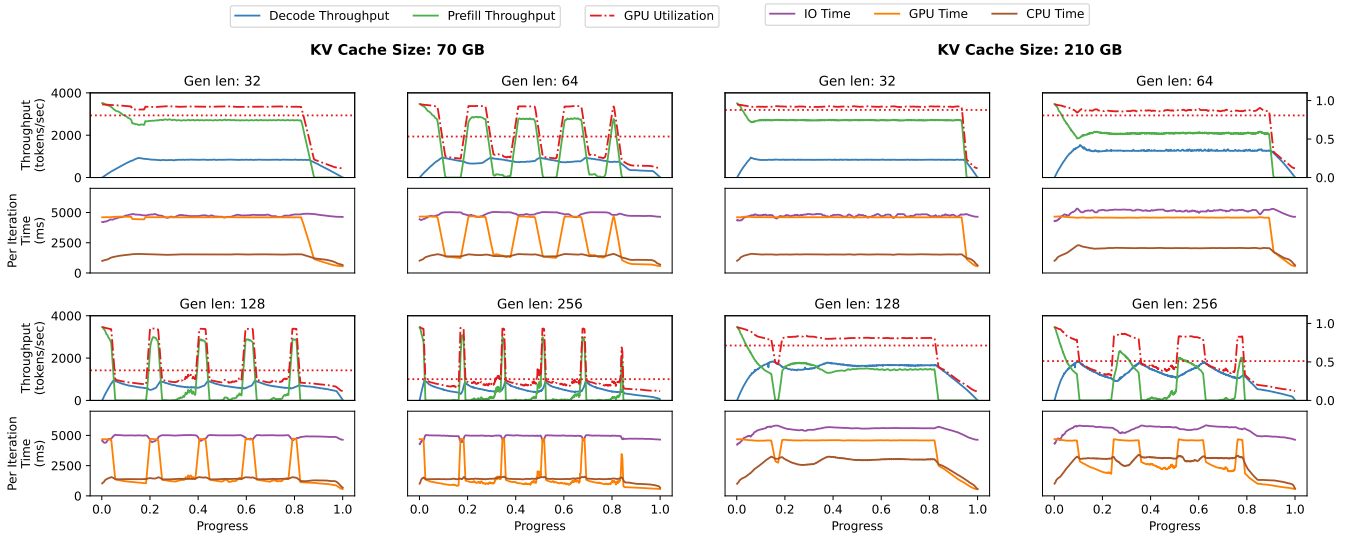


Figure 13: Execution status of MoE-Lens for running `MTBench` on `Mixtral8x7B`, with different maximum generation length and KV cache size. The first and third row illustrate how the throughput and GPU utilization changes with workload progress. The second and the fourth rows show the corresponding IO, GPU computation, and CPU attention time for each inference pass.

and increasing the cache size yields no further performance benefit. However, the advantage of a larger KV cache becomes evident at generation lengths of 64 or more. With 210GB of KV cache and a generation length of 64, decode and prefill throughput curves are noticeably smoother, reflecting fewer sequence preemptions due to ample cache capacity. This leads to higher overall throughput and better GPU utilization. A similar trend is observed for generation lengths of 128 and 256. Preemptions, if any, occur only in the early stages of execution, and the throughput stabilizes quickly. In the 256-token case, the duration of prefill stalls significantly decreases, further enhancing throughput. In both cases, the larger KV cache leads to substantial performance improvements.

The Bandwidth Competition between CPU Attention and CPU-GPU Weight Transfer. When the KV cache is large, the CPU attention computation must scan through a substantial number of KV cache blocks, concurrent with CPU-GPU weight transfers for GPU computation. These two operations contend for shared CPU-side resources, particularly memory bandwidth. When the maximum generation length is 256 and the KV cache size is 210GB, CPU attention time becomes significant relative to IO transfer time. This contention at the CPU memory controller slows down weight transfers, increasing the time to transfer weights from CPU to GPU from approximately 5 seconds to 6 seconds. Interestingly, IO transfer time decreases when preemption begins—fewer sequences remain in the decode stage, reducing the demand on CPU attention and thus easing the pressure on the memory subsystem.

9 Related Work

Resource-constrained LLM Inference. To enable LLM inference on resource-constrained hardware like PCs and low-end servers where the GPU memory capacity is limited, prior works focus on offloading GPU states to CPU [18, 19, 38, 39, 45, 46] and disks [3, 34, 38]. MoE-lightning [9] is the state-of-the-art MoE inference system for resource-constrained environments. It provides a CPU-GPU IO-aware performance model, HRM, on offloading KV cache and attention computation to CPUs. On comparison, MoE-Lens provides a more comprehensive and fine-grained performance model that goes beyond CPU–GPU I/O considerations by accounting for CPU architecture resources and sequence-level scheduling dynamics, and a system significantly outperforms MoE-lightning.

Online LLM Inference Optimization. Online LLM systems with strict latency constraints are usually distributed [33, 36, 41, 42, 47]. Prior works focus on diverse optimization objectives, including but not limited to latency/throughput [23, 25, 26, 35, 51, 52], cost [21, 43], energy efficiency [32, 40, 41]. The online LLM serving system usually employs prefill decode disaggregation [33, 36] to achieve low latency for token generation. Techniques like continuous batching [12] also let the new sequences prefill while others are decoding, but they do not discuss their dynamics for inference under resource-constrained environments, and focus on online serving. In contrast, MoE-Lens provides a detailed performance model to quantify the impact of prefill-decode overlap in resource-constrained environments, and demonstrates how to achieve this with weight transfer and attention computation on the CPU in a balanced manner. This differs fundamentally from continuous batching, whose techniques cannot be directly applied in our setting due to the differing coordination and resource constraints.

Algorithmic Techniques for LLM Acceleration. Another line of research in accelerating LLM inference focuses on trading off the generation accuracy with the LLM inference speed, such as quantization [17, 28, 50], kv cache compression [7, 49], developing attention variants [29, 48], etc. MoE-Lens focuses on improving the hardware resource utilization for MoE inference in resource-constrained environments, without algorithmic changes.

10 Conclusion

This paper uncovered a significant opportunity to improve performance in resource-constrained, batch-processing of MoE LLM

inference. In CPU–GPU hybrid execution, we showed that *effectively utilizing CPU memory capacity* is key to boosting end-to-end throughput, as it enables more tokens to be processed on the GPU. Building on this insight, we developed a theoretical performance model that captures architectural heterogeneity across CPU, GPU, and their interconnects, as well as workload heterogeneity between prefill and decode stages. The model not only identifies critical performance bottlenecks but also predicts overall performance with an average validation accuracy of 94%. Using these insights, we designed an inference system that achieves a 4.6× average speedup (up to 25.5×) over the state-of-the-art.

Acknowledgments

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