IMPINJ®

MONZA® X-2K

DURA DATASHEET
IPJ-P6001-Q2AT

OVERVIEW

Monza® X-2K Dura is a UHF Gen2 RFID IC product with 2176 bits of Non Volatile Memory (NVM) and an I2C interface.

As an I2C device Monza® X-2K Dura operates as a standard I2C EEPROM. The contents of this EEPROM can also be accessed wirelessly via the UHF Gen2 RFID Protocol.

FEATURES

- EPCglobal and ISO 18000-63 compliant, Gen2V2 compliant.
- 2176 bits of user NVM
- 5 One Time Programmable (OTP) blocks (1664/2160 bits) via BlockPermalock feature supported by both I2C and EPC Gen2 interface
- QT for read control and data privacy on RF link
- I2C slave interface with NVM read and write
- −17dBm typical read sensitivity when using a single RF antenna port, -24dBm with DC input
- −19.5dBm typical read sensitivity when using dual RF antenna ports
- −12dBm typical write sensitivity when using a single RF antenna port
- I2C control of RF access
- Write wakeup mode

NAME	DESCRIPTION	CHARACTERISTIC
RF1_P	Differential RF Input Port 1	1.6kΩ, 1pF
RF1_N		−17 dBm single-port sensitivity;
RF2_P	Differential RF Input Port 2	−19.5 dBm True3D sensitivity
RF2_N		
DCI	DC Input	1.6–3.6V
SCL	I2C Clock Input	VIH/L=70% / 30% DCI
SDA	I2C Data Input	IOL=6mA @ 0.4V
GND		

TABLE OF CONTENTS

1   INTRODUCTION

1.1   Scope

This datasheet defines the physical and logical specifications for Gen 2-compliant Monza X-2K Dura tag chip, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2   Reference Documents

EPC^{tm} Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0 (Gen 2 Specification). The conventions used in the Gen 2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Monza X-2K Dura Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen 2 Specification.

EPC™ Tag Data Standards Specification

EPCglobal "Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices" v.1.2.4, August 4, 2006. (Monza X-2K Dura tag chips are compliant with this Gen 2 interoperability standard.)

I2C Specification Rev. 03, June 19 2007, NXP Doc UM10204

2   FUNCTIONAL DESCRIPTION

Monza® X-2K Dura chips enable users to communicate wirelessly with the processor inside electronic devices using standard Gen 2 RFID readers, unlocking many new benefits for consumer electronics manufacturers, retailers and end users. Monza X-2K Dura connects to the processor of an electronic device through a standard I2C bus. This enables the processor to read and write the Monza X chip memory with information that is accessible to UHF Gen 2 RFID readers even when the electronic device is powered off. By enabling electronic devices to communicate with RFID readers, Monza X chips deliver a wide range of extended capabilities such as theft deterrence in the supply chain and device configuration/upgrades at point of sale and beyond.
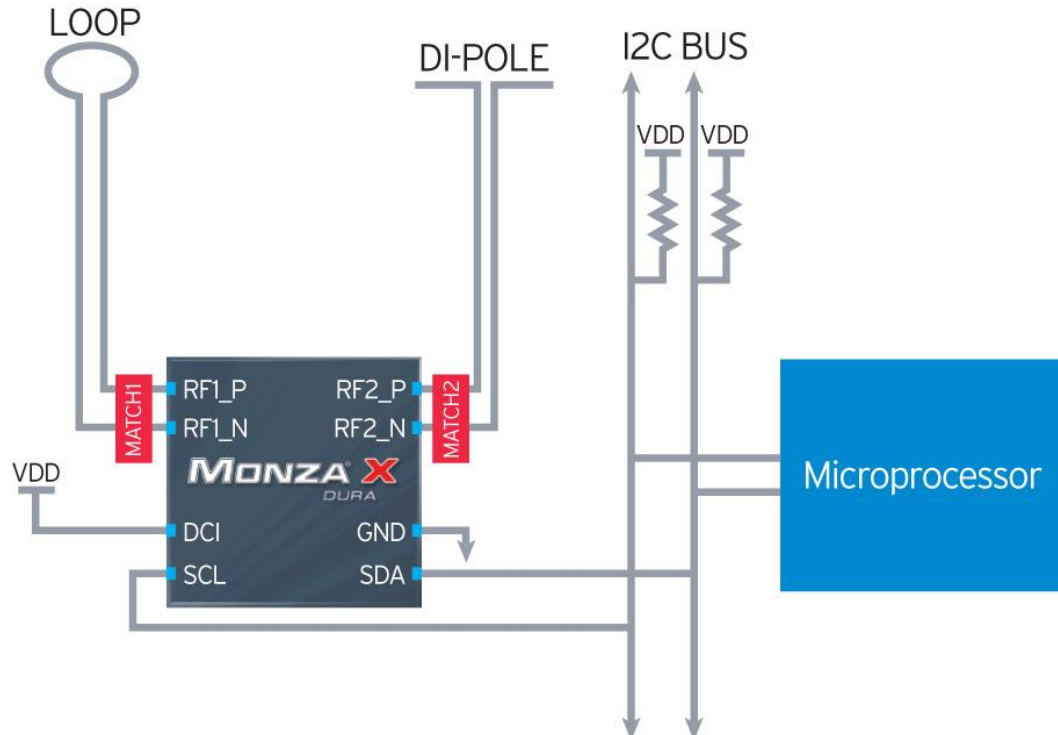
Figure 1 – Monza X-2K Dura connects with microprocessor through I2C bus

2.1   Reader Communications (Gen2/RF Commands)

A reader communicates with Monza® X-2K Dura using standard Gen2 RFID commands. Please see the EPCglobal Class-1 Generation-2 UHF RFID Air-Interface Protocol V1.2.0 for details.

The Gen 2 memory map is shown in Figure 2.

MEM BANK	MEM BANK BIT ADDR	BIT NUMBER (0–F)	GEN2 PERM
User (11₂)	870h-87Fh	USER [15 : 0]	R/W
	860h-86Fh	USER [31 : 16]	R/W
	…	…	R/W
	10h-1Fh	USER [2159 : 2144]	R/W
	00h-0Fh	USER [2175 : 2160]	R/W
TID (10₂)	B0h-BFh	QT_EPC [15 : 0]	R/W
	A0h-AFh	QT_EPC [31 : 16]	R/W
	90h-9Fh	QT_EPC [47 : 32]	R/W
	80h-8Fh	QT_EPC [63 : 48]	R/W
	70h-7Fh	QT_EPC [79 : 64]	R/W
	60h-6Fh	QT_EPC [95 : 80]	R/W
	50h-5Fh	TID_SERIAL [15 : 0]	R
	40h-4Fh	TID_SERIAL [31 : 16]	R
	30h-3Fh	TID_SERIAL [47 : 32]	R
	20h-2Fh	TDTS [15 : 0] = 0x2000	R
	10h-1Fh	TID_DESIGNER [3 : 0] = 0001₂ · TID_MODEL [11 : 0] = 000101000000₂ (Gen2 model number is address 14h to 1Fh)	R
	00h-0Fh	CLASS_ID [7 : 0] = 11100010₂ · XTID = 1 · TID_DESIGNER [10 : 4] = 0000000₂ (Gen2 mask designer is address 08h to 13h)	R
EPC (01₂)	90h-9Fh	EPC [15 : 0]	R/W
	80h-8Fh	EPC [31 : 16]	R/W
	…	…	R/W
	30h-3Fh	EPC [111 : 96]	R/W
	20h-2Fh	EPC [127 : 112]	R/W
	10h-1Fh	EPC_LENGTH [4 : 0] · UMI · XI = 0 · NSI [8 : 0] (Numbering System Identifier, default 000000000₂)	R/W
	00h-0Fh	EPC_CRC [15 : 0]	R
Reserved (00₂)	A0h-AFh	RFU = 0 · WWU · BPL_EN · QT_SR · QT_MEM · DCI_RF_EN · RF_DIS [1 : 0]	R
	90h-9Fh	RESERVED	R
	80h-8Fh	RESERVED	R
	70h-7Fh	RESERVED	R
	60h-6Fh	RESERVED	R
	50h-5Fh	RESERVED	R
	40h-4Fh	LOCK_KILL [1 : 0] · LOCK_ACCESS [1 : 0] · LOCK_EPC [1 : 0] · LOCK_USER [1 : 0] · BLOCK_PERMALOCK [0 : 4] · KILL · I2C_ADDR [1 : 0]	R
	30h-3Fh	ACCESS_PASSWORD [15 : 0]	R/W
	20h-2Fh	ACCESS_PASSWORD [31 : 16]	R/W
	10h-1Fh	KILL_PASSWORD [15 : 0]	R/W
	00h-0Fh	KILL_PASSWORD [31 : 16]	R/W

Figure 2– Gen2 Interface Memory Map

2.2 Support for Optional Gen 2 Commands

Following optional Gen 2 commands are supported:

COMMAND	CODE	LENGTH	DETAILS
Access	11000110	56	
BlockWrite	11000111	>57	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code (000000002) if it receives a valid two-word command with an odd value pointer • Returns error code (000000002) if it receives a command for more than two words • Does not respond to block write commands of zero words
BlockPermalock	11001001	>66	• Five blocks Four, 512 bits in size One 128 bits in size Command can be disabled through I2C

2.3 I2C Interface (SDA, SCL, DCI Pins)

I2C is a standard two-wire interface (clock and data) that supports multiple addressable chips on a bus. Monza® X-2K Dura only supports slave capability. Monza® X-2K Dura's I2C features are compatible with the industry-standard I2C bus. Specifically Monza® X-2K Dura is compatible with I2C specification (I2C Rev 0.03, June 19 2007, NXP Doc UM10204). Monza® X-2K Dura implements the following I2C capabilities:

- I2C slave
- I2C Start Condition
- I2C Repeated Start Condition
- I2C Stop Condition
- I2C Acknowledge
- I2C 7-bit slave address with two NVM programmable bits XX (1101XXM)
- Fast mode transfer rates of 0-400kbits/second
- The DCI voltage provides I2C bus VOH/VOL reference and power.

When an I2C master addresses Monza® X-2K Dura it must format its write transactions as described here. In addition to the I2C device address Monza® X-2K Dura has a memory address that a master writes on every write transaction. This 9-bit memory address specifies which memory byte the master is addressing. The MSB of the memory address replaces the LSB of the I2C device address, bit M in the device ID (A8).

The memory address stored in Monza® X-2K Dura is only changed during a write transaction (R/W == 0). During a read transaction Monza® X-2K Dura ignores the A8 bit in the first byte and there is no following byte. A master only writes a memory address, and future read transactions use the previously written address. A diagram of a transaction that writes the memory address is shown in Figure 3. All bit positions are explicitly shown so the boundary between the I2C device address and the Monza® X-2K Dura memory address is clear. Subsequent diagrams do not explicitly show these address bits.
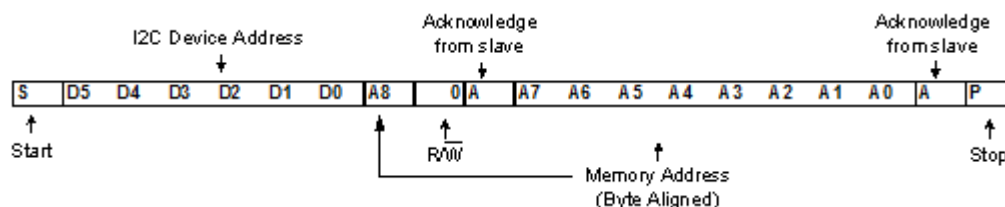
Figure 3 – Addressing the device and setting the memory address

When performing an NVM write a master transmits data after the memory address. Monza® X-2K Dura's NVM is organized as 16-bit words. Writes must align on word boundaries. The NVM allows one- or two-word writes (equivalent to two- or four-byte writes). When executing a one-word write Monza® X-2K Dura ignores the LSB (A0) of the memory address. When executing a two-word write Monza® X-2K Dura ignores the two LSBs (A1, A0) of the memory address. If the write transaction is valid then Monza® X-2K Dura begins the NVM write after receiving a stop from the I2C master. Monza® X-2K Dura will not respond to subsequent I2C transactions for the duration of the NVM write operation. The write time for one- and two-word write operations is the same. A one-word NVM write transaction is shown in Figure 4.

Monza® X-2K Dura may observe several types of invalid NVM-write transactions. If a master sends one or three data bytes then Monza® X-2K Dura will not perform the write (recall that Monza® X-2K Dura writes 16-bit words). If a master sends more than two words then Monza® X-2K Dura will not perform the write. Monza® X-2K Dura also checks the memory address and will not perform a write if the address is invalid (but note that Monza® X-2K Dura updates its memory address even if the address is invalid).
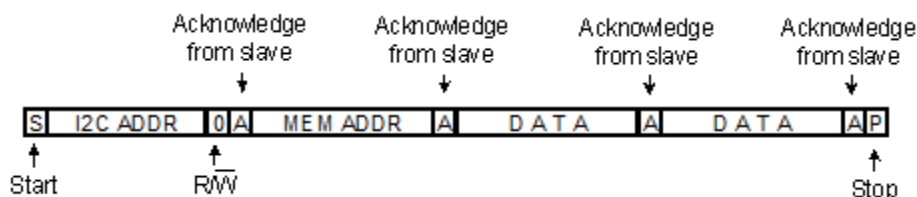
Figure 4 – One-word Monza® X-2K Dura write transaction

Figure 5 shows a read transaction. The read starts from the stored address. Monza® X-2K Dura increments the address as it sends each data byte. Monza® X-2K Dura ignores the MSB of the memory address when the R/W==1.
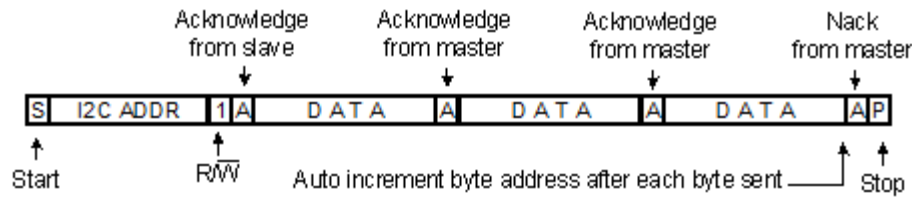
Figure 5 – Monza® X-2K Dura read transaction

Reads start from the stored address and continue to the end of memory, at which point Monza® X-2K Dura will cease exchanging data over I2C. Monza® X-2K Dura will send all ones if the master continues to read beyond the end of the memory. To read from a new location the master must send a new address. The master may halt the read at a byte boundary and later initiate a new read transaction starting from that byte. For completeness the combined write transaction then read transaction is shown in Figure 6.

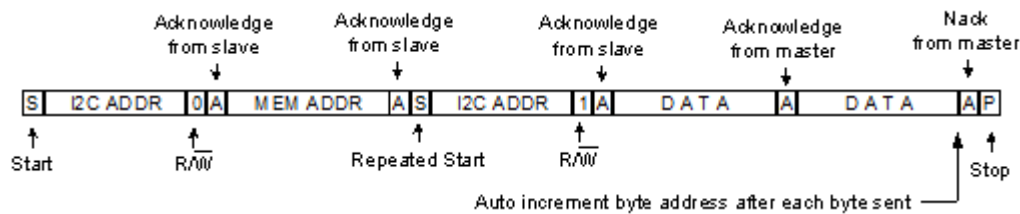**Figure 6 – Write transaction to set address followed by repeated start and read transaction.**

Monza® X-2K Dura ignores all Gen2 Lock, Kill permissions when reading / writing over I2C. The I2C port has read access to the entire NVM. The I2C port has write access to most, but not all, of the NVM. Monza® X-2K Dura precludes a master from writing its manufacturing calibration fields (shown as Reserved in the I2C memory map of Figure 7); these locations are read-only.

2.4   I2C Memory Map

Gen 2 and I2C have different views on how a memory map is organized. In I2C everything is done according to bytes. One uses byte addressing, byte writing, and byte reading. In Gen2 things are done in terms of bits or 16 bit words.

Monza® X-2K Dura is a hybrid of these two approaches. It forces I2C to do one word or two word writes, but allows for byte wise reading and addressing. When reading via I2C the first bit read is always bit seven within the byte. The next byte read is at the next higher I2C byte address. The I2C memory map in byte wise format is shown in Figure 7.

An additional memory map that shows bit addressing from I2C in a word wise format is shown in Figure 8.

MEMORY BANK	I2C BYTE ADDR	BIT NUMBER IN BYTE								I2C PERM
		7	6	5	4	3	2	1	0	
TID (10$_2$)	335	TID_SERIAL (Byte 1)								R
	334	TID_SERIAL (Byte 0)								R
	333	0x00								R
	332	0x20								R
	331	TID_MODEL [7 : 0] =01000000$_2$								R
	330	TID_DESIGNER [3 : 0] = 0001$_2$				TID_MODEL [11 : 8] = 0001$_2$				R
	329	XTID = 1	TID_DESIGNER [10 : 4] = 0000000$_2$ (Gen2 mask designer is address 08$_h$ to 13$_h$)							R
	328	CLASS_ID [7 : 0] = 11100010$_2$								R
	327	QT_EPC								R/W
	326	QT_EPC								R/W
	. . .	QT_EPC								R/W
	316	QT_EPC								R/W
	315	TID_SERIAL (Byte 5)								R
	314	TID_SERIAL (Byte 4)								R
	313	TID_SERIAL (Byte 3)								R
	312	TID_SERIAL (Byte 2)								R
User (11$_2$)	311	USER								R/W
	310	USER								R/W
	. . .	USER								R/W
	41	USER								R/W
	40	USER								R/W
EPC (01$_2$)	39	EPC								R/W
	38	EPC								R/W
	. . .	EPC								R/W
	24	EPC								R/W
	23	NSI [7 : 0]								R/W
	22	EPC_LENGTH [4 : 0]					UMI	XI = 0	NSI [8]	R/W
Reserved (00$_2$)	21	RFU = 0	WWU	BPL_EN	QT_SR	QT_MEM	DCI_RF_EN	RF_DIS [1 : 0]		R/W
	20	RFU (WRITE as 00000000$_2$)								R/W
	19	RESERVED								R
	. . .	RESERVED								R
	10	RESERVED								R
	9	BLOCK_PERMALOCK [0 : 4]					KILL	I2C_ADDR [1 : 0]		R/W
	8	LOCK_KILL [1 : 0]		LOCK_ACCESS [1 : 0]		LOCK_EPC [1 : 0]		LOCK_EPC [1 : 0]		R/W
	7	ACCESS_PASSWORD								R/W
	6	ACCESS_PASSWORD								R/W
	5	ACCESS_PASSWORD								R/W
	4	ACCESS_PASSWORD								R/W
	3	KILL_PASSWORD								R/W
	2	KILL_PASSWORD								R/W
	1	KILL_PASSWORD								R/W
	0	KILL_PASSWORD								R/W

Figure 7 – I2C Interface Memory Map in a Byte Wise format

Figure 8 – I2C Interface Memory Map in a Word Wise format

MEM BANK	MEM BANK BIT ADDR	BIT NUMBER (0 : F)	I2C PERM
User (11$_2$)	870$_h$-87F$_h$	USER [15 : 0]	R/W
	860$_h$-86F$_h$	USER [31 : 16]	R/W
	…	…	R/W
	10$_h$-1F$_h$	USER [2159 : 2144]	R/W
	00$_h$-0F$_h$	USER [2175 : 2160]	R/W
TID (10$_2$)	B0$_h$-BF$_h$	QT_EPC [15 : 0]	R/W
	A0$_h$-AF$_h$	QT_EPC [31 : 16]	R/W
	90$_h$-9F$_h$	QT_EPC [47 : 32]	R/W
	80$_h$-8F$_h$	QT_EPC [63 : 48]	R/W
	70$_h$-7F$_h$	QT_EPC [79 : 64]	R/W
	60$_h$-6F$_h$	QT_EPC [95 : 80]	R/W
	50$_h$-5F$_h$	TID_SERIAL [15 : 0]	R
	40$_h$-4F$_h$	TID_SERIAL [31 : 16]	R
	30$_h$-3F$_h$	TID_SERIAL [47 : 32]	R
	20$_h$-2F$_h$	TDTS [15 : 0] = 0x2000	R
	10$_h$-1F$_h$	[0:3] TID_DESIGNER [3 : 0] = 0001$_2$; [4:F] TID_MODEL [11 : 0] = 000101000000$_2$ (Gen2 model number is address 14$_h$ to 1F$_h$)	R
	00$_h$-0F$_h$	[0:7] CLASS_ID [7 : 0] = 11100010$_2$; [8] XTID = 1; [9:F] TID_DESIGNER [10 : 4] = 0000000$_2$ (Gen2 mask designer is address 08$_h$ to 13$_h$)	R
EPC (01$_2$)	90$_h$-9F$_h$	EPC [15 : 0]	R/W
	80$_h$-8F$_h$	EPC [31 : 16]	R/W
	…	…	R/W
	30$_h$-3F$_h$	EPC [111 : 96]	R/W
	20$_h$-2F$_h$	EPC [127 : 112]	R/W
	10$_h$-1F$_h$	[0:4] EPC_LENGTH [4 : 0]; [5] UMI; [6] XI = 0; [7:F] NSI [8 : 0] (Numbering System Identifier, default 000000000$_2$)	R/W
	00$_h$-0F$_h$	EPC_CRC [15 : 0]	R
Reserved (00$_2$)	A0$_h$-AF$_h$	[0:8] RFU = 0; [9] WWU; [A] BPL_EN; [B] QT_SR; [C] QT_MEM; [D] DCI_RF_EN; [E:F] RF_DIS [1 : 0]	R/W
	90$_h$-9F$_h$	RESERVED	R
	80$_h$-8F$_h$	RESERVED	R
	70$_h$-7F$_h$	RESERVED	R
	60$_h$-6F$_h$	RESERVED	R
	50$_h$-5F$_h$	RESERVED	R
	40$_h$-4F$_h$	[0:1] LOCK_KILL [1 : 0]; [2:3] LOCK_ACCESS [1 : 0]; [4:5] LOCK_EPC [1 : 0]; [6:7] LOCK_USER [1 : 0]; [8:C] BLOCK_PERMALOCK [0 : 4]; [D] KILL; [E:F] I2C_ADDR [1 : 0]	R/W
	30$_h$-3F$_h$	ACCESS_PASSWORD [15 : 0]	R/W
	20$_h$-2F$_h$	ACCESS_PASSWORD [31 : 16]	R/W
	10$_h$-1F$_h$	KILL_PASSWORD [15 : 0]	R/W
	00$_h$-0F$_h$	KILL_PASSWORD [31 : 16]	R/W

2.5   I2C Control of Monza® X-2K Dura Behavior

The I2C interface can control Monza® X-2K Dura behavior by writing to bytes 8 or 9, 20 or 21, and 22 or 23. The following sections describe how control bits in these words change the behavior.

2.6   Monza® X-2K Dura I2C and Gen2 Lock Bits

The lock bits for the kill password (LOCK_KILL[1:0]), the access password LOCK_ACCESS[1:0]), the EPC memory bank (LOCK_EPC[1:0]), and the USER memory bank (LOCK_ USER[1:0]) are in byte eight of memory. In each of these lock bit pairs bit one corresponds to pwd-write or pwd-read/write and bit zero corresponds to the permalock bit. Note that the I2C can always change the state of these bits and that their permissions only apply to the RF Gen2 interface.

Table 2.1 – *Lock* Bit-field functionality for EPC and User memory banks

PWD-WRITE	PERMALOCK	DESCRIPTION
0	0	Associated memory bank is writeable from either the **open** or **secured** states.
0	1	Associated memory bank is permanently writeable from either the **open** or **secured** states and may never be locked.
1	0	Associated memory bank is writeable from the **secured** state but not from the **open** state.
1	1	Associated memory bank is not writeable from any state.

Table 2.2 – *Lock* Bit-field functionality for Access and Kill passwords

PWD-READ/WRITE	PERMALOCK	DESCRIPTION
0	0	Associated password location is readable and writeable from either the **open** or **secured** states.
0	1	Associated password location is permanently readable and writeable from either the **open** or **secured** states and may never be locked.
1	0	Associated password location is readable and writeable from the **secured** state but not from the **open** state.
1	1	Associated password location is not readable or writeable from any state.

2.7   Monza® X-2K Dura I2C and Gen2 BlockPermalock

Monza® X-2K Dura will segments user memory into five blocks. Blocks zero through four may be blockpermalocked from either the Gen2 interface or the I2C interface. A blockpermalocked block allows reads but not writes to the block. Blockpermalocking is permanent for blocks one through four and may not be unlocked from either interface. The blockpermalock may be undone for block zero from the I2C interface and I2C ignores the blockpermalock permission for block zero.

The five blocks as seen from the I2C interface are shown in Figure 9. The five blocks in the User memory bank as seen from the Gen2 interface are:

- Block 0: bit address 0 to bit address 511 (512 bit block size)
- Block 1: bit address 512 to bit address 1023 (512 bit block size)
- Block 2: bit address 1024 to bit address 1535 (512 bit block size)
- Block 3: bit address 1536 to bit address 2047 (512 bit block size)
- Block 4: bit address 2048 to bit address 2175 (128 bit block size)

Please see the Gen2 specification for details on how a reader may lock the memory via *BlockPermalock* command.

The mechanism for a microprocessor permalocking over I2C is as follows: Execute a one-word (2 byte) write to bytes eight and nine (word address four). There are five blockpermalock bits in byte nine that control the write permission to the five user-memory blocks. Monza® X-2K Dura will bitwise OR each of the current permalock bits with the four bits corresponding to blocks one through four and write the updated word into NVM. Block zero may be unlocked via the I2C interface. Monza® X-2K Dura does not allow unlocking of blockpermalocked memory in blocks one through four via either the Gen2 interface or I2C interface.

To control the Gen2 interface access to the *BlockPermalock* command the I2C interface will have a *BlockPermalock* command enable bit that only it can write to. When the bit is set Monza® X-2K Dura will execute valid *BlockPermalock* commands and when it is cleared it will ignore all *BlockPermalock* commands. The location of the BPL_EN bit is in bit five of byte 21.

MEMORY BANK	I2C BYTE ADDR	BIT NUMBER IN BYTE								I2C BLOCK PERMA LOCKABLE	GEN2 BLOCK PERMA LOCKABLE
		7	6	5	4	3	2	1	0		
User (11$_2$)	311	USER (Block 4)								Yes	Yes
	. . .	USER (Block 4)								Yes	Yes
	296	USER (Block 4)								Yes	Yes
	295	USER (Block 3)								Yes	Yes
	. . .	USER (Block 3)								Yes	Yes
	233	USER (Block 3)								Yes	Yes
	232	USER (Block 3)								Yes	Yes
	231	USER (Block 2)								Yes	Yes
	. . .	USER (Block 2)								Yes	Yes
	169	USER (Block 2)								Yes	Yes
	168	USER (Block 2)								Yes	Yes
	167	USER (Block 1)								Yes	Yes
	. . .	USER (Block 1)								Yes	Yes
	105	USER (Block 1)								Yes	Yes
	104	USER (Block 1)								Yes	Yes
	103	USER (Block 0)								No	Yes
	. . .	USER (Block 0)								No	Yes
	41	USER (Block 0)								No	Yes
	40	USER (Block 0)								No	Yes

Figure 9 – BlockPermalock blocks as seen from the I2C interface

2.8 Monza® X-2K Dura I2C Control of I2C_ADDR[1:0] Bits

The I2C_ADDR[1:0] bits in byte 9 contain the I2C device address bits D2 and D1 respectively. These bits are meant to be reconfigurable in order to avoid address conflicts on the I2C bus, allowing four different address possibilities. These bits are configurable only via I2C, not RF. The factory default value for these bits is 11$_b$, corresponding to a default I2C slave address of 1101**110**$_b$.

2.9 Monza® X-2K Dura Control of the QT Function

The QT_SR and QT_MEM bits control in byte 21 control the QT functionality of Monza® X-2K Dura. They have no effect on I2C operation and only change RF Gen2 behavior. The two bits operate independently from each other. The QT_SR bit turns on Monza® X-2K Dura's short range mode when it is set. When Monza® X-2K Dura is in short range, operations in OPEN or SECURED states are required to be close to the reader. Note, however, that if the Monza® X-2K Dura antenna has a gain < -9dBi, there will be no

OPEN or SECURED access through the RF port when the QT_SR bit is set. The QT_MEM bit controls how Monza® X-2K Dura's memory appears to the Gen2 interface. When the bit is set Monza® X-2K Dura is in public mode: user memory bank is hidden, TID serialization is hidden, and uses its QT_EPC in the EPC bank. When the bit is cleared Monza® X-2K Dura is in private mode and all of its memory is exposed. The memory map in

MEM BANK	MEM BANK BIT ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	GEN2 PERM
User (11₂)	870h-87Fh	USER [15 : 0]																R/W
	860h-86Fh	USER [31 : 16]																R/W
	…	…																R/W
	10h-1Fh	USER [2159 : 2144]																R/W
	00h-0Fh	USER [2175 : 2160]																R/W
TID (10₂)	B0h-BFh	QT_EPC [15 : 0]																R/W
	A0h-AFh	QT_EPC [31 : 16]																R/W
	90h-9Fh	QT_EPC [47 : 32]																R/W
	80h-8Fh	QT_EPC [63 : 48]																R/W
	70h-7Fh	QT_EPC [79 : 64]																R/W
	60h-6Fh	QT_EPC [95 : 80]																R/W
	50h-5Fh	TID_SERIAL [15 : 0]																R
	40h-4Fh	TID_SERIAL [31 : 16]																R
	30h-3Fh	TID_SERIAL [47 : 32]																R
	20h-2Fh	TDTS [15 : 0] = 0x2000																R
	10h-1Fh	TID_DESIGNER [3 : 0] = 0001₂				TID_MODEL [11 : 0] = 000101000000₂ (Gen2 model number is address 14h to 1Fh)												R
	00h-0Fh	CLASS_ID [7 : 0] = 11100010₂								XTID = 1	TID_DESIGNER [10 : 4] = 0000000₂ (Gen2 mask designer is address 08h to 13h)							R
EPC (01₂)	90h-9Fh	EPC [15 : 0]																R/W
	80h-8Fh	EPC [31 : 16]																R/W
	…	…																R/W
	30h-3Fh	EPC [111 : 96]																R/W
	20h-2Fh	EPC [127 : 112]																R/W
	10h-1Fh	EPC_LENGTH [4 : 0]					UMI	XI = 0	NSI [8 : 0] (Numbering System Identifier, default 000000000₂)										R/W
	00h-0Fh	EPC_CRC [15 : 0]																R
Reserved (00₂)	A0h-AFh	RFU = 0									WWU	BPL_EN	QT_SR	QT_MEM	DCI_RF_EN	RF_DIS [1 : 0]			R
	90h-9Fh	RESERVED																R
	80h-8Fh	RESERVED																R
	70h-7Fh	RESERVED																R
	60h-6Fh	RESERVED																R
	50h-5Fh	RESERVED																R
	40h-4Fh	LOCK_KILL [1 : 0]		LOCK_ACCESS [1 : 0]		LOCK_EPC [1 : 0]		LOCK_USER [1 : 0]		BLOCK_PERMALOCK [0 : 4]					KILL	I2C_ADDR [1 : 0]		R
	30h-3Fh	ACCESS_PASSWORD [15 : 0]																R/W
	20h-2Fh	ACCESS_PASSWORD [31 : 16]																R/W
	10h-1Fh	KILL_PASSWORD [15 : 0]																R/W
	00h-0Fh	KILL_PASSWORD [31 : 16]																R/W

Figure 2 shows the Monza® X-2K Dura memory in private mode.

2.10 Monza® X-2K Dura I2C Control of Gen2 Response to Ack Command

The length field in byte 22 may be written from I2C. The length field specifies the number of words backscattered in response to a Gen2 *Ack* command. Byte 22 also contains an NVM space for the UMI bit which may be read or written from I2C. The NVM bit is not used since it is automatically calculated per the Gen2 specification. The Gen2 UMI bit is calculated from the bitwise or of bits 4 through 0 in byte 40.

2.11 RF Access Control

Monza® X-2K Dura provides three levels of control over RF access as follows:

1. Setting either or both the RF1_DIS or RF2_DIS bits in byte 21 of the NVM disables RF access on the corresponding RF port. These bits are configurable only via I2C, not RF. The factory defaults are 0, enabling RF1 and RF2.

2. Setting the DCI_RF_EN bit to 0 in byte 21 of the NVM inhibits all RF access when DCI voltage is present. This takes precedence over the state of the RF1_DIS, RF2_DIS bit in #1 above. This bit is also only configurable from I2C, not RF. This bit is set by factory default to 0. Thus, by default, there is RF access to RF1, RF2 when DCI voltage is NOT present and no RF access when DCI voltage is present. The specification V_{RFON} determines the DCI voltage that inhibits RF.

3. Setting the KILL bit 2 in byte 9 of the NVM will inhibit all RF access. This bit can be set from RF using a Gen2 KILL command or by writing from I2C. This is the normal mechanism for a reader to disable a chip. This KILL bit takes precedence over both #1 and #2 above. I2C can re-write this bit back to 0 and thus reverse and RF KILL command. The factory default for KILL is 0.

The factories defaults are set so Monza® X-2K Dura operates like any other RFID tag when DCI voltage is not present. When DCI voltage is present the default behavior, through mechanism #2 above, is to inhibit all RF access. The KILL bit is always set to 0 at the factory by Gen2 definition. In conventional RFID chips once this bit is set to 1 a chip is dead and can never be resurrected. Monza® X-2K Dura, having a hard wired I2C interface, allows un-doing the KILL operation from I2C.

2.12 Gen2/I2C Arbitration

If the DCI_RF_EN bit is set to one then Monza® X-2K Dura has three different operating states as shown in Figure 10. The states are "*Internal Control*", "*I2C Control*", and "*Idle or RF Receive*". If the DCI_RF_EN bit is set to zero then Monza® X-2K Dura will not respond to RF commands when in the *Idle or RF Receive* state.

Internal Control: Monza® X-2K Dura is in *Internal Control* when (1) executing an initialization sequence, (2) writing the NVM or (3) backscattering a response to an RF command. When in *Internal Control* Monza® X-2K Dura ignores I2C transactions or RF commands.

I2C Control: Monza® X-2K Dura is in *I2C Control* when a master is issuing commands to Monza® X-2K Dura over the I2C bus. I2C Control starts when Monza® X-2K Dura detects a matching device ID and is not under *Internal Control*. The I2C bus master releases control of Monza® X-2K Dura either by ending a transaction with a stop bit or by issuing a subsequent start with a non-matching device ID. If Monza® X-2K Dura was commanded to perform an NVM write then it moves to *Internal Control*, otherwise it returns to idle. When in *I2C Control* Monza® X-2K Dura ignores all RF commands. Note that the master may stall the I2C bus (by holding SCL low) in the middle of a transaction and prevent RF access until releasing the bus.

Idle or RF Receive: Monza® X-2K Dura is in *Idle or RF Receive* when receiving an RF command or when idle. After receiving a command Monza® X-2K Dura transitions to *Internal Control* to execute the command. Executing a command may cause Monza® X-2K Dura to (1) backscatter a reply (2) write to NVM or (3) change internal states. An I2C transaction may interrupt Monza® X-2K Dura in *Idle or RF Receive*– by this means the I2C port exercises priority over the RF port and may not be locked out. Note that I2C is locked out when Monza® X-2K Dura transitions to *Internal Control* to execute the command.

In certain operating states and under certain conditions Monza® X-2K Dura may appear unresponsive to an I2C master for up to 20 milliseconds (During a slow Gen2 backscatter). This datasheet recommends that an I2C master have a retry algorithm that can accommodate Monza® X-2K Dura being busy.
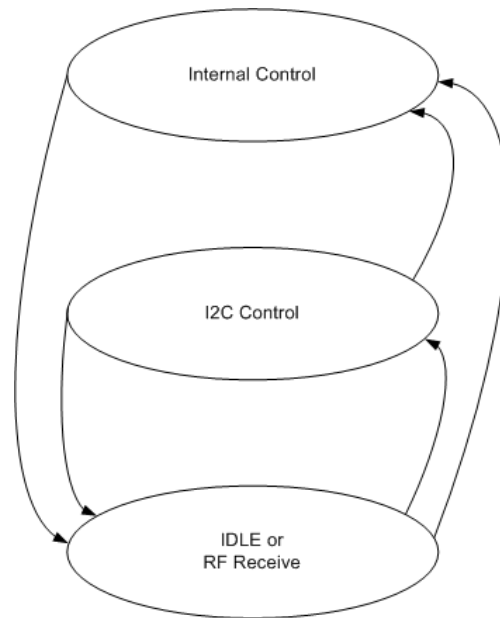
Figure 10 – Monza® X-2K Dura operating states

2.13 Write Wakeup Mode

Monza® X-2K Dura has a wake up feature that is tied to writes being performed over the Gen2 interface. In order to enable this feature the I2C master must set the WWU bit (bit 6 of byte 21) to one. Then the master must set the Monza® X-2K Dura's DCI pin to 0V (Sleep mode). The SCL and SDA lines must remain high, but draw no current. A reader may continue to interact with Monza® X-2K Dura on the RF ports. If a reader performs a write operation, and the wake up mode is set, Monza® X-2K Dura will assert the SCL I/O pulling the SCL line low for the duration of the write operation, approximately 4ms. This transition may then be detected by the sleeping master and used to wake up the system.
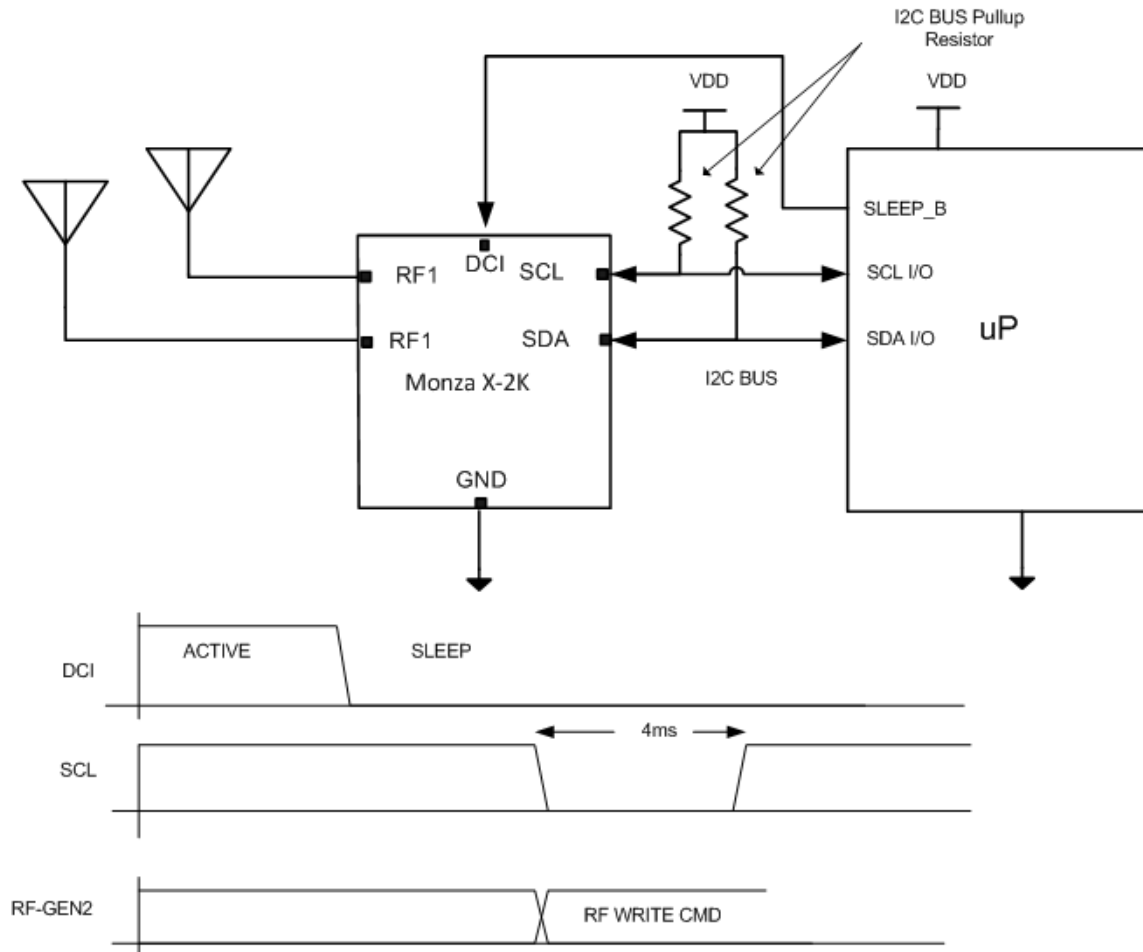
Figure 11 – Monza® X-2K Dura write wake up mode schematic and timing diagram

3 CHIP CHARACTERISTICS

3.1 Physical Characteristics

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
IC package	Chip package	All	XQFN 8L 1.65×1.65×0.35mm				
Pin count	Package pins	All		8		pins	2 – Port1 RF+/– 2 – Port2 RF+/– 2 – DCI/gnd 2 – I2C(SDA/SCL)

SYMBOL	MIN.	NOM.	MAX.
A	0.30	0.325	0.35
A1	0.00	0.02	0.05
A3		0.127 REF	
b	0.15	0.20	0.25
D	1.55	1.60	1.65
E	1.55	1.60	1.65
e		0.55 BSC	
e1		0.50 BSC	
e2		0.60 BSC	
L	0.25	0.30	0.35
L1	0.05	–	0.15

Notes:
1. All dimensions are in millimeter.
2. Max. package warpage is 0.05mm.
3. Maximum allowabe burrs is 0.076mm in all di
4. Pin #1 ID on top will be laser/ink marked.
5. Dimension applies to metalized terminal and
   between 0.20 and 0.25mm from terminal tip.
6. Applied only for terminals.
7. Applied for exposed pad and terminals.
8. Refer JEDEC MO-255.
9. Exposed pad finish NiPdAu.

Tolerances:
aaa = 0.1 (Coplanarity top surface)
bbb = 0.1 (Position lead)
ccc = 0.05 (Parallelism top & bottom)
ddd = 0.05 (Position lead)
eee = 0.05 (Coplanarity bottom surface)

Figure 12– Packing Dimensions

3.2　Absolute Maximum Ratings

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
Absolute maximum pin voltage	Absolute maximum voltage on any chip pin	All except DCI	–0.3		4.1	V	From the I2C spec, the max DC voltage is 3.3V+20% (max operating voltage) + 0.5V for survivability
ESD		HBM	2			kV	
		CDM	500			V	
Operating Temperature	Temperature for full specified performance		-25		+85	°C	See Read/Write Sensitivity for temperature ranges in Section 3.4
Persistence Temperature	Temperature for Gen2 flag persistence		-25		+40	°C	As per the Gen2 v.1.2.0 specification for flag persistence
Storage temperature	Temperature for 10-yr NVM retention		–40		+85	°C	See Impinj's NVM usage model
Assembly survival temp	Temperature for reflow soldering / assembly				+260	°C	Peak temp of JEDEC-MO255 for lead free soldering
Moisture Sensitivity Level	Moisture/Reflow Sensitivity Classification			MSL 1			According to IPC/JEDEC's J-STD-20

3.3   Reflow Temperature Profile

t=1493 y=261.52
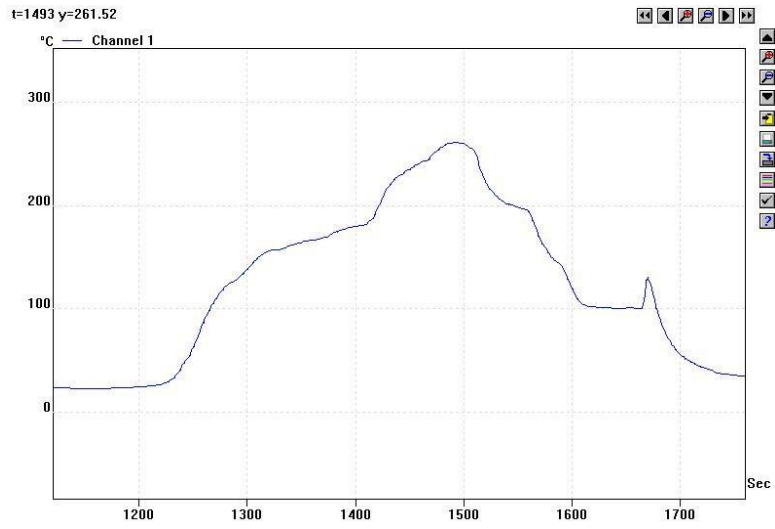
3.4   Electrical Characteristics

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
RF Performance							
S$_{READ}$	Matched RF Input Read Sensitivity DRM, M=4	No DC Input		-17		dBm	Using DC Input, Monza X-2K Dura can be used in Battery Assisted Passive mode to increase read/write range
		With DC Input at 0°C to +85°C		-24		dBm	
		With DC Input at 0°C to -25°C		-20		dBm	
S$_{WRITE}$	Matched RF Input Write Sensitivity DRM, M=4	No DC Input		−12		dBm	
		With DC Input at 0°C to +85°C		-24		dBm	
		With DC Input at 0°C to -25°C		-20		dBm	
Rp	Parallel Equivalent Real Input Impedance	At Sensitivity		1600		Ohms	
Cp	Parallel Equivalent RF Input Capacitance			1		pF	

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
POWER							
V_{DCI}	DCI Input Voltage/I2C Reference		1.6		3.6	V	These DCI voltages are with a ±100mV tolerance
I_{DCW}	Current drawn by chip during write	$1.6<V_{DCI}<2.0$		100	200	µA	Nominal 80uA at 1.6V
		$2.0<V_{DCI}<3.6$		140	220		
I_{DCI}	Current drawn by chip during read or idle	$1.6<V_{DCI}<2.0$		15	30	µA	
		$2.0<V_{DCI}<3.6$		20	40		
T_{PU}	Power Up Time. Time from V_{DCI} applied until I2C accepts transactions.	$V_{DCI}=1.6V$			2	ms	NOTE: I2C will not interrupt a write operation. This could delay I2C access up to 20ms if RF is writing.
V_{RF_EN}	Max Vdd for which RF will always be enabled				0.25	V	Applies if the DCI_RF_EN bit is set to 0.
V_{RF_DIS}	Min Vdd for which RF will always be disabled						

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
I2C							
V_{IH}	HIGH-level input voltage	All	70%			%V_{DCI}	
V_{IL}	LOW-level input voltage	All			30%	%V_{DCI}	From the section 6 of the I2Cspecification
V_{HYS}	Input hysteresis	All	0.1			V	
I_{OL}	LOW-level output current	V_{OL}=0.4	3[**]			mA	
T_{OF}	Output Fall Time	Bus C= 40-400pf	20		250	ns	
C_I	Pin Capacitance				10	pF	Total capacitive load on the SDA/SCL pins
I_{IL}	SCL/SDA Input Leakage Current	Vin=3.7V 0V<V_{DCI}<3.7V		1	100	nA	Within I2C spec limit of 10uA

[**]I_{OL} is tested with worst case minimum pull-up resistance value of 536 ohms at 2v. Applications should use as high pull-up resistance as possible consistent with the bus capacitance for the application. See the I2C specification for choosing pull-up resistor values.   Values of 5K or more are typical in low power applications

3.5 Memory Characteristics

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
EPC memory	EPC NVM	In private mode only		128		bits	User writeable. This memory is hidden over RF when QT is enabled.
User memory	Total user NVM	In private mode only		2176		bits	User defined memory space. This memory is hidden over RF when QT is enabled
QT alternative EPC	Alternative EPC presented during RF singulation	In public mode only		96		bits	A user can switch the tag's RF QUERY–ACK response from EPC to alternative EPC using the QT command
Kill/Access Passwords	Password NVM	Access required		64		bits	Standard 32-bit Gen2 access and kill passwords
TID mfg#/serial#	TID ROM	In private mode only		96		bits	TID serial number is hidden over RF when QT is enabled
Total Memory	Total memory size			2560		bits	
T$_{WRITE}$	Memory write time 16 or 32 bits			4.7	5	ms	

3.6   RF Functionality

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
Air protocol	Gen2 V1.2.0	All					No recommissioning; no blockerase
RF ports	Number of RF ports	All		2			Dual-differential RF ports
RF Port Disable	NVM Settable bit per port						The operation of one or both RF ports may be disabled by setting NVM bits through the I2Cport
DC Blocks RF	NVM Settable bit						Option to allow the presence of DC to disable both RF ports

3.7 I2C Characteristics

PARAMETER	DESCRIPTION	CONDITION	MIN	NOM	MAX	UNITS	COMMENTS
I2C port	Number of ports	All			1		Slave I2C (SCL/SDA)
I2C functionality	Compatible with I2C-bus specification and user manual Rev. 03 – 19 June 2007	All		R/W			An external device can R/W memory
Supported I2C features	**Features:** **Slave Configuration** Start condition mandatory Stop condition mandatory Acknowledge mandatory 7-bit slave address mandatory						
I2Cwrite size	Word size for I2C write	All	16		32	bits	Writes are on word addresses and not byte addresses
I2C read size	Word size for I2C read	All		N×8		bits	May read data 8bits at a time, where N is limited by start address and bank size
I2C memory arbitration	RF/I2C port priority	All		1st			RF/I2C arbitrate for NVM access
I2C Address	I2C Device Address	All		1101XXM[1]			XX is I2C_ADDR[1:0]
Transfer rates	I2C transfer data rates	All	0		400	kbps	I2C fast mode

[1]Monza(R) X-2K Dura operates like most I2C EEPROM devices in that the LSB of the 7-bit I2C device address is the MSB of the NVM address. The 8 LSBs of the NVM address are sent in the next I2C byte.

3.8   NVM Usage Model

Rows are 32 bits long on even word boundaries (ie, words 0 and 1 are row 0 for user memory).

MAXIMUM CONDITION			RETENTION (YEARS)
Writes per row	Total writes	Power-on time	
10	100	5 yr	50
1k	10k	1 yr	10
10k	100k	2k hours	1

3.9   Environmental Compliance

REQUIREMENT	COMMENTS
RoHS	Monza X-2K Dura is RoHS compliant. It meets the directive 2002/95/EC (RoHS). RoHS declaration letter is available upon request.
REACH	Monza X-2K Dura does not, to our current knowledge, contain substances above the legal threshold that are on the Candidate List of Substances of Very High Concern (SVHC). Our company's intention is that all products sold to our EU and EEA customers by our legal entities in Europe are compliant with REACH regulatory requirements. REACH declaration letter is available upon request.

4   PRODUCT DELIVERY SPECIFICATIONS

4.1   Marking Specification
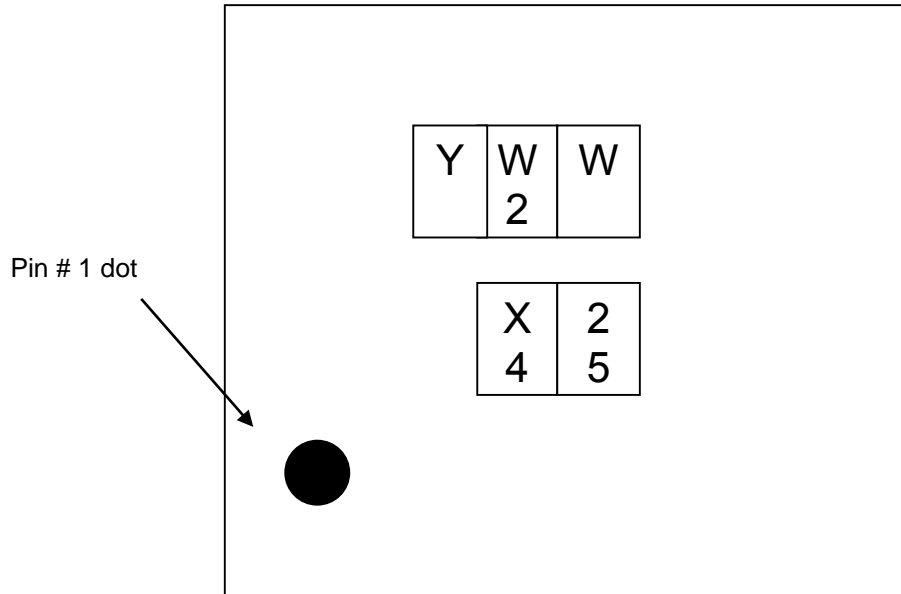
Y= Year of production (1 = 2011, 2 = 2012 …)

WW = Work Week of production

X2 = Product Code (Monza X-2K Dura)

4.2 Tape and Reel Specification
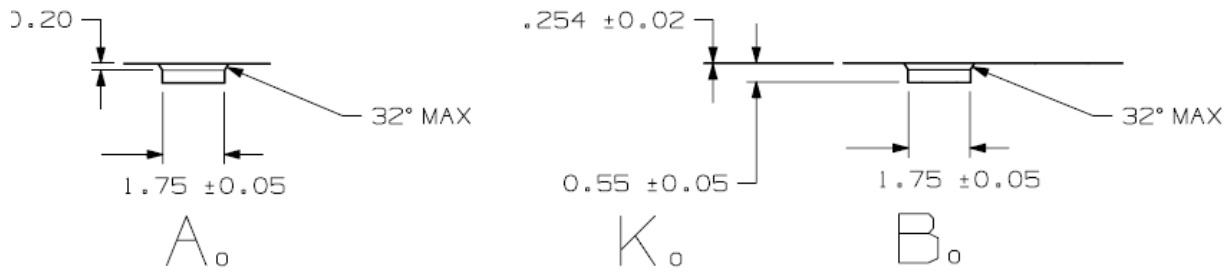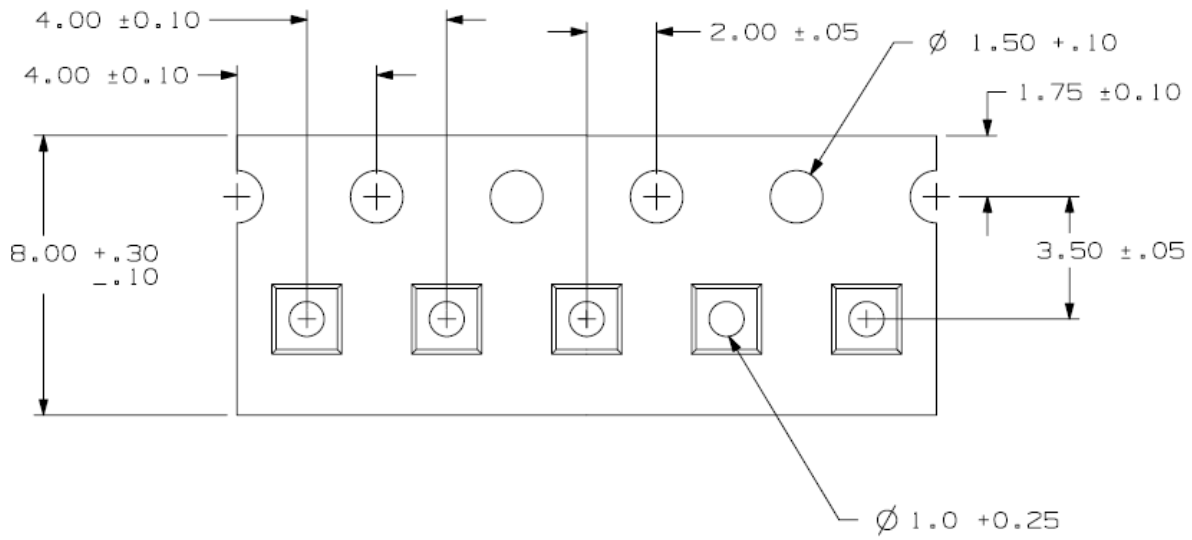
Parts per reel / Minimum order quantity: 3000

5   ERRATA

The following table lists the known issues in Monza® X-2K Dura

ISSUE NUMBER	DESCRIPTION
1	When writing from the I2C block the cache for the PC length field is not properly updated after I2C writes. The part must be power cycled to have the cache updated.
2	If QT features are changed from I2C, then the changes don't take effect until power is cycled. Specifically, Monza® X-2K Dura does not recache the QT_MEM (1 = Monza® X-2K Dura is using the alternate EPC) or QT_SR (1 = tag is in short range) when written from I2C. It needs to be power cycled for the change to take effect.

6   FOOTPRINT COMPATIBILITY WITH IMPINJ® MONZA® X-2K DURA

Monza® X-8K Dura (Part Order#: IPJ-P6005-X2AT) is a higher memory capacity version of Monza® X-2K Dura.

Monza® X-8K Dura is designed to have 8192 bits of user NVM, enabling more OTP blocks. Its package dimensions are 2.0x2.0x0.35 mm. It is designed to be a drop-in replacement for Monza X-2K Dura if the layout footprint recommended below is used. For more details about the Monza® X-8K Dura including product availability, please contact Impinj.
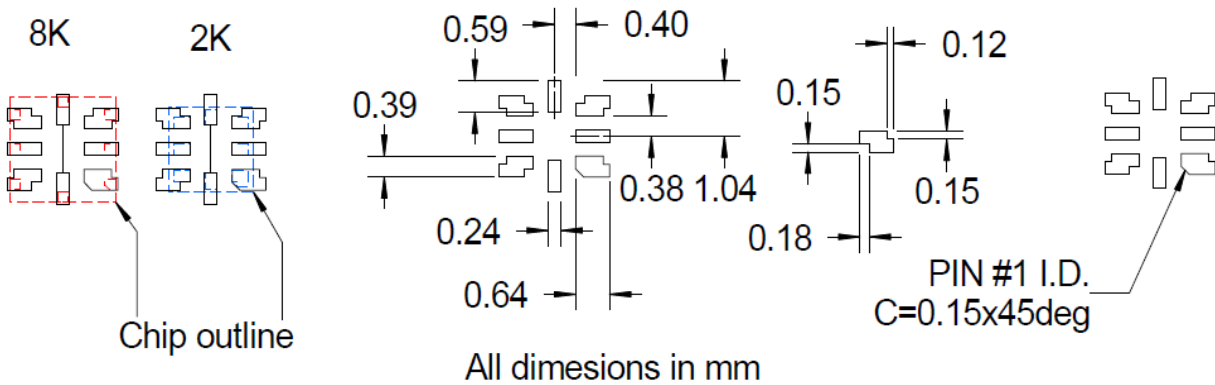
Figure 13 – Recommended common layout footprint for Monza® X-2K Dura and Monza® X-8K Dura

7 ORDERING INFORMATION

Contact sales@impinj.com for ordering support.

MODEL	PART NUMBER	USER MEMORY	PACKAGE SIZE
Monza X-2K Dura	IPJ-P6001-Q2AT	2,176 bits	1.6 x 1.6 x 0.35 mm
Monza X-8K Dura	IPJ-P6005-X2AT	8,192 bits	2.0 x 2.0 x 0.35 mm

8 NOTICES

Impinj gives no representation or warranty, express or implied, for accuracy or reliability of information in this document. Impinj reserves the right to change its products and services and this information at any time without notice.

EXCEPT AS PROVIDED IN IMPINJ'S TERMS AND CONDITIONS OF SALE (OR AS OTHERWISE AGREED IN A VALID WRITTEN INDIVIDUAL AGREEMENTWITH IMPINJ), IMPINJ ASSUMES NO LIABILITY WHATSOEVER AND IMPINJ DISCLAIMS ANY EXPRESS OR IMPLIEDWARRANTY, RELATED TO SALE AND/OR USE OF IMPINJ PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE,MERCHANTABILITY,OR INFRINGEMENT.

NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY PATENT, COPYRIGHT, MASKWORK RIGHT, OR OTHER INTELLECTUALPROPERTY RIGHT IS GRANTED BY THIS DOCUMENT.

Impinj assumes no liability for applications assistance or customer product design. Customers should provide adequate design and operating safeguards to minimize risks.

Impinj products are not designed, warranted or authorized for use in any product or application where a malfunction may reasonably be expected to cause personal injury or death, or property or environmental damage ("hazardous uses"), including but not limited to military applications; life-support systems; aircraft control, navigation or communication; air-traffic management; or in the design, construction, operation, or maintenance of a nuclear facility. Customers must indemnify Impinj against any damages arising out of the use of Impinj products in any hazardous uses.

Trademarks

Impinj, Monza, Speedway, xArray are trademarks or registered trademarks of Impinj, Inc. All other product or service names are trademarks of their respective companies. For a complete list of Impinj Trademarks visit: www.impinj.com/trademarks.

Patents

The products referenced in this document may be covered by one or more U.S. patents. See www.impinj.com/patents for details.