Datasheet

IMPINJ M830/M850 SERIES TAG CHIPS

TAG CHIP DATASHEET

IPJ-M830A-A00

IPJ-M850A-A00

Version 1.1

www.impinj.com

1 OVERVIEW

Impinj® M800 series RAIN RFID tag chips provide high performance, fast inventory capability, and advanced features for next-generation, universal RAIN RFID tags.

The Impinj M800 series includes the Impinj M830 and M850 tag chips which can be attached to or embedded in nearly any item, anywhere in the world, to enable solutions for enterprise use case challenges and to open new possibilities in retail and supply chain applications. The Impinj M800 series' leading-edge performance extends tag read range and enables connectivity of small retail merchandise such as jewelry and cosmetics and enhancing the efficiency of package and asset tracking applications. With new improvements to Impinj AutoTune™ adaptive tuning and unmatched readability, the Impinj M830 and M850 boost performance for small tag designs to meet enterprise performance requirements, making them truly universal tag chips that simplify retail and supply chain RAIN deployments. Additionally, the new Impinj Enduro™ V2 bonding pads strengthen tag chip adhesive bonding, providing optimal mechanical stability, assembly consistency, and manufacturing reliability for inlays, leading to outstanding durability over the lifespan of a tag. The Impinj M800 series sets the standard in RAIN RFID innovation, building upon trusted and proven Impinj technology while introducing new capabilities to help users tag more items, read them from farther away, and expand IoT connectivity.

The Impinj M830 and M850 tag chips are distinguished by the amount of EPC and user memory available, as shown in the summary section below. These Impinj tag chips provide increased sensitivity, improved readability, advanced features, and are compatible with the global GS1 UHF Gen2v2 standard which ISO/IEC standardized as 18000-63.

When combined with a next-generation reader like the Impinj R700 RAIN RFID reader, Impinj M800 series-based tags help to advance RAIN RFID performance at dock doors, conveyors, and store exits.

1.1 Specifications Summary

- Read sensitivity of up to -25.5 dBm with a dipole antenna
- Write sensitivity of up to -20 dBm with a dipole antenna
- 96 bits of Serialized TID with 48-bit serial number
- Two memory configuration options:
    - Impinj M830: 128 bits of EPC memory, 0 bits of user memory
    - Impinj M850: 96 bits of EPC memory, 32 bits of user memory
- Drop-in inlay compatibility between Impinj M700 and M800 series tag chips
- ISO/IEC 18000-63:2015 and EPCglobal Gen2v2 compliant

1.2 Features Summary

The Impinj platform lays a foundation for the development of IoT solutions, RAIN devices, and RAIN tags, extending the Internet's reach from the cloud, through edge connectivity devices, all the way to physical items. As part of the platform, Impinj uniquely provides patented features and technologies that extend the capabilities of a standardized RAIN system. These include: Impinj AutoTune V3, Enduro V2, FastID, Integra V2, MarginRead, Protected Mode, and TagFocus. Please see below for details about key features.

- **Impinj AutoTune™ V3 Adaptive RF Tuning** — Optimizes performance to the tag's environment for improved readability across different materials, tag form factors, and operating frequencies.
- **Impinj Integra™ V2 Memory Diagnostics** — Suite of diagnostics that verifies tag chip health and validates data encoding to consistently deliver more accurate data and reliable tags. This includes built-in memory error detection with parity checking applied throughout normal Gen2v2 operation.
- **Impinj Protected Mode** — Enables loss prevention and protects consumer privacy by making a tag invisible to RAIN readers. The tag can be returned to normal operation and made visible to readers using a secure password.

- **User-Selectable Memory Map** – Enables user to switch between M830 and M850 memory maps one time.
- **Short-Range Mode** — Decreases a tag's read range by >90% via the EPCglobal Gen2v2 *Untraceable* command.
- **Shared *Access* and *Kill* Passwords** — Protects tag memory blocks or permanently deactivates the tag.
- **Impinj Enduro™ V2 IC Bonding Technology** — Patented bonding pad design optimizes eco-friendly tag performance and delivers high-quality tags for improved tag yield, reliability, and durability.
- **Impinj TagFocus™ Read Redundancy Prevention** — Unique algorithm prevents multiple reads of the same chip so that hard-to-read tags can be read more accurately within a complex population of tags.
- **Impinj FastID™ High-Speed Reading** — Reduces inventory time by simplifying the tag-identification steps needed when using a TID-based numbering system.
- **Self-Serialization** — Scalable built-in serialization.

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2 INTRODUCTION

2.1 Scope

This datasheet defines the physical and logical specifications for EPCglobal Gen2-compliant Impinj M800 series tag chips, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

2.2 Reference Documents

The following reference documents were used to compile this datasheet:

- EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen2v2 Specification) Release 2.1, Jul 2018
    - The conventions used in the Gen2v2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this datasheet. Users of this datasheet should familiarize themselves with the Gen2v2 Specification.
- Impinj M830 and M850 Wafer Specification
- Impinj Wafer Map Orientation Guide
- TID Memory Maps for Impinj Monza Self-Serialization Application Note
- EPC™ Tag Data Standard (TDS) Release 2.0, Aug 2022
- Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices Release.2.0.1, Feb 2016

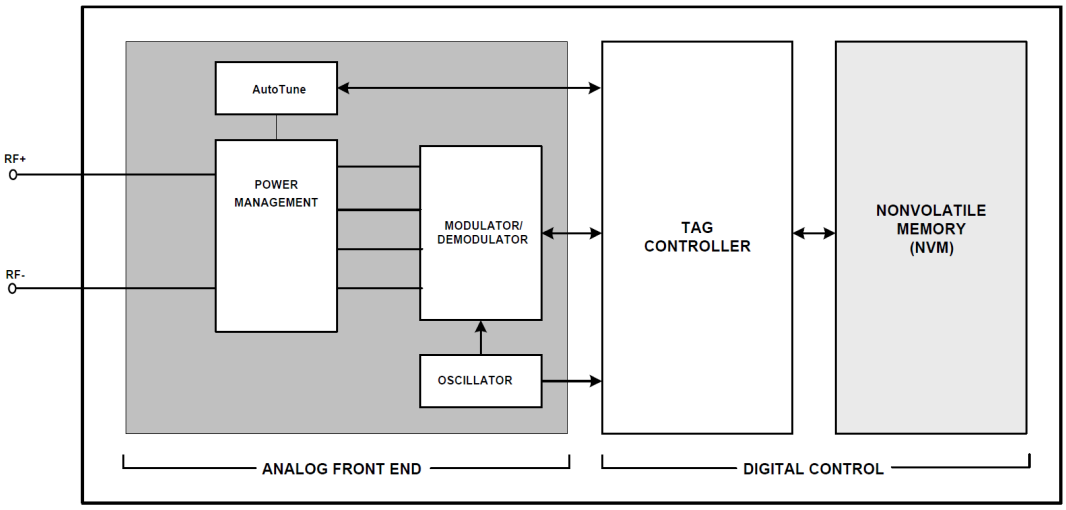
Consult these documents for more information about compliance standards and specifications.

3 FUNCTIONAL DESCRIPTION

The Impinj M800 series tag chips fully support all mandatory commands of the EPCglobal Gen2v2 specification as well as optional commands and features (see Support for Optional Gen2v2 Commands, section 3.2).

3.1 Impinj M800 Series Tag Chip Block Diagram

Figure 1: Block Diagram



3.1.1 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader's RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

3.1.2 Impinj AutoTune V3

The Impinj AutoTune V3 block adjusts Impinj M800 series tag chip power harvesting from the inlay antenna by adjusting the chip's input capacitance. The refined tuning algorithm improves symmetry around tag resonances and widens the dynamic range of the IC sensitivity across the entire 860-960 MHz UHF spectrum. Impinj AutoTune adjustment occurs at every IC power up and is held for the remainder of the time that the tag chip is powered. For information on how to read out the Impinj AutoTune values or configure this feature, refer to the Memory Map Selection section.

3.1.3 Modulator/Demodulator

The Impinj M800 series tag chips demodulate any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK with PIE encoding. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna ports between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

3.1.4 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that carries out command sequences and performs a number of overhead duties.

3.1.5 Nonvolatile Memory

The Impinj M800 series tag chip embedded memory is nonvolatile memory (NVM) cell technology, specifically optimized for RFID applications. All programming overhead circuitry is integrated on chip. Impinj M800 series tag chip NVM provides 10,000 write cycle endurance or 10-year data retention.

The memory write speed for Impinj M800 series is 2.9 ms per *Write*, *BlockWrite*, *Lock* or *Kill* operation, for writing up to 32 bits.

The NVM block is organized into three segments:

- EPC memory:
  - Impinj M830: 128 bits
  - Impinj M850: 96 bits
  - The Protocol-Control word contains an additional 9 programmable bits
- User memory:
  - Impinj M830: 0 bits
  - Impinj M850: 32 bits
- Reserved memory, which includes the shared access and kill passwords, and feature and chip control words

The ROM-based Tag Identification (TID) memory contains the EPCglobal class ID, the manufacturer identification, and the model number. It also contains an extended TID consisting of a 16-bit header and 48-bit serialization.

See Table 1 for the Impinj M800 series memory organization.

Table 1: Impinj M800 Series Memory Organization

Memory Section	Impinj M830	Impinj M850
EPC	128 bits	96 bits
User	0 bits	32 bits
TID (not changeable)	Serial Number – 48 bits	Serial Number – 48 bits
	Extended TID Header – 16 bits	Extended TID Header – 16 bits
	Company/Model Number – 32 bits	Company/Model Number – 32 bits
Reserved	Chip Configuration	Chip Configuration
	Kill Password – 32 bits, shared	Kill Password – 32 bits, shared
	Access Password – 32 bits, shared	Access Password – 32 bits, shared

3.2 Support for Optional Gen2v2 Commands

Impinj M800 series tag chips support the optional commands listed in Table 2. For further details on these commands, refer to the EPC™ Radio-Frequency Identity Protocols Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz (Gen2v2 Specification).

Table 2: Supported EPCglobal Gen2v2 Specification Commands

Command	Details
Access	• Supports full functionality of the Access command • Allows control of user access to write and/or lock the tag
BlockWrite	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code “Not supported” (00000001_2) if it receives a valid two-word command with an odd value pointer • Returns error code “Not supported” (00000001_2) if it receives a command for more than two words • Does not respond to BlockWrite commands of zero words
Lock	• Separately lockable EPC and User memory banks • Lockable access and kill password – these passwords share the same lock status and cannot be locked independently from each other. For further details on locking the shared password, see section 4.8.1.3 • The TID memory bank is perma-locked at the factory and is read only
Untraceable	• Impinj M800 series tag chips support only the Range parameter of the Untraceable command to shift between short/reduced range and full, normal operating range. This includes supporting temporarily toggling the range. • The EPC length field (L bits) must match the EPC length field (StoredPC bits 10_h – 14_h) • For an alternative method to set a tag for short-range, see section 4.8.2

3.3 Impinj Integra V2 Memory Diagnostics

Impinj M800 series tag chips have improved data integrity features that enhance encoding and data reliability. These features include Memory Parity Self-Check and the *MarginRead* command.

3.3.1 Memory Parity Self-Check

The Impinj Integra V2 self-check feature in Impinj M800 series tag chips include automatic word-wise parity checking for all memory spaces. Automatic parity checking prevents tags from sending corrupt data to a reader during Gen2v2 inventory rounds or read operations.

The tag has an additional parity bit for each word stored on the chip used for implementing memory parity checks during typical Gen2v2 operations described in this section. The parity bits are used for internal parity checking and are not directly readable.

3.3.1.1 Factory Memory Parity Check

At IC power-up, parity is checked in Reserved memory words 4 and 5 and TID memory words 0 - 5. The tag will not send any response if parity fails on any of these words. If the tag backscatters an RN16, e.g. in response to a *Query* command during an inventory, the parity check has passed for this memory.

3.3.1.2 EPC Parity Check

During a typical inventory round, the EPC data, as specified by the EPC length, is checked for parity errors. If an error is detected in the EPC data at IC power-up, the tag will respond with a zero-length EPC. If an error is detected in the PC word, the tag will respond with a zero-length EPC and an inverted PacketCRC. If there are no parity errors, the tag will respond with the expected EPC data.

3.3.1.3 Read Memory Parity Check

Parity is checked on individual words of memory by issuing a *Read* command. The target word(s) will be checked for parity errors. If an error is detected, tag will respond with the read data and an inverted CRC. If there are no parity errors, the tag will respond with the expected data.

3.3.1.4 Shared Password Parity Check

Parity is checked on the shared password by issuing a *Kill* or *Access* command sequence. If an error is detected in the shared password, the tag will not be able to enter the **killed** or **secured** states and the tag will respond with the error codes shown below. If no errors are detected, the tag responds as expected and may therefore enter the **killed** or **secured** states by issuing the *Kill* or *Access* command sequences, respectively, with the correct password.

- *Kill* command sequence: tag with parity error in shared password responds with an error code as if the kill password = 0
    - Tag sends error code 00000000_2
- *Access* command sequence: tag with parity error in shared password responds with an error code indicating the access is disallowed
    - Tag sends error code 00000000_2

3.3.2 Recommended Memory Parity Self-Check Usage Guidelines

Memory Parity Self-Check is designed to allow reliable, automatic screening capabilities to improve quality when manufacturing RAIN RFID tags with Impinj endpoint ICs. Memory failures are rare but are a reality of RFID tag manufacturing. In RAIN RFID, there are potential points of failure throughout the tag manufacturing ecosystem before finished tags are attached to items—from the silicon manufacturing process through inlay manufacturing, label conversion, and finally the printing and encoding of finished tags. If the integrity of a tag is compromised, it should be screened out as early as possible.

The Impinj Integra V2 Memory Parity Self-Check provides a seamless, built-in mechanism to minimize the risk of damaged parts being put into service. Bit flips are easily screened on Impinj M800 series tag chips as they will self-report issues, checking their memory during every Gen2v2 inventory round or read operation.

- If inventory rounds or read operations complete successfully, no parity errors were detected
- If locking an Impinj M800 series tag with a non-zero password, parity will be checked on the shared password automatically during the normal lock command sequence.
    - An *Access* command sequence is required before issuing a *Lock* command to a tag with a non-zero password
    - Parity on the shared password is checked in response to the *Access* command
    - If the *Access* command sequence is successful, no parity errors were detected in the password

3.3.3 MarginRead Command

MarginRead is a Gen2v2-compliant custom command supported by Impinj tag chips with Impinj Integra. This command allows a reader to explicitly verify that each bit of the tag chip NVM is strongly written and has sufficient charge margin for reliable operation. It is used for tag quality control to ensure data integrity and for failure analysis.

Table 3, Table 4, and Table 5 provide details about the custom Impinj *MarginRead* command.

Table 3: *MarginRead* Command Code

Command	Code	Length	Details
MarginRead	1110000000000001	≥ 67 bits	• The MarginRead command allows checking for sufficient write margin of known data • The tag must be in the open or secured state to respond to the command • If a tag receives a MarginRead command with an invalid handle, it ignores that command • The tag responds with the Insufficient Power error code if the power is too low to execute a MarginRead • The tag responds with the Other error code if the margin is bad for a memory bit specified by the mask or if a non-matching bit is sent by the reader • The MarginRead command is only applicable for programmable sections of the memory and will ignore all mask bits that correspond to non-programmable parts of the memory.

Table 4: *MarginRead* Command Details

MarginRead Command	Code	Mem Bank	Bit Pointer	Length	Mask	RN	CRC-16
#bits	16	2	EBV	8	Variable	16	16
Details	11100000 00000001	00: Reserved 01: EPC 10: TID 11: User	Starting Bit Address Pointer	Length in Bits	Mask Value	Handle	CRC-16

Table 5: *MarginRead* Command Field Descriptions

Field	Description
Mem Bank	The memory bank to access
Bit Pointer	An EBV that indicates the starting bit address of the mask
Length	Length of the mask field from 1-255 A value of zero shall result in the command being ignored
Mask	This field must match the expected values of the bits The chip checks that each bit matches what is in the mask field with margin
RN	The tag will ignore any MarginRead command received with an invalid handle

The tag response to the *MarginRead* Command uses the preamble specified by the TRext value in the *Query* command that initiated the round. See Table 6 for tag response details.

Table 6: Tag Response to a Passing *MarginRead* Command

Response	Header	RN	CRC-16
#bits	1	16	16
Description	0	Handle	CRC-16

3.3.4 Recommended MarginRead Usage Guidelines

There are several ways that the *MarginRead* command could be used with Impinj M800 series tag chips. Impinj M800 series ICs are pre-serialized at the factory; the *MarginRead* command allows a programming reader to check that the pre-serialized data is written correctly and does not need to be re-encoded. Another recommended use of *MarginRead* is secondary and independent verification of the encoding quality. *MarginRead* can also be used for diagnosis when doing failure analysis on tags.

3.4 Impinj Protected Mode

The Impinj M800 series tag chips include an advanced tag data protection feature that can be used to enhance consumer privacy while supporting EAS and loss prevention capabilities.

A tag with an Impinj M800 series tag chip can be made invisible to RAIN RFID readers using Impinj Protected Mode. It allows a tag to become completely RF silent to all Gen2v2 commands but return to normal Gen2v2 operation when it receives the correct command sequence.

For more information on enabling Impinj Protected Mode in Impinj M800 series tag chips, please request support through the Impinj Support Portal at https://support.impinj.com.

3.5 Advanced Impinj Inventory Features

Impinj tag chips support two unique, patented features that work within the RAIN standard and boost inventory performance for traditional EPC and TID-based applications:

- Impinj TagFocus mode minimizes redundant reads of strong tags, allowing the reader to focus on weak tags that are typically the last to be found. Using Impinj TagFocus, readers can suppress previously read tags by indefinitely refreshing their S1 B state.
- Impinj FastID™ mode makes TID-based applications practical by boosting TID-based inventory speeds. Readers can inventory both the EPC and the TID without having to perform access commands. Setting the EPC word length to zero enables TID-only serialization.

3.6 Pad Descriptions

Impinj M800 series tag chips have two external Impinj Enduro pads available to the user: one RF+ pad, and one RF- pad. RF+ and RF- form a single differential antenna port, as shown in Table 7 (see also Figure 2 and Figure 3). Note that neither of these pads connects to the chip substrate.

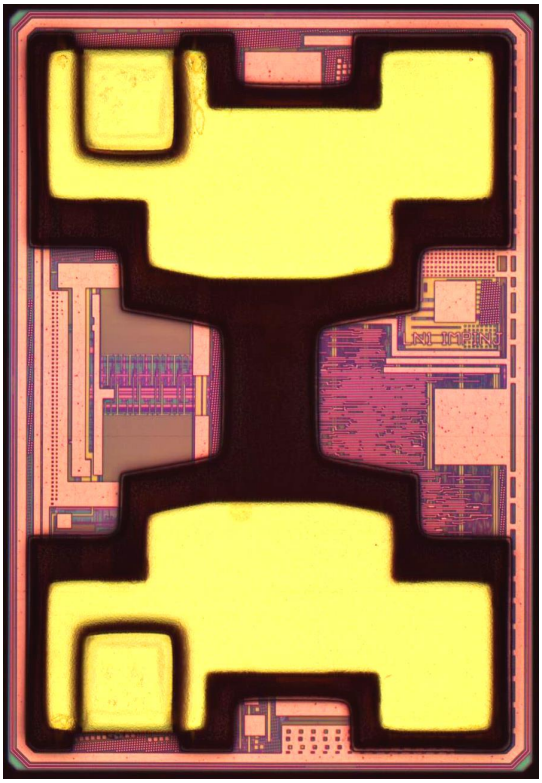
Table 7: Pad Descriptions

External Signals	External Pad	Description
RF+	1	Differential RF Input Pads for Antenna
RF-	2	

3.7 Differential Antenna Input

All interaction with the Impinj M800 series tag chips, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via the chip's differential antenna port. The differential antenna port is connected with the RF+ pad connected to one terminal and the RF- pad connected to the other terminal.

Figure 2: Impinj M800 Series Tag Chip Die Orientation



Note: This image is for illustration purposes only.

3.8 Impinj M800 Series Antenna Reference Designs

Impinj M800 series tag chips are designed to be drop-in compatible in the same inlay antenna designs. Impinj has reference designs available for use by Impinj customers under the terms of the Impinj Antenna License Agreement.

Access to these reference design documents is restricted. To access these documents, users must obtain access permission by creating an Impinj access account and submitting a request form through the

Impinj Partner Access page. Once Impinj has accepted their request, users can use their access credentials to view the Impinj Endpoint IC reference design documents page on the Support Portal.

3.9 Impinj M800 Series Tag Chip Dimensions

Chip dimensions for Impinj M830/M850

- 362.0 µm x 247.0 µm rectangular die size
- 109.5 µm x 215.0 µm pad size
- 111.0 µm pad spacing at center of die
- 187.2 µm pad spacing at edge of die

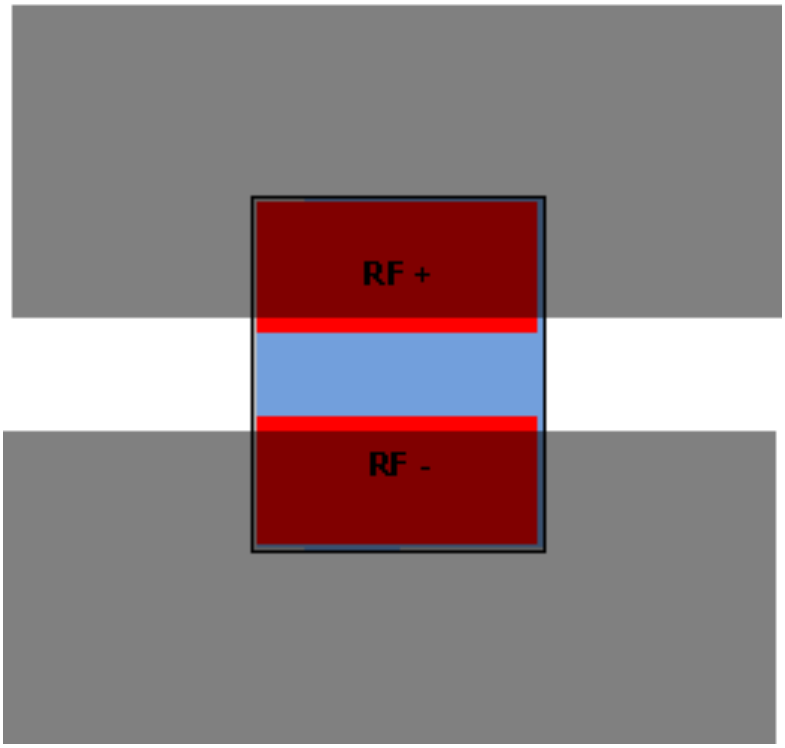
4 INTERFACE CHARACTERISTICS

This section describes the RF interface of the tag chip and the modulation characteristics of both communication links: reader-to-tag (Forward Link) and tag-to-reader (Reverse Link).

4.1 Antenna Connections

Figure 3 shows antenna connections for Impinj M800 series tag chips.

Figure 3: Antenna Connection for Inlay Production



This connection configuration for inlay production connects the Impinj M800 series tag chip RF+ pad to one antenna terminal and the RF- pad to the opposite polarity terminal. Impinj Enduro pads allow relatively coarse antenna geometry, and thus enable relaxed resolution requirements for antenna patterning compared to bumped products. The diagram in Figure 3 shows the recommended antenna trace arrangement and chip placement, with antenna traces partially overlapping the Impinj Enduro pads but not extending into the clear space between Enduro pads.

4.2 Impedance Parameters

To realize the full performance potential of the Impinj M800 series tag chips, it is imperative that the antenna present the appropriate impedance at its terminals. A simplified lumped element tag chip model,

shown in Figure 4, is the conjugate of the optimum source impedance, which is *not* equal to the chip input impedance. This indirect, source-pull method of deriving the port model is necessary due to the non-linear, time-varying nature of the tag RF circuits. The model is a good mathematical fit for the chip over a broad frequency range.

The lumped element values are listed in Table 8, where C_{mount} is the parasitic capacitance due to the antenna trace overlap with the chip surface, C_p appears at the chip terminals and is intrinsic to the chip, and R_p represents the energy conversion and energy absorption of the RF circuits.

Figure 4: Tag Chip Linearized RF Model

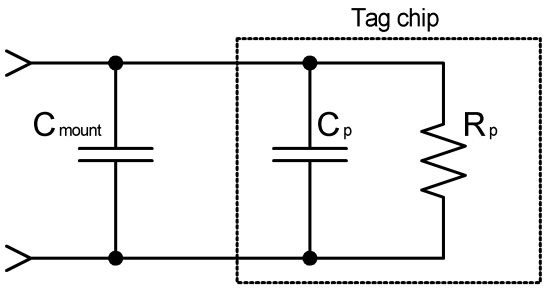


Table 8 shows the values for the chip port model for Impinj M800 series tag chips, which apply to all frequencies of the primary regions of operation (including North America and Europe).

Table 8: Impinj M800 Series RF Parameters

Parameter	Typical Value	Comments
R_p	3.50 kΩ	Calculated for linearized RF model shown in Figure 4.
C_p	0.930 pF	Intrinsic chip capacitance when AutoTune is mid-range, including Enduro pads.
C_{mount}	0.115 pF	Typical capacitance due to adhesive and antenna mount parasitics.
Total Load Capacitance	1.045 pF	Total load capacitance presented to antenna model of Figure 4 is: $C_p + C_{mount}$
Read Sensitivity	- 25.5 dBm	Measured in a 50-ohm system using a response to a Query command with a +2.15 dBi gain ideal dipole antenna.
Write Sensitivity	- 20.0 dBm	

4.3 Reader-to-Tag (Forward Link) Signal Characteristics

Table 9: Forward Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by a tag with dipole antenna while sitting on a maximum power reader antenna
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth	80		100	%	(A-B)/A, A=envelope max., B=envelope min.
Ripple, Peak-to-Peak			5	%	Portion of A-B
Rise Time (tr,10-90%)	0		0.33Tari	sec	
Fall Time (tf,10-90%)	0		0.33Tari	sec	
Tari*	6.25		25	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.265 Tari,2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)

***Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.**

4.4 Tag-to-Reader (Reverse Link) Signal Characteristics

Table 10: Reverse Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $\|\Delta\Gamma\|$ due to Modulation		0.8			$\|\Delta\Gamma\| = \left\|\Gamma_{reflect} - \Gamma_{absorb}\right\|$ (per read/write sensitivity, Table 8)
Duty Cycle	45	50	55	%	
Symbol Period	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency*	40		640	kHz	

*** Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.**

4.5 Impinj M830 Tag Chip Memory Map

Table 11: Impinj M830 Physical/Logical Memory Map

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Address															
			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
10_2	TID (ROM)	80_h-$8F_h$	S0	S2	S3	S0	SL	S2	SL	S3	RFU[7:0] = 00_h							
		50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header = 2000_h															
		10_h-$1F_h$	MDID[3:0] = 1_h				Model Number = $1B0_h$											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	MDID[8:4] = 00_h				
01_2	EPC (NVM)	90_h-$9F_h$	EPC[15:0]															
		80_h-$8F_h$	EPC[31:16]															
		70_h-$7F_h$	EPC[47:32]															
		60_h-$6F_h$	EPC[63:48]															
		50_h-$5F_h$	EPC[79:64]															
		40_h-$4F_h$	EPC[95:80]															
		30_h-$3F_h$	EPC[111:96]															
		20_h-$2F_h$	EPC[127:112]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU[12:0]=000_h													ATV[2:0]		
		70_h-$7F_h$	Factory Calibration C[15:0]															
		60_h-$6F_h$	Factory Calibration B[15:0]															
		50_h-$5F_h$	Factory Calibration A[15:0]															
		40_h-$4F_h$	Internal Config [15:5]											SR	M	Internal Config [2:1]		A
		30_h-$3F_h$	Shared Access Password[15:0]															
		20_h-$2F_h$	Shared Access Password[31:16]															
		10_h-$1F_h$	Shared Kill Password[15:0]															
		00_h-$0F_h$	Shared Kill Password[31:16]															

Note: The Impinj M800 series tag chips have a single 32-bit password; the access and kill passwords are shared and aliased over one another.

4.6 Impinj M850 Tag Chip Memory Map

Table 12: Impinj M850 Physical/Logical Memory Map

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Address															
			0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
11_2	USER (NVM)	10_h-$1F_h$	User[15:0]															
		00_h-$0F_h$	User[31:16]															
10_2	TID (ROM)	80_h-$8F_h$	S0	S2	S3	S0	SL	S2	SL	S3	RFU[7:0] = 00_h							
		50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header = 2000_h															
		10_h-$1F_h$	MDID[3:0] = 1_h				Model Number = $1B0_h$											
		00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	MDID[8:4] = 00_h				
01_2	EPC (NVM)	70_h-$7F_h$	EPC[15:0]															
		60_h-$6F_h$	EPC[31:16]															
		50_h-$5F_h$	EPC[47:32]															
		40_h-$4F_h$	EPC[63:48]															
		30_h-$3F_h$	EPC[79:64]															
		20_h-$2F_h$	EPC[95:80]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	140_h-$14F_h$	RFU[12:0]=000_h													ATV[2:0]		
		70_h-$7F_h$	Factory Calibration C[15:0]															
		60_h-$6F_h$	Factory Calibration B[15:0]															
		50_h-$5F_h$	Factory Calibration A[15:0]															
		40_h-$4F_h$	Internal Config [15:5]											SR	M	Internal Config [2:1]		A
		30_h-$3F_h$	Shared Access Password[15:0]															
		20_h-$2F_h$	Shared Access Password[31:16]															
		10_h-$1F_h$	Shared Kill Password[15:0]															
		00_h-$0F_h$	Shared Kill Password[31:16]															

Note: The Impinj M800 series tag chips have a single 32-bit password; the access and kill passwords are shared and aliased over one another.

4.7 Logical vs. Physical Bit Identification

For the purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address, used for the memory bank bit addresses, describes the addressing used to access the memory.

4.8 Reserved Memory

Reserved memory contains the kill and access passwords, at bit locations 00-1F$_h$ and 20-3F$_h$ respectively. These passwords are the same for Impinj M800 tag chips and are programmed to zero at the factory. Reserved memory also contains three user configuration bits for Impinj M830/M850, which may only be changed in the **secured** state with a non-zero access password unless otherwise noted. The tag will transition from the **open** to **secured** state by receiving an *Access* command sequence with correct access password. Tags with a zero access password do not need the *Access* command sequence to transition to the **secured** state.

- SR = the short-range bit. This bit is set to zero at the factory. When this bit is set to one, the chip will operate in a short-range mode. The chip will not respond at all unless it is in short-range. This bit may be changed from the **secured** state with a non-zero password. This bit is at Reserved memory bit location 4B$_h$ for Impinj M830 and M850. See section 4.8.2 for more details.
- M = the memory map selection bit. At the factory, this bit is set to one for Impinj M830 and set to zero for Impinj M850. This bit may be written only once from the **secured** state with a zero or non-zero password. This bit is at Reserved memory bit location 4C$_h$ for Impinj M830 and M850. See section 4.8.2 for more details.
- A = the AutoTune disable bit. This bit is set to zero at the factory. When the AutoTune disable bit is zero, Impinj AutoTune works as normal. When the bit is one, Impinj AutoTune is disabled and the capacitance on the front end assumes the mid-range value. This bit may be changed from the **secured** state with a zero or non-zero password. This bit is at Reserved memory bit location 4F$_h$ for all Impinj M800 tag chips. See section 4.8.3 for more details.

To write these three bits for Impinj M830/M850, a *Write* command or single word *BlockWrite* command must be issued to word 4 of Reserved memory. These bits must be written at the same time. The SR and A bits may be changed multiple times but the M bit may only be written once. When writing to this word to set the configuration bits, use the payloads as shown in Table 13 for Impinj M830/M50. The AutoTune value is marked ATV[2:0] in word 14$_h$ for Impinj M830/M850. The AutoTune value represents the tuning capacitance scale, from zero to four.

Table 13: Writing User Configurable Bits for Impinj M830/M850, Word 4_h of Reserved Memory

Payload (Hex)	Payload (Binary)	Short-range Bit, SR	Memory Map Bit, M	AutoTune Disable Bit, A	Comments
0000	0000 0000 000**0** 0**0**0**0**	**0**	**0**	**0**	Default values. Tag will be in normal range with AutoTune enabled. The M bit will be set to the Impinj M850 memory map, with 96 bits of EPC memory and 32 bits of User memory.
0008	0000 0000 000**0** **1**00**0**	**0**	**1**	**0**	Default values. Tag will be in normal range with AutoTune enabled. The M bit will be set to the Impinj M830 memory map, with 128 bits of EPC memory and no User memory.
0010	0000 0000 000**1** 000**0**	**1**	**0**	**0**	Tag will be in short-range with AutoTune enabled. The M bit will be set to the Impinj M850 memory map, with 96 bits of EPC memory and 32 bits of User memory.
0001	0000 0000 000**0** 000**1**	**0**	**0**	**1**	Tag will be in normal range with AutoTune disabled. The M bit will be set to the Impinj M850 memory map, with 96 bits of EPC memory and 32 bits of User memory.
0011	0000 0000 000**1** 000**1**	**1**	**0**	**1**	Tag will be in short-range with AutoTune disabled. The M bit will be set to the Impinj M850 memory map, with 96 bits of EPC memory and 32 bits of User memory.

Note: This word must be written to in the secured state. If changing the SR bit, the tag must also have a non-zero access password, entering the secured state using the Access command. The M bit may only be written once – after it is written once, this word can be re-written but the M bit value will not change.

4.8.1 Shared Access and Kill Password

Impinj M800 series tag chips have a single 32-bit password; the access and kill passwords are shared and aliased over one another. The same password is used for both *Access* and *Kill* commands. *Write, BlockWrite* or *Lock* commands to the access password will affect the kill password and vice versa. The password may be read or written from either address. Multi-row reads of the Reserved memory bank will return the same password for words 0-1 and 2-3. The default value for the shared password is all zeroes. Impinj M800 series tag chips will respond to *Access*, *Kill* and *Lock* commands as if the access and kill passwords were logically independent even though they share the same physical memory.

4.8.1.1 Access Password

The single shared 32-bit password functions as the access password in Reserved memory 20_h to $3F_h$, MSB first. The default value is all zeroes. Tags with a non-zero access password will require a reader to issue this password as part of an *Access* command before transitioning to the **secured** state. The password stored in the access password location will always have the same value and lock status as the kill password.

4.8.1.2 Kill Password

The single shared 32-bit password functions as the kill password in Reserve Memory 00_h to $1F_h$, MSB first. The default value is all zeroes. Tags with a non-zero kill password will require a reader to issue this password as part of *Kill* command before permanently transitioning to the **killed** state. Tags in the **killed** state will not respond to any commands. A tag will not execute a kill operation if its kill password is all zeroes.

4.8.1.3 Locking Password

Impinj M800 series tag chips must have the access and kill passwords locked in the same way. The table below lists specific examples of valid payloads for locking the access and kill passwords. It is possible to lock additional memory alongside the passwords as well – additional payloads are supported as long as the access and kill password lock settings are set to the same value during the lock operation. If the payload for the *Lock* command is not valid, the tag chip will respond back with an error code "Not supported" (00000001_b). For further details about the *Lock* command, refer to the Gen2v2 specification.

Table 14: Supported *Lock* Command Payloads for Locking Passwords

Lock Command Payload (Hex)	Lock Command Payload (Binary)	Description
A0000	1010 0000 0000 0000 0000	Access and kill passwords are unlocked and are readable or writable from the **open** or **secured** states.
F0000	1111 0000 0000 0000 0000	Access and kill passwords are permanently unlocked and are readable or writable from the **open** or **secured** states.
A0280	1010 0000 0010 1000 0000	Access and kill passwords are locked and are readable or writable from the **secured** state but not from the **open** state.
F03C0	1111 0000 0011 1100 0000	Access and kill passwords are permanently locked and are not readable or writable from any state.

4.8.2 Short-range Mode

Impinj M800 series tag chips come with a short-range capability to enhance consumer privacy. The short-range bit (SR) in Reserved memory may be written when the tag is in the **secured** state with a non-zero access password. The tag chip would require an *Access* command with the correct access password to transition from the **open** to **secured** state.

- The factory programmed value of the short-range bit is zero, which means the tag operates at full range and short-range is disabled.
- To enable short-range, a reader writes the SR bit to a one. The tag will only respond when it is near the reader, reducing the IC's read range to less than $1/10^{th}$ of its normal range.
- To disable short-range mode, a reader writes the SR bit to a zero.

Refer to Table 13 for example values to configure bits in Reserved memory.

Short-range may also be configured using the Gen2v2 *Untraceable* command by specifying the *range* field as described below. The tag must be in the **secured** state with a non-zero access password in order to use the *Untraceable* command.

- If the *range* field is set to 10_2: the SR bit will be set to one and the tag will be set to short-range operation.
- If the *range* field is set to 00_2: the SR bit will be set to zero and the tag will be set to normal range operation.

- If the *range* field is set to 01_2: the SR bit will not be changed but the tag will operate as per the inverse of the SR bit value. For example:
    - If the tag is in normal range with SR = 0, and in the **secured** state when it receives an *Untraceable* command with range = 01_2, it will function in short-range operation until it loses energy. This may be used to ensure that a reader has enough power to communicate with a short-range tag before committing the change to memory.
    -

4.8.3 Memory Map Selection

The memory map selection bit is in word 4_h, marked M in the memory map. The Impinj M830 and M850 are electrically identical chips with different default memory map selections set at the factory:

- Impinj M830 has a default M bit value of one, which selects the memory map with 128 bits of EPC memory and no User memory. Refer to Table 11 for memory map details.
- Impinj M850 has a default M bit value of zero, which selects the memory map with 96 bits of EPC memory and 32 bits of User memory. Refer to Table 12 for memory map details.

The M bit may be written only once from the **secured** state. The value may be permanently locked by re-writing the default value or changed only one time from zero to one (for the M850) or from one to zero (for the M830) to select the other memory map. After the memory map selection bit is written, it is locked and may not be changed again. In addition, if any valid *Lock* command is issued to the tag, the memory map selection bit will be permanently locked.

Note: The value of the M bit does not affect the Model Number in the TID, which is fixed.

4.8.4 Impinj AutoTune Disable and AutoTune Value

The AutoTune disable bit is in word 4_h, marked A in the memory map. The AutoTune value is marked ATV[2:0] in word 14_h for Impinj M830/M850. The AutoTune value represents the tuning capacitance scale, from zero to four. A value of zero removes 100 fF of capacitance across the RF input of the tag and a value of four adds 100 fF across the RF input of the chip. See Table 15 for the mapping between AutoTune value and the change in input capacitance. A reader acquires the AutoTune value by issuing a single word *Read* command to the appropriate word in the Reserved memory bank. The AutoTune value is not writable.

- The factory programmed value of the AutoTune disable bit is zero, enabling AutoTune by default.
- To disable AutoTune, a reader writes the A bit to a one. When the AutoTune bit is disabled, the capacitance across the RF input is set to 0 fF. Note that the readout of AutoTune value represents the value the IC would have tuned to with AutoTune enabled, and not the current capacitance across the RF input to the tag.
- To re-enable AutoTune, a reader writes the A bit to a zero.

Refer to Table 13 for example values to configure bits in Reserved memory.

Table 15: Impinj AutoTune Value

Impinj Autotune Value	Change in Input Capacitance (fF)
0_h	-100
1_h	-40
2_h	0
3_h	+40
4_h	+100

4.9 EPC Memory (EPC Data, Protocol Control Bits, and CRC16)

As per the Gen2v2 specification, tag chip EPC memory contains a 16-bit cyclic-redundancy check word (CRC16) at memory addresses 00_h to $0F_h$; the 16 protocol-control bits (PC) at memory addresses 10_h to $1F_h$; and an EPC value beginning at address 20_h.

4.9.1 CRC16

The tag calculates the CRC16 upon power-up over the stored PC bits and the EPC specified by the EPC length field in the stored PC.

4.9.2 Protocol Control Word and Extended Protocol Control Word

The 16 protocol control bits, or PC word, include a five-bit EPC length (L bits), a one-bit read-only User memory indicator (UMI), a one-bit read-only extended protocol control indicator (XI), and nine bits of programmable memory from 17_h to $1F_h$ for the numbering system identifier toggle bit, T, and either Reserved for Future Use or Application Family Identifier (RFU or AFI), bits 18_h to $1F_h$.

- For Impinj M830 tag chips, the UMI bit is set to 0 to indicate the absence of User memory. The factory default PC word value is 3000_h.
- For Impinj M850 tag chips, the UMI bit is set to 1 to indicate the presence of User memory. The factory default PC word value is 3400_h.

Impinj M830 and M850 tag chips do not implement XPC_W1.

Table 16: StoredPC Bit Values Following the Gen2v2 Specification

EPC Memory Bank Bit Address	Name	How Set?	Descriptor	Setting
10_h-14_h	L bits	Written	EPC length field	
15_h	UMI	Fixed	User memory indicator (File_0 indicator)	0: Impinj M830 1: Impinj M850
16_h	XI	Computed (to a value of 0)	XPC_W1 indicator	0: Impinj M830/M850, as the tag has no XPC_W1
17_h	T	Written	Numbering System Identifier Toggle	0: Tag is used in a GS1 EPCglobal™ Application 1: Tag is used in a non-GS1 EPCglobal™ Application
18_h-$1F_h$	RFU or AFI	Per the Application	Reserved for Future Use or Application Family Identifier	GS1 EPCglobal™ Application: RFU and fixed at zero Non-GS1 EPCglobal™ Application: See ISO/IEC 15961

For more details about the PC field or the CRC16, see the Gen2v2 specification.

A tag reply to an ACK command, during an inventory round, will be determined by which bits are set in the PC word and if the tag is backscattering a truncated EPC. The following table shows the possible tag responses for Impinj M800 series tag chips, following the Gen2v2 specification.

Table 17: Tag reply to an ACK command from the Gen2v2 specification

T	XI	XEB	Trunc-ation	C AND immed	Tag Backscatter				Notes
					PC	XPC	EPC[1]	CRC	
0	0	0	0	0	StoredPC(10_h–$1F_h$)	None	Full	PacketCRC	Impinj M830/M850 do NOT implement XPC_W1
0	0	0	1	0	00000_2	None	Truncated	PacketCRC	
1	0	0	1	0	00000_2	None	Truncated	PacketCRC	
1	0	0	0	0	StoredPC(10_h – $1F_h$),	None	Full	PacketCRC	

[1]Full means an EPC whose length is specified by the L bits in the StoredPC; truncated means an EPC whose length is shortened by a prior Select command specifying truncation. See Select command details in the Gen2v2 specification for more details.

4.9.3 EPC Data

The EPC memory bank of Impinj M830 tag chips supports a maximum EPC size of 128 bits, and a maximum EPC size of 96 bits for M850 (see Table 1). The default EPC length from the factory is 96 bits. It is possible to adjust the EPC length according to the parameters laid out in the Gen2v2 standard by adjusting the five-bit EPC length in the PC word. The EPC value written into the chip from the factory is

listed below in Table 18. The “X” nibbles in the pre-programmed EPC are pre-serialized values that follow the Impinj Monza Self-Serialization formula for Impinj M800 series tag chips.

For more details on the pre-serialization formula used to generate the factory-programmed EPC, refer to the TID Memory Maps for Monza Self-Serialization.

Table 18: EPC at Factory-Program

Impinj Part Number	Tag Chip Model	Factory default PC Bits (HEX)	EPC Value Pre-programmed at the Factory (hex)
IPJ-M830A-A00	Impinj M830	3000	E280 11B0 A5XX XXXX XXXX XXXX
IPJ-M850A-A00	Impinj M850	3400	E280 11B0 A5XX XXXX XXXX XXXX

4.10 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data as shown in Table 19.

- The EPCglobal™ Class ID ($E2_h$) is stored in TID bit locations 00_h-07_h.
- Bit 08_h is the XTID (X) indicator bit; X has a value of 1 to indicate the presence of an extended TID, consisting of a 16-bit header and a 48-bit serialization.
- Bit 09_h is the Security (S) indicator bit; S has a value of 0 to indicate the Impinj M830 and M850 tag chips do not support the *Authenticate* and/or *Challenge* commands.
- Bit $0A_h$ is the File (F) indicator bit; F has a value of 0 to indicate the Impinj M830 and M850 tag chips do not support the *FileOpen* command.
- The GS1-assigned 9-bit Manufacturer Identifier (MDID) for Impinj is 000000001_2 and is located in TID memory bit locations $0B_h$-13_h. (Note: the location of the MDID is shown in Tag Memory, section 0, and the bit details are given in Table 19.)
- The Impinj M800 tag chip model number is located in TID memory bit locations 14_h-$1F_h$. See Table 20 for details on Impinj M800 series tag model numbers.
- TID bit locations 80_h-87_h contain read-only flag state bits. The flag state values are mapped to memory and may be used to read the current flag states or may be used for tag filtering with the *Select* command. For the S0, S2 and S3 bits, a value of 0 indicates the tag is in the A state for the given session, and a value of 1 indicates the tag is in the B state. If the SL flag is asserted, the SL bit will be 1; if de-asserted, the SL bit will be 0. Using any combination of these bits allows for selected tags based on any or all of these states through a single *Select* command.

Table 19: TID Memory Details

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Address															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10_2	TID (ROM)	80_h-$8F_h$	S0	S2	S3	S0	SL	S2	SL	S3	RFU[7:0] = 00_h							
		50_h-$5F_h$	TID_SERIAL[15:0]															
		40_h-$4F_h$	TID_SERIAL[31:16]															
		30_h-$3F_h$	TID_SERIAL[47:32]															
		20_h-$2F_h$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
		10_h-$1F_h$	MDID[3:0]				*Tag Model Number*											
			0	0	0	1												
		00_h-$0F_h$	EPCglobal™ Class ID								X	S	F	MDID[8:4]				
			1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0

Table 20: Impinj M800 Series Tag Model Number Details

Tag chip model	Tag Model Number	
	Hex	Binary
Impinj M830	1B0	0001 1011 0000
Impinj M850	1B0	0001 1011 0000

4.11 User Memory

The Impinj M850 tag chip user memory bank contains 32 bits of memory: two 16-bit words at memory addresses 00_h to $1F_h$. The Impinj M830 tag chip contains no user memory bank. For further details about writing to user memory, refer to the Gen2v2 specification.

5 ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed in this section may cause permanent damage to the tag chip. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

The tag chip is designed to be used within the temperature ranges listed in Table 21. These ranges specify the operating, storage, and survival conditions for the tag chip. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 21: Temperature Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Extended Operating Temperature	–40		+85	°C	Default range for all functional and performance requirements except write operations. Write operations are limited to the Gen2 extended temperature range maximum of 65°C.
Storage Temperature	–40		+85/125	°C	At 125°C data retention is 1 year
Assembly Survival Temperature			260	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

5.2 Electrostatic Discharge (ESD) Tolerance

The tag chip is guaranteed to survive ESD as specified in Table 22.

Table 22: ESD Limits

Parameter	Minimum	Typical	Maximum	Units	Comments
ESD			2,000	V	HBM (Human Body Model)

5.3 NVM Use Model

Tag memory is designed to endure 10,000 write cycles or retain data for 10 years.

6 ORDERING INFORMATION

Contact sales@impinj.com for ordering support.

Table 23: Ordering Information

Part Number	Form	Product	Processing Flow
IPJ-M830A-A00	Wafer	Impinj M830 tag chip	Padded, thinned (to ~120 µm) and diced
IPJ-M850A-A00	Wafer	Impinj M850 tag chip	Padded, thinned (to ~120 µm) and diced

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