SL3S1203\_1213 UCODE G2iL and G2iL+ Rev. 4.5 — 12 February 2019

**Product data sheet COMPANY PUBLIC** 

#### **General description** 1

NXP's UCODE G2iL series transponder ICs offer leading-edge read range and support industry-first features such as a Tag Tamper Alarm, Data Transfer, Digital Switch, and advanced privacy-protection modes.

Very high chip sensitivity (-18 dBm) enables longer read ranges with simple, single-port antenna designs. When connected to a power supply, the READ as well as the WRITE range can be boosted to a sensitivity of -27 dBm. In fashion and retail the UCODE G2iL series improve read rates and provide for theft deterrence. For consumer electronics the UCODE G2iL series is suited for device configuration, activation, production control, and PCB tagging. In authentication applications the transponders can be used to protect brands and guard against counterfeiting. They can also be used to tag containers, electronic vehicles, airline baggage, and more.

In addition to the EPC specifications the G2iL offers an integrated Product Status Flag (PSF) feature and read protection of the memory content.

On top of the G2iL features the G2iL+ offers an integrated tag tamper alarm, RF field detection, digital switch, external supply mode, read range reduction and data transfer mode.



#### 2 Features and benefits

### 2.1 Key features

- UHF RFID Gen2 tag chip according EPCglobal v1.2.0 with 128 bit EPC memory
- · Memory read protection
- Integrated Product Status Flag (PSF)
- Tag tamper alarm
- · RF field detection
- · Digital switch
- · Data transfer mode
- Real Read Range Reduction (Privacy Mode)
- External supply mode where both the READ & WRITE range are boosted to -27dBm

#### **2.1.1 Memory**

- 128-bit of EPC memory
- 64-bit Tag IDentifier (TID) including 32-bit factory locked unique serial number
- 32-bit kill password to permanently disable the tag
- 32-bit access password to allow a transition into the secured state
- Data retention: 20 years
- Broad international operating frequency: from 840 MHz to 960 MHz
- Long read/write ranges due to extremely low power design
- Reliable operation of multiple tags due to advanced anti-collision
- READ protection
- WRITE Lock
- Wide specified temperature range: -40 °C up to +85 °C

#### 2.2 Key benefits

#### 2.2.1 End user benefit

- Prevention of unauthorized memory access through read protection
- Indication of tag tampering attempt by use of the tag tamper alarm feature
- Electronic device configuration and / or activation by the use of the digital switch / data transfer mode
- Theft deterrence supported by the PSF feature (PSF alarm or EPC code)
- · Small label sizes, long read ranges due to high chip sensitivity
- Product identification through unalterable extended TID range, including a 32-bit serial number
- Reliable operation in dense reader and noisy environments through high interference suppression

#### 2.2.2 Antenna design benefits

- High sensitivity enables small and cost efficient antenna designs
- Low Q-Value eases broad band antenna design for global usage

SL3S1203\_1213

#### 2.2.3 Label manufacturer benefit

- · Consistent performance on different materials due to low Q-factor
- · Ease of assembly and high assembly yields through large chip input capacitance
- Fast first WRITE of the EPC memory for fast label initialization

#### 2.3 Custom commands

- PSF Alarm
  - Built-in PSF (Product Status Flag), enables the UHF RFID tag to be used as EAS tag (Electronic Article Surveillance) tag without the need for a back-end data base.
- Read Protect
   Protects all memory content including CRC16 from unauthorized reading.
- ChangeConfig
   Configures the additional features of the chip like external supply mode, tamper alarm, digital switch, read range reduction or data transfer.

The UCODE G2iL is equipped with a number of additional features and custom commands. Nevertheless, the chip is designed in a way standard EPCglobal READ/ WRITE/ACCESS commands can be used to operate the features. No custom commands are needed to take advantage of all the features in case of unlocked EPC memory.

**UCODE G2iL and G2iL+** 

## 3 Applications

#### 3.1 Markets

- Fashion (Apparel and footwear)
- Retail
- Electronics
- Fast Moving Consumer Goods
- Asset management
- Electronic Vehicle Identification

## 3.2 Applications

- · Supply chain management
  - Item level tagging
  - Pallet and case tracking
- · Container identification
- Product authentication
- PCB tagging
- · Cost efficient, low level seals
- · Wireless firmware download
- · Wireless product activation

Outside above mentioned applications, please contact NXP Semiconductors for support.

UCODE G2iL and G2iL+

## 4 Ordering information

#### **Table 1. Ordering information**

| Type number    | Package |         |   |                |
|----------------|---------|---------|---|----------------|
|                | Name    | IC type | Description   | Version        |
| SL3S1203FUF    | Wafer   | G2iL    | bumped die on sawn 8" 75 µm wafer   | not applicable |
| SL3S1213FUF    | Wafer   | G2iL+   | bumped die on sawn 8" 75 µm wafer   | not applicable |
| SL3S1203FUD/BG | Wafer   | G2iL    | bumped die on sawn 8" 120 µm wafer,<br>7 µm Polyimide spacer                                | not applicable |
| SL3S1213FUD/BG | Wafer   | G2iL+   | bumped die on sawn 8" 120 µm wafer,<br>7 µm Polyimide spacer                                | not applicable |
| SL3S1203FTB0   | XSON6   | G2iL    | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm | SOT886F1       |

UCODE G2iL and G2iL+

## 5 Marking

#### Table 2. Marking codes

| Type number  | Marking code | Comment    | Version |
|--------------|--------------|------------|---------|
| SL3S1203FTB0 | UN           | UCODE G2iL | SOT886  |

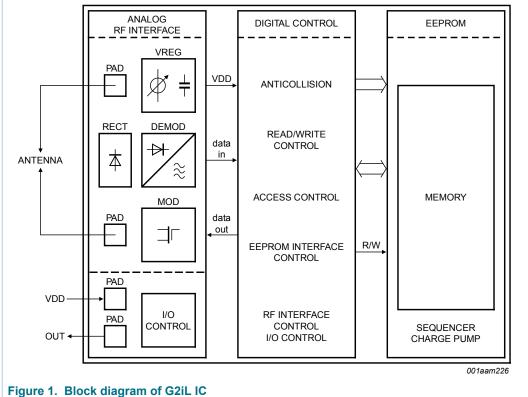
#### **Block diagram** 6

The SL3S12x3 IC consists of three major blocks:

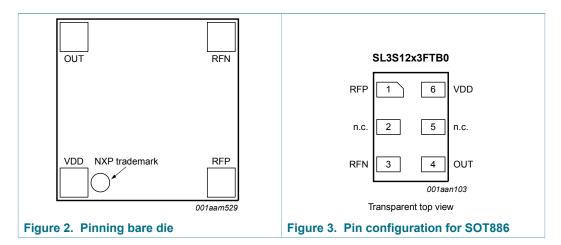
- Analog Interface
- Digital Control
- EEPROM

The analog part provides stable supply voltage and demodulates data received from the reader for being processed by the digital part. Further, the modulation transistor of the analog part transmits data back to the reader.

The digital section includes the state machines, processes the protocol and handles communication with the EEPROM, which contains the EPC and the user data.



## 7 Pinning information



## 7.1 Pin description

Table 3. Pin description bare die

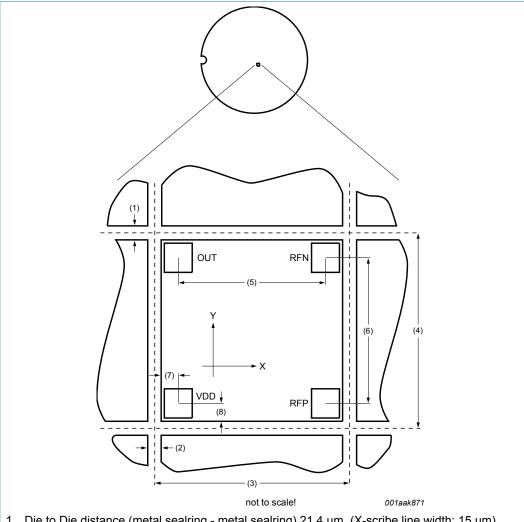
| Symbol | Description                  |
|--------|------------------------------|
| OUT    | output pin                   |
| RFN    | grounded antenna connector   |
| VDD    | external supply              |
| RFP    | ungrounded antenna connector |

Table 4. Pin description SOT886

| Pin | Symbol | Description                  |
|-----|--------|------------------------------|
| 1   | RFP    | ungrounded antenna connector |
| 2   | n.c.   | not connected                |
| 3   | RFN    | grounded antenna connector   |
| 4   | OUT    | output pin                   |
| 5   | n.c.   | not connected                |
| 6   | VDD    | external supply              |

## Wafer layout

### 8.1 Wafer layout



- 1. Die to Die distance (metal sealring metal sealring) 21,4 μm, (X-scribe line width: 15 μm)
- 2. Die to Die distance (metal sealring metal sealring) 21,4 μm, (Y-scribe line width: 15 μm)
- 3. Chip step, x-length: 485 µm
- 4. Chip step, y-length: 435 μm
- 5. Bump to bump distance X (OUT RFN): 383 μm
- 6. Bump to bump distance Y (RFN RFP): 333 µm
- 7. Distance bump to metal sealring X:  $40.3 \mu m$  (outer edge top metal)
- 8. Distance bump to metal sealring Y: 40,3 µm

Bump size X x Y: 60 µm x 60 µm

Remark: OUT and VDD are used with G2iL+ only

Figure 4. G2iL wafer layout

## 9 Mechanical specification

The UCODE G2iL/G2iL+ wafers are available in 75  $\mu$ m and 120  $\mu$ m thickness. The 75  $\mu$ m thick wafer allows ultra thin label design but require a proper tuning of the glue dispenser during production. Because of the more robust structure of the 120  $\mu$ m wafer, the wafer is ideal for harsh applications. The 120  $\mu$ m thick wafer is also enhanced with 7 $\mu$ m Polyimide spacer allowing additional protection of the active circuit.

### 9.1 Wafer specification

See [2].

#### 9.1.1 Wafer

## Table 5. Specifications

| Wafer                         |  |  |  |
|-------------------------------|--|--|--|
| Designation                   | each wafer is scribed with batch number and wafer number |  |  |
| Diameter                      | 200 mm (8")  |  |  |
| Thickness                     |  |  |  |
| SL3S12x3FUF                   | 75 μm ± 15 μm  |  |  |
| SL3S12x3FUD                   | 120 μm ± 15 μm   |  |  |
| Number of pads                | 4  |  |  |
| Pad location                  | non diagonal/ placed in chip corners                     |  |  |
| Distance pad to pad RFN-RFP   | 333.0 µm   |  |  |
| Distance pad to pad OUT-RFN   | 383.0 µm   |  |  |
| Process                       | CMOS 0.14 μm   |  |  |
| Batch size                    | 25 wafers  |  |  |
| Potential good dies per wafer | 139.351  |  |  |
| Wafer backside                |  |  |  |
| Material                      | Si   |  |  |
| Treatment                     | ground and stress release                                |  |  |
| Roughness                     | $R_a$ max. 0.5 $\mu$ m, $R_t$ max. 5 $\mu$ m             |  |  |
| Chip dimensions               |  |  |  |
| Die size including scribe     | 0.485 mm × 0.435 mm = 0.211 mm <sup>2</sup>              |  |  |
| Scribe line width:            | x-dimension = 15 μm                                      |  |  |
|                               | y-dimension = 15 μm                                      |  |  |
| Passivation on front          |  |  |  |
| Туре                          | Sandwich structure                                       |  |  |
| Material                      | PE-Nitride (on top)                                      |  |  |
| Thickness                     | 1.75 µm total thickness of passivation                   |  |  |
| Polyimide spacer              | 7 μm ± 1 μm (SL3S12x3FUD only)                           |  |  |

| Au bump                |                      |
|------------------------|----------------------|
| Bump material          | > 99.9 % pure Au     |
| Bump hardness          | 35 – 80 HV 0.005     |
| Bump shear strength    | > 70 MPa             |
| Bump height            |                      |
| SL3S12x3FUF            | 18 μm                |
| SL3S12x3FUD            | 25 μm <sup>[1]</sup> |
| Bump height uniformity |                      |
| within a die           | ± 2 μm               |
| – within a wafer       | ± 3 µm               |
| – wafer to wafer       | ± 4 μm               |
| Bump flatness          | ± 1.5 μm             |
| Bump size              |                      |
| – RFP, RFN             | 60 × 60 µm           |
| – OUT, VDD             | 60 × 60 μm           |
| Bump size variation    | ± 5 μm               |

<sup>[1]</sup> Because of the 7 µm spacer, the bump will measure 18 µm relative height protruding the spacer.

#### 9.1.2 Fail die identification

No inkdots are applied to the wafer.

Electronic wafer mapping (SECS II format) covers the electrical test results and additionally the results of mechanical/visual inspection.

See [2]

### 9.1.3 Map file distribution

See [2]

## 10 Functional description

#### 10.1 Air interface standards

The UCODE G2iL fully supports all parts of the "Specification for RFID Air Interface EPCglobal, EPC Radio-Frequency Identity Protocols, Class-1 Generation-2 UHF RFID, Protocol for Communications at 860 MHz to 960 MHz, Version 1.2.0".

#### 10.2 Power transfer

The interrogator provides an RF field that powers the tag, equipped with a UCODE G2iL. The antenna transforms the impedance of free space to the chip input impedance in order to get the maximum possible power for the G2iL on the tag. The G2iL+ can also be supplied externally.

The RF field, which is oscillating on the operating frequency provided by the interrogator, is rectified to provide a smoothed DC voltage to the analog and digital modules of the IC.

The antenna that is attached to the chip may use a DC connection between the two antenna pads. Therefore the G2iL also enables loop antenna design. Possible examples of supported antenna structures can be found in the reference antenna design guide.

#### 10.3 Data transfer

### 10.3.1 Reader to tag Link

An interrogator transmits information to the UCODE G2iL by modulating an UHF RF signal. The G2iL receives both information and operating energy from this RF signal. Tags are passive, meaning that they receive all of their operating energy from the interrogator's RF waveform. In order to further improve the read range the UCODE G2iL+ can be externally supplied as well so the energy to operate the chip does not need to be transmitted by the reader.

An interrogator is using a fixed modulation and data rate for the duration of at least one inventory round. It communicates to the G2iL by modulating an RF carrier using DSB-ASK with PIE encoding.

For further details refer to Section 16, [1]. Interrogator-to-tag (R=>T) communications.

#### 10.3.2 Tag to reader Link

An interrogator receives information from a G2iL by transmitting an unmodulated RF carrier and listening for a backscattered reply. The G2iL backscatters by switching the reflection coefficient of its antenna between two states in accordance with the data being sent. For further details refer to Section 16, [1], chapter 6.3.1.3.

The UCODE G2iL communicates information by backscatter-modulating the amplitude and/or phase of the RF carrier. Interrogators shall be capable of demodulating either demodulation type.

The encoding format, selected in response to interrogator commands, is either FM0 baseband or Miller-modulated subcarrier.

#### 10.4 G2iL and G2iL+ differences

The UCODE G2iL is tailored for application where mainly EPC or TID number space is needed. The G2iL+ in addition provides functionality such as tag tamper alarm, external supply operation to further boost read/write range (external supply mode), a Privacy mode reducing the read range or I/O functionality (data transfer to externally connected devices) required.

The following table provides an overview of G2iL, G2iL+ special features.

Table 6. Overview of G2iL and G2iL+ features

| Features                           | G2iL | G2iL+ |
|------------------------------------|------|-------|
| Read protection (bankwise)         | yes  | yes   |
| PSF (Built-in Product Status Flag) | yes  | yes   |
| Backscatter strength reduction     | yes  | yes   |
| Real read range reduction          | yes  | yes   |
| Digital switch / Digital input     | -    | yes   |
| External supply mode               | -    | yes   |
| RF field detection                 | -    | yes   |
| Data transfer                      | -    | yes   |
| Tag tamper alarm                   | -    | yes   |

#### 10.5 Supported commands

The G2iL supports all mandatory EPCglobal V1.2.0 commands.

In addition the G2iL supports the following optional commands:

- ACCESS
- Block Write (32 bit)

The G2iL features the following **custom** commands described more in detail later:

- ResetReadProtect (backward compatible to G2X)
- ReadProtect (backward compatible to G2X)
- ChangeEAS (backward compatible to G2X)
- EAS\_Alarm (backward compatible to G2X)
- ChangeConfig (new with G2iL)

#### 10.6 G2iL, G2iL+ memory

The G2iL, G2iL+ memory is implemented according EPCglobal Class1Gen2 and organized in three sections:

Table 7. G2iL memory sections

| Name   | Size    | Bank |
|--|---------|------|
| Reserved memory (32 bit ACCESS and 32 bit KILL password) | 64 bit  | 00b  |
| EPC (excluding 16 bit CRC-16 and 16 bit PC)              | 128 bit | 01b  |
| G2iL Configuration Word                                  | 16 bit  | 01b  |

| Name  | Size   | Bank |
|---|--------|------|
| TID (including permalocked unique 32 bit serial number) | 64 bit | 10b  |

The logical address of all memory banks begin at zero (00h).

In addition to the three memory banks one configuration word to handle the G2iL specific features is available at EPC bank 01 address 200h. The configuration word is described in detail in Section 10.7.1.

Memory pages (16 bit words) pre-programmed to zero will not execute an erase cycle before writing data to it. This approach accelerates initialization of the chip and enables faster programming of the memory.

### 10.6.1 G2iL, G2iL+ overall memory map

Table 8. G2iL, G2iL+ overall memory map

| Bank<br>address | Memory address | Type     | Content                              | Initial           | Remark                       |
|-----------------|----------------|----------|--------------------------------------|-------------------|------------------------------|
| Bank 00         | 00h to 1Fh     | reserved | kill password                        | all 00h           | unlocked memory              |
|                 | 20h to 3Fh     | reserved | access password                      | all 00h           | unlocked memory              |
| Bank 01<br>EPC  | 00h to 0Fh     | EPC      | CRC-16: refer to [1]                 |                   | memory mapped calculated CRC |
|                 | 10h to 14h     | EPC      | backscatter length                   | 00110b            | unlocked memory              |
|                 | 15h            | EPC      | UMI                                  | 0b                | unlocked memory              |
|                 | 16h            | EPC      | XPC indicator                        | 0b                | hardwired to 0               |
|                 | 17h to 1Fh     | EPC      | numbering system indicator           | 00h               | unlocked memory              |
|                 | 20h to 9Fh     | EPC      | EPC                                  | [1]               | unlocked memory              |
| Bank 01         | 200h           | EPC      | tamper alarm flag                    | 0b <sup>[2]</sup> | indicator bit                |
| Config Word     | 201h           | EPC      | external supply flag or input signal | 0b <sup>[2]</sup> | indicator bit                |
|                 | 202h           | EPC      | RFU                                  | 0b <sup>[2]</sup> | locked memory                |
|                 | 203h           | EPC      | RFU                                  | 0b <sup>[2]</sup> | locked memory                |
|                 | 204h           | EPC      | invert digital output:               | 0b <sup>[2]</sup> | temporary bit                |
|                 | 205h           | EPC      | transparent mode on/off              | 0b <sup>[2]</sup> | temporary bit                |
|                 | 206h           | EPC      | transparent mode data/raw            | 0b <sup>[2]</sup> | temporary bit                |
|                 | 207h           | EPC      | RFU                                  | 0b <sup>[2]</sup> | locked memory                |
|                 | 208h           | EPC      | RFU                                  | 0b <sup>[2]</sup> | locked memory                |
|                 | 209h           | EPC      | max. backscatter strength            | 1b <sup>[2]</sup> | unlocked memory              |
|                 | 20Ah           | EPC      | digital output                       | 0b <sup>[2]</sup> | unlocked memory              |
|                 | 20Bh           | EPC      | read range reduction on/off          | 0b <sup>[2]</sup> | unlocked memory              |
|                 | 20Ch           | EPC      | RFU                                  | 0b <sup>[2]</sup> | locked memory                |
|                 | 20Dh           | EPC      | read protect EPC Bank                | 0b <sup>[2]</sup> | unlocked memory              |
|                 | 20Eh           | EPC      | read protect TID                     | 0b <sup>[2]</sup> | unlocked memory              |
|                 | 20Fh           | EPC      | PSF alarm flag                       | 0b <sup>[2]</sup> | unlocked memory              |

# UCODE G2iL and G2iL+

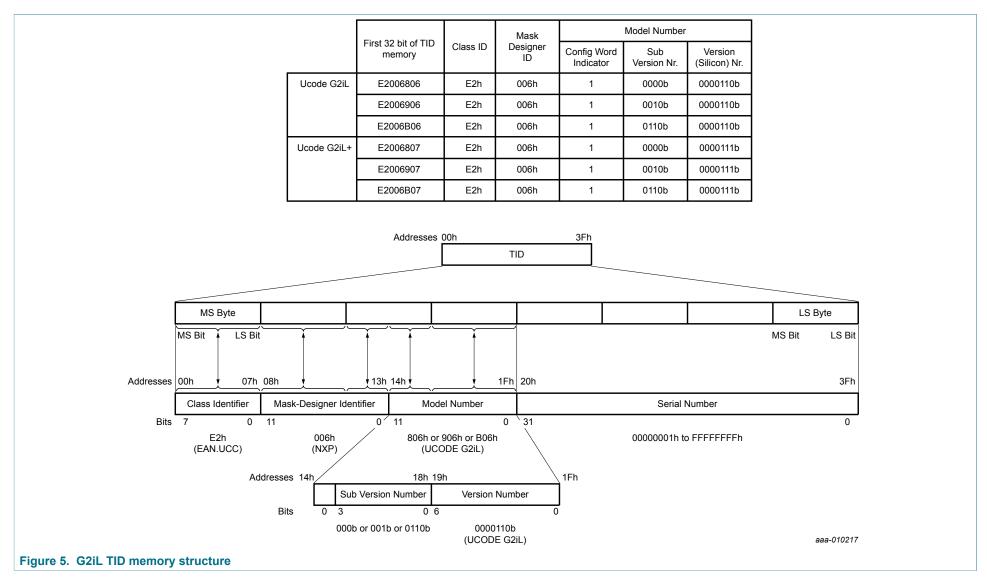
| Bank<br>address | Memory address | Туре | Content                      | Initial             | Remark        |
|-----------------|----------------|------|------------------------------|---------------------|---------------|
| Bank 10         | 00h to 07h     | TID  | allocation class identifier  | 1110 0010b          | locked memory |
| TID             | 08h to 13h     | TID  | tag mask designer identifier | 0000 0000 0110b     | locked memory |
|                 | 14h            | TID  | config word indicator        | 1b <sup>[3]</sup>   | locked memory |
|                 | 14h to 1Fh     | TID  | tag model number             | TMNR <sup>[1]</sup> | locked memory |
|                 | 20h to 3Fh     | TID  | serial number                | SNR                 | locked memory |

See Figure 5
See also Table 12 for further details.
Indicates the existence of a Configuration Word at the end of the EPC number [1] [2] [3]

NXP Semiconductors SL3S1203\_1213

**UCODE G2iL and G2iL+** 

## 10.6.2 G2iL TID memory details



#### 10.7 Custom commands

The UCODE G2iL, G2iL+ is equipped with a number of additional features and custom commands.

Nevertheless, the chip is designed in a way standard EPCglobal READ/WRITE/ACCESS commands can be used to operate the features.

The memory map stated in the previous section describes the Configuration Word used to control the additional features located at address 200h of the EPC memory. For this reason the standard READ/WRITE commands of an UHF EPCglobal compliant reader can be used to select the flags or activate/deactivate features.

The features can only be activated/deactivated (written) using standard EPC WRITE command as long the EPC is not locked. In case the EPC is locked either the bank needs to be unlocked to apply changes or the ChangeConfig custom command is used to change the settings.

The UCODE G2iL is also equipped with the complete UCODE G2X command set for backward compatibility reasons. Nevertheless, the one ChangeConfig command of the G2iL can be used instead of the entire G2X command set.

Bit 14h of the TID indicates the existence of a Configuration Word. This flag will enable selecting Config-Word enhanced transponders in mixed tag populations.

#### 10.7.1 ChangeConfig

Although G2iL is tailored for supply chain management, item level tagging and product authentication the G2iL+ version enables active interaction with products. Among the password protected features are the capability of download firmware to electronics, activate/deactivate electronics which can also be used as theft deterrence, a dedicated privacy mode by reducing the read range, integrated PSF (Product Status Flag) or Tag Tamper Alarm.

The G2iL ChangeConfig custom command allows handling the special NXP Semiconductors features described in the following paragraph. Please also see the memory map in <u>Section 10.6</u> and "<u>Section 10.7.2</u>. If the EPC memory is not write locked the standard EPC READ/WRITE command can be used to change the settings.

## G2iL, G2iL+ special features 1

UCODE G2iL and G2iL+ common special features are:

- Bank wise read protection (separate for EPC and TID)
   EPC bank and the serial number part of the TID can be read protected independently.
   When protected reading of the particular memory will return '0'. The flags of the configuration word can be selected using the standard SELECT<sup>2</sup> command. Only read protected parts will then participate an inventory round. The G2X ReadProtect command will set both EPC and TID read protect flags.
- Integrated PSF (Product Status Flag)

SL3S1203\_1213

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved.

<sup>1</sup> The features can only be manipulated (enabled/disabled) with unlocked EPC bank, otherwise the ChangeConfig command can be used.

<sup>2</sup> SELECT has to be applied onto the Configuration Word with pointer address 200h. Selecting bits within the Configuration Word using a pointer address not equal to 200h is not possible.

The PSF is a general purpose flag that can be used as an EAS (Electronic Article Surveillance) flag, quality checked flag or similar.

The G2iL offers two ways of detecting an activated PSF. In cases extremely fast detection is needed the EAS\_Alarm command can be used. The UCODE G2iL will reply a 64-bit alarm code like described in section EAS\_Alarm upon sending the command. As a second option the EPC SELECT<sup>2</sup> command selecting the PSF flag of the configuration word can be used. In the following inventory round only PSF enabled chips will reply their EPC number.

#### · Backscatter strength reduction

The UCODE G2iL features two levels of backscatter strengths. Per default maximum backscatter is enabled in order to enable maximum read rates. When clearing the flag the strength can be reduced if needed.

#### Real Read Range Reduction 4R

Some applications require the reduction of the read range to close proximity for privacy reasons. Setting the 4R flag will significantly reduce the chip sensitivity to +12 dBm. The +12 dBm have to be available at chip start up (slow increase of field strength is not applicable). For additional privacy, the read protection can be activated in the same configuration step. The related flag of the configuration word can be selected using the standard SELECT<sup>2</sup> command so only chips with reduced read range will be part of an inventory.

**Remark:** The attenuation will result in only a few centimeter of read range at 36 dBm EIRP!

UCODE G2iL+ specific special features are: 1

#### • Tag Tamper Alarm (G2iL+ only)

The UCODE G2iL+ Tamper Alarm will flag the status of the VDD to OUT pad connection which can be designed as an predetermined breaking point (see Figure 6).

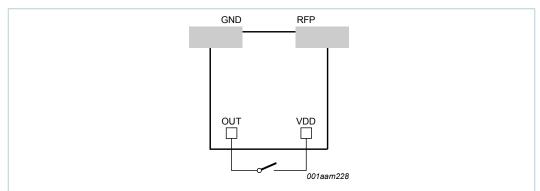


Figure 6. Schematic of connecting VDD and OUT pad with a predetermined breaking point to turn a standard RFID label into a wireless safety seal

The status of the pad connection (open/closed) can be read in the configuration register and/or selected using the EPC SELECT<sup>2</sup> This feature will enable designing a wireless RFID safety seal. When breaking the connection by peeling off the label or manipulating a lock an alarm can be triggered.

### • RF field detection (G2iL+ only)

The UCODE G2iL+ VDD pin can be also used as a RF field detector. Upon bringing the tag within an RF field, a pulse signal will be immediately sent from the VDD test pad. (for details see [3]).

• Digital Switch (G2iL+ only)

SL3S1203\_1213

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved

The UCODE G2iL+ OUT pin can be used as digital switch. The state of the output pad can be switched to VDD or GND depending on the Digital OUT bit of the Configuration Word register. The state of the output is persistent in the memory even after KILL or switching off the supply. This feature will allow activating/deactivating externally connected peripherals or can be used as theft deterrence of electronics. The state of the OUT pin can also be changed temporary by toggling the 'Invert Digital Output' bit.

#### • Data transfer Mode (G2iL+ only)

In applications where not switching the output like described in "Digital Switch" but external device communication is needed the G2iL+ Data Transfer Mode can be used by setting the according bit of the Configuration Word register. When activated the air interface communication will be directly transferred to the OUT pad of the chip. Two modes of data transfer are available and can be switched using the Transparent Mode DATA/RAW bit.

The default Transparent Mode DATA will remove the Frame Sync of the communication and toggle the output with every raising edge in the RF field. This will allow implementing a Manchester type of data transmission.

The Transparent Mode RAW will switch the demodulated air interface communication to the OUT pad.

#### • External Supply Indicator - Digital Input (G2iL+ only)

The VDD pad of the UCODE G2iL+ can be used as a single bit digital input pin. The state of the pad is directly associated with the External Supply Indicator bit of the configuration register. Simple one bit return signaling (chip to reader) can be implemented by polling this Configuration Word register flag. RF reset is necessary for proper polling.

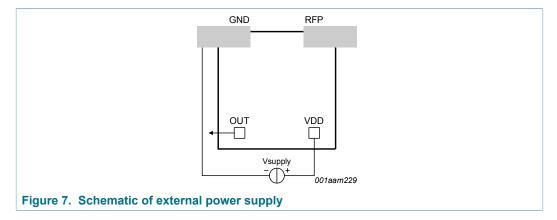
#### • External Supply Mode (G2iL+ only)

The UCODE G2iL+ can be supplied externally by connecting 1.85 V (lout =  $0\mu$ A) supply. When externally supplied less energy from the RF field is needed to operate the chip. This will not just enable further improved sensitivity and read ranges (up to -27 dBm) but also enable a write range that is equal to the read range.

The figure schematically shows the supply connected to the UCODE G2iL+.

**Remark:** When permanently externally supplied there will not be a power-on-reset. This will result in the following limitations:

- When externally supplied session flag S0 will keep it's state during RF-OFF phase.
- When externally supplied session flag S2, S3, SL will have infinite persistence time and will behave similar to S0.
- Session flag S1 will behave regular like in pure passive operation.



SL3S1203\_1213

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved

Table 9. ChangeConfig custom command

| _           | Command              | RFU      | Data                     | RN     | CRC-16 |
|-------------|----------------------|----------|--------------------------|--------|--------|
| No. of bits | 16                   | 8        | 16                       | 16     | 16     |
| Description | 11100000<br>00000111 | 00000000 | Toggle bits<br>XOR RN 16 | handle | -      |

The bits to be toggled in the configuration register need to be set to '1'.

E.g. sending 0000 0000 0001 0001 XOR RN16 will activate the 4R and PSF. Sending the very same command a second time will disable the features again.

The reply of the ChangeConfig will return the current register setting.

Table 10. ChangeConfig custom command reply

|             | Header | Status bits | RN     | CRC-16 |
|-------------|--------|-------------|--------|--------|
| No. of bits | 1      | 16          | 16     | 16     |
| Description | 0      | Config-Word | Handle | -      |

Table 11. ChangeConfig command-response table

| Starting state                 | Condition  | Response   | Next state |
|--------------------------------|--|--|------------|
| ready                          | all  | -  | ready      |
| arbitrate, reply, acknowledged | all  | -  | arbitrate  |
| open                           | valid handle Status word needs to change         | Backscatter unchanged<br>Config-WordConfig-Word<br>immediately | open       |
|                                | valid handle Status word does not need to change | Backscatter Config-Word immediately                            | open       |
| secured                        | valid handle Status word needs to change         | Backscatter modified Config-<br>Word, when done                | secured    |
|                                | valid handle Status word does not need to change | Backscatter Config-Word immediately                            | secured    |
| killed                         | all  | -  | killed     |

The features can only be activated/deactivated using standard EPC WRITE if the EPC bank is unlocked. The permanent and temporary bits of the Configuration Word can be toggled without the need for an ACCESS password in case the ACCESS password is set to zero. In case the EPC bank is locked the lock needs to be removed before applying changes or the ChangeConfig command has to be used.

### 10.7.2 G2iL, G2iL+ special features control mechanism

Special features of the G2iL are managed using a configuration word (Config-Word) located at address 200h in the EPC memory bank.

The entire Config-Word is selectable (using the standard EPC SELECT<sup>3</sup> command) and can be read using standard EPC READ command and modified using the standard EPC WRITE or ChangeConfig custom command in case the EPC memory is locked for writing.

ChangeConfig can be executed from the OPEN and SECURED state.

The chip will take all "Toggle Bits" for '0' if the chip is in the OPEN state or the ACCESS password is zero; therefore it will not alter any status bits, but report the current status only. The command will be ignored with an invalid CRC-16 or an invalid handle. The chip will then remain in the current state. The CRC-16 is calculated from the first command-code bit to the last handle bit.

A ChangeConfig command without frame-sync and proceeding Req\_RN will be ignored. The command will also be ignored if any of the RFU bits are toggled.

In order to change the configuration, to activate/deactivate a feature a '1' has to be written to the corresponding register flag to toggle the status. E.g. sending 0x0002 to the register will activate the read protection of the TID. Sending the same command a second time will again clear the read protection of the TID. Invalid toggling on indicator or RFU bits are ignored.

Executing the command with zero as payload or in the OPEN state will return the current register settings. The chip will reply to a successful ChangeConfig with an extended preamble regardless of the TRext value of the Query command.

After sending a ChangeConfig an interrogator shall transmit CW for less than T<sub>Reply</sub> or 20 ms, where T<sub>Reply</sub> is the time between the interrogator's ChangeConfig command and the chip's backscattered reply. An interrogator may observe three possible responses after sending a ChangeConfig, depending on the success or failure of the operation

- ChangeConfigChangeConfig succeeded: The chip will backscatter the reply shown above comprising a header (a 0-bit), the current Status Word setting, the handle, and a CRC-16 calculated over the 0-bit, the status word and the handle. If the interrogator observes this reply within 20 ms then the ChangeConfig completed successfully.
- The chip encounters an error: The chip will backscatter an error code during the CW period rather than the reply shown below (see EPCglobal Spec for error-code definitions and for the reply format).
- ChangeConfig does not succeed: If the interrogator does not observe a reply within 20 ms then the ChangeStatus did not complete successfully. The interrogator may issue a Req\_RN command (containing the handle) to verify that the chip is still in the interrogator's field, and may reissue the ChangeConfig command.

The G2iL configuration word is located at address 200h of the EPC memory and is structured as following:

SL3S1203\_1213

<sup>3</sup> SELECT has to be applied onto the Configuration Word with pointer address 200h. Selecting bits within the Configuration Word using a pointer address not equal to 200h is not possible.

Table 12. Address 200h to 207h

| Indicator bits   |                           |     | Temporary bits |               |   |                    |     |
|------------------|---------------------------|-----|----------------|---------------|---|--------------------|-----|
| Tamper indicator | External supply indicator | RFU | RFU            | Invert Output |   | Data mode data/raw | RFU |
| 0                | 1                         | 2   | 3              | 4             | 5 | 6                  | 7   |

#### Table 13. Address 208h to 20Fh

| Permanent bits |                           |                |              |     |             |             |                  |
|----------------|---------------------------|----------------|--------------|-----|-------------|-------------|------------------|
| RFU            | max. backscatter strength | Digital output | Privacy mode | RFU | Protect EPC | Protect TID | PSF Alarm<br>bit |
| 8              | 9                         | 10             | 11           | 12  | 13          | 14          | 15               |

The configuration word contains three different type of bits:

Indicator bits cannot be changed by command:
 Tag Tamper Alarm Indicator

External Supply Indicator (digital input)

• Temporary bits are reset at power up:

Invert Output
Transparent Mode on/off

Data Mode data/raw

• Permanent bits: permanently stored bits in the memory

Max. Backscatter Strength

Digital Output

Read Range Reduction

Read Protect EPC

Read Protect TID

**PSF Alarm** 

#### ReadProtect<sup>4</sup>

The G2iL ReadProtect custom command enables reliable read protection of the entire G2iL memory. Executing ReadProtect from the Secured state will set the ProtectEPC and ProtectTID bits of the Configuration Word to '1'. With the ReadProtect-Bit set the G2iL will continue to work unaffected but veil its protected content.

The read protection can be removed by executing Reset ReadProtect. The ReadProtect-Bits will than be cleared.

Devices whose access password is zero will ignore the command. A frame-sync must be pre-pended the command.

After sending the ReadProtect command an interrogator shall transmit CW for the lesser of  $T_{Reply}$  or 20 ms, where  $T_{Reply}$  is the time between the interrogator's ReadProtect command and the backscattered reply. An interrogator may observe three possible responses after sending a ReadProtect, depending on the success or failure of the operation:

 ReadProtect succeeds: After completing the ReadProtect the G2iL shall backscatter the reply shown in <u>Table 15</u> comprising a header (a 0-bit), the tag's handle, and a

SL3S1203\_1213

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved.

<sup>4</sup> Note: The ChangeConfig command can be used instead of "ReadProtect", "ResetReadProtect", "ChangeEAS".

CRC-16 calculated over the 0-bit and handle. Immediately after this reply the G2iL will render itself to this ReadProtect mode. If the interrogator observes this reply within 20 ms then the ReadProtect completed successfully.

- The G2iL encounters an error: The G2iL will backscatter an error code during the CW period rather than the reply shown in the EPCglobal Spec (see Annex I for error-code definitions and for the reply format).
- ReadProtect does not succeed: If the interrogator does not observe a reply within 20 ms then the ReadProtect did not complete successfully. The interrogator may issue a Req\_RN command (containing the handle) to verify that the G2iL is still in the interrogation zone, and may re-initiate the ReadProtect command.

The G2iL reply to the ReadProtect command will use the extended preamble shown in EPCglobal Spec (Figure 6.11 or Figure 6.15), as appropriate (i.e. a Tag shall reply as if TRext=1) regardless of the TRext value in the Query that initiated the round.

Table 14. ReadProtect command

|             | Command           | RN     | CRC-16 |
|-------------|-------------------|--------|--------|
| # of bits   | 16                | 16     | 16     |
| description | 11100000 00000001 | handle | -      |

Table 15. G2iL reply to a successful ReadProtect procedure

|             | Header | RN     | CRC-16 |
|-------------|--------|--------|--------|
| # of bits   | 1      | 16     | 16     |
| description | 0      | handle | -      |

Table 16. ReadProtect command-response table

| Starting State                 | Condition   | Response                      | Next State |
|--------------------------------|---|-------------------------------|------------|
| ready                          | all   | _                             | ready      |
| arbitrate, reply, acknowledged | all   | _                             | arbitrate  |
| open                           | all   | -                             | open       |
| secured                        | valid handle & invalid access password              | _                             | arbitrate  |
|                                | valid handle & valid<br>non zero access<br>password | Backscatter handle, when done | secured    |
|                                | invalid handle                                      | _                             | secured    |
| killed                         | all   | _                             | killed     |

## 10.7.3 Reset ReadProtect<sup>3</sup>

Reset ReadProtect allows an interrogator to clear the ProtectEPC and ProtectTID bits of the Configuration Word. This will re-enable reading of the related G2iL memory content.

For details on the command response please refer to Table 17.

SL3S1203\_1213

After sending a Reset ReadProtect an interrogator shall transmit CW for the lesser of  $T_{Reply}$  or 20 ms, where  $T_{Reply}$  is the time between the interrogator's Reset ReadProtect command and the G2iL backscattered reply. A Req\_RN command prior to the Reset ReadProtect is necessary to successfully execute the command. A frame-sync must be pre-pended the command.

An interrogator may observe three possible responses after sending a Reset ReadProtect, depending on the success or failure of the operation:

- Reset ReadProtect succeeds: After completing the Reset ReadProtect a G2iL will backscatter the reply shown in <u>Table 18</u> comprising a header (a 0-bit), the handle, and a CRC-16 calculated over the 0-bit and handle. If the interrogator observes this reply within 20 ms then the Reset ReadProtect completed successfully.
- The G2iL encounters an error: The G2iL will backscatter an error code during the CW period rather than the reply shown in <u>Table 18</u> (see EPCglobal Spec for error-code definitions and for the reply format).
- Reset ReadProtect does not succeed: If the interrogator does not observe a reply
  within 20 ms then the Reset ReadProtect did not complete successfully. The
  interrogator may issue a Req\_RN command (containing the handle) to verify that
  the G2iL is still in the interrogation zone, and may reissue the Reset ReadProtect
  command.

The G2iL reply to the Reset ReadProtect command will use the extended preamble shown in EPCglobal Spec (Figure 6.11 or Figure 6.15), as appropriate (i.e. a G2iL will reply as if TRext=1 regardless of the TRext value in the Query that initiated the round.

The Reset ReadProtect command is structured as following:

- 16 bit command
- Password: 32 bit Access-Password XOR with 2 times current RN16
   Remark: To generate the 32 bit password the 16 bit RN16 is duplicated and used two times to generate the 32 bit (e.g. a RN16 of 1234 will result in 1234 1234).
- 16 bit handle
- CRC-16 calculate over the first command-code bit to the last handle bit

Table 17. Reset ReadProtect command

|             | Command              | Password                         | RN     | CRC-16 |
|-------------|----------------------|----------------------------------|--------|--------|
| # of bits   | 16                   | 32                               | 16     | 16     |
| description | 11100000<br>00000010 | (access<br>password) ⊗<br>2*RN16 | handle | -      |

Table 18. G2iL reply to a successful Reset ReadProtect command

|             | Header | RN     | CRC-16 |
|-------------|--------|--------|--------|
| # of bits   | 1      | 16     | 16     |
| description | 0      | handle | -      |

Table 19. Reset ReadProtect command-response table

| Starting State                 | Condition                              | Response                      | Next State |
|--------------------------------|--|-------------------------------|------------|
| ready                          | all                                    | _                             | ready      |
| arbitrate, reply, acknowledged | all                                    | _                             | arbitrate  |
| open                           | valid handle & valid access password   | Backscatter handle, when done | open       |
|                                | valid handle & invalid access password | _                             | arbitrate  |
|                                | invalid handle                         | _                             | open       |
| secured                        | valid handle & valid access password   | Backscatter handle, when done | secured    |
|                                | valid handle & invalid access password | _                             | arbitrate  |
|                                | invalid handle                         | _                             | secured    |
| killed                         | all                                    | _                             | killed     |

## 10.7.4 ChangeEAS<sup>3</sup>

UCODE G2iL equipped RFID tags will also feature a stand-alone operating EAS alarm mechanism for fast and offline electronic article surveillance. The PSF bit of the Configuration Word directly relates to the EAS Alarm feature. With an PSF bit set to '1' the tag will reply to an EAS\_Alarm command by backscattering a 64 bit alarm code without the need of a Select or Query. The EAS is a built-in solution so no connection to a backend database is required. In case the EAS\_Alarm command is not implemented in the reader a standard EPC SELCET to the Configuration Word and Query can be used. When using standard SELECT/QUERY the EPC will be returned during inventory.

ChangeEAS can be executed from the Secured state only. The command will be ignored if the Access Password is zero, the command will also be ignored with an invalid CRC-16 or an invalid handle, the G2iL will than remain in the current state. The CRC-16 is calculated from the first command-code bit to the last handle bit. A frame-sync must be pre-pended the command.

The G2iL reply to a successful ChangeEAS will use the extended preamble, as appropriate (i.e. a Tag shall reply as if TRext=1) regardless of the TRext value in the Query that initiated the round.

After sending a ChangeEAS an interrogator shall transmit CW for less than  $T_{Reply}$  or 20 ms, where  $T_{Reply}$  is the time between the interrogator's ChangeEAS command and the G2iL backscattered reply. An interrogator may observe three possible responses after sending a ChangeEAS, depending on the success or failure of the operation

- ChangeEAS succeeds: After completing the ChangeEAS a G2iL will backscatter the
  reply shown in <u>Table 21</u> comprising a header (a 0-bit), the handle, and a CRC-16
  calculated over the 0-bit and handle. If the interrogator observes this reply within
  20 ms then the ChangeEAS completed successfully.
- The G2iL encounters an error: The G2iL will backscatter an error code during the CW period rather than the reply shown in <u>Table 21</u> (see EPCglobal Spec for error-code definitions and for the reply format).
- ChangeEAS does not succeed: If the interrogator does not observe a reply within 20 ms then the ChangeEAS did not complete successfully. The interrogator may

issue a Req\_RN command (containing the handle) to verify that the G2iL is still in the interrogator's field, and may reissue the ChangeEAS command.

Upon receiving a valid ChangeEAS command a G2iL will perform the commanded set/reset operation of the PSF bit of the Configuration Word.

If PSF bit is set, the EAS\_Alarm command will be available after the next power up and reply the 64 bit EAS code upon execution. Otherwise the EAS\_Alarm command will be ignored.

Table 20. ChangeEAS command

|             | - table 201 Ontaing 022 to Community |                                  |        |        |  |
|-------------|--------------------------------------|----------------------------------|--------|--------|--|
|             | Command                              | ChangeEAS                        | RN     | CRC-16 |  |
| # of bits   | 16                                   | 1                                | 16     | 16     |  |
| description | 11100000<br>00000011                 | 1 set PSF bit<br>0 reset PSF bit | handle |        |  |

Table 21. G2iL reply to a successful ChangeEAS command

|             | Header | RN     | CRC-16 |
|-------------|--------|--------|--------|
| # of bits   | 1      | 16     | 16     |
| description | 0      | handle | -      |

Table 22. ChangeEAS command-response table

| Starting State                 | Condition      | Response                      | Next state |
|--------------------------------|----------------|-------------------------------|------------|
| ready                          | all            | _                             | ready      |
| arbitrate, reply, acknowledged | all            | _                             | arbitrate  |
| open                           | all            | _                             | open       |
| secured                        | valid handle   | backscatter handle, when done | secured    |
|                                | invalid handle | _                             | secured    |
| killed                         | all            | _                             | killed     |

#### 10.7.5 EAS Alarm

Upon receiving an EAS\_Alarm custom command the UCODE G2iL will immediately backscatter an EAS-Alarmcode in case the PSF bit of the Configuration Word is set. The alarm code is returned without any delay caused by Select, Query and without the need for a backend database.

The EAS feature of the G2iL is available after enabling it by sending a ChangeEAS command described in Section 10.7.4 or after setting the PSF bit of the Configuration Word to '1'. With the EAS-Alarm enabled the G2iL will reply to an EAS\_Alarm command by backscattering a fixed 64 bit alarm code. A G2iL will reply to an EAS\_Alarm command from the ready state only. As an alternative to the fast EAS\_Alarm command a standard SELECT <sup>2</sup> (upon the Configuration Word) and QUERY can be used.

If the PSF bit is reset to '0' by sending a ChangeEAS command in the password protected Secure state or clearing the PSF bit the G2iL will not reply to an EAS\_Alarm command.

The EAS Alarm command is structured as following:

- 16 bit command
- 16 bit inverted command
- DR (TRcal divide ratio) sets the T=>R link frequency as described in EPCglobal Spec. 6.3.1.2.8 and Table 6.9.
- M (cycles per symbol) sets the T=>R data rate and modulation format as shown in EPCglobal Spec. Table 6.10.
- TRext chooses whether the T=>R preamble is pre-pended with a pilot tone as described in EPCglobal Spec. 6.3.1.3.

A preamble must be pre-pended the EAS\_Alarm command according EPCglobal Spec, 6.3.1.2.8.

Upon receiving an EAS\_Alarm command the tag loads the CRC5 register with 01001b and backscatters the 64 bit alarm code accordingly. The reader is now able to calculate the CRC5 over the backscattered 64 bits received to verify the received code.

Table 23. EAS Alarm command

|             | Command                   | Inv_Command          | DR                        | М  | TRext                                       | CRC-16 |
|-------------|---------------------------|----------------------|---------------------------|--|---|--------|
| # of bits   | 16                        | 16                   | 1                         | 2  | 1   | 16     |
| description | 11100000 <b>0 0000100</b> | 00011111<br>11111011 | 0: DR = 8<br>1: DR = 64/3 | 00: M = 1<br>01: M = 2<br>10: M = 4<br>11: M = 8 | 0: no pilot<br>tone<br>1: use pilot<br>tone | -      |

Table 24. G2iL reply to a successful EAS\_Alarm command

|             | Header | EAS Code   |
|-------------|--------|------------|
| # of bits   | 1      | 64         |
| description | 0      | CRC5 (MSB) |

Table 25. EAS\_Alarm command-response table

| Starting State                 | Condition                            | Response               | Next state |
|--------------------------------|--------------------------------------|------------------------|------------|
| ready                          | PSF bit is set<br>PSF bit is cleared | backscatter alarm code | ready      |
| arbitrate, reply, acknowledged | all                                  | _                      | arbitrate  |
| open                           | all                                  | _                      | open       |
| secured                        | all                                  | _                      | secured    |
| killed                         | all                                  | _                      | killed     |

## 11 Limiting values

## Table 26. Limiting values<sup>[1][2]</sup>

In accordance with the Absolute Maximum Rating System (IEC 60134).

Voltages are referenced to RFN

| Symbol           | Parameter                       | Conditions  |         | Min  | Max  | Unit |
|------------------|---------------------------------|---|---------|------|------|------|
| Bare die ar      | nd SOT886 limitations           |   |         |      |      |      |
| T <sub>stg</sub> | storage temperature             |   |         | -55  | +125 | °C   |
| T <sub>amb</sub> | ambient temperature             |   |         | -40  | +85  | °C   |
| V <sub>ESD</sub> | electrostatic discharge voltage | Human body model                                  | [3] [4] | _    | ± 2  | kV   |
| Pad limitat      | ions                            |   |         |      |      |      |
| Vi               | input voltage                   | absolute limits, VDD-OUT pad                      |         | -0.5 | +2.5 | V    |
| l <sub>o</sub>   | output current                  | absolute limits input/output current, VDD-OUT pad |         | -0.5 | +0.5 | mA   |
| P <sub>i</sub>   | input power                     | maximum power dissipation, RFP pad                |         | -    | 100  | mW   |

<sup>[1]</sup> Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in the Operating Conditions and Electrical Characteristics section of this specification is not implied.

#### **CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

<sup>[2]</sup> This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.

<sup>3]</sup> ANSI/ESDA/JEDEC JS-001

<sup>[4]</sup> For ESD measurement, the die chip has been mounted into a CDIP20 package.

### 12 Characteristics

### 12.1 UCODE G2iL, G2iL+ bare die characteristics

Table 27. G2iL. G2iL+ RF interface characteristics (RFN, RFP)

| Symbol              | Parameter                    | Conditions   |             | Min | Тур      | Max | Unit |
|---------------------|------------------------------|--|-------------|-----|----------|-----|------|
| f <sub>i</sub>      | input frequency              |  |             | 840 | -        | 960 | MHz  |
| Normal m            | ode - no external supply,    | read range reduction OFF                             |             |     |          |     |      |
| P <sub>i(min)</sub> | minimum input power          | READ sensitivity                                     |             | -   | -18      | -   | dBm  |
| P <sub>i(min)</sub> | minimum input power          | WRITE sensitivity, (write range/ read range - ratio) |             | -   | 30       | -   | %    |
| C <sub>i</sub>      | input capacitance            | parallel   | [4]         | -   | 0.77     | -   | pF   |
| Q                   | quality factor               | 915 MHz  | [4]         | -   | 9.7      | -   | -    |
| Z                   | impedance                    | 866 MHz  | [4]         | -   | 25 -j237 | -   | Ω    |
|                     |                              | 915 MHz  | [4]         | -   | 23 -j224 | -   | Ω    |
|                     |                              | 953 MHz  | [4]         | -   | 21 -j216 | -   | Ω    |
| External s          | upply mode - VDD pad su      | pplied, read range reduction OFF                     |             |     |          |     |      |
| P <sub>i(min)</sub> | minimum input power          | Ext. supplied READ                                   | [1] [2]     | -   | -27      | -   | dBm  |
|                     |                              | Ext. supplied WRITE                                  | [2]         | -   | -27      | -   | dBm  |
| Z                   | impedance                    | externally supplied, 915 MHz                         | [4]         | -   | 7 -j230  | -   | Ω    |
| Read rang           | e reduction ON - no<br>upply |  |             |     |          |     |      |
| P <sub>i(min)</sub> | minimum input power          | 4R on READ   | [1] [2] [5] | -   | +12      | -   | dBm  |
|                     |                              | 4R on WRITE  | [2] [5]     | -   | +12      | -   | dBm  |
| Z                   | impedance                    | 4R on, 915 MHz                                       | [4]         | -   | 18 -j2   | -   | Ω    |
| Modulatio           | n resistance                 |  |             |     |          |     |      |
| R                   | resistance                   | modulation resistance, max. backscatter = off        | [6]         | -   | 170      | -   | Ω    |
|                     |                              | modulation resistance, max. backscatter = on         | [7]         | -   | 55       | -   | Ω    |

<sup>[1]</sup> [2] [3]

Power to process a Query command. Measured with a 50  $\Omega$  source impedance. Results in approx. -18.5 dBm tag sensitivity on a 2 dBi gain antenna.

At minimum operating power.

<sup>[4]</sup> [5] It has to be assured the reader (system) is capable of providing enough field strength to give +12 dBm at the chip otherwise communication with the chip will not be possible.

Enables tag designs to be within ETSI limits for return link data rates of e.g. 320 kHz/M4. Will result in up to 10 dB higher tag backscatter power at high field strength.

Table 28. VDD pin characteristics

| Symbol              | Parameter                                      | Conditions                                  |                | Min | Тур | Max  | Unit |
|---------------------|--|---|----------------|-----|-----|------|------|
| Minimum             | supply voltage/current - w                     | ithout assisted EEPROM WRITE                | [1] [2]<br>[3] |     |     |      |      |
| $V_{DD}$            | supply voltage                                 | minimum voltage                             |                | -   | -   | 1.8  | V    |
| I <sub>DD</sub>     | supply current                                 | minimum current, I <sub>out-^-</sub> = 0 μA |                | -   | -   | 7    | μΑ   |
|                     |  | I <sub>out</sub> = 100 μA                   |                | -   | -   | 110  | μΑ   |
| Minimum             | supply voltage/current - as                    | ssisted EEPROM READ and WRITE               | [4] [2]<br>[3] |     |     |      |      |
| $V_{DD}$            | supply voltage                                 | minimum voltage, I <sub>out</sub> = 0 μA    |                | -   | 1.8 | 1.85 | V    |
|                     |  | I <sub>out</sub> = 100 μA                   |                | -   | -   | 1.95 | V    |
| I <sub>DD</sub>     | supply current                                 | minimum current, I <sub>out</sub> = 0 μA    |                | -   | -   | 125  | μA   |
|                     |  | I <sub>out</sub> = 100 μA                   |                | -   | -   | 265  | μΑ   |
| Maximum             | supply voltage/current                         |   | [2] [5]        |     |     |      |      |
| $V_{DD}$            | supply voltage                                 | absolute maximum voltage                    |                | 2.2 | -   | -    | V    |
| I <sub>i(max)</sub> | maximum input current absolute maximum current |   |                | 280 | -   | -    | μA   |

- Activates Digital Output (OUT pin), increases read range (external supplied).
- Operating the chip outside the specified voltage range may lead to undefined behaviour.
- Either the voltage or the current needs to be above given values to guarantee specified functionality.
- Activates Digital Output (OUT pin), increases read and write range (external supplied).
- No proper operation is guaranteed if both, voltage and current, limits are exceeded.

#### Table 29. G2iL, G2iL+ VDD and OUT pin characteristics

| Symbol              | Parameter                        | Conditions                              |     | Min | Тур | Max | Unit |
|---------------------|----------------------------------|---|-----|-----|-----|-----|------|
| OUT pin             | characteristics                  |   |     |     |     |     |      |
| V <sub>OL</sub>     | Low-level output voltage         | Isink = 1 mA                            |     | -   | -   | 100 | mV   |
| V <sub>OH</sub>     | HIGH-level output voltage        | VDD = 1.8 V; Isource<br>= -100 μA       |     | 1.5 | -   | -   | V    |
| VDD/OUT             | pin characteristics              |   |     |     |     |     |      |
| C <sub>L</sub>      | load capacitance                 | VDD - OUT pin max.                      | [1] | -   | -   | 5   | pF   |
| V <sub>o</sub>      | output voltage                   | maximum RF peak voltage on VDD-OUT pins | [2] | -   | -   | 500 | mV   |
| VDD/OUT             | pin tamper alarm characteristics |   | [3] |     |     |     |      |
| R <sub>L(max)</sub> | maximum load resistance          | resistance range high                   | [4] | -   | -   | <2  | ΜΩ   |
| R <sub>L(min)</sub> | minimum load resistance          | resistance range low                    | [5] | >20 | -   | -   | ΜΩ   |

- Is the sum of the allowed capacitance of the VDD and OUT pin referenced to RFN.
- Is the maximum allowed RF input voltage coupling to the VDD/OUT pin to guarantee undisturbed chip functionality.
- [3] [4] [5] Resistance between VDD and OUT pin in checked during power up only.
- Resistance range to achieve tamper alarm flag = 1.
- Resistance range to achieve tamper alarm flag = 0:

For further reading we recommend application note "FAQ UCODE G2iL+" ([3]) describing the output characteristics more in detail. An example schematic is available in application

SL3S1203\_1213

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved.

note "UCODE G2iL+ Demo board Manual" ([4]). The documents are available at NXP Document Control or at the website www.nxp.com.

Table 30. G2iL, G2iL+ memory characteristics

| Symbol                 | Parameter       | Conditions               |  | Min  | Тур                  | Max | Unit  |
|------------------------|-----------------|--------------------------|--|------|----------------------|-----|-------|
| EEPROM characteristics |                 |                          |  |      |                      |     |       |
| t <sub>ret</sub>       | retention time  | T <sub>amb</sub> ≤ 55 °C |  | 20   | -                    | -   | year  |
| N <sub>endu(W)</sub>   | write endurance |                          |  | 1000 | 10000 <sup>[1]</sup> | -   | cycle |

<sup>[1]</sup>  $T_{amb} \le 25 \,^{\circ}C$ 

#### 12.2 UCODE G2iL SOT886 characteristics

Table 31. G2iL RF interface characteristics (RFN, RFP)

| Symbol              | Parameter  | Conditions       |          | Min | Тур       | Max | Unit    |  |  |  |
|---------------------|--|------------------|----------|-----|-----------|-----|---------|--|--|--|
| Normal mo           | Normal mode - no external supply, read range reduction OFF |                  |          |     |           |     |         |  |  |  |
| P <sub>i(min)</sub> | minimum input power  | READ sensitivity | [1][2]   | -   | -17.6     | -   | dB<br>m |  |  |  |
| Z                   | impedance  | 915 MHz          | [3]      | -   | 21 -j199  | -   | Ω       |  |  |  |
| Normal mo           | de - externally supplied, r                                | ead range reduc  | ction OF | F   |           |     |         |  |  |  |
| P <sub>i(min)</sub> | minimum input power  | READ sensitivity | [1][2]   | -   | -27       | -   | dB<br>m |  |  |  |
| Z                   | impedance  | 915 MHz          | [3]      | -   | 5.6 -j204 | -   | Ω       |  |  |  |

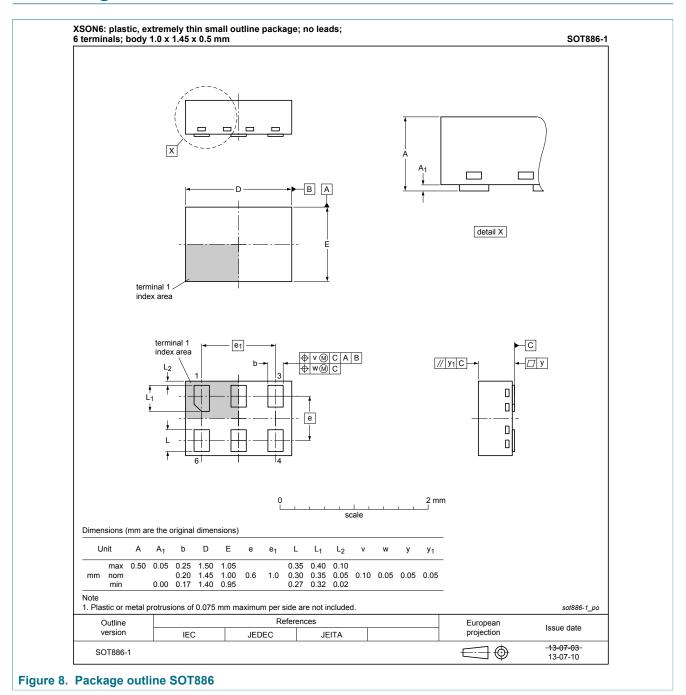
<sup>[1]</sup> Power to process a Query command.

Remark: For DC and memory characteristics refer to Table 28, Table 29 and Table 30.

<sup>[2]</sup> Measured with a 50  $\Omega$  source impedance.

<sup>[3]</sup> At minimum operating power.

# 13 Package outline



UCODE G2iL and G2iL+

## 14 Packing information

#### **14.1 Wafer**

See [2]

### 14.2 SOT886

Part orientation T1. For details please refer to <a href="http://www.standardics.nxp.com/packaging/packing/pdf/sot886.t1.t4.pdf">http://www.standardics.nxp.com/packaging/packing/pdf/sot886.t1.t4.pdf</a>

## 15 Abbreviations

Table 32. Abbreviations

| Acronym | Description   |
|---------|---|
| CRC     | Cyclic Redundancy Check   |
| CW      | Continuous Wave   |
| DSB-ASK | Double Side Band-Amplitude Shift Keying   |
| DC      | Direct Current  |
| EAS     | Electronic Article Surveillance   |
| EEPROM  | Electrically Erasable Programmable Read Only Memory   |
| EPC     | Electronic Product Code (containing Header, Domain Manager, Object Class and Serial Number) |
| FM0     | Bi phase space modulation   |
| G2      | Generation 2  |
| IC      | Integrated Circuit  |
| PIE     | Pulse Interval Encoding   |
| RRRR    | Real Read Range Reduction   |
| PSF     | Product Status Flag   |
| RF      | Radio Frequency   |
| UHF     | Ultra High Frequency  |
| SECS    | Semi Equipment Communication Standard   |
| TID     | Tag IDentifier  |

**UCODE G2iL and G2iL+** 

### 16 References

- [1] EPCglobal: EPC Radio-Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz 960 MHz, Version 1.1.0 (December 17, 2005)
- [2] Data sheet Delivery type description General specification for 8" wafer on UV-tape with electronic fail die marking, BU-ID document number: 1093\*\*<sup>5</sup>
- [3] Application note AN10840 FAQ UCODE G2i
- [4] Application note AN11237 UCODE G2iM+ demo board documentation

## 17 Revision history

## Table 33. Revision history

| Table 33. Revision hist | ory   |                              |                     |                          |
|-------------------------|---|------------------------------|---------------------|--------------------------|
| Document ID             | Release date  | Data sheet status            | Change notice       | Supersedes               |
| SL3S1203_1213 v.4.5     | 20190212  | Product data sheet           | -                   | SL3S1203_1213 v.4.4      |
| Modifications:          | <u>Section 16</u> : updated   |                              |                     |                          |
| SL3S1203_1213 v.4.4     | 20140317  | Product data sheet           | -                   | SL3S1203_1213 v.4.3      |
| Modifications:          | <ul> <li><u>Table 8</u>: Table notes upo</li> <li><u>Figure 5</u>: TIDs updated</li> </ul>                                    | lated                        |                     |                          |
| SL3S1203_1213 v.4.3     | 20131127  | Product data sheet           | -                   | SL3S1203_1213 v.4.2      |
| Modifications:          | Figure 5: updated   |                              |                     |                          |
| SL3S1203_1213 v.4.2     | 20130701  | Product data sheet           | -                   | SL3S1203_1213 v.4.1      |
| Modifications:          | <ul><li>Update of delivery form</li><li>Update RF field detection</li></ul>   | n                            |                     |                          |
| SL3S1203_1213 v.4.1     | 20120917  | Product data sheet           | -                   | SL3S1203_1213 v.4.0      |
| Modifications:          | Update of delivery form   |                              |                     |                          |
| SL3S1203_1213 v.4.0     | 20120227  | Product data sheet           | -                   | SL3S1203_1213 v.3.9      |
| Modifications:          | Figure 4 "G2iL wafer layer  | out": Figure notes (1) and   | (2) updated         |                          |
| SL3S1203_1213 v.3.9     | 20120130  | Product data sheet           | -                   | SL3S1203_1213 v.3.8      |
| Modifications:          | <ul><li>Table 6 "Specifications":</li><li>Section 15.2.1 "General</li></ul>   |                              |                     |                          |
| SL3S1203_1213 v.3.8     | 20120111  | Product data sheet           | -                   | SL3S1203_1213 v.3.7      |
| Modifications:          | Section 8.1 "Wafer layout   | ıt": Figure notes (1) and (2 | ?) updated          |                          |
| SL3S1203_1213 v.3.7     | 20111124  | Product data sheet           | -                   | SL3S1203_1213 v.3.6      |
| Modifications:          | <ul><li>Table 11 "G2iL, G2iL+ o</li><li>Table 34 "G2iL, G2iL+ R</li></ul>   | • • •                        |                     | dated                    |
| SL3S1203_1213 v.3.6     | 20110803  | Product data sheet           | -                   | SL3S1203_1213 v.3.5      |
| Modifications:          | Real Read Range Reduce  | ction feature added to G2i   | Ĺ                   |                          |
| SL3S1203_1213 v.3.5     | 20110531  | Product data sheet           | -                   | SL3S1203_1213 v.3.4      |
| Modifications:          | Superfluous text remove   | d from Table 6               |                     |                          |
| SL3S1203_1213 v.3.4     | 20110511  | Product data sheet           | -                   | SL3S1203_1213 v.3.3      |
| Modifications:          | <ul> <li>Security status changed</li> <li>Delivery form of FCS2 st</li> <li>Section 13 "Package information" added</li> </ul> | rap added                    | ndling information' | ' and Section 16 "Packin |
| SL3S1203_1213 v.3.3     | 20110131  | Product data sheet           | -                   | SL3S1203_1213 v.3.2      |
| Modifications:          | <ul> <li>Section 4 "Ordering infor</li> <li>Section 9 "Mechanical sp</li> <li>Replaced wording of "Ch</li> </ul>              | pecification": updated acco  | ording to the new   |                          |
| SL3S1203_1213 v.3.2     | 20101109  | Product data sheet           | -                   | SL3S1203_1213 v.3.1      |
|                         |   |                              |                     |                          |

SL3S1203\_1213

UCODE G2iL and G2iL+

| Document ID         | Release date  | Data sheet status    | Change notice     | Supersedes          |
|---------------------|---|----------------------|-------------------|---------------------|
| Modifications:      | Version SOT886F1 adde     Section 5 "Marking", Sec<br>added | <del></del>          | and Section 14 "P | acking information" |
| SL3S1203_1213 v.3.1 | 20100922  | Product data sheet   | -                 | SL3S1203_1213 v.3.0 |
| Modifications:      | General Modifications                                       |                      |                   |                     |
| SL3S1203_1213 v.3.0 | 20100621  | Product data sheet   | -                 | 178810              |
| Modifications:      | General update  | '                    | ,                 |                     |
| 178810              | 20100304  | Objective data sheet | -                 | -                   |

## 18 Legal information

#### 18.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <a href="http://www.nxp.com">http://www.nxp.com</a>.

#### 18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

#### 18.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

SL3S1203\_1213

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2019. All rights reserved.

**UCODE G2iL and G2iL+** 

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications. In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall

use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

#### 18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

UCODE — is a trademark of NXP B.V.

UCODE G2iL and G2iL+

## **Tables**

| Tab. 1.  | Ordering information5                  | Tab. 19. | Reset ReadProtect command-response       |    |
|----------|--|----------|--|----|
| Tab. 2.  | Marking codes6                         |          | table                                    | 25 |
| Tab. 3.  | Pin description bare die 8             | Tab. 20. | ChangeEAS command                        |    |
| Tab. 4.  | Pin description SOT8868                | Tab. 21. | G2iL reply to a successful ChangeEAS     |    |
| Tab. 5.  | Specifications 10                      |          | command                                  | 26 |
| Tab. 6.  | Overview of G2iL and G2iL+ features 13 | Tab. 22. | ChangeEAS command-response table         | 26 |
| Tab. 7.  | G2iL memory sections                   | Tab. 23. | EAS Alarm command                        | 27 |
| Tab. 8.  | G2iL, G2iL+ overall memory map 14      | Tab. 24. | G2iL reply to a successful EAS Alarm     |    |
| Tab. 9.  | ChangeConfig custom command20          |          | command                                  | 27 |
| Tab. 10. | ChangeConfig custom command reply 20   | Tab. 25. | EAS_Alarm command-response table         | 27 |
| Tab. 11. | ChangeConfig command-response table 20 | Tab. 26. | Limiting values                          | 28 |
| Tab. 12. | Address 200h to 207h22                 | Tab. 27. | G2iL, G2iL+ RF interface characteristics |    |
| Tab. 13. | Address 208h to 20Fh 22                |          | (RFN, RFP)                               | 29 |
| Tab. 14. | ReadProtect command23                  | Tab. 28. | VDD pin characteristics                  | 30 |
| Tab. 15. | G2iL reply to a successful ReadProtect | Tab. 29. | G2iL, G2iL+ VDD and OUT pin              |    |
|          | procedure                              |          | characteristics                          | 30 |
| Tab. 16. | ReadProtect command-response table23   | Tab. 30. | G2iL, G2iL+ memory characteristics       | 31 |
| Tab. 17. | Reset ReadProtect command24            | Tab. 31. | G2iL RF interface characteristics (RFN,  |    |
| Tab. 18. | G2iL reply to a successful Reset       |          | RFP)                                     | 31 |
|          | ReadProtect command24                  | Tab. 32. | Abbreviations                            |    |
|          |  | Tab. 33. | Revision history                         | 36 |
|          |  |          |  |    |

SL3S1203\_1213

UCODE G2iL and G2iL+

## **Figures**

| Fig. 1. | Block diagram of G2iL IC7     | Fig. 6. | Schematic of connecting VDD and OUT pad      |    |
|---------|-------------------------------|---------|--|----|
| Fig. 2. | Pinning bare die8             |         | with a predetermined breaking point to turn  |    |
| Fig. 3. | Pin configuration for SOT8868 |         | a standard RFID label into a wireless safety |    |
| Fig. 4. | G2iL wafer layout9            |         | seal   | 18 |
| Fig. 5. | G2iL TID memory structure16   | Fig. 7. | Schematic of external power supply           | 19 |
| Ü       | •                             | Fig. 8. | Package outline SOT886                       | 32 |

### **Contents**

| 1               | General description1                         |   |
|-----------------|--|---|
| 2               | Features and benefits2                       |   |
| 2.1             | Key features 2                               | 2 |
| 2.1.1           | Memory2                                      | 2 |
| 2.2             | Key benefits2                                | 2 |
| 2.2.1           | End user benefit2                            |   |
| 2.2.2           | Antenna design benefits2                     |   |
| 2.2.3           | Label manufacturer benefit3                  |   |
| 2.3             | Custom commands                              |   |
| 3               | Applications4                                |   |
| 3.1             | Markets4                                     |   |
| 3.2             | Applications4                                |   |
| 3.2<br><b>4</b> | Ordering information                         |   |
| •               |  |   |
| 5               | Marking6                                     |   |
| 6               | Block diagram7                               |   |
| 7               | Pinning information                          |   |
| 7.1             | Pin description8                             |   |
| 8               | Wafer layout9                                |   |
| 8.1             | Wafer layout9                                | ) |
| 9               | Mechanical specification10                   |   |
| 9.1             | Wafer specification10                        | ) |
| 9.1.1           | Wafer 10                                     | ) |
| 9.1.2           | Fail die identification11                    | i |
| 9.1.3           | Map file distribution11                      | ĺ |
| 10              | Functional description12                     | 2 |
| 10.1            | Air interface standards12                    |   |
| 10.2            | Power transfer                               |   |
| 10.3            | Data transfer                                |   |
| 10.3.1          | Reader to tag Link                           |   |
| 10.3.2          | Tag to reader Link                           |   |
| 10.3.2          | G2iL and G2iL+ differences                   |   |
| 10.4            | Supported commands                           |   |
| 10.5            | G2iL, G2iL+ memory13                         |   |
| 10.6.1          |  |   |
| 10.6.1          | G2iL, G2iL+ overall memory map14             |   |
| 10.6.2          | G2iL TID memory details                      | , |
|                 |  |   |
| 10.7.1          | ChangeConfig17                               | • |
| 10.7.2          | G2iL, G2iL+ special features control         |   |
|                 | mechanism21                                  |   |
| 10.7.3          | Reset ReadProtect3                           |   |
| 10.7.4          | ChangeEAS325                                 |   |
| 10.7.5          | EAS_Alarm26                                  |   |
| 11              | Limiting values28                            |   |
| 12              | Characteristics29                            |   |
| 12.1            | UCODE G2iL, G2iL+ bare die characteristics29 |   |
| 12.2            | UCODE G2iL SOT886 characteristics31          |   |
| 13              | Package outline32                            |   |
| 14              | Packing information33                        |   |
| 14.1            | Wafer33                                      |   |
| 14.2            | SOT88633                                     |   |
| 15              | Abbreviations34                              |   |
| 16              | References                                   |   |
| 17              | Revision history36                           |   |
| • •             |  | • |

| 18 Legal i | nformation | 38 |
|------------|------------|----|
|------------|------------|----|

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2019.

All rights reserved.