Digital Design and Computer Architecture LU

Lab Protocol

Exercise I

Hasan Ismail Yilmaz, 12019840
e12019840@student.tuwien.ac.at

Vienna, April 7, 2022

Task 1: Introduction and Preparations

Subtask 1

Create a screenshot of the RTL netlist viewer, showing how the outputs of the PLL are connected to the rest of the system!

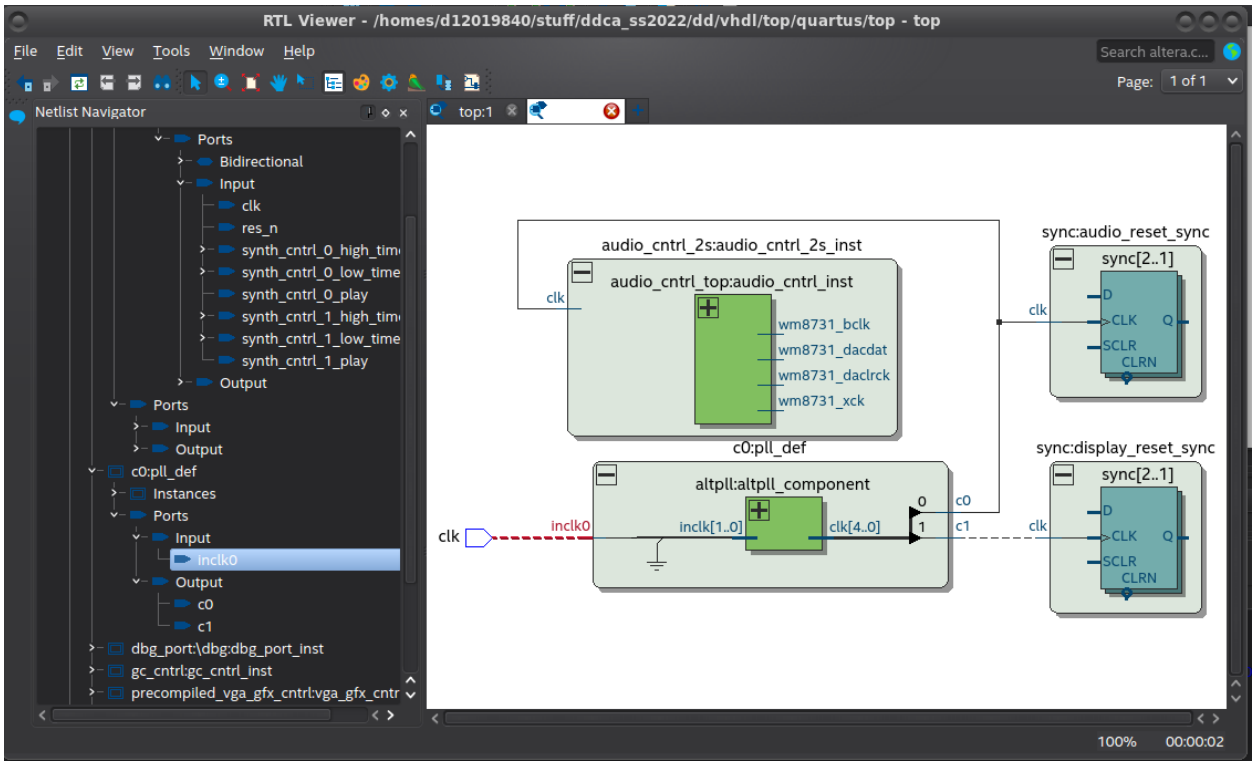

Figure 1: RTL netlist viewer screenshot

END Subtask 1

Task 2: GameCube Controller

Subtask 2

Analyse the resource usage of your gc_cntrl! You can find this information in the compilation report under the entry “Analysis&Synthesis”.

	Combinational ALUTs	Dedicated Logic Registers
Absolute number	153	197
% of whole design	3.9%	7.36%
% of whole FPGA resources		

END Subtask 2

Task 3: Decimal Printer

Subtask 3

Include the state graph of the state machine you designed and briefly explain how it works.

You can use `dia` to draw the diagram. The provided makefile automatically converts dia files to PDFs and places them in the `dia/pdf` directory. However, any other method for drawing pictures is also fine.

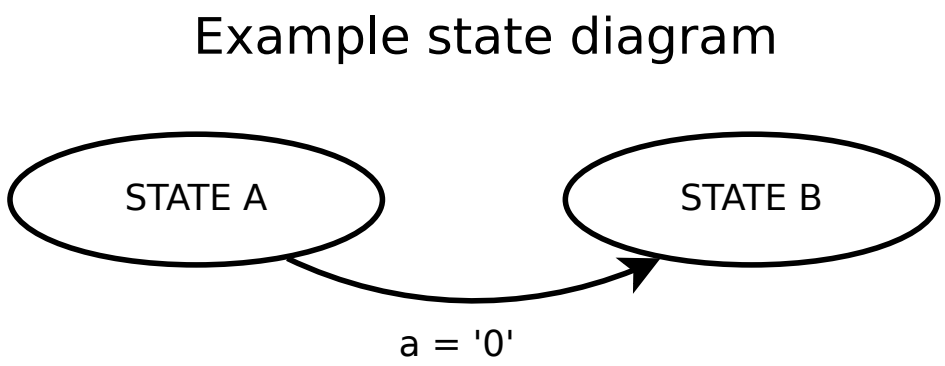

Figure 2: FSM state graph

END Subtask 3