ELEN0040 – Digital Electronics
2024 - Introduction to laboratories

LIÈGE université
Sciences Appliquées

Arthur Fyon
afyon@uliege.be

Contact & information

- Teaching assistants:
  - Anaïs Halin (anais.halin@uliege.be) → Tutorials
  - Arthur Fyon (afyon@uliege.be) → Labs & Project
    Office: 1.15 @ B28 Montefiore

- Course materials:
  - ~~Website (link)~~
  - Everything on myUliege

Organization

- 2 mandatory lab sessions:
  - 1st Combinatorial and sequential logic
  - 2nd Introduction to VHDL programming
- Organization (labs are **MANDATORY**: if not realized, no final grades):
  - **How?** Lab sessions realized by groups of 4 students (⚠ same group as the one for the project)
  - **What?** 2 sessions of 4h (half a day)
  - **Where?** R100 @ B28 Montefiore (at the end of the hallway in front of you when you enter the main door)
  - **When?** Fill in the Forms with your group number of your team (here). Schedule will be realized using these Forms results. Please, fill the Forms with **all** the possibilities of your group in order to facilitate the organization (if you still don't have a group by the deadline, fill in the Forms alone)
  - **Deadline:** next Friday 01/03/2022

R100 equipments: bench

R100 equipments: power button

R100 equipments: multimeter

R100 equipments: multimeter

- Current OR voltage measurement (not both at the same time!)
  - AC or DC mode
  - Different measurement ranges
- Resistance and capacitance measurements
- Continuity measurement
- Frequency measurement
- And many others

Always check that the terminals you are using are coherent with the measurement you want to perform !

R100 equipments: oscilloscope

R100 equipments: oscilloscope

Main settings:

- Time scale
- Voltage scale
- Voltage/time offset
- Trigger position
- Channel display
- Automatic measurements
- And many others

R100 equipments: DC voltage generator

R100 equipments: DC voltage generator

- 2 equivalent models depending on the bench
- 0V-30V with current limiters

R100 equipments: AC voltage generator

R100 equipments: AC voltage generator

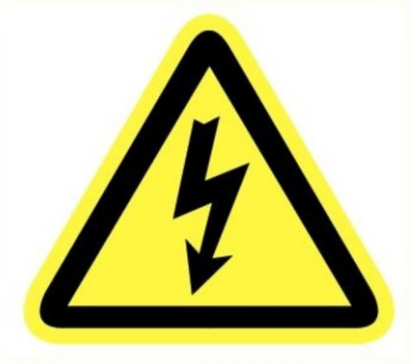
Main settings:

- Frequency range
- Fine tune of the frequency
- Voltage amplitude
- Voltage offset
- Wave form (sine, square, triangle)
- Attenuator of -20/40 dB

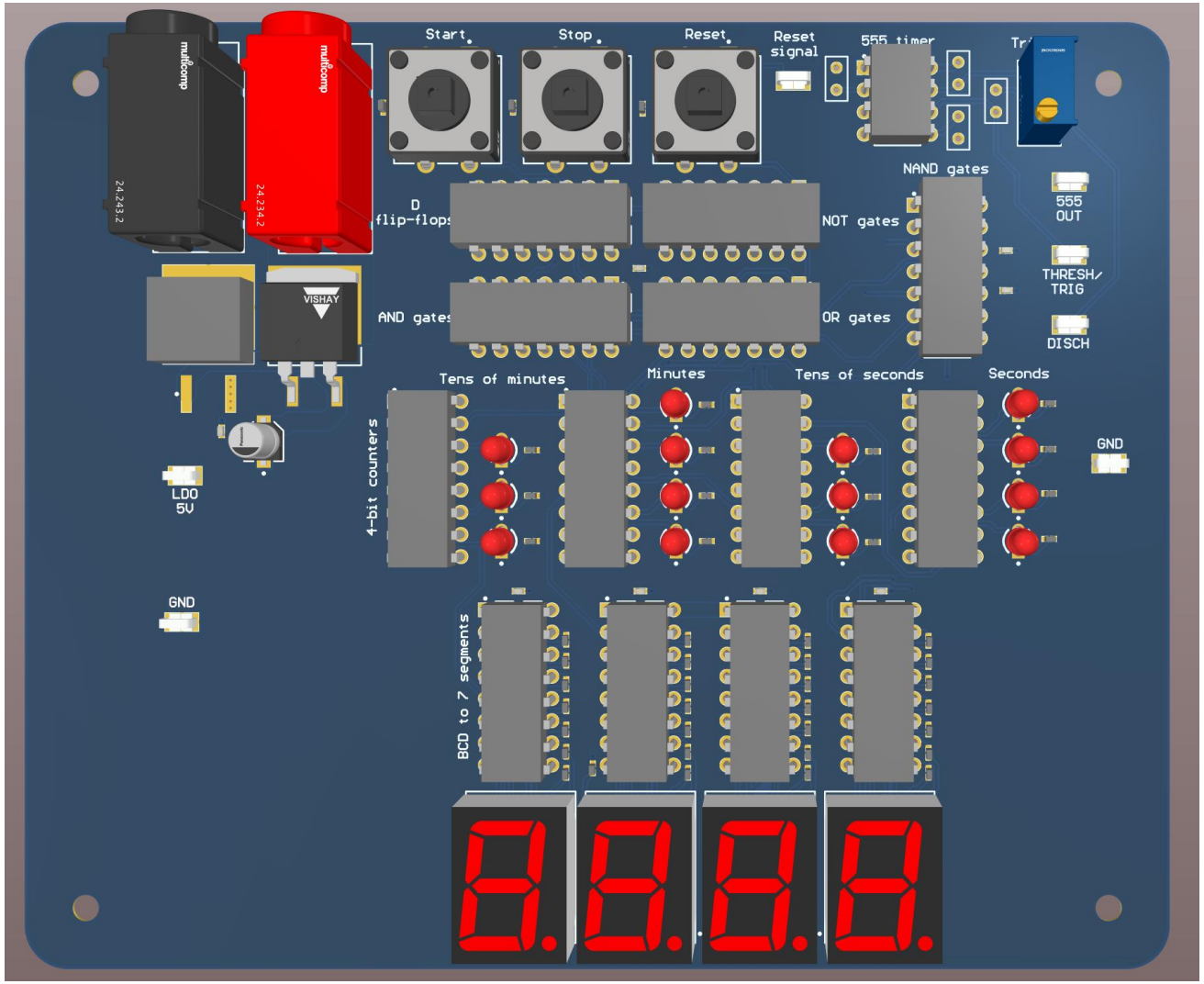
Safety notice

- Male and female plugs must fit → don't force it
- Set up your equipment properly before powering up
- Be careful with exposed wires and connections
- Take care with metallic objects (that might be electrical conductors)
- When in doubt, **ask!**

You are the actor of your own safety!



1st laboratory: Combinatorial and sequential logic

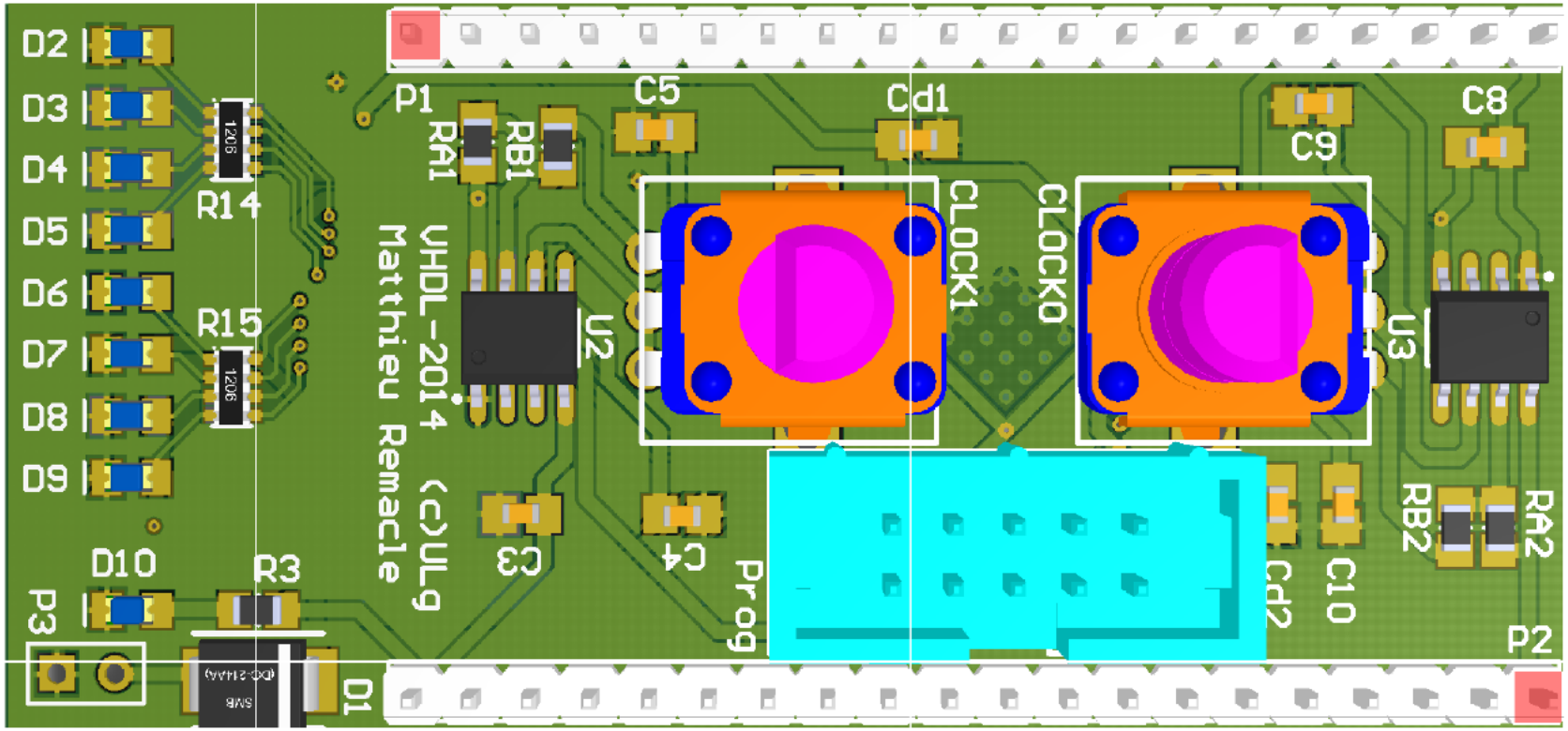


You will learn to construct a digital clock using:

- 555 timer
- 4-bit counters
- logic gates
- LEDs
- 7-segment displays
- and others

Read the introduction of the pdf document *ELEN0040_Lab_1__Instruction.pdf*. Install Logisim on your laptop **BEFORE** attending the lab (instructions in the above document).

2nd laboratory: Getting started with the CPLD



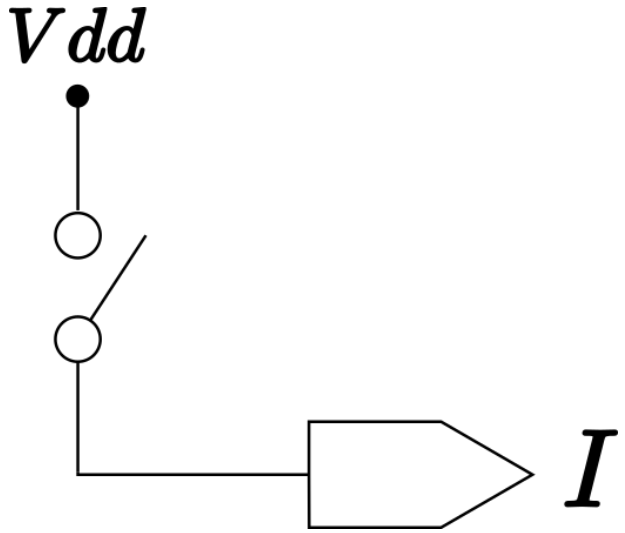
- Programmed through the USB-blaster and Quartus
- 9V battery supply
- In order to avoid I/O electrical conflicts (input/output configuration), I/O protected by 220 Ω resistors

2nd laboratory & project: Some instructions

- Install Quartus on your Windows/Linux **BEFORE** attending the lab (Quartus is not supported on Mac and a virtual machine might be tricky to use with the USB ports). Follow the steps described in the beginning of the pdf document *ELEN0040_Lab_2__Instructions.pdf*
- Come to my office during next week (send me an email) to get your CPLD (you will have to buy a 9V battery)
  - No deposit but it is **mandatory** to return the CPLD after the presentation of your project
  - It is **prohibited** to weld the CPLD to a stripboard or PCB (use tulip supports)
- Q/A sessions related to the project will be organized each week.

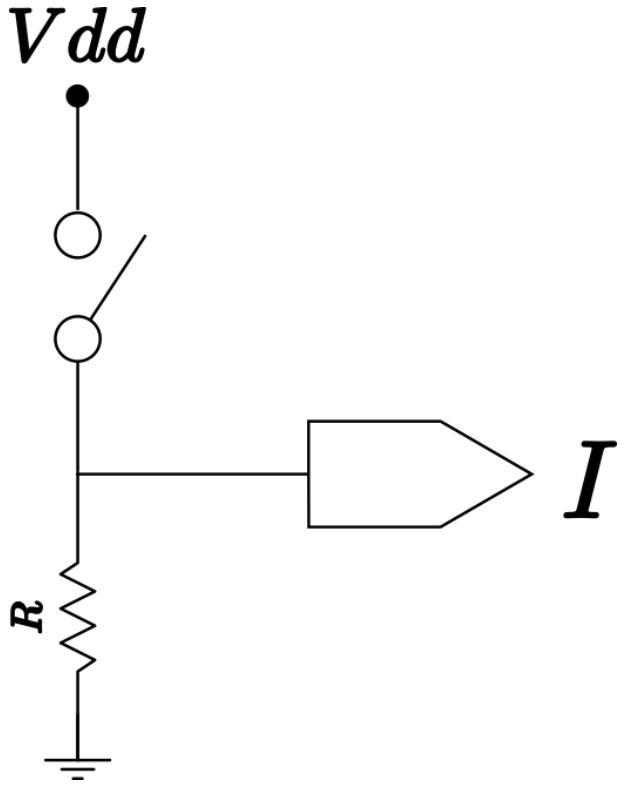
Some tips for the labs: button

NOT to do



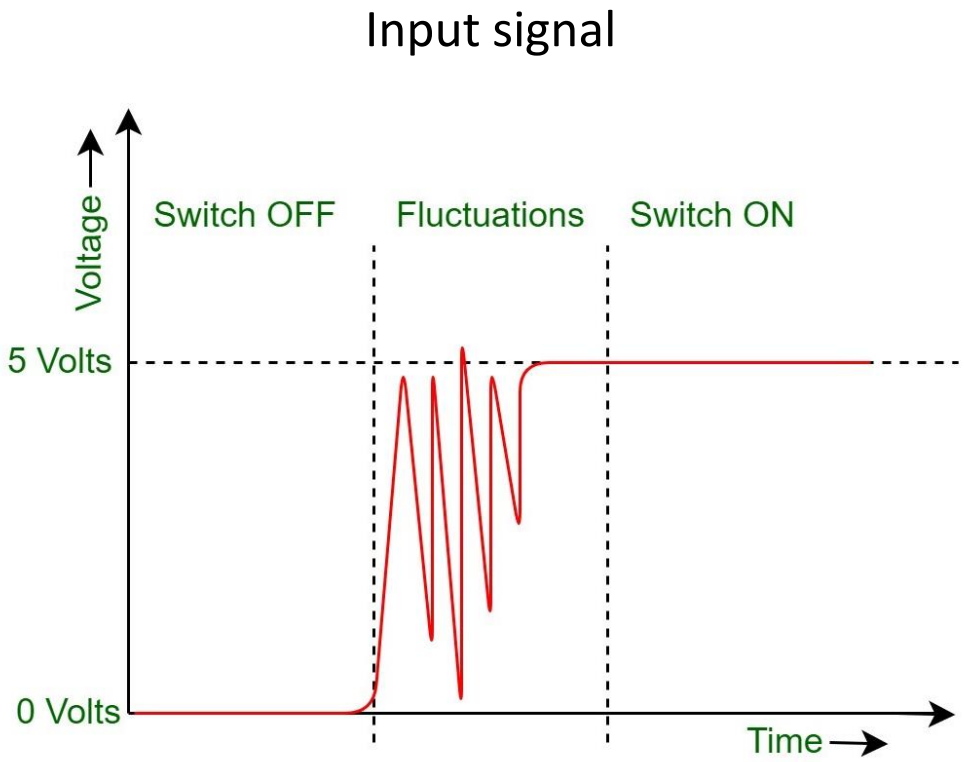
Take care to floating voltages

Add a pull-down resistor



NB: the positions of the button and resistor can be swapped

Some tips for the labs: button



2 solutions:

- A numerical filter implemented in the CPLD (and using several logic units)
- A low-pass filter to cut the high frequencies and smooth the signal