In [1]:

```
# CNF equation:
# (x2 ∨ x4 ∨ x6 ∨ ¬x8 ∨ x10 ∨ x12 ∨ ¬x13 ∨ ¬x14)
#  ∧ (¬x1 ∨ x2 ∨ x3 ∨ x4 ∨ ¬x5 ∨ x8 ∨ ¬x9 ∨ ¬x10 ∨ x14 ∨ ¬x15)
#  ∧ (x2 ∨ ¬x3 ∨ ¬x6 ∨ ¬x8 ∨ x11 ∨ x13)
#  ∧ (x3 ∨ x4 ∨ ¬x5 ∨ x7 ∨ ¬x8 ∨ x9 ∨ ¬x10 ∨ x12 ∨ ¬x14)
#  ∧ (x2 ∨ ¬x4 ∨ x6 ∨ ¬x7 ∨ x8 ∨ ¬x10 ∨ x13 ∨ ¬x15)


import numpy as np

# Importing standard Qiskit libraries
from qiskit import *
from qiskit.circuit import *
from qiskit.tools.jupyter import *
from qiskit.visualization import *
from ibm_quantum_widgets import *
from qiskit.providers.aer import QasmSimulator
from qiskit.circuit.library.standard_gates import XGate,ZGate,HGate


# Loading your IBM Quantum account(s)
#provider = IBMQ.load_account()

q_reg = QuantumRegister(20, 'q')
c_reg = ClassicalRegister(15, 'c')
circuit = QuantumCircuit(q_reg, c_reg)


# Qslice 0
circuit.append(HGate(),[q_reg[0]])
circuit.append(HGate(),[q_reg[1]])
circuit.append(HGate(),[q_reg[2]])
circuit.append(HGate(),[q_reg[3]])
circuit.append(HGate(),[q_reg[4]])
circuit.append(HGate(),[q_reg[5]])
circuit.append(HGate(),[q_reg[6]])
circuit.append(HGate(),[q_reg[7]])
circuit.append(HGate(),[q_reg[8]])
circuit.append(HGate(),[q_reg[9]])
circuit.append(HGate(),[q_reg[10]])
circuit.append(HGate(),[q_reg[11]])
circuit.append(HGate(),[q_reg[12]])
circuit.append(HGate(),[q_reg[13]])
circuit.append(HGate(),[q_reg[14]])
circuit.barrier(q_reg)
# Qslice 1
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[9]])
circuit.append(XGate(),[q_reg[11]])
# Qslice 2
circuit.append(XGate().control(8),[q_reg[1], q_reg[3], q_reg[5], q_reg[7], q_reg
[9], q_reg[11], q_reg[12], q_reg[13],  q_reg[15]])
# Qslice 3
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[3]])
```

```
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[9]])
circuit.append(XGate(),[q_reg[11]])
circuit.append(XGate(),[q_reg[15]])
circuit.barrier(q_reg)
# Qslice 4
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[13]])
# Qslice 5
circuit.append(XGate().control(10),[q_reg[0], q_reg[1], q_reg[2], q_reg[3], q_re
g[4], q_reg[7], q_reg[8], q_reg[9], q_reg[13], q_reg[14],  q_reg[16]])
# Qslice 6
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[13]])
circuit.append(XGate(),[q_reg[16]])
circuit.barrier(q_reg)
# Qslice 7
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[10]])
circuit.append(XGate(),[q_reg[12]])
# Qslice 8
circuit.append(XGate().control(6),[q_reg[1], q_reg[2], q_reg[5], q_reg[7], q_reg
[10], q_reg[12],  q_reg[17]])
# Qslice 9
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[10]])
circuit.append(XGate(),[q_reg[12]])
circuit.append(XGate(),[q_reg[17]])
circuit.barrier(q_reg)
# Qslice 10
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[6]])
circuit.append(XGate(),[q_reg[8]])
circuit.append(XGate(),[q_reg[11]])
# Qslice 11
circuit.append(XGate().control(9),[q_reg[2], q_reg[3], q_reg[4], q_reg[6], q_reg
[7], q_reg[8], q_reg[9], q_reg[11], q_reg[13],  q_reg[18]])
# Qslice 12
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[6]])
circuit.append(XGate(),[q_reg[8]])
circuit.append(XGate(),[q_reg[11]])
circuit.append(XGate(),[q_reg[18]])
circuit.barrier(q_reg)
# Qslice 13
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[12]])
# Qslice 14
circuit.append(XGate().control(8),[q_reg[1], q_reg[3], q_reg[5], q_reg[6], q_reg
```

```
[7], q_reg[9], q_reg[12], q_reg[14],  q_reg[19]])
# Qslice 15
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[12]])
circuit.append(XGate(),[q_reg[19]])
circuit.barrier(q_reg)
# Qslice 16
circuit.append(ZGate().control(4),[q_reg[15], q_reg[16], q_reg[17], q_reg[18],
q_reg[19]])
circuit.barrier(q_reg)
# Qslice 15
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[12]])
circuit.append(XGate(),[q_reg[19]])
# Qslice 14
circuit.append(XGate().control(8),[q_reg[1], q_reg[3], q_reg[5], q_reg[6], q_reg
[7], q_reg[9], q_reg[12], q_reg[14],  q_reg[19]])
# Qslice 13
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[12]])
circuit.barrier(q_reg)
# Qslice 12
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[6]])
circuit.append(XGate(),[q_reg[8]])
circuit.append(XGate(),[q_reg[11]])
circuit.append(XGate(),[q_reg[18]])
# Qslice 11
circuit.append(XGate().control(9),[q_reg[2], q_reg[3], q_reg[4], q_reg[6], q_reg
[7], q_reg[8], q_reg[9], q_reg[11], q_reg[13],  q_reg[18]])
# Qslice 10
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[6]])
circuit.append(XGate(),[q_reg[8]])
circuit.append(XGate(),[q_reg[11]])
circuit.barrier(q_reg)
# Qslice 9
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[10]])
circuit.append(XGate(),[q_reg[12]])
circuit.append(XGate(),[q_reg[17]])
# Qslice 8
circuit.append(XGate().control(6),[q_reg[1], q_reg[2], q_reg[5], q_reg[7], q_reg
[10], q_reg[12],  q_reg[17]])
# Qslice 7
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[10]])
circuit.append(XGate(),[q_reg[12]])
circuit.barrier(q_reg)
# Qslice 6
circuit.append(XGate(),[q_reg[1]])
```

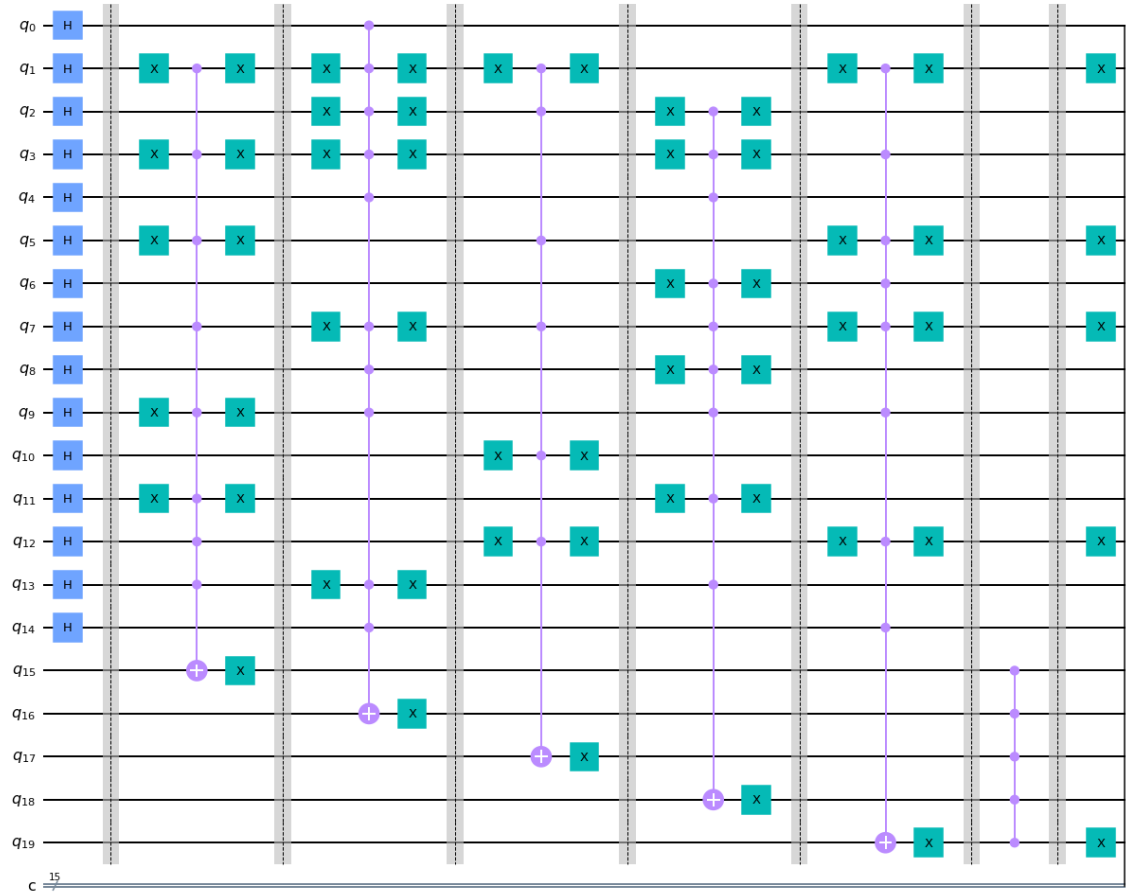
```
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[13]])
circuit.append(XGate(),[q_reg[16]])
# Qslice 5
circuit.append(XGate().control(10),[q_reg[0], q_reg[1], q_reg[2], q_reg[3], q_re
g[4], q_reg[7], q_reg[8], q_reg[9], q_reg[13], q_reg[14],  q_reg[16]])
# Qslice 4
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[13]])
circuit.barrier(q_reg)
# Qslice 3
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[9]])
circuit.append(XGate(),[q_reg[11]])
circuit.append(XGate(),[q_reg[15]])
# Qslice 2
circuit.append(XGate().control(8),[q_reg[1], q_reg[3], q_reg[5], q_reg[7], q_reg
[9], q_reg[11], q_reg[12], q_reg[13],  q_reg[15]])
# Qslice 1
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[9]])
circuit.append(XGate(),[q_reg[11]])
circuit.barrier(q_reg)
# Qslice 17
circuit.append(HGate(),[q_reg[0]])
circuit.append(HGate(),[q_reg[1]])
circuit.append(HGate(),[q_reg[2]])
circuit.append(HGate(),[q_reg[3]])
circuit.append(HGate(),[q_reg[4]])
circuit.append(HGate(),[q_reg[5]])
circuit.append(HGate(),[q_reg[6]])
circuit.append(HGate(),[q_reg[7]])
circuit.append(HGate(),[q_reg[8]])
circuit.append(HGate(),[q_reg[9]])
circuit.append(HGate(),[q_reg[10]])
circuit.append(HGate(),[q_reg[11]])
circuit.append(HGate(),[q_reg[12]])
circuit.append(HGate(),[q_reg[13]])
circuit.append(HGate(),[q_reg[14]])
# Qslice 18
circuit.append(XGate(),[q_reg[0]])
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[4]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[6]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[8]])
circuit.append(XGate(),[q_reg[9]])
```

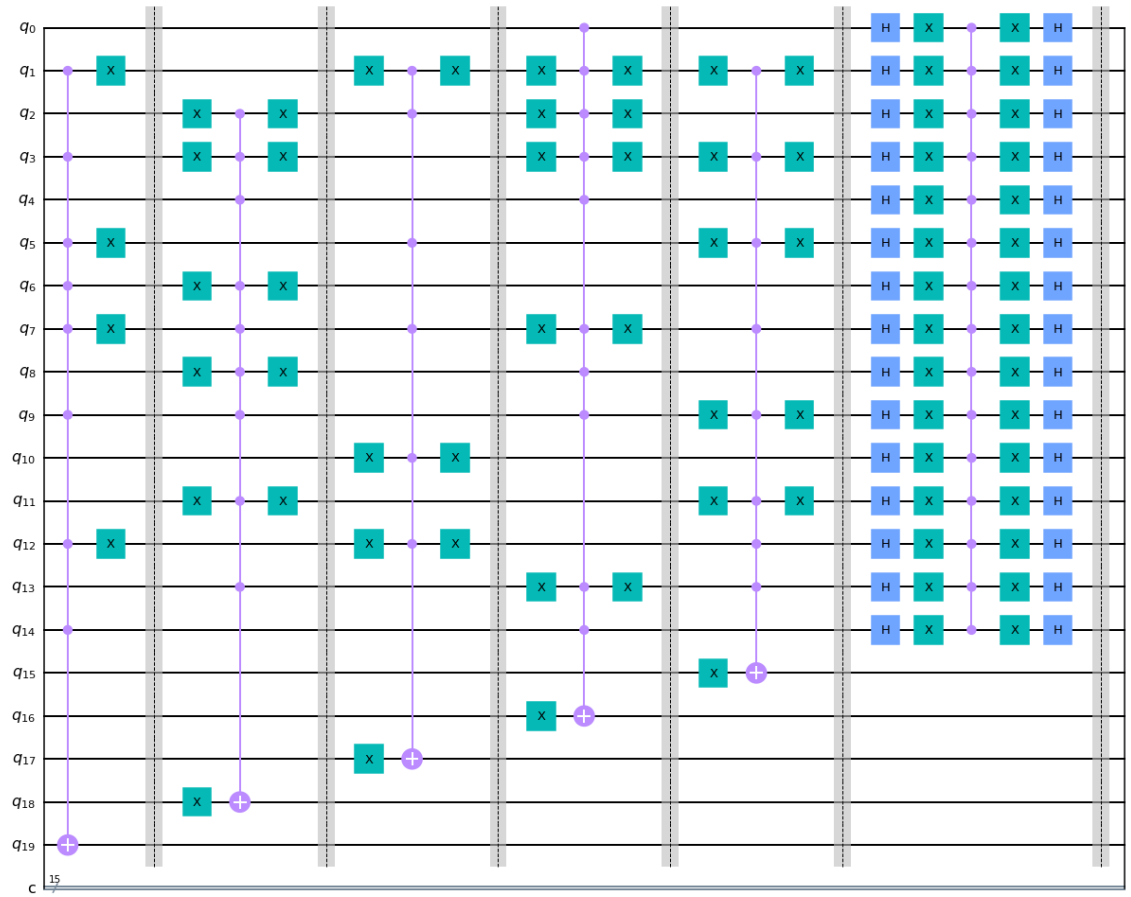
```
circuit.append(XGate(),[q_reg[10]])
circuit.append(XGate(),[q_reg[11]])
circuit.append(XGate(),[q_reg[12]])
circuit.append(XGate(),[q_reg[13]])
circuit.append(XGate(),[q_reg[14]])
# Qslice 19
circuit.append(ZGate().control(14),[q_reg[0], q_reg[1], q_reg[2], q_reg[3], q_re
g[4], q_reg[5], q_reg[6], q_reg[7], q_reg[8], q_reg[9], q_reg[10], q_reg[11], q_
reg[12], q_reg[13],  q_reg[14]])
# Qslice 18
circuit.append(XGate(),[q_reg[0]])
circuit.append(XGate(),[q_reg[1]])
circuit.append(XGate(),[q_reg[2]])
circuit.append(XGate(),[q_reg[3]])
circuit.append(XGate(),[q_reg[4]])
circuit.append(XGate(),[q_reg[5]])
circuit.append(XGate(),[q_reg[6]])
circuit.append(XGate(),[q_reg[7]])
circuit.append(XGate(),[q_reg[8]])
circuit.append(XGate(),[q_reg[9]])
circuit.append(XGate(),[q_reg[10]])
circuit.append(XGate(),[q_reg[11]])
circuit.append(XGate(),[q_reg[12]])
circuit.append(XGate(),[q_reg[13]])
circuit.append(XGate(),[q_reg[14]])
# Qslice 21
circuit.append(HGate(),[q_reg[0]])
circuit.append(HGate(),[q_reg[1]])
circuit.append(HGate(),[q_reg[2]])
circuit.append(HGate(),[q_reg[3]])
circuit.append(HGate(),[q_reg[4]])
circuit.append(HGate(),[q_reg[5]])
circuit.append(HGate(),[q_reg[6]])
circuit.append(HGate(),[q_reg[7]])
circuit.append(HGate(),[q_reg[8]])
circuit.append(HGate(),[q_reg[9]])
circuit.append(HGate(),[q_reg[10]])
circuit.append(HGate(),[q_reg[11]])
circuit.append(HGate(),[q_reg[12]])
circuit.append(HGate(),[q_reg[13]])
circuit.append(HGate(),[q_reg[14]])
circuit.barrier(q_reg)
# Qslice 22
circuit.measure(q_reg[0], c_reg[0])
circuit.measure(q_reg[1], c_reg[1])
circuit.measure(q_reg[2], c_reg[2])
circuit.measure(q_reg[3], c_reg[3])
circuit.measure(q_reg[4], c_reg[4])
circuit.measure(q_reg[5], c_reg[5])
circuit.measure(q_reg[6], c_reg[6])
circuit.measure(q_reg[7], c_reg[7])
circuit.measure(q_reg[8], c_reg[8])
circuit.measure(q_reg[9], c_reg[9])
circuit.measure(q_reg[10], c_reg[10])
circuit.measure(q_reg[11], c_reg[11])
circuit.measure(q_reg[12], c_reg[12])
circuit.measure(q_reg[13], c_reg[13])
circuit.measure(q_reg[14], c_reg[14])
```

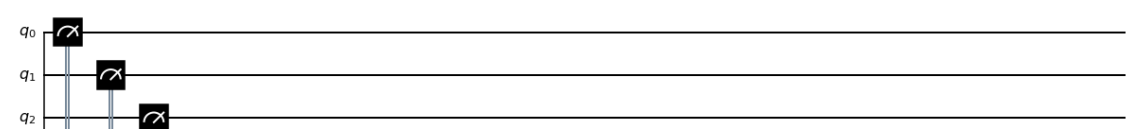
```
circuit.draw('mpl')
```

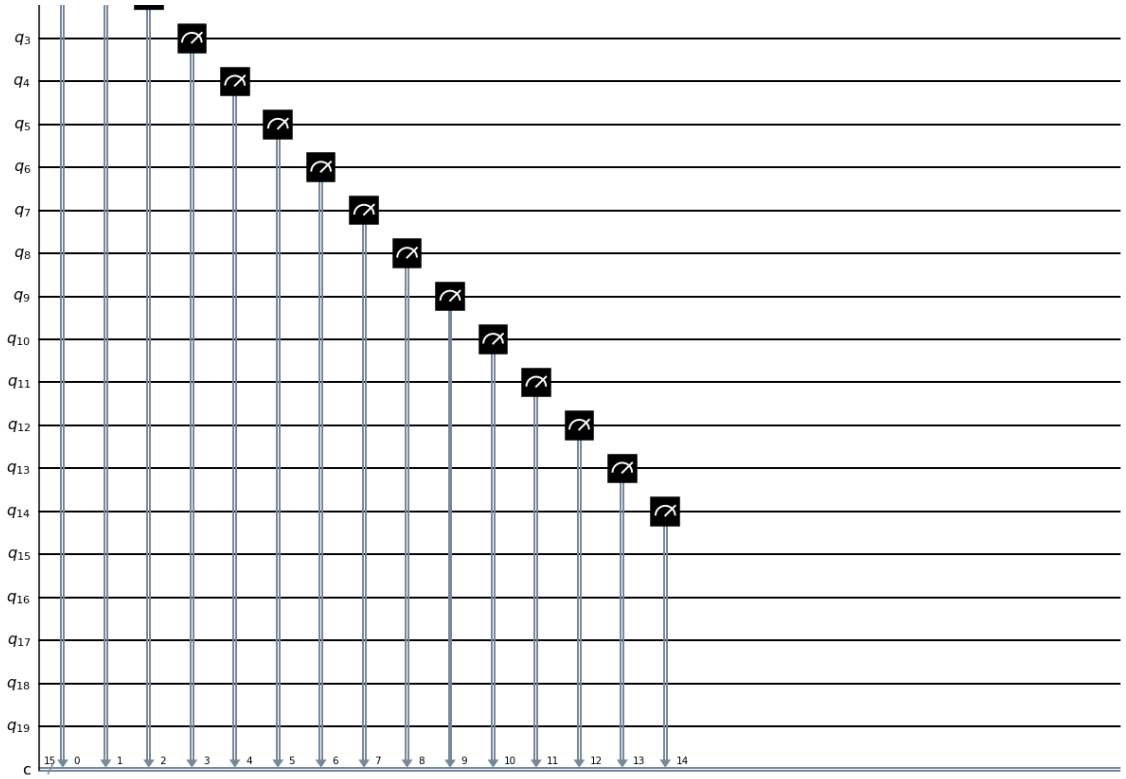
```
<frozen importlib._bootstrap>:219: RuntimeWarning: scipy._lib.messag
estream.MessageStream size changed, may indicate binary incompatibil
ity. Expected 56 from C header, got 64 from PyObject
```

Out[1]:


q0
q1
q2
q3
q4
q5
q6
q7
q8
q9
q10
q11
q12
q13
q14
q15
q16
q17
q18
q19
c
15


q0
q1
q2
q3
q4
q5
q6
q7
q8
q9
q10
q11
q12
q13
q14
q15
q16
q17
q18
q19
c
15


q0
q1
q2


q3
q4
q5
q6
q7
q8
q9
q10
q11
q12
q13
q14
q15
q16
q17
q18
q19
c
15
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14

In [2]:

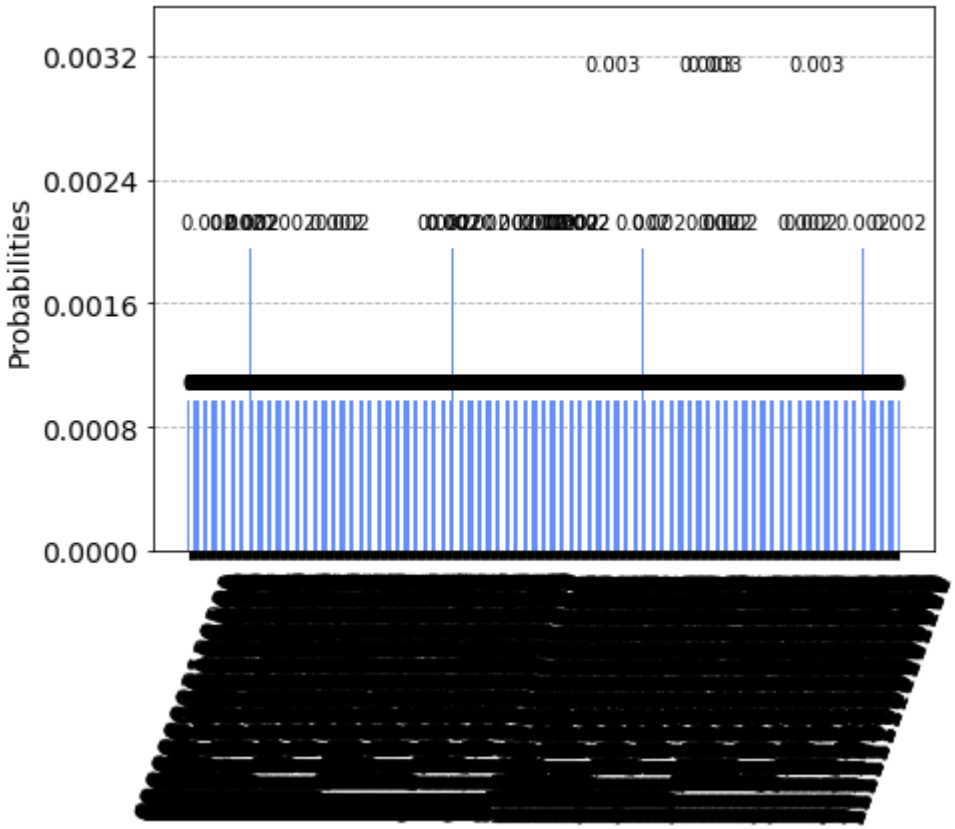
```
from qiskit import Aer
from qiskit.compiler import transpile
from qiskit.visualization import plot_histogram

# Use Aer's qasm_simulator
backend_sim = Aer.get_backend('qasm_simulator')

# Execute the circuit on the qasm simulator.
# We've set the number of repeats of the circuit
# to be 1024, which is the default.
job_sim = backend_sim.run(transpile(circuit, backend_sim), shots=1024)

# Grab the results from the job.
result_sim = job_sim.result()
counts = result_sim.get_counts(circuit)
plot_histogram(counts)
```

Out[2]:



In [3]:

```
print(counts)
```

```
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```

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