Aula 04

Nome: Guilherme Fróes Camba de Freitas | Matricula: 718116

Nome: Bernardo Ferreira Temponi | Matricula: 699469

Nome: Diego Basilio Arruda | Matricula: 701139

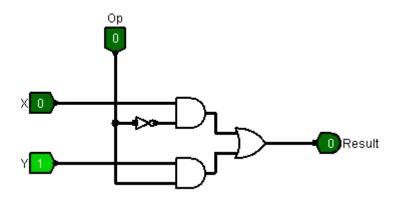
Unidade Logica Aritimetica (ULA)

1. Tabela

	S=	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
Α	0000	1111	1111	0000	0000	1111	1111	0000	0000	1111	1111	0000	0000	1111	1111	0000	0000
В	0000																
Α	0001	1110	1110	0000	0000	1110	1110	0000	0000	1111	1111	0001	0001	1111	1111	0001	0001
В	0001																
Α	0010	1101	1101	0000	0000	1101	1101	0000	0000	1111	1111	0010	0010	1111	1111	0010	0010
В	0010																
Α	0100	1011	1011	0000	0000	1011	1011	0000	0000	1111	1111	0100	0100	1111	1111	0100	0100
В	0100																
Α	1000	0111	0111	0000	0000	0111	0111	0000	0000	1111	1111	1000	1000	1111	1111	1000	1000
В	1000																

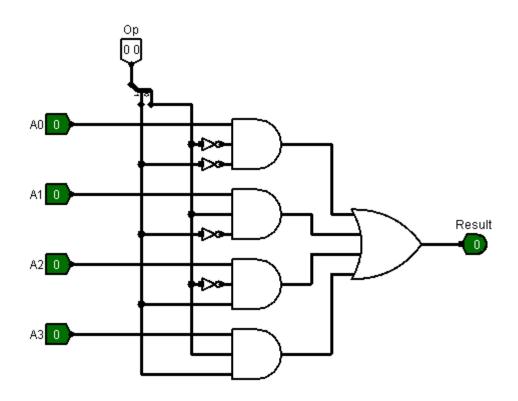
MUX 1 bit

1. Logisim



MUX 4 bit

1. Logisim



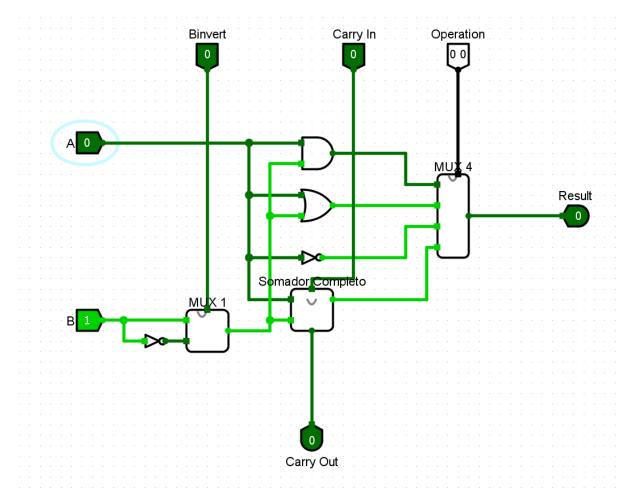
Teste da ULA

Inicio:

A=0;

B=1;

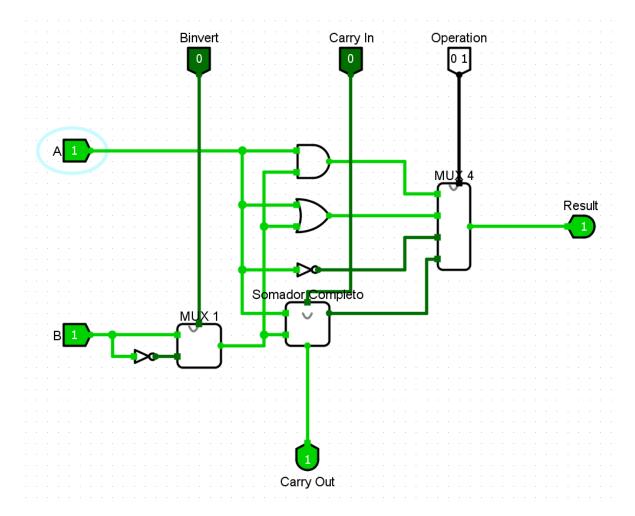
AND(A,B);



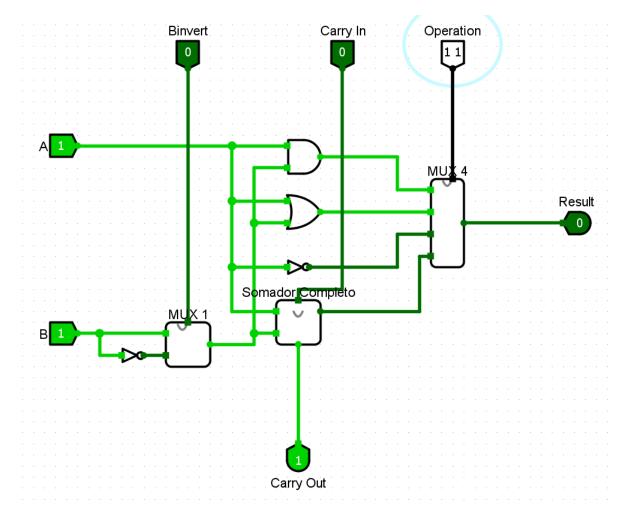
A=1;

B=1;

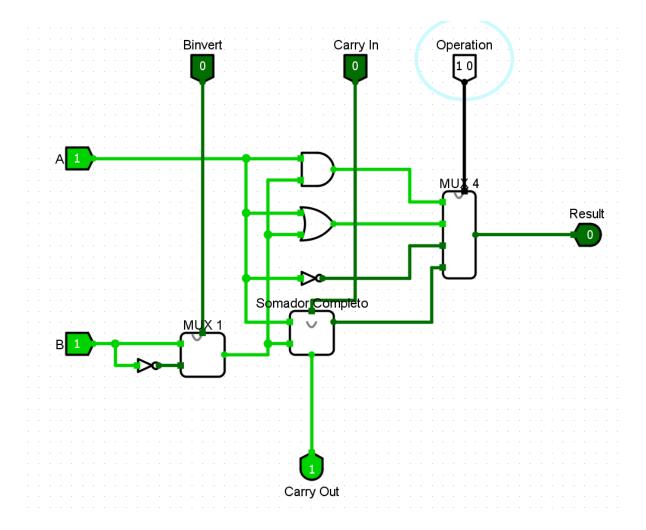
OR(A,B);



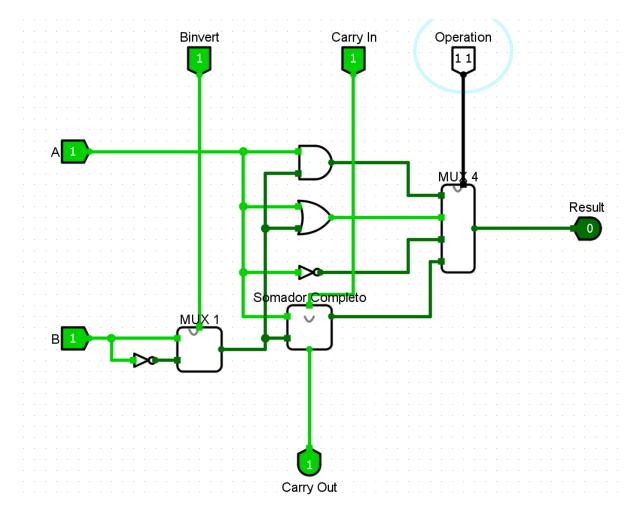
SOMA(A,B);



NOT(A);



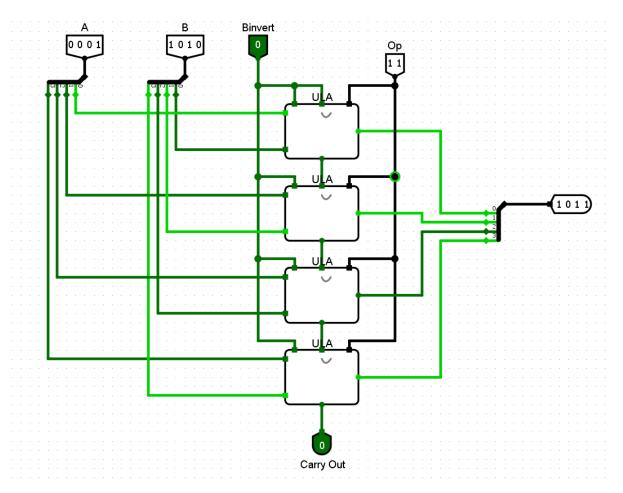
SOMA (A,-B);



Fim.

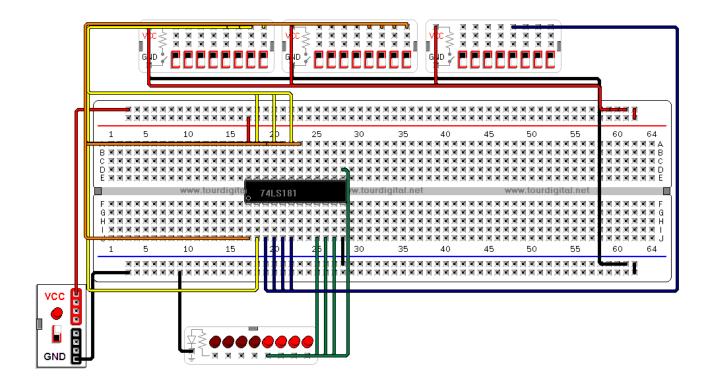
Unidade Logica Aritimetica 4 bits (ULA 4)

1. Logisim

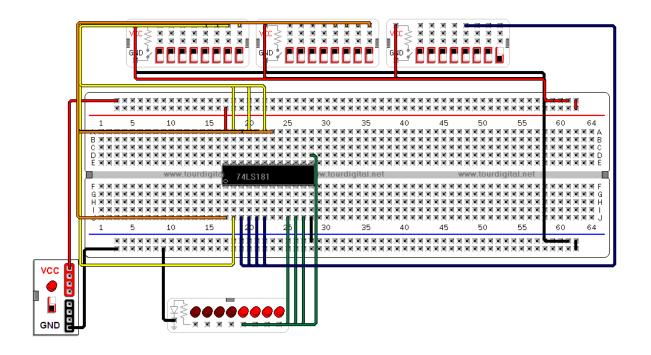


2. Simulador 97

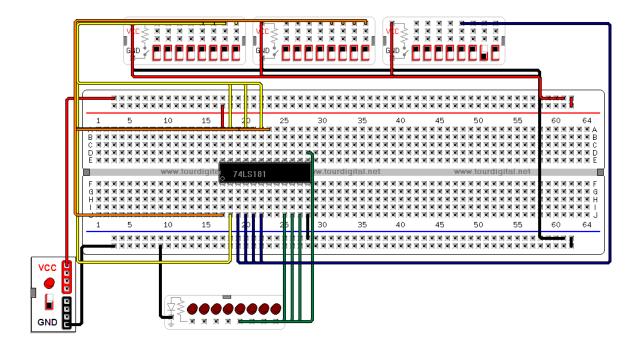
NOT(A)



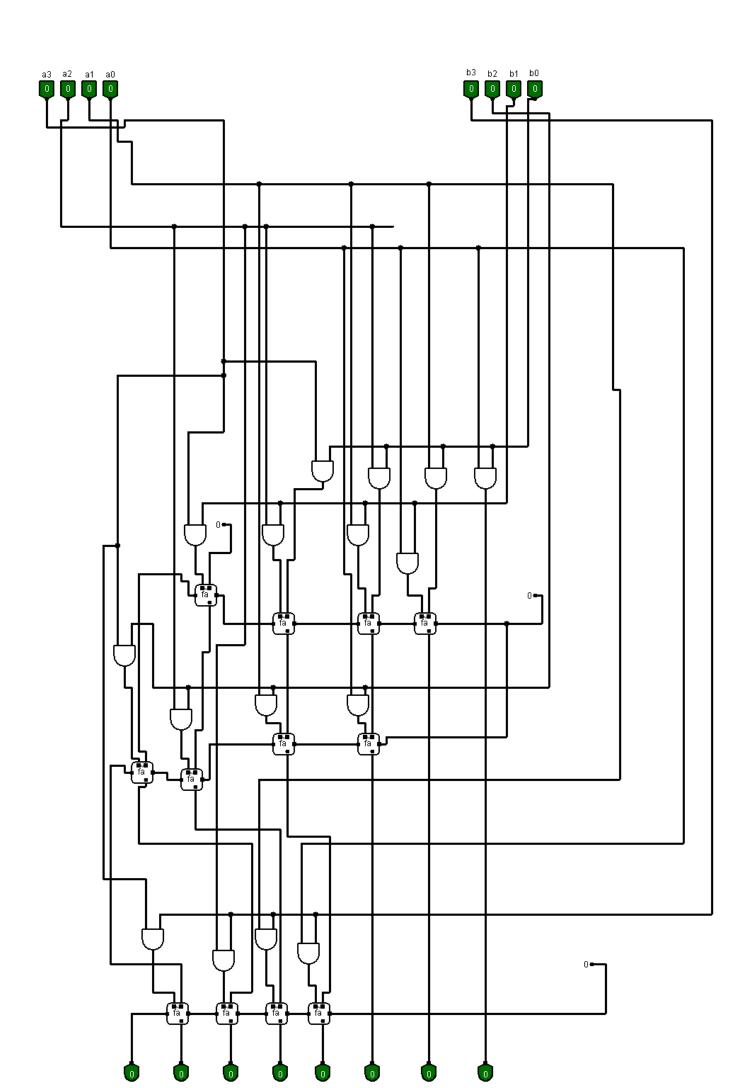
NOT(OR(A,B))



AND(NOT(A),B)



Multiplicador 4bits



Somador completo de 1 bit

